Si5323

PRELIMINARY DATA SHEET

PIN-PROGRAMMABLE PRECISION CLOCK MULTIPLIER/JITTER ATTENUATOR

Description

The Si5323 is a jitter-attenuating precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, Ethernet, and Fibre Channel. The Si5323 accepts dual clock inputs ranging from 8 kHz to 707 MHz and generates two equal frequency-multiplied clock outputs ranging from 8 kHz to 1050 MHz. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel rates. The Si5323 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5, or 3.3 V supply, the Si5323 is ideal for providing clock multiplication and jitter attenuation in high performance timing applications.

Applications

- SONET/SDH OC-48/STM-16 and OC-192/STM-64 line cards
- GbE/10GbE, 1/2/4/8/10GFC line cards
- ITU G.709 line cards
- Optical modules
- Test and measurement
- Synchronous Ethernet

Features

- Selectable output frequencies ranging from 8 kHz to 1050 MHz
- Ultra-low jitter clock outputs with jitter generation as low as 0.3 ps rms (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (60 Hz to 8.4 kHz)
- Meets OC-192 GR-253-CORE jitter specifications
- Dual clock inputs w/manual or automatically controlled hitless switching
- Dual clock outputs with selectable signal format (LVPECL, LVDS, CML, CMOS)
- Support for ITU G.709 FEC ratios (255/238, 255/237, 255/236)
- LOL, LOS alarm outputs
- Pin-controlled output phase adjust
- Pin-programmable settings
- On-chip voltage regulator for 1.8 ±5%, 2.5 or 3.3 V ±10% operation
- Small size: 6 x 6 mm 36-lead QFN
- Pb-free, ROHS compliant

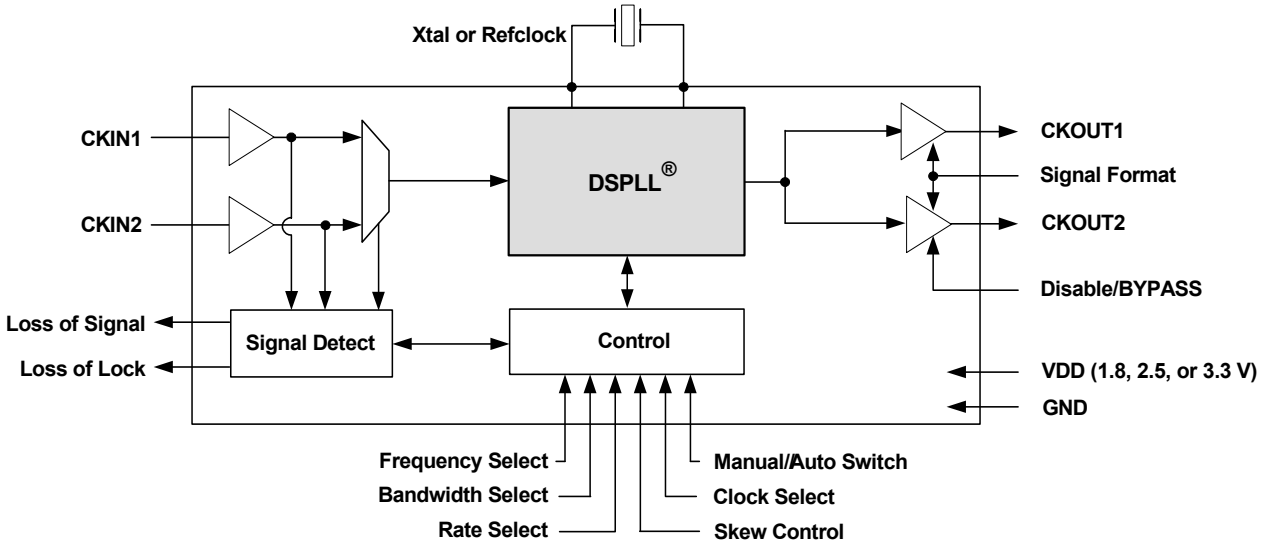


Table 1. Performance Specifications

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Range	T_A		–40	25	85	ºC
Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
			1.71	1.8	1.89	V
Supply Current	I_{DD}	f_{OUT} = 622.08 MHz Both CKOUTs enabled LVPECL format output		251	279	mA
		CKOUT2 disabled	—	217	243	mA
		f_{OUT} = 19.44 MHz Both CKOUTs enabled CMOS format output	—	204	234	mA
		CKOUT2 disabled	—	194	220	mA
		Tristate/Sleep Mode		165	TBD	mA
Input Clock Frequency (CKIN1, CKIN2)	CK_F	Input frequency and clock multiplication ratio pin-selectable from table of values using FRQSEL and FRQTBL settings. Consult Silicon Laboratories configuration software DSPLL*sim* or Any-Rate Precision Clock Family Reference Manual at www.silabs.com/timing (click on Documentation) for table selections.	0.008	—	707.35	MHz
Output Clock Frequency (CKOUT1, CKOUT2)	CK_{OF}		0.008	—	1049.76	MHz
3-Level Input Pins						
Input Mid Current	I_{IMM}	See Note 2.	–2	—	2	µA
Input Clocks (CKIN1, CKIN2)						
Differential Voltage Swing	CK_{NDPP}		0.25	—	1.9	VPP
Common Mode Voltage	CK_{NVCM}	1.8 V ±5%	0.9	—	1.4	V
		2.5 V ±10%	1.0	—	1.7	V
		3.3 V ±10%	1.1	—	1.95	V
Rise/Fall Time	CK_{NTRF}	20–80%	—	—	11	ns
Duty Cycle	CKN_{DC}	Whichever is smaller	40	—	60	%
(Minimum Pulse Width)			2	—	—	ns
Output Clocks (CKOUT1, CKOUT2)						
Common Mode	V_{OCM}	LVPECL 100 Ω load line-to-line	V_{DD} – 1.42	—	V_{DD} – 1.25	V
Differential Output Swing	V_{OD}		1.1	—	1.9	V
Single Ended Output Swing	V_{SE}		0.5	—	0.93	V
Rise/Fall Time	CKO_{TRF}	20–80%	—	230	350	ps

Notes:

1. For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing (click on Documentation)
2. This is the amount of leakage that the 3-level input can tolerate from an external driver. See the Family Reference Manual. In most designs, an external resistor voltage divider is recommended.

Table 1. Performance Specifications (Continued)
(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Duty Cycle Uncertainty	CKO_{DC}	LVPECL Differential 100 Ω Line-to-Line Measured at 50% point	–40	—	40	ps
PLL Performance						
Jitter Generation	J_{GEN}	f_{IN} = f_{OUT} = 622.08 MHz, LVPECL output format 50 kHz–80 MHz	—	0.3	TBD	ps rms
		12 kHz–20 MHz	—	0.3	TBD	ps rms
Jitter Transfer	J_{PK}		—	0.05	0.1	dB
External Reference Jitter Transfer	J_{PKEXTN}		—	TBD	TBD	dB
Phase Noise	CKO_{PN}	f_{IN} = f_{OUT} = 622.08 MHz 100 Hz offset	—	TBD	TBD	dBc/Hz
		1 kHz offset	—	TBD	TBD	dBc/Hz
		10 kHz offset	—	TBD	TBD	dBc/Hz
		100 kHz offset	—	TBD	TBD	dBc/Hz
		1 MHz offset	—	TBD	TBD	dBc/Hz
Subharmonic Noise	SP_{SUBH}	Phase Noise @ 100 kHz Offset	—	TBD	TBD	dBc
Spurious Noise	SP_{SPUR}	Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz)	—	TBD	TBD	dBc
Package						
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	38	—	ºC/W

Notes:
1. For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing (click on Documentation)
2. This is the amount of leakage that the 3-level input can tolerate from an external driver. See the Family Reference Manual. In most designs, an external resistor voltage divider is recommended.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 3.6	V
LVCMOS Input Voltage	V_{DIG}	–0.3 to (V_{DD} + 0.3)	V
Operating Junction Temperature	T_{JCT}	–55 to 150	C
Storage Temperature Range	T_{STG}	–55 to 150	C
ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN–		2	kV
ESD MM Tolerance; All pins except CKIN+/CKIN–		200	V
ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN–		700	V
ESD MM Tolerance; CKIN+/CKIN–		150	V
Latch-Up Tolerance		JESD78 Compliant	

Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

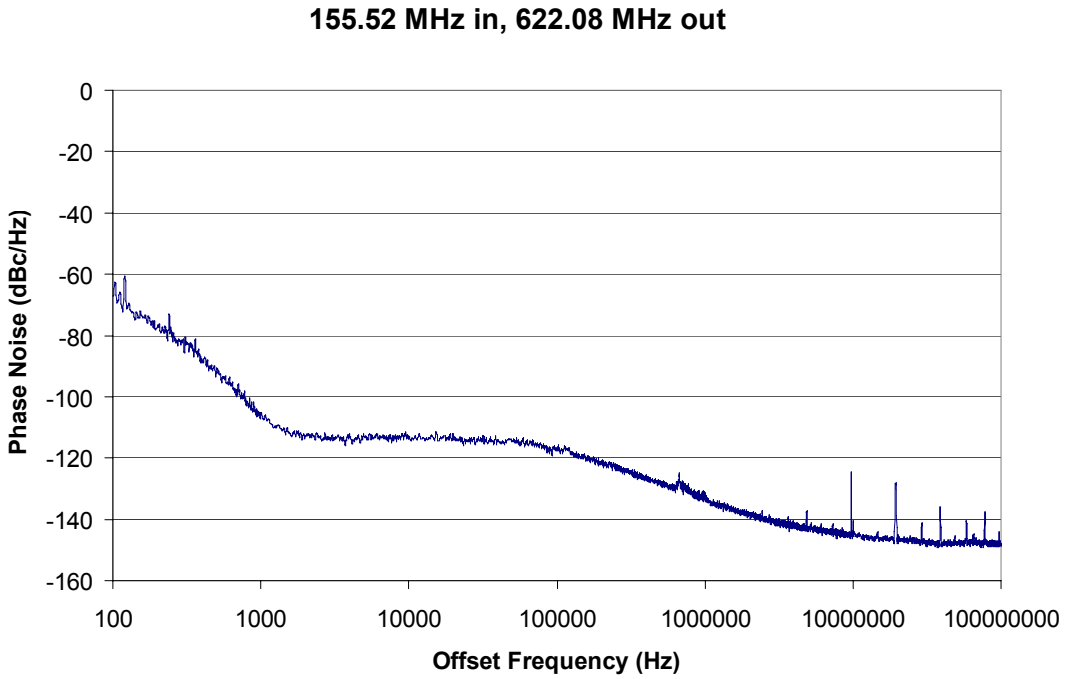
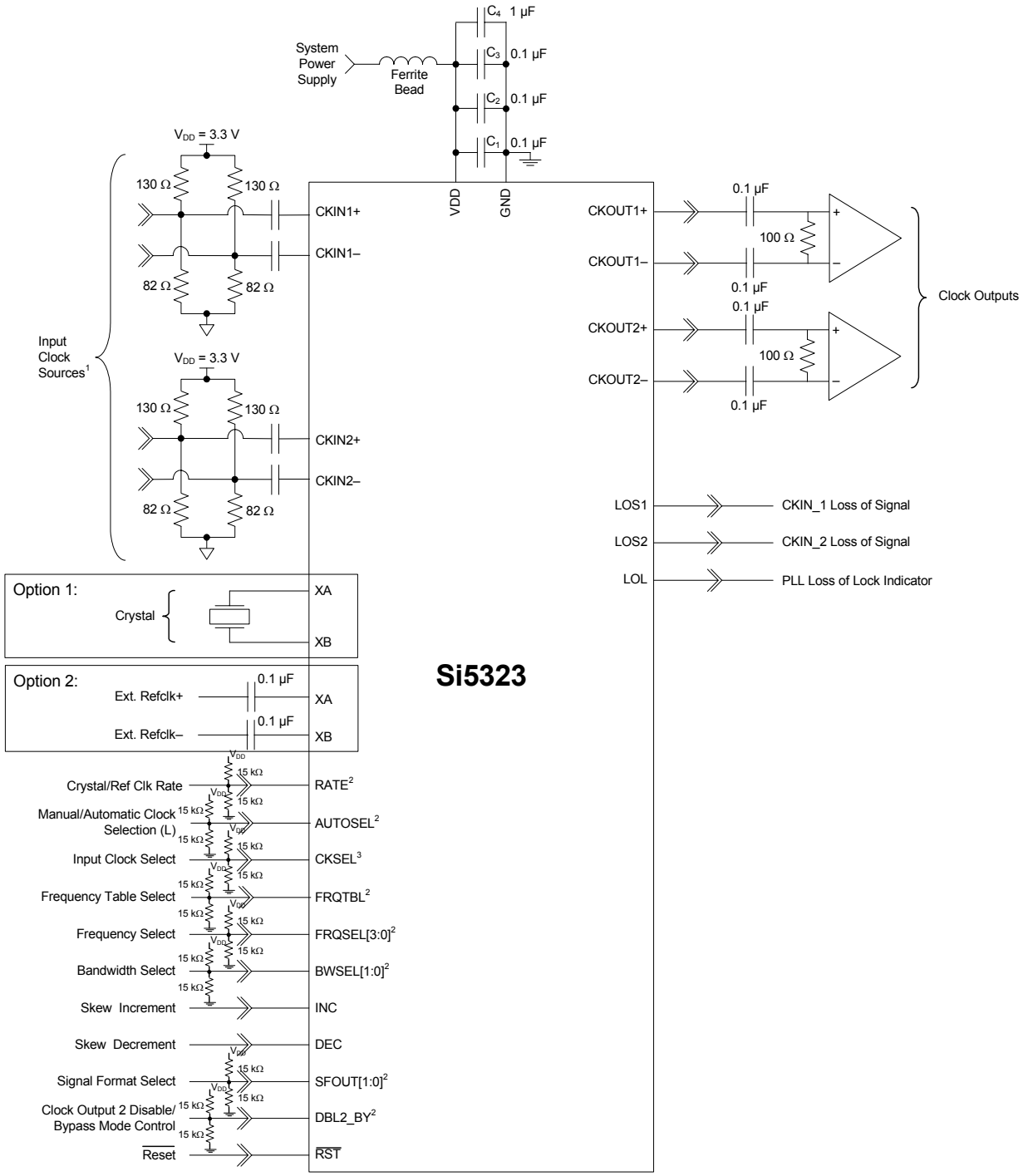


Figure 1. Typical Phase Noise Plot

Jitter Band	Jitter, RMS
Brick Wall, 100 Hz to 100 MHz	1,279 fs
SONET_OC48, 12 kHz to 20 MHz	315 fs
SONET_OC192_A, 20 kHz to 80 MHz	335 fs
SONET_OC192_B, 4 MHz to 80 MHz	194 fs
SONET_OC192_C, 50 kHz to 80 MHz	318 fs
Brick Wall, 800 Hz to 80 MHz	343 fs



Notes:
1. Assumes differential LVPECL termination (3.3 V) on clock inputs.
2. Denotes tri-level input pins with states designated as L (ground), M (V_{DD}/2), and H (V_{DD}).
3. Assumes manual input clock selection.

Figure 2. Si5323 Typical Application Circuit

1. Functional Description

The Si5323 is a jitter-attenuating precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, Ethernet, and Fibre Channel. The Si5323 accepts dual clock inputs ranging from 8 kHz to 707 MHz and generates two frequency-multiplied clock outputs ranging from 8 kHz to 1050 MHz. The two input clocks are at the same frequency and the two output clocks are at the same frequency. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel rates. In addition to providing clock multiplication in SONET and datacom applications, the Si5323 supports SONET-to-datacom frequency translations. Silicon Laboratories offers a PC-based software utility, DSPLL*sim*, that can be used to look up valid Si5323 frequency translations. This utility can be downloaded from http://www.silabs.com/timing (click on Documentation).

The Si5323 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5323 PLL loop bandwidth is selectable via the BWSEL[1:0] pins and supports a range from 60 Hz to 8.4 kHz. The DSPLL*sim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5323 supports hitless switching between the two input clocks in compliance with GR-253-CORE and GR-1244-CORE that greatly minimizes the propagation of phase transients to the clock outputs during an input clock transition (<200 ps typ). Manual and automatic revertive and non-revertive input clock switching options are available via the AUTOSEL input pin. The Si5323 monitors both input clocks for loss-of-signal and provides a LOS alarm when it detects missing pulses on either input clock. The device monitors the lock status of the PLL. The lock detect algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock.

The Si5323 provides a digital hold capability that allows the device to continue generation of a stable output clock when the selected input reference is lost. During digital hold, the DSPLL generates an output frequency based on a historical average that existed a fixed amount of time before the error event occurred, eliminating the effects of phase and frequency transients that may occur immediately preceding digital hold.

The Si5323 has two differential clock outputs. The electrical format of the clock outputs is programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, the second clock output can be powered down to minimize power consumption. The phase difference between the selected input clock and the output clocks is adjustable in 200 ps increments for system skew control. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

1.1. External Reference

An external, 38.88 MHz clock or a low-cost 114.285 MHz 3rd overtone crystal is used as part of a fixed-frequency oscillator within the DSPLL. This external reference is required for the device to perform jitter attenuation. Silicon Laboratories recommends using a high-quality crystal. Specific recommendations may be found in the Family Reference Manual. An external clock from a high quality OCXO or TCXO can also be used as a reference for the device.

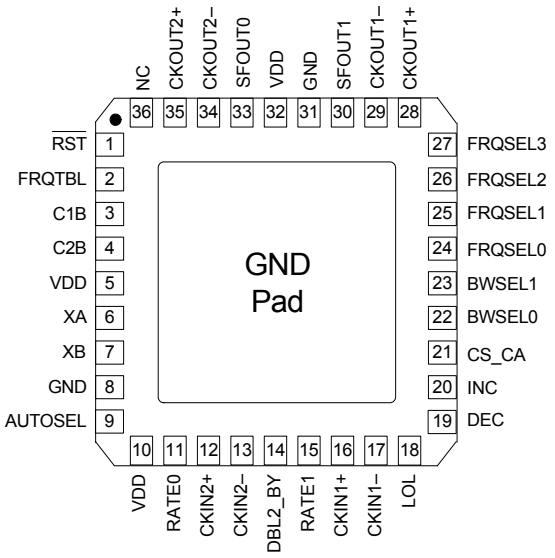
In digital hold, the DSPLL remains locked to this external reference. Any changes in the frequency of this reference when the DSPLL is in digital hold will be tracked by the output of the device. Note that crystals can have temperature sensitivities.

1.2. Further Documentation

Consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual (FRM) for detailed information about the Si5323. Additional design support is available from Silicon Laboratories through your distributor.

Silicon Laboratories has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection. The FRM and this utility can be downloaded from http://www.silabs.com/timing (click on Documentation).

2. Pin Descriptions: Si5323



Pin assignments are preliminary and subject to change.

Table 3. Si5323 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1	$\overline{\text{RST}}$	I	LVCMOS	**External Reset.** Active low input that performs external hardware reset of device. Resets all internal logic to a known state. Clock outputs are tristated during reset. After rising edge of $\overline{\text{RST}}$ signal, the Si5323 will perform an internal self-calibration when a valid input signal is present. This pin has a weak pull-up.
2	FRQTBL	I	3-Level	**Frequency Table Select.** Selects SONET/SDH, datacom, or SONET/SDH to datacom frequency table. L = SONET/SDH M = Datacom H = SONET/SDH to Datacom This pin has a weak pull-up and weak pull-down and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
3	C1B	O	LVCMOS	**CKIN1 Loss of Signal.** Active high loss-of-signal indicator for CKIN1. Once triggered, the alarm will remain active until CKIN1 is validated. 0 = CKIN1 present 1 = LOS on CKIN1

Table 3. Si5323 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
4	C2B	O	LVCMOS	**CKIN2 Loss of Signal.** Active high loss-of-signal indicator for CKIN2. Once triggered, the alarm will remain active until CKIN2 is validated. 0 = CKIN2 present 1 = LOS on CKIN2
5, 10, 32	V_{DD}	V_{DD}	Supply	**Supply.** The device operates from a 1.8, 2.5, or 3.3 V supply. Bypass capacitors should be associated with the following V_{DD} pins: 5 0.1 µF 10 0.1 µF 32 0.1 µF A 1.0 µF should also be placed as close to device as is practical.
7 6	XB XA	I	Analog	**External Crystal or Reference Clock.** External crystal should be connected to these pins to use internal oscillator based reference. Refer to Family Reference Manual for interfacing to an external reference. External reference must be from a high-quality clock source (TCXO, OCXO). Frequency of crystal or external clock is set by the RATE pins.
8, 31	GND	GND	Supply	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device.
9	AUTOSEL	I	3-Level	**Manual/Automatic Clock Selection.** Three level input that selects the method of input clock selection to be used. L = Manual M = Automatic non-revertive H = Automatic revertive This pin has a weak pull-up and weak pull-down and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
11 15	RATE0 RATE1	I	3-Level	**External Crystal or Reference Clock Rate.** Three level inputs that select the type and rate of external crystal or reference clock to be applied to the XA/XB port. Refer to the Family Reference Manual for settings. These pins have both a weak pull-up and a weak pull-down and default to M. These pins have both weak pull-ups and weak pull-downs and default to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
12 13	CKIN2+ CKIN2–	I		**Clock Input 2.** Differential input clock. This input can also be driven with a single-ended signal. Input frequency selected from a table of values. The same frequency must be applied to CKIN1 and CKIN2.

Table 3. Si5323 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
14	DBL2_BY	I	3-Level	**Output 2 Disable/Bypass Mode Control.** Controls enable of CKOUT2 divider/output buffer path and PLL bypass mode. L = CKOUT2 enabled M = CKOUT2 disabled H = Bypass mode with CKOUT2 enabled This pin has a weak pull-up and weak pull-down and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
16 17	CKIN1+ CKIN1–	I	Multi	**Clock Input 1.** Differential input clock. This input can also be driven with a single-ended signal. Input frequency selected from a table of values. The same frequency must be applied to CKIN1 and CKIN2.
18	LOL	O	LVCMOS	**PLL Loss of Lock Indicator.** This pin functions as the active high PLL loss of lock indicator. 0 = PLL locked 1 = PLL unlocked
19	DEC	I	LVCMOS	**Skew Decrement.** A pulse on this pin decreases the input to output device skew by $1/f_{OSC}$ (approximately 200 ps). There is no limit on the range of skew adjustment by this method. If both INC and DEC are tied high, phase buildout is disabled and the device maintains a fixed-phase relationship between the selected input clock and the output clock during an input clock transition. Detailed operations and timing characteristics for this pin may be found in the Any-Rate Precision Clock Family Reference Manual. This pin has a weak pull-down.
20	INC	I	LVCMOS	**Skew Increment.** A pulse on this pin increases the input to output device skew by $1/f_{OSC}$ (approximately 200 ps). There is no limit on the range of skew adjustment by this method. If both INC and DEC are tied high, phase buildout is disabled and the device maintains a fixed-phase relationship between the selected input clock and the output clock during an input clock transition. Detailed operations and timing characteristics for this pin may be found in the Any-Rate Precision Clock Family Reference Manual. **Note:** If NI_HS = 4, increment is not available. This pin has a weak pull-down.

Table 3. Si5323 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
21	CS_CA	I/O	LVCMOS	**Input Clock Select/Active Clock Indicator.** **Input**: If manual clock selection mode is chosen (AUTOSEL = L), this pin functions as the manual input clock selector. This input is internally deglitched to prevent inadvertent clock switching during changes in the CS input state. 0 = Select CKIN1 1 = Select CKIN2 If configured as input, must be set high or low. **Output**: If automatic clock selection mode is chosen (AUTOSEL = M or H), this pin indicates which of the two input clocks is currently the active clock. If alarms exist on both CKIN1 and CKIN2, indicating that the digital hold state has been entered, CA will indicate the last active clock that was used before entering the hold state. 0 = CKIN1 active input clock 1 = CKIN2 active input clock
23 22	BWSEL1 BWSEL0	I	3-Level	**Bandwidth Select.** Three level inputs that select the DSPLL closed loop bandwidth. Detailed operations and timing characteristics for these pins may be found in the Any-Rate Precision Clock Family Reference Manual. These pins have both weak pull-ups and weak pull-downs and default to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
27 26 25 24	FRQSEL3 FRQSEL2 FRQSEL1 FRQSEL0	I	3-Level	**Multiplier Select.** Three level inputs that select the input clock and clock multiplication ratio, depending on the FRQTBL setting. Consult the Any-Rate Precision Clock Family Reference Manual or DSPLLsim configuration software for settings, both available for download at www.silabs.com/timing (click on Documentation). These pins have both weak pull-ups and weak pull-downs and default to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
29 28	CKOUT1– CKOUT1+	O	Multi	**Clock Output 1.** Differential output clock with a frequency selected from a table of values. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.

Table 3. Si5323 Pin Descriptions (Continued)

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>I/O</th><th>Signal Level</th><th>Description</th></tr>
<tr><td>33
30</td><td>SFOUT0
SFOUT1</td><td>I</td><td>3-Level</td><td>Signal Format Select.
Three level inputs that select the output signal format (common mode voltage and differential swing) for both CKOUT1 and CKOUT2.
<table>
<tr><th>SFOUT[1:0]</th><th>Signal Format</th></tr>
<tr><td>HH</td><td>Reserved</td></tr>
<tr><td>HM</td><td>LVDS</td></tr>
<tr><td>HL</td><td>CML</td></tr>
<tr><td>MH</td><td>LVPECL</td></tr>
<tr><td>MM</td><td>Reserved</td></tr>
<tr><td>ML</td><td>LVDS—Low Swing</td></tr>
<tr><td>LH</td><td>CMOS</td></tr>
<tr><td>LM</td><td>Disable</td></tr>
<tr><td>LL</td><td>Reserved</td></tr>
</table>
These pins have both weak pull-ups and weak pull-downs and default to M.
Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.</td></tr>
<tr><td>34
35</td><td>CKOUT2–
CKOUT2+</td><td>O</td><td>Multi</td><td>Clock Output 2.
Differential output clock with a frequency selected from a table of values. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.</td></tr>
<tr><td>36</td><td>NC</td><td>—</td><td>—</td><td>No Connect.
These pins must be left unconnected for normal operation.</td></tr>
<tr><td>GND
PAD</td><td>GND</td><td>GND</td><td>Supply</td><td>Ground Pad.
The ground pad must provide a low thermal and electrical impedance to a ground plane.</td></tr>
</table>

3. Ordering Guide

Ordering Part Number	Package	ROHS6, Pb-Free	Temperature Range
Si5323-C-GM	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C

4. Package Outline: 36-Pin QFN

Figure 3 illustrates the package details for the Si5323. Table 4 lists the values for the dimensions shown in the illustration.

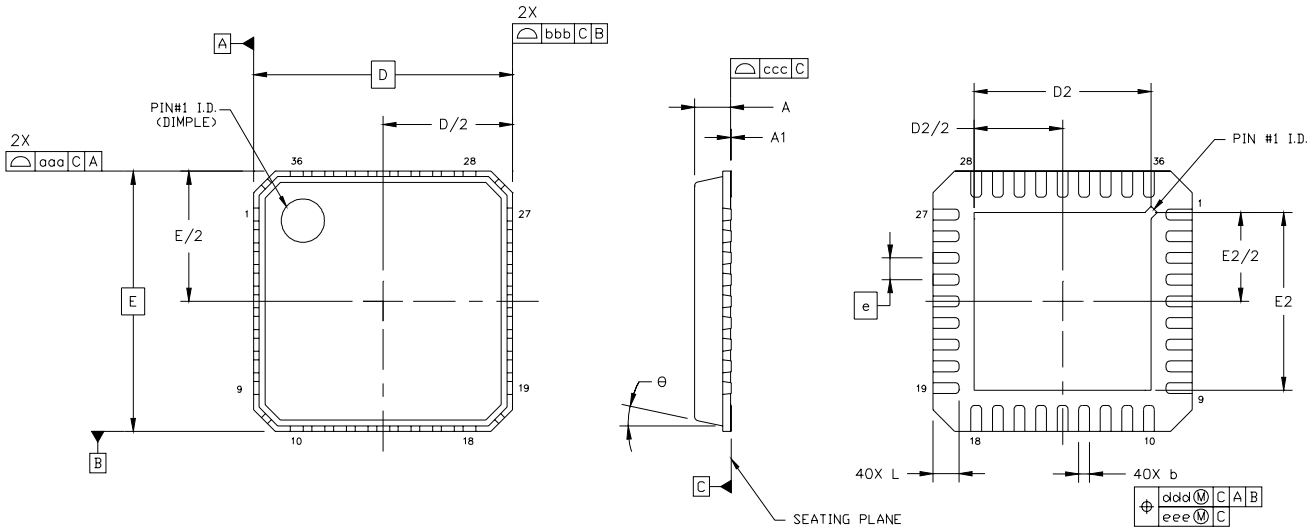


Figure 3. 36-Pin Quad Flat No-lead (QFN)

Table 4. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	3.95	4.10	4.25
e		0.50 BSC	
E		6.00 BSC	
E2	3.95	4.10	4.25

Symbol	Millimeters		
	Min	Nom	Max
L	0.50	0.60	0.70
θ	—	—	12º
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.05

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VJJD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

5. Recommended PCB Layout

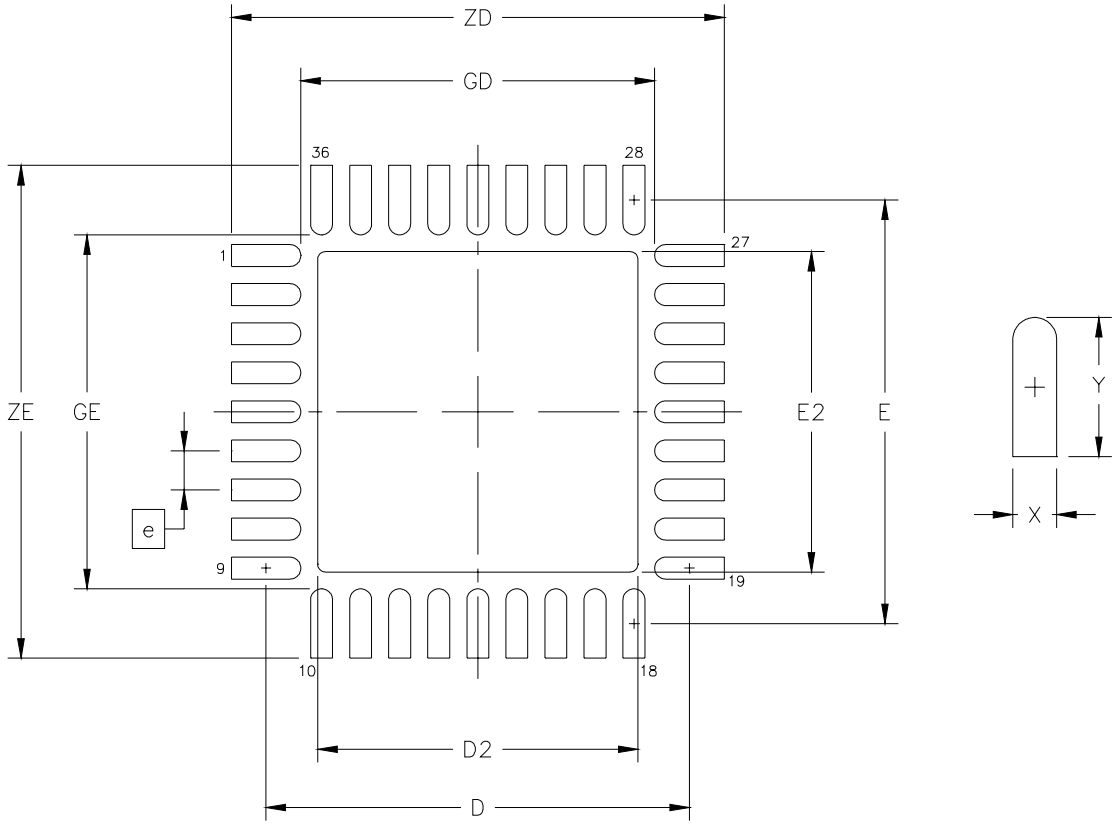


Figure 4. PCB Land Pattern Diagram

Table 5. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	5.42 REF.	
D	5.42 REF.	
E2	4.00	4.20
D2	4.00	4.20
GE	4.53	—
GD	4.53	—
X	—	0.28
Y	0.89 REF.	
ZE	—	6.31
ZD	—	6.31

Notes (General):

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes (Solder Mask Design):

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Notes (Stencil Design):

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Notes (Card Assembly):

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Changed LVTTL to LVCMOS in Table 2, “Absolute Maximum Ratings,” on page 3.
- Added Figure 1, “Typical Phase Noise Plot,” on page 4.
- Updated Figure 2, “Si5323 Typical Application Circuit,” on page 5 to show external reference interface.
- Added RATE0 and expanded the RATE[1:0] description in 2. "Pin Descriptions: Si5323”.
- Updated 3. "Ordering Guide" on page 12.
- Added 5. "Recommended PCB Layout”.

Revision 0.2 to Revision 0.3

- Changed 1.8 V operating range to ±5%.
- Updated Table 1 on page 2.
- Updated Table 2 on page 3.
- Added table under Figure 1 on page 4.
- Updated 1. "Functional Description" on page 6.
- Clarified 2. "Pin Descriptions: Si5323" on page 7 including pull-up/pull-down.
- Updated SFOUT values.

NOTES:

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