



## **Tentative Product Specification**

**Module name: P0430WQLC-T**

**Issue date: 2009/05/27**

**Version: 1.8**

<b>Customer</b>		
<b>Approved by Customer</b>		
<b>Approved by CMEL</b>		
<b>PD Division</b>	<b>ENG Division</b>	<b>QA Dept</b>

**FOR MORE INFORMATION:**

AZ DISPLAYS, INC.

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[Http://www.AZDISPLAYS.com](http://www.AZDISPLAYS.com)

**Note:**

1. The information contained herein may be change without prior notice. It is therefore advisable to contact CHI MEI EL Corp. before designed your product based on this specification.
2. This tentative product specification is for reference, some item or setting maybe changed for evaluation.



**Reversion History**

<b>Version</b>	<b>Date</b>	<b>Page</b>	<b>Description</b>
Ver.1.0	2007/12/26	All	Tentative specification was first issued
Ver.1.1	2008/03/19	10,11,12 15,16,17 18	Add IC Initial Register Setting Modify Pin Assignment Change External Dimension
Ver.1.2	2008/04/08	10 14 19 20	Change Typical Luminance Add System Diagram Add Reliability Test Add Package Drawing
Ver.1.3	2008/07/21	9,10,11	Modify Electro-Optical Characteristic
Ver.1.4	2008/09/24	3 18	Add Weight of Mechanical Data Add Test and Measurement Conditions
Ver.1.5	2008/10/02	19	Modify Package Drawing
Ver.1.6	2008/11/21	10	Modify Life Time
Ver.1.7	2009/04/21	3 9,10,11 19 21	Modify Absolute Maximum Ratings Modify Initial Register Setting Add Handling, Storage, Panel ID Label Naming Rule and Warranty
Ver.1.8	2009/05/27	9,10,11	Modify Electro-Optical Characteristic Change CIE and Gamma



### 1. Purpose:

This documentation defines general product specification for OLED module supplied by CMEL. The information described in this technical specification is tentative. Please Contact CMEL's representative while your product is modified.

### 2. General Description:

- Driving Mode: Active Matrix
- Color Mode: Full Color (16M color)
- Driver IC: HX5116, COG Assembly
- Interface: 8bit serial RGB and 24bit parallel RGB interface
- Application: Portable DVD, PMP, GPS, Photo Frame etc.
- RoHS Compatible

### 3. Mechanical Data:

No.	Items	Specification	Unit
1	Diagonal Size	4.3	Inch
2	Resolution	480 x RGB x 272	
3	Pixel Pitch	198 x 198	um
4	Active Area	95.0 x 53.8	mm
5	Outline Area	103.5 x 67	mm
6	Thickness	2.05	mm
7	Weight	39.6	g

### 4. Absolute Maximum Ratings:

Absolute ratings of environment :

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T <sub>ST</sub>	-40	+85	°C	(1)
Operating Ambient Temperature	T <sub>OP</sub>	-20	+60	°C	(2)

Note (1) The storage duration for both critical temperature (-40 & 85°C) meet reliability test criteria.

(2) The operating duration for both critical temperature (-20 & 60°C) meet reliability test criteria.

## 5. Electrical Characteristic:

### DC Characteristic

#### DC Characteristics

(Unless otherwise specified, Voltage Referenced to VSS = 0V, VCC = 1.5 to 3.6V, T<sub>A</sub> = -20 to 70C)

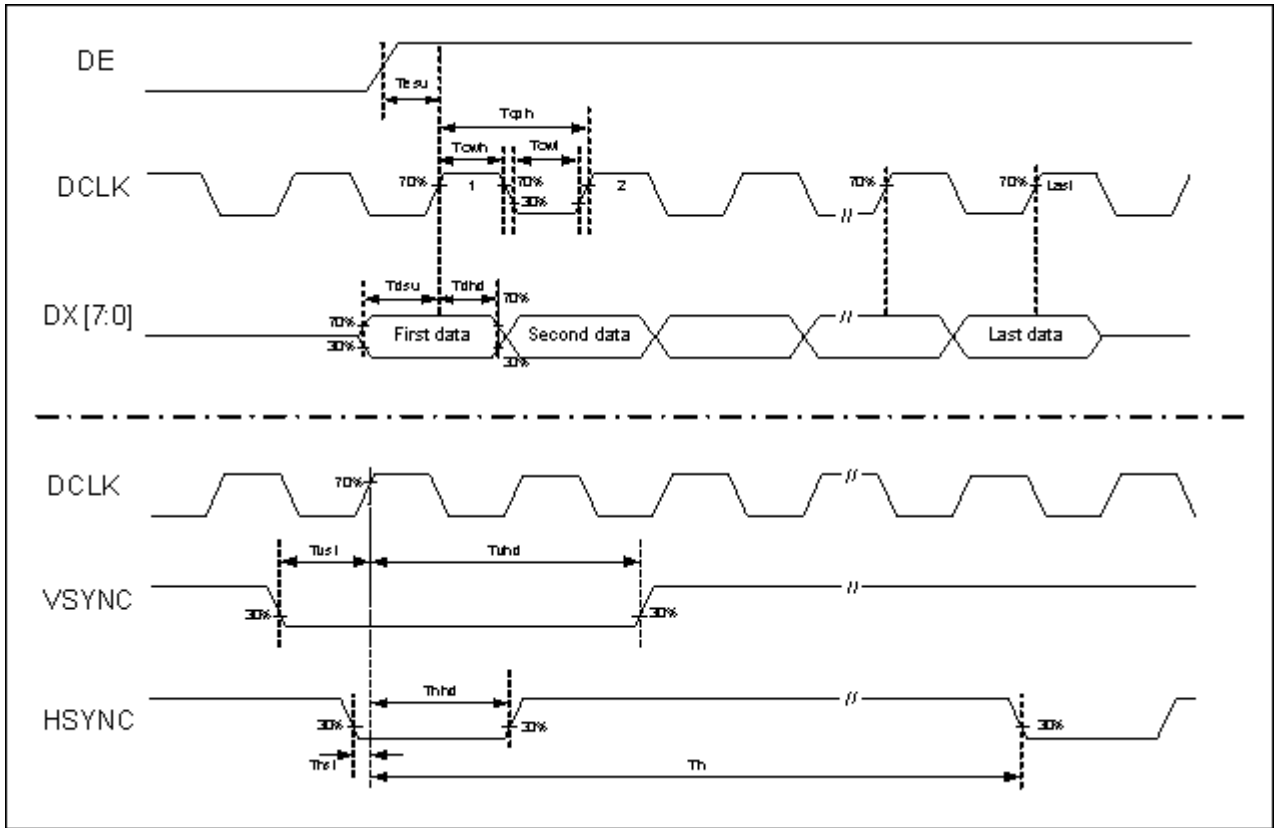
Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
System power supply pins of the logic block	VCC	-	1.5	-	3.6	V
Booster Reference Supply Voltage Range	VCI	-	3.0	-	3.6	V
DDVDH Output Voltage 1	DDVDH	Set CP1X=0	4.9	5.1	5.3	V
DDVDH Output Voltage 2	DDVDH	Set CP1X=1	5.8	6.0	6.2	V
VGAM1OUT Output Voltage 1	VGAM1OUT	Set CP1X=0	4.7	4.8	4.9	V
VGAM1OUT Output Voltage 2	VGAM1OUT	Set CP1X=1	5.7	5.8	5.9	V
Gate driver High Output Voltage	VGH	-	+3	-	+8	V
Gate driver Low Output Voltage	VGL	-	-8	-	-3	V
OLED Diode Refer Voltage	ARREF	-	-8	-	+8	V
Logic High Output Voltage	VOH	I <sub>out</sub> =-400μA	0.8 * VCC	-	VCC	V
Logic Low Output Voltage	VOL	I <sub>out</sub> =400μA	0	-	0.2 * VCC	V
Logic High Input voltage	VIH	-	0.8 * VCC	-	VCC	V
Logic Low Input voltage	VIL		0	-	0.2 * VCC	V
Logic Input Current	IIL/IIH	No pull up or pull low	-1	-	1	μA
Pull high resistance	RH	Pull up pins	600	900	1200	KΩ
Pull low resistance	RL	Pull low pins	600	900	1200	KΩ
High Output Current	IOH	S1~S107, V <sub>o</sub> =4.9V vs. 4V	50	-	-	μA
Low Output Current	IOL	S1~S107, V <sub>o</sub> =0.1V vs. 1V	-	-	-50	μA
Output leakage Current	IOZ	-	-1	-	1	μA
Output voltage offset	VOS	S1~S107, V <sub>o</sub> =0.1V~DDVDH-0.1V		±10		mV
Output voltage deviation	VOD	S1~S107, V <sub>o</sub> =0.1V~DDVDH-0.1V		±10		mV
Analog standby current	ISTB	VCI=3.0V, Stand by mode		-	10	uA
Analog operating current	IVCI	VCI=3.0V, S1~S160 no load		-	20	mA
Logic Pins Input Capacitance	CIN	-	-	5	7.5	pF



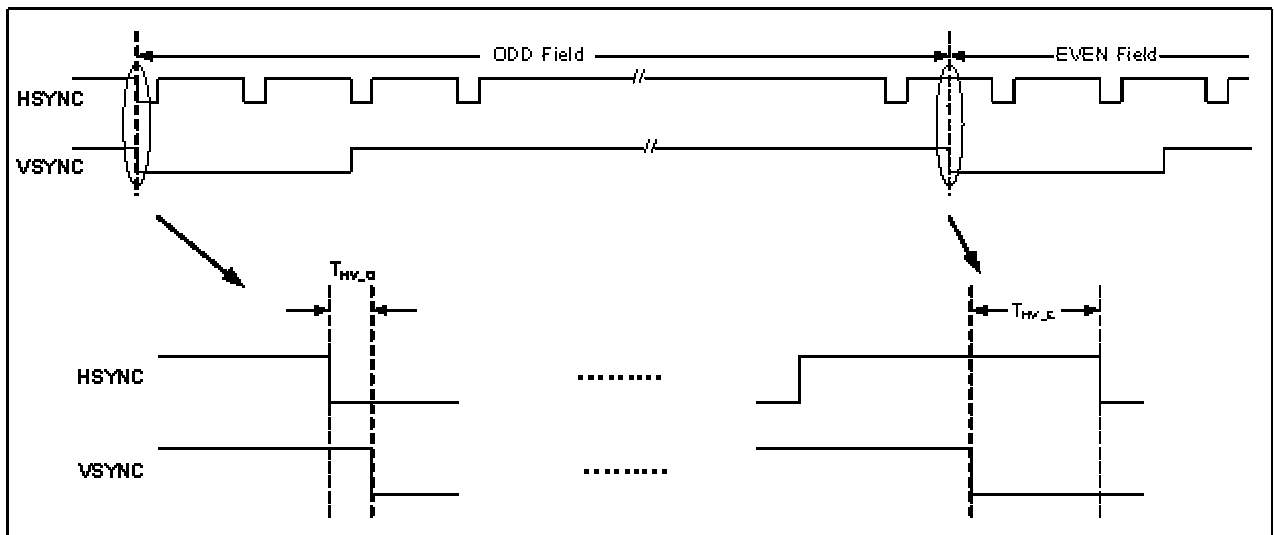
**AC Characteristic**

AC Electrical Characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
HSYNC setup time	$T_{hst}$	10	-	-	ns
HSYNC hold time	$T_{hhd}$	10	-	-	ns
VSYNC setup time	$T_{vst}$	10	-	-	ns
VSYNC hold time	$T_{vhd}$	10	-	-	ns
Data setup time	$T_{dsu}$	10	-	-	ns
Data hold time	$T_{dhd}$	10	-	-	ns
DE setup time	$T_{esu}$	10	-	-	ns
VSYNC falling to HSYNC falling time on odd field @ RGB mode	$T_{HV\_O}$	-4	0	+4	$T_{CPH}$
VSYNC falling to HSYNC falling time on even field @ RGB mode	$T_{HV\_E}$	0.4	0.5	0.6	$T_H$
Source output settling time	$T_{ST}$	-	3	-	$\mu s$
Source output loading R	$R_{SL}$	-	25	-	K ohm
Source output loading C	$C_{SL}$	-	16	-	pF
Gate signals settling time (90%)	$T_{GL}$	-	0.5	-	$\mu s$
Gate signals loading R	$R_{GL}$	-	5.6	-	K ohm
Gate signals loading C	$C_{GL}$	-	30	-	pF
SW signals settling time (90%)	$T_{SW}$	-	0.6	-	$\mu s$
SW signals loading R	$R_{SW}$	-	1.4	-	K ohm
SW signals loading C	$C_{SW}$	-	85.5	-	pF



Clock and Data input waveforms



Define the HSYNC to VSYNC timing for RGB mode

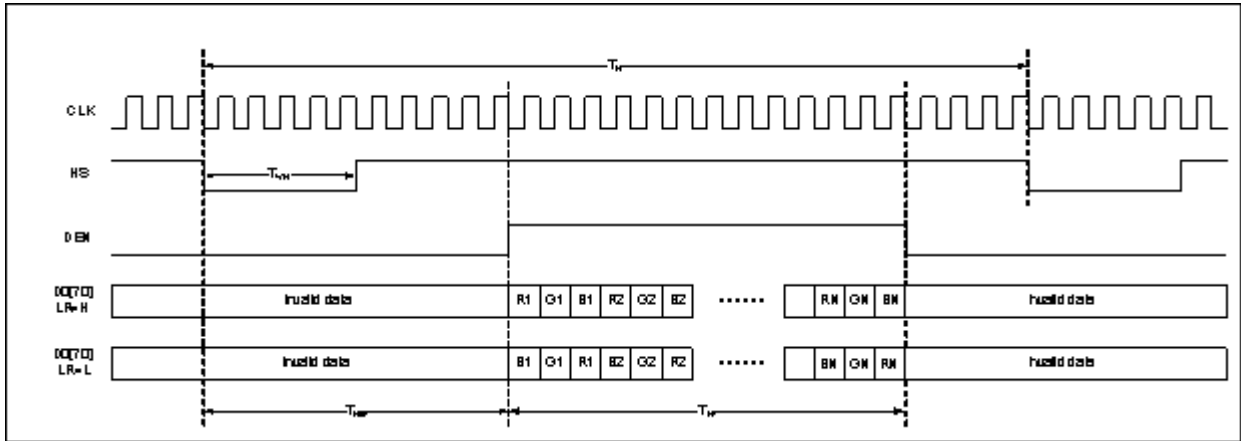


5.2.2 480RGB X 272 serial RGB interface

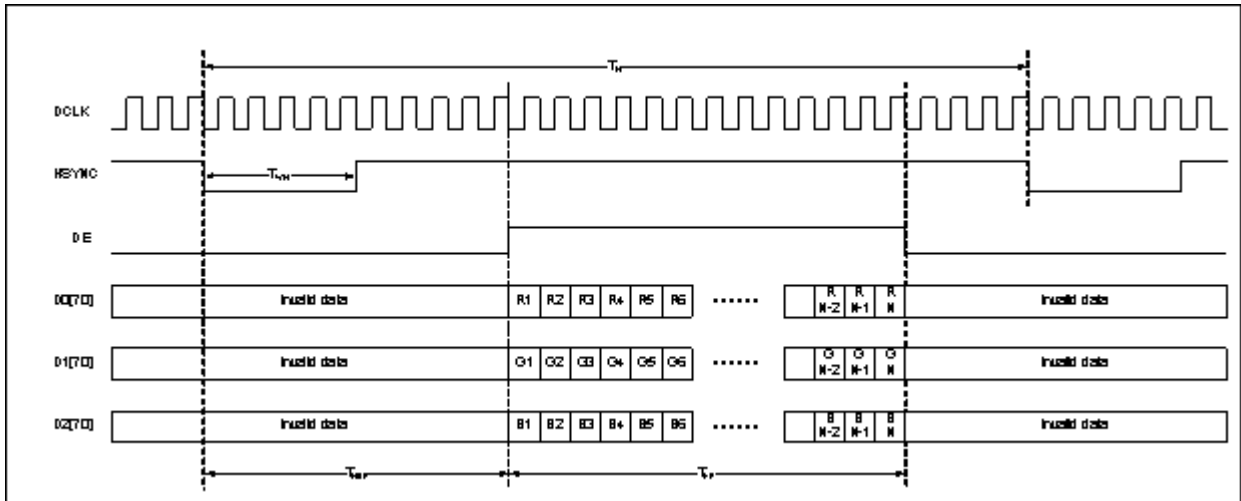
PARAMETER	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	$F_{CPH}$	33.3	-	-	MHz
DCLK period	$T_{CPH}$	-	-	30	ns
DCLK pulse duty	$T_{CWH}$	40	50	60	%
HSYNC period	$T_H$	-	1836	-	$T_{CPH}$
HSYNC pulse width	$T_{WH}$	5	90	-	$T_{CPH}$
HSYNC-first horizontal data time	$T_{HBP}$	274	306	337	$T_{CPH}$
DE pulse width	$T_{EP}$	-	1440	-	$T_{CPH}$
VSYNC pulse width	$T_{WV}$	1	3	5	$T_H$
VSYNC-1 <sup>st</sup> Data input (DE) time	$T_{VBP}$	4	20	35	$T_H$
VSYNC period	$T_V$	302	-	-	$T_H$

5.2.2 480RGB X 272 parallel RGB interface

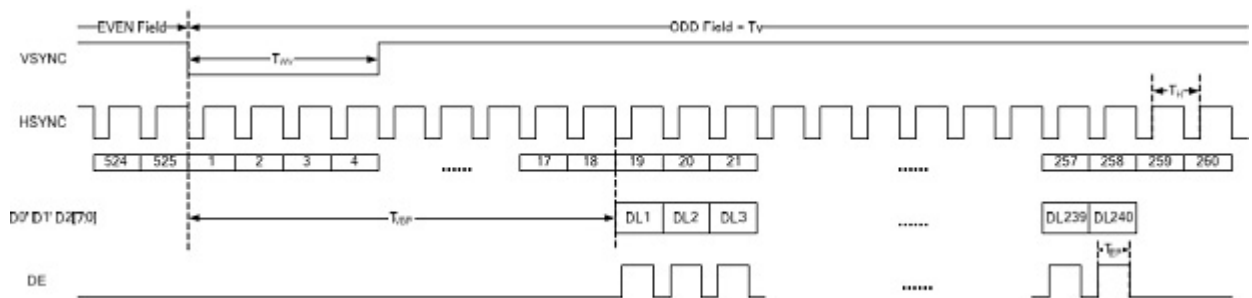
PARAMETER	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	$F_{CPH}$	11.1	-	-	MHz
DCLK period	$T_{CPH}$	-	-	90	ns
DCLK pulse duty	$T_{CWH}$	40	50	60	%
HSYNC period	$T_H$	-	612	-	$T_{CPH}$
HSYNC pulse width	$T_{WH}$	5	30	-	$T_{CPH}$
HSYNC-first horizontal data time	$T_{HBP}$	70	102	133	$T_{CPH}$
DE pulse width	$T_{EP}$	-	480	-	$T_{CPH}$
VSYNC pulse width	$T_{WV}$	1	3	5	$T_H$
VSYNC-1 <sup>st</sup> Data input (DE) time	$T_{VBP}$	4	20	35	$T_H$
VSYNC period	$T_V$	302	-	-	$T_H$



Serial RGB Horizontal Data Format



Parallel RGB Horizontal Data Format



Digital RGB Vertical Data Format



**6. Electro-Optical Characteristic:**

Items	Symbol	Min	Typ.	Max	Unit	Remark
Operating Luminance	L	170	200	230	Cd/m <sup>2</sup>	(1)(5)
Power Consumption	Pon		700	950	mW	30% pixels on (1)
Maximum Current	Icc		220	302	mA	(1)
Response Time	Tres			50	uS	(2)
CIE <sub>x</sub> (White)	W <sub>x</sub>	0.23	0.28	0.33	-	(5)
CIE <sub>y</sub> (White)	W <sub>y</sub>	0.25	0.30	0.35	-	(5)
CIE <sub>x</sub> (Red)	R <sub>x</sub>	0.615	0.655	0.695	-	(5)
CIE <sub>y</sub> (Red)	R <sub>y</sub>	0.300	0.340	0.380	-	(5)
CIE <sub>x</sub> (Green)	G <sub>x</sub>	0.195	0.235	0.275	-	(5)
CIE <sub>y</sub> (Green)	G <sub>y</sub>	0.610	0.650	0.690	-	(5)
CIE <sub>x</sub> (Blue)	B <sub>x</sub>	0.100	0.140	0.180	-	(5)
CIE <sub>y</sub> (Blue)	B <sub>y</sub>	0.105	0.145	0.185	-	(5)
Viewing Angle	VA	160	170		Degree	(3)
Contrast	CR	5000:1	10000:1			(4)
Operation Lifetime	LTop	30000			Hrs	(1)(6)

Note:

Measuring surrounding: dark room

Surrounding temperature: 25°C

(1) Test condition:

a. AR\_VDD= **5.2V +/-0.03V**, AR\_VSS= **-4.8V +/-0.03V**

b. IC Initial Register Setting:

<b>24-bit parallel RGB (DE)</b>	<b>Ver. 5</b>
Index_out(0x04); Parameter_out(0x23); //set display mode 24-bit parallel RGB (DE)	
Index_out(0x05); Parameter_out(0x82); //set display mode	
Index_out(0x07); Parameter_out(0x0F); //set driver capability	
Index_out(0x34); Parameter_out(0x18); //set display timing	
Index_out(0x35); Parameter_out(0x28); //set display timing	
Index_out(0x36); Parameter_out(0x16); //set display timing	
Index_out(0x37); Parameter_out(0x01); //set display timing	
Index_out(0x02); Parameter_out(0x02); //OTP On	



Index_out(0x0A);	Parameter_out(0x8A); //VGHVGL=+/-6V
Index_out(0x09);	Parameter_out(0x26); //VGAM1OUT=4.95V
Index_out(0x10);	Parameter_out(0x7A); //set R slop
Index_out(0x11);	Parameter_out(0x78); //set G slop
Index_out(0x12);	Parameter_out(0x75); //set B slop
Index_out(0x13);	Parameter_out(0x00); //set R_0
Index_out(0x14);	Parameter_out(0x02); //set R_10
Index_out(0x15);	Parameter_out(0x00); //set R_36
Index_out(0x16);	Parameter_out(0x01); //set R_80
Index_out(0x17);	Parameter_out(0x01); //set R_124
Index_out(0x18);	Parameter_out(0x01); //set R_168
Index_out(0x19);	Parameter_out(0x01); //set R_212
Index_out(0x1A);	Parameter_out(0x04); //set R_255
Index_out(0x1B);	Parameter_out(0x00); //set G_0
Index_out(0x1C);	Parameter_out(0x07); //set G_10
Index_out(0x1D);	Parameter_out(0x03); //set G_36
Index_out(0x1E);	Parameter_out(0x03); //set G_80
Index_out(0x1F);	Parameter_out(0x05); //set G_124
Index_out(0x20);	Parameter_out(0x05); //set G_168
Index_out(0x21);	Parameter_out(0x03); //set G_212
Index_out(0x22);	Parameter_out(0x0A); //set G_255
Index_out(0x23);	Parameter_out(0x00); //set B_0
Index_out(0x24);	Parameter_out(0x03); //set B_10
Index_out(0x25);	Parameter_out(0x01); //set B_36
Index_out(0x26);	Parameter_out(0x00); //set B_80
Index_out(0x27);	Parameter_out(0x00); //set B_124
Index_out(0x28);	Parameter_out(0x00); //set B_168
Index_out(0x29);	Parameter_out(0x00); //set B_212
Index_out(0x2A);	Parameter_out(0x01); //set B_255
Index_out(0x06);	Parameter_out(0x03); //set display on
AR_VDD= +5.2V	
AR_VSS= -4.8V	

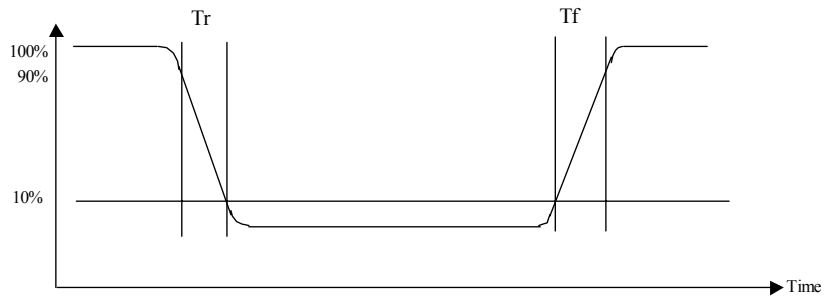
<b>8-bit serial RGB (DE)</b>		<b>Ver. 5</b>
Index_out(0x04);	Parameter_out(0x21); //set display mode 8-bit serial RGB (DE)	
Index_out(0x05);	Parameter_out(0x82); //set display mode	
Index_out(0x07);	Parameter_out(0x0F); //set driver capability	



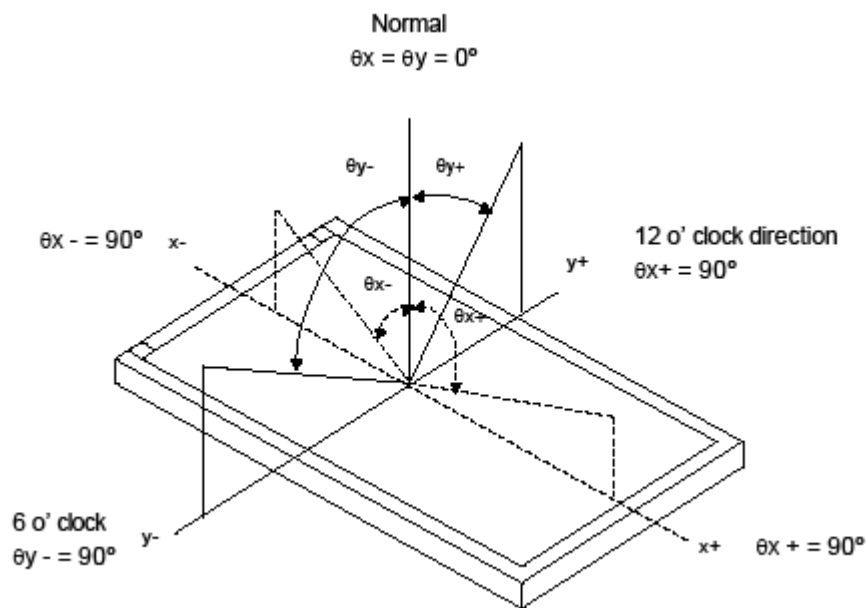
Index_out(0x34);	Parameter_out(0x48); //set display timing
Index_out(0x35);	Parameter_out(0x78); //set display timing
Index_out(0x36);	Parameter_out(0x42); //set display timing
Index_out(0x37);	Parameter_out(0x01); //set display timing
Index_out(0x02);	Parameter_out(0x02); //OTP On
Index_out(0x0A);	Parameter_out(0x8A); //VGHVGL=+/-6V
Index_out(0x09);	Parameter_out(0x26); //VGAM1OUT=4.95V
Index_out(0x10);	Parameter_out(0x7A); //set R slop
Index_out(0x11);	Parameter_out(0x78); //set G slop
Index_out(0x12);	Parameter_out(0x75); //set B slop
Index_out(0x13);	Parameter_out(0x00); //set R_0
Index_out(0x14);	Parameter_out(0x02); //set R_10
Index_out(0x15);	Parameter_out(0x00); //set R_36
Index_out(0x16);	Parameter_out(0x01); //set R_80
Index_out(0x17);	Parameter_out(0x01); //set R_124
Index_out(0x18);	Parameter_out(0x01); //set R_168
Index_out(0x19);	Parameter_out(0x01); //set R_212
Index_out(0x1A);	Parameter_out(0x04); //set R_255
Index_out(0x1B);	Parameter_out(0x00); //set G_0
Index_out(0x1C);	Parameter_out(0x07); //set G_10
Index_out(0x1D);	Parameter_out(0x03); //set G_36
Index_out(0x1E);	Parameter_out(0x03); //set G_80
Index_out(0x1F);	Parameter_out(0x05); //set G_124
Index_out(0x20);	Parameter_out(0x05); //set G_168
Index_out(0x21);	Parameter_out(0x03); //set G_212
Index_out(0x22);	Parameter_out(0x0A); //set G_255
Index_out(0x23);	Parameter_out(0x00); //set B_0
Index_out(0x24);	Parameter_out(0x03); //set B_10
Index_out(0x25);	Parameter_out(0x01); //set B_36
Index_out(0x26);	Parameter_out(0x00); //set B_80
Index_out(0x27);	Parameter_out(0x00); //set B_124
Index_out(0x28);	Parameter_out(0x00); //set B_168
Index_out(0x29);	Parameter_out(0x00); //set B_212
Index_out(0x2A);	Parameter_out(0x01); //set B_255
Index_out(0x06);	Parameter_out(0x03); //set display on
AR_VDD= +5.2V	
AR_VSS= -4.8V	



(2) Response Time test condition



(3) Viewing angle test condition:



(4) Contrast

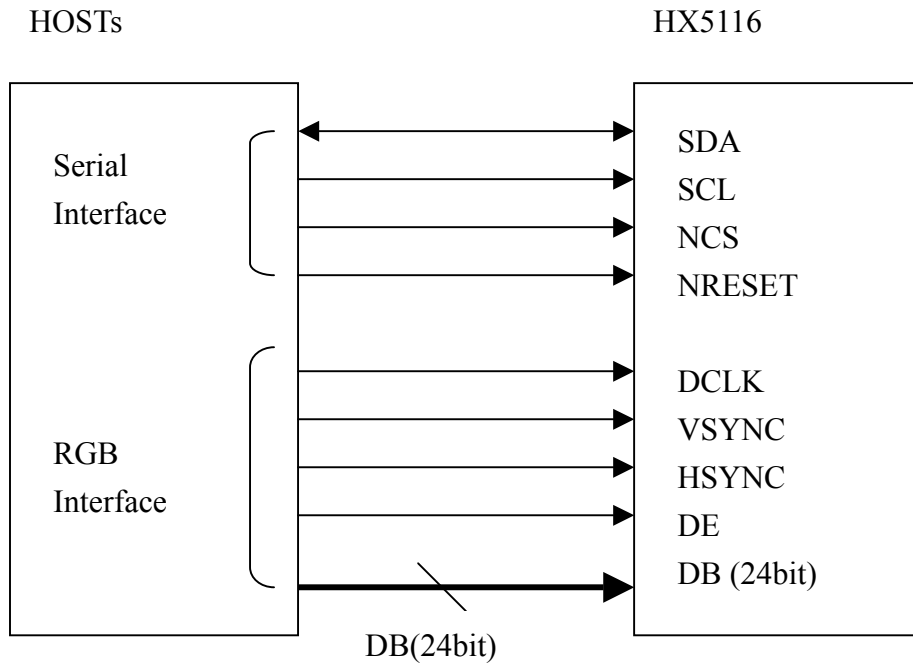
$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

(5) Optical tester: CA210

(6) Operation Life Time is defined when the luminance decay to less than 50% of the initial luminance during the average operation. The Luminance of the average operation is defined picture changing 30% power consumption at full on 200nits.



7. System Diagram:





8. Pin Assignment:

PIN	Symbol	I/O	Description	Remarks			
1	TP1	I	Touch panel P1				
2	TP2	I	Touch panel P2				
3	TP3	I	Touch panel P3.				
4	TP4	I	Touch panel P4				
5	AR_VSS	I	Negative voltage for OLED				
6	AR_VSS	I	Negative voltage for OLED				
7	TEST1_VS	open	<b>CMEL test pin, it must be open.</b>				
8	AR_VDD	I	Positive voltage for OLED				
9	AR_VDD	I	Positive voltage for OLED				
10	TEST2_VD	open	<b>CMEL test pin, it must be open.</b>				
11	ARREF	I/O	Panel refers voltage of the regulator ARREF or external input voltage. (-8V~+8V)				
12	VGL	I/O	Low Voltage output of regulator VGL or external input voltage. (-3V~8V)				
13	VGH	I/O	High Voltage output of regulator VGH or external input voltage. (+3V~+8V)				
14	LVO	I/O	<b>Negative output voltage of the booster2. (-8.5V)</b>				
15	C22N	I/O	Connect to the step-up circuit, capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.				
16	C22P						
17	HVO	I/O	Positive output voltage of the booster2. (8.5V)				
18	C21P	I/O	Connect to the step-up circuit, capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.				
19	C21N						
20	C11N	I/O	Connect to the step-up circuit, 4capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.				
21	C11P						
22	C12N						
23	C12P						
24	PVSS	P	Charge pump ground pin, it must connect to external ground.				
25	DDVDH	I/O	Output voltage of the booster1. (5.1V/6.0V)				
26	VSSA	P	<b>Analog ground pin. It must connect to external ground.</b>				
27	VSSA	P	<b>Analog ground pin. It must connect to external ground.</b>				
28	VCI	P	<b>A power supply for the Analog circuit. (3.0V~3.6V)</b>				
29	VCI	P	<b>A power supply for the Analog circuit. (3.0V~3.6V)</b>				
30	VGAM1OUT	I/O	Output voltage of the VGAM1OUT regulator and used positive power of source driver. (4.8V/5.8V)				
31	VDDD	I/O	Internal logic voltage input or output pin VDC_ENB=0, VDDD is output, please connect to 1uF capacitor.				
			<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>VDC0</td> <td>VDDD</td> <td>Status</td> </tr> </table>	VDC0	VDDD	Status	
VDC0	VDDD	Status					



		<table border="1"> <tr> <td>0</td> <td>1.8V</td> <td>Normal display</td> </tr> <tr> <td>1</td> <td>2.5V</td> <td>OTP program</td> </tr> </table>		0	1.8V	Normal display	1	2.5V	OTP program	
0	1.8V	Normal display								
1	2.5V	OTP program								
		VDC_ENB=1, VDDD is input. (Input range = 1.6V~2.75V)								
32	VCC	P	A power supply for the Digital circuit. (1.5V~3.6V)							
33	VSSD	P	Digital ground pin. It must connect to external ground.							
34	NRESET	I	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied. (Normally pull high)							
35	NCS	I	Serial Interface chip enable pin. (Normally pull high)							
36	SCL	I	Serial Interface clock input pin. (Normally pull high)							
37	SDA	I	Serial Interface data line. (Normally pull high)							
38	DE	I	Data enable: When VSYNC+HSYNC+DE mode, DE=H: Data enable, DE=L: Data disable (Black). (Normally pull low)							
39	VSYNC	I	Frame synchronizing signal. If VSPL=0: Active low. If VSPL=1: Active high.							
40	HSYNC	I	Line synchronizing signal. If HSPL=0: Active low. If HSPL=1: Active high.							
41	DCLK	I	Dot clock signal. If DPL=0: Data are input on the rising edge of DOTCLK. If DPL=1: Data are input on the falling edge of DOTCLK.							
42	D27	I	Digital data input. DX0 is LSB and DX7 is MSB. (Normally pull low) 1. If parallel RGB input mode is used, D0X, D1X, and D2X indicate R, G, and B data in turn. 2. If serial RGB or RGBD or CCIR601 or CCIR656 input mode is selected, only D07~D00 are used, and others short to GND. <b>DX7~DX0 has 8-bit width, respectively to compose 16,777,216 color and 256 gray scale of 1 pixel.</b>							
43	D26									
44	D25									
45	D24									
46	D23									
47	D22									
48	D21									
49	D20									
50	D17									
51	D16									
52	D15									
53	D14									
54	D13									
55	D12									
56	D11									
57	D10									
58	D07									



59	D06			
60	D05			
61	D04			
62	D03			
63	D02			
64	D01			
65	D00			
66	TEST3_W	open	CMEL test pin, it must be open.	
67	AR_VDD	I	Positive voltage for OLED	
68	AR_VDD	I	Positive voltage for OLED	
69	AR_VSS	I	Negative voltage for OLED	
70	AR_VSS	I	Negative voltage for OLED	
71	TEST4_P	open	CMEL test pin, it must be open.	





**10. Reliability Test:**

No	Item	Specification
1	High Temp. Storage	85°C, 240hr
2	Low Temp. Storage	-40°C, 240hr
3	High Temp. Operation	60°C, 240hr
4	Low Temp. Operation	-20°C, 240hr
5	High Temp./ High Hum. Storage	85°C, 85 % RH, 120 hr
6	High Temp./ High Hum. Operation	60°C, 90 % RH, 240hr
7	Thermal Shock storage	-40°C, 30 min. --> 85°C, 30 min., 100 cycles
8	ESD	(1) Contact discharge mode: +/- 2kV, 3 times/FPC pin (2) Air discharge mode: +/- 8 kV, 10 times/central area
9	Packing Test	Drop 1 corner, 3 sides, 6 faces, 1 time for each; Height: follow ISTA standard. Follow ISTA standard, 1.14Grms Test axis: X, Y, Z

**Test and measurement conditions**

- All measurements shall not be started until the specimens attain to temperature stability.
- The degradation of Polarizer is ignored for item 1, 5 & 6.
- The test pattern at operating condition is 30%P.C. alternating pictures.

**Evaluation Criteria**

- No damage to glass or encapsulation
- No drastic change to display
- Defects / Mura follow product specification
- Luminance: Within +/-50% of initial value
- Current consumption: within +/-50% of initial value



### 11. Handling:

Do not scratch the surface of the polarizer film as it is easily damaged.

When cleaning the display surface, use soft cloth with solvent (as recommended below) and wipe lightly

- Ethyl alcohol
- Isopropyl alcohol

Do not wipe the display surface with dry or hard materials that damage the polarizer surface.

Since this OLED panel is made of glass, dropping the module or banging it against hard objects may cause cracks or fragmentation.

Do not disassemble the OLED module as it may cause permanent damage.

Hold OLED very carefully when placing OLED module into the system housing. Do not excessive stress or pressure to OLED module.

### 12. Storage:

Storing in a polyethylene bag with the opening sealed.

Placing in a dark place where neither exposure to direct sunlight nor any fluorescent light is permitted and keep at room temperature & room humidity.

Storing with no contact with polarizer surface.

( It is recommended to store them in the inner container which we delivered. )

### 13. Panel ID Label Naming Rule

Single format example:

P0730WQLC-TA	Model ID(Gamma Code)
T1895066NG0113	Panel ID
A882501EL100013A	Module Information



14. Package:

Work

Description

Date

Changed\_By/Approved\_By

ECN No.

Remark

1. One tray with 6 pcs panel module.
2. Take EPE sheet 1 pcs above the tray.
3. Take empty tray 1 pcs top of the substantial tray.
4. Circle the belt 1.5 loops around and fixed the trays by velcro (魔鬼沾).
5. Place one stack with a Drier into an anti-static bag.
6. Use clean tape to seal the bag.

FPC Pin direction must follow the arrowhead MP number label must upturn

x 1pcs(Empty)

x 10pcs(panel 60pcs)

Final Hot Sealing

S/N Label

Carton Label

9. One box package.

8. Place three stacks into the carton.

7. Take EPE foam 2 pcs to hold one Bag.

9. Carton

8. Carton Label(Must align the corner points)

9	Carton	1	box	78-X0000039
8	Carton Label	1	pc	78-X0000011
7	EPE Foam	6	pc	78-X0000022
6	S/N Label	3	pc	78-X0000008
5	Anti-Static vacuum bag	3	pc	78-X0000006
4	Drier	3	pc	78-X0000001
3	Belt	6	pc	78-X0000060
2	EPE Sheet	30	pc	78-X0000041
1	Tray	33	pc	78-X0000040

TITLE		PACKAGE P0430M23303A		DRAWING	
Approved	JC KAO	Drawing No.	P0430M23303A	2D REV.	A
Checked	LIXY TSAI	Part No.		3D REV.	
Drawer	EDMUND HUANG	Material		Sheet	1 / 1
Designer	EDMUND HUANG	Date	25/Sept/03	Scale	1:1
			Unit	mm	

CHI MEI EL CORPORATION

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## 15. Warranty

Warranty term is 12 months of reliability characteristics of quality level after the outgoing date in Chi Mei EL Corporation.

Chi Mei EL Corporation could compensate for defectives, which happen within warranty term under condition that products should be stored or be used as specified under normal condition within the contents of specification.

Otherwise, it is unable to compensate for defectives when below items happen:

- (1) Defectives happen by customer's mistake such as careless handling or design change, etc.
- (2) Defectives caused by natural uncontrolled disaster.
- (3) The direct and/or indirect damage caused by unapproved or disagreed use behavior, condition, environment, which is over or not belong to the product specification or other related technique document published by CMEL.

After 12 months of warranty term, all replacement for defectives will be charged.