28F001BX-T/B 1M (128K x 8) CMOS FLASH MEMORY

SmartDie Product Specification

- **High Integration Blocked Architecture**
  - **One 8 KByte Boot Block with Lock Out**
  - **Two 4 KByte Parameter Blocks**
  - **One 112 KByte Main Block**
  - **T = Top Boot, B = Bottom Boot**
- **100,000 Erase/Program Cycles Per Block**
- **Simplified Program and Erase**
  - **Automated Algorithms via On-Chip Write State Machine (WSM)**
- **SRAM-Compatible Write Interface**
- **Deep-Powerdown Mode**
  - **0.05 μA I_{CC} Typical**
  - **0.8 μA I_{PP} Typical**
- **12.0V $\pm$5% V_{PP}**
- **High-Performance Read**
  - **70 ns Maximum Access Time**
  - **5.0V $\pm$5% V_{CC}**
- **Hardware Data Protection Feature**
  - **Erase/Write Lockout During Power Transitions**
- **ETOX™ III Nonvolatile Flash Technology**
  - **EPROM-Compatible Process Base**
  - **High-Volume Manufacturing Experience**
- **Intel SmartDie Product**
  - **Full AC/DC Testing at Die Level**
  - **0°C–80°C (Junction) Temperature Range**
  - **Available in 70 ns, 90 ns and 120 ns Access Times**

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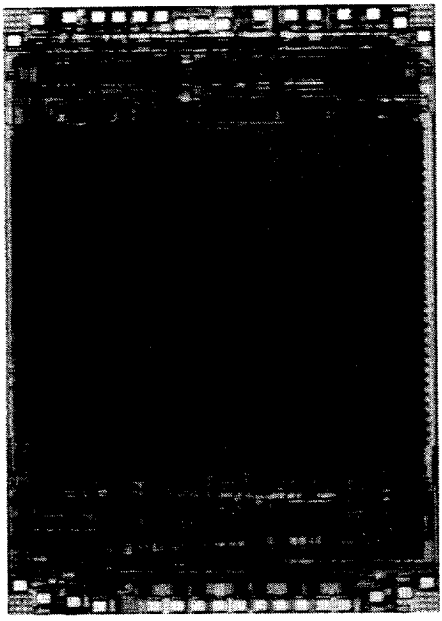
NOTICE: This document contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. This specification is subject to change without notice.

REFERENCE INFORMATION: The information in this document is provided as a supplement to the Standard Package Data Sheet on a specific product. Please reference the Standard Package Data Sheet (Order No. 290406) for additional product information and specifications not found in this document.

*Other brands and names are the property of their respective owners.

October 1994
Order Number: 271303-001



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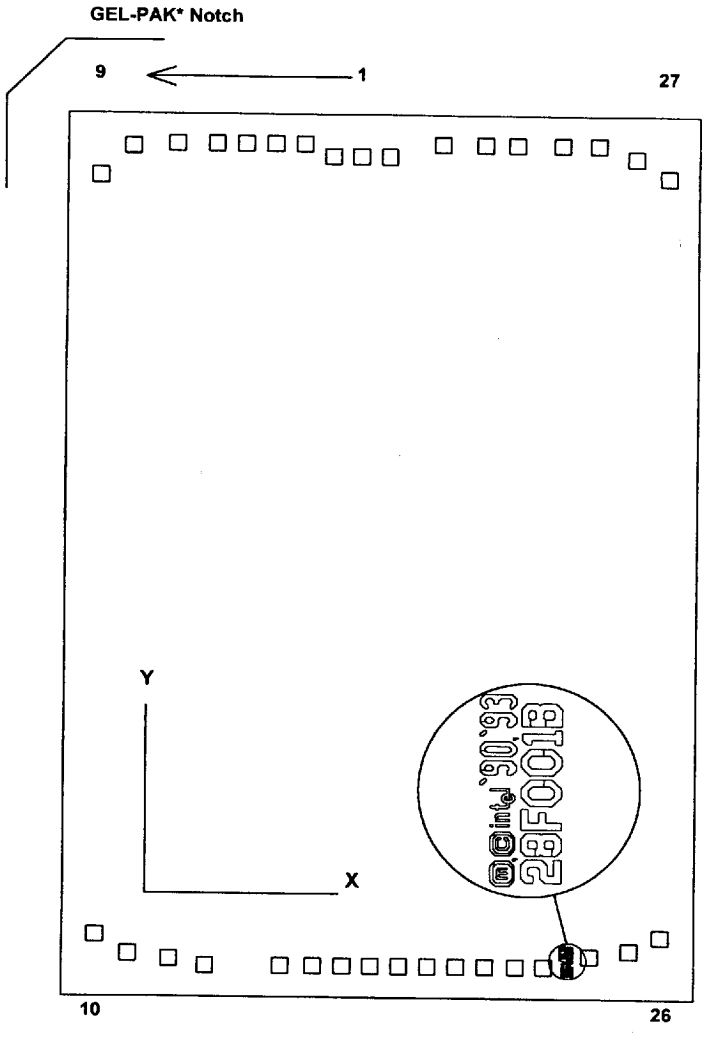
28F001BX-T/B 1 M (128K x 8) CMOS Flash Memory Die Photo

1.0 DIE SPECIFICATIONS



NOTES:
Figure 1 indicates actual orientation of the die in the GEL-PAK* (shipping container). The 45° notch shown on the plot indicates the location of the 45° notch on the GEL-PAK.

Figure 1. 28F001BX-T/B 1M (128K x 8) CMOS FLASH MEMORY Die/Bond Pad Layout

1.1 Pad Description

Table 1. 28F001BX-T/B 1M (128K x 8) CMOS Flash Memory Bond Pad Center Data

Pad	Signal	Pad Center			
		(Mils = 0.001 in.)		(Microns)	
		X	Y	X	Y
001	V_{CC}	−5.7	106.1	−144	2695
002	V_{PP}	−13.0	106.1	−329	2695
003	A16	−20.3	109.3	−516	2776
004	A15	−27.8	109.3	−706	2776
005	A12	−35.4	109.3	−900	2776
006	A7	−42.9	109.3	−1089	2776
007	A6	−53.1	109.3	−1348	2776
008	A5	−64.4	108.7	−1636	2761
009	A4	−72.7	100.9	−1847	2564
010	A3	−72.5	−101.1	−1843	−2569
011	A2	−64.1	−106.1	−1629	−2695
012	A1	−53.5	−107.5	−1360	−2730
013	A0	−44.3	−109.3	−1125	−2775
014	DQ0	−24.9	−109.3	−631	−2776
015	DQ1	−16.5	−109.3	−420	−2776
016	DQ2	−9.0	−109.3	−228	−2776
017	V_{SS}	−1.7	−109.3	−42	−2776
018	V_{SS}	5.6	−109.3	143	−2776
019	DQ3	12.9	−109.3	328	−2776
020	DQ4	20.3	−109.3	514	−2776
021	DQ5	27.7	−109.3	704	−2776
022	DQ6	35.5	−109.3	901	−2776
023	DQ7	42.8	−109.3	1086	−2776
024	CE#	54.4	−106.3	1382	−2700
025	A10	64.5	−104.8	1639	−2662
026	OE#	72.5	−101.1	1841	−2569
027	A11	73.2	100.9	1858	2564
028	A9	64.9	105.9	1648	2690
029	A8	55.3	109.3	1405	2776
030	A13	46.0	109.3	1167	2776
031	A14	34.3	109.3	870	2776

Table 1. 28F001BX-T/B 1M (128K x 8) CMOS Flash Memory Bond Pad Center Data (Continued)

Pad	Signal	Pad Center			
		(Mils = 0.001 in.)		(Microns)	
		X	Y	X	Y
032	PWD#	26.1	109.3	664	2776
033	WE#	15.2	109.3	386	2776
034	V_{CC}	1.6	106.1	41	2695

Notes:
1. X-Y pad coordinates represent bond pad centers and are relative to center of die.
2. The symbol "#" is used at the end of the signal name to denote an active low signal.

2.0 INTEL DIE PRODUCTS PROCESSING

TEST PROCEDURE

Intel has instituted full-speed functional testing at the die level for all SmartDie products. This level of testing is ordinarily performed only after assembly into a package. Each die is tested to the same electrical limits as the equivalent packaged unit.

WAFER PROBE

Wafer probing is performed on every wafer produced in an Intel Fab. The process consists of specific electrical tests as well as device-specific functionality tests.

At the wafer level, built-in test structures are probed to verify that device electrical characteristics are in control and meet specifications. Measurements are made of transistor threshold voltages and current characteristics; poly and contact resistance; gate oxide and junction integrity; and specific parameters critical to the particular technology and device type. Wafer-to-wafer, across-the-wafer run-to-run variation and conformance to spec limits are checked.

The actual devices on each wafer are then probed for both functionality and performance to specifications. Additional reliability tests are also included in the probe steps.

WAFER SAW

Probed wafers are transferred to Intel's assembly sites to be sawed. The saw cuts totally through the wafer.

DIE INSPECTION

Upon completion of the wafer saw, the die are moved to pick and place equipment that removes reject die. The remaining die are submitted to the same visual inspection as standard packaged product. The compliant die are then transferred to GEL-PAKs for shipment.

PACKING PROCEDURE

Intel will ship all Intel die products in GEL-PAKs. GEL-PAKs eliminate the die edge damage usually associated with die cavity plates or chip trays.

The backside of each die adheres to the gel membrane in the GEL-PAK, eliminating the risk of damage to the active die surface. A simple vacuum release mechanism allows for pick and place removal at the customer's site.

Only die from the same wafer lot are packaged together in a GEL-PAK, and all die are placed in the GEL-PAKs with a consistent orientation. The GEL-PAKs are then sealed and labeled with the following information:

- Intel Die Products
- Intel Part Number
- Spec
- Customer Part Number (if applicable)
- Fab Lot Number
- Quantity
- Assembly Lot Traveler Number
- Seal Date
- ROM Code (if applicable)

NOTE:
GEL-PAKs require a Vacuum Release Station. For additional information about GEL-PAKs, contact Vichem Corporation.

INSPECTION STEPS

Multiple inspection steps are performed during the die fabrication and packing flow. These steps are performed according to the same specifications and criteria established for Intel's standard packaged product. Specific inspection steps include a wafer saw visual as well as a final die visual just before die are sealed in moisture barrier bags.

STORAGE REQUIREMENTS

Intel die products will be shipped in GEL-PAKs and sealed in a moisture-barrier anti-static bag with a desiccant. No special storage procedures are required while the bag is still unopened. Once opened, the GEL-PAK should be stored in a dry, inert atmosphere to prevent corrosion of the bond pads.

ESD

Components are ESD sensitive.

3.0 SPECIFICATIONS

Specifications within this document are specific to a particular die revision and are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

3.1 Flash Memory Handling Requirements

There are two key areas of concern for the X28F001BX. First, avoid exposing FLASH devices to ultraviolet light. Erasing the device under a UV light will erase device specific control information affecting device performance. Second, do not expose the device to temperatures above 350°C for greater than 10 minutes. Operation above this time/temperature envelope may cause damage to device reference cells.

3.2 Physical Specifications

Substrate Bias Condition: Float (Self-biasing to V_{SS}). Alternative is to drive V_{SS}.

Post-Saw Die Dimensions:

Mils: X = 161 ±0.5, Y = 234 ±0.5

See associated Die/Bond Pad Layout for X, Y orientation.

Die Backside Material (outer most layer first):
Polished Bare Silicon

Pad Passivation Opening Size:
Mils: 4.1 x 4.1 (single pads),
Microns: 105 x 105 (single pads),

Die Thickness: 17 ±1 mils

Minimum Pad Pitch:
Pads may not be evenly pitched. Minimum pitch is 185 microns (7.3 mils).

Bond Pad Metalization (outer most layer first)
0.9 Microns Aluminum (0.5% Copper)
0.1 Microns Titanium

Die Revision: A

Pads per Die: 34

Intel Fabrication Process: ETOX III (min. feature size 0.8 microns)

Passivation: (outer most layer first)
2.3 Microns B-Pyrox, 1.1 Microns Oxynitride

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3.3 DC Specifications

ABSOLUTE MAXIMUM RATINGS*

GEL-PAK Storage Temperature ..... 0°C to +70°C
For other absolute maximum ratings, reference the 28F001BX-T/28F001BX-B data sheet, Order No. 290406.

OPERATING CONDITIONS*

V_{CC}(Supply Voltage) ..... 5.0V ±0.25V
T_J(Junction Temperature Under Bias) ..... 0°C to 80°C

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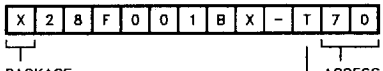
****WARNING:** Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.0 DEVICE NOMENCLATURE



VALID COMBINATIONS:

X28F001BX-T70	X28F001BX-B70
X28F001BX-T90	X28F001BX-B90
X28F001BX-T120	X28F001BX-B120

271303-3

5.0 REFERENCE INFORMATION

Title	Order No.
28F001BX-T/28F001BX-B 1M (128K x 8) CMOS Flash Memory	290406
ER-20, ETOX™ II Flash Memory Technology	294005
RR-60, ETOX™ II Flash Memory Reliability Data Summary	293002
AP-316, Using Flash Memory for In-System Reprogrammable Nonvolatile Storage	292046
AP-341, Designing an Updatable BIOS Using Flash Memory	292077

6.0 REVISION HISTORY

Rev	Date	Description
−001	6/94	Initial release