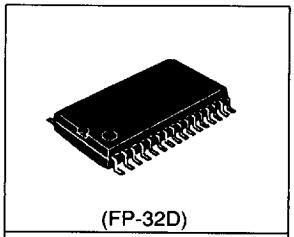
4M (512K x 8-bit) Flash Memory

■ DESCRIPTION

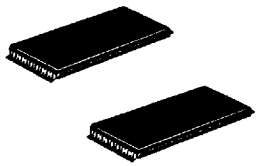
The Hitachi HN29C4001 is a 4-Megabit CMOS Flash Memory organized as 524,288 x 8-bit. The HN29C4001 is capable of in-system electrical chip erasure and reprogramming.

The HN29C4001 programs and erases data with a 12 V V_{PP} supply and a 5 V V_{CC} supply. The HN29C4001 conforms to the JEDEC Standard Dual-Supply EEPROM Command Set.

Hitachi's HN29C4001 is offered in JEDEC-Standard Byte-Wide EPROM pinouts in 32-lead SOP and TSOP packages. This allows an easy upgrade from the HN28F101, 1 Megabit Flash Memory, as well as socket replacement with EPROMs and Mask ROMs. The HN29C4001 TSOP is offered in both standard and reverse bend pinouts.



(FP-32D)



(TFP-32D) and (TFP-32DR)

■ FEATURES

- Dual Power Supply:
  V_{CC} = 5 V ± 10%
  V_{PP} = 12.0 V ± 0.6 V (Erase/Program)
- Fast Access Times:
  150 ns/170 ns (max)
- Low Power Dissipation:
  Read Current: 50 mA (max)
  Standby Current: 20 µA (max)
- Byte Programming:
  Programming Time: 25 µs/Byte (typ)
  Address, Data, Control Latch Function
- Electrical Chip Erase:
  Erase Time: 1 sec (typ)
- Erase Endurance:
  10,000 times (min)
- Pin Arrangement:
  JEDEC Standard Byte-Wide EPROM
  EPROM and Mask ROM Compatible
- Packages:
  32-lead Plastic SOP
  32-lead Plastic TSOP (Type I)

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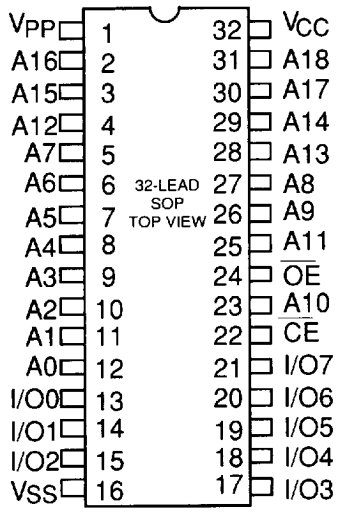
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN29C4001FP-15	150 ns	32-lead Plastic SOP
HN29C4001FP-17	170 ns	(FP-32D)
HN29C4001T-15	150 ns	32-lead Plastic TSOP
HN29C4001T-17	170 ns	(TFP-32D)
HN29C4001R-15	150 ns	32-lead Plastic TSOP
HN29C4001R-17	170 ns	(TFP-32DR)
		Reverse bend

■ PIN ARRANGEMENT

HN29C4001FP Series



(PinD32.HN28F4001)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
I/O_0 - I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground

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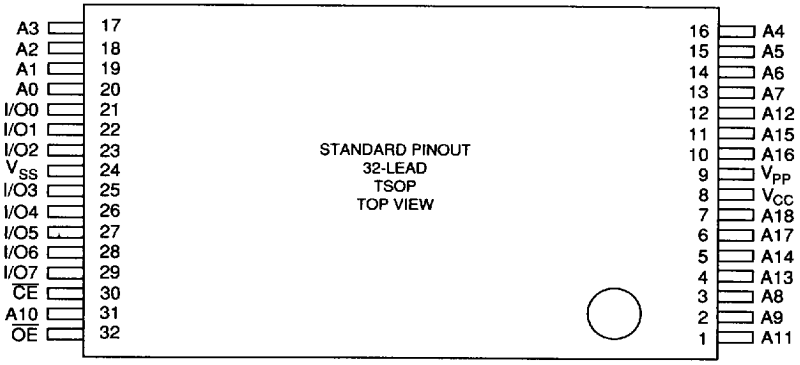
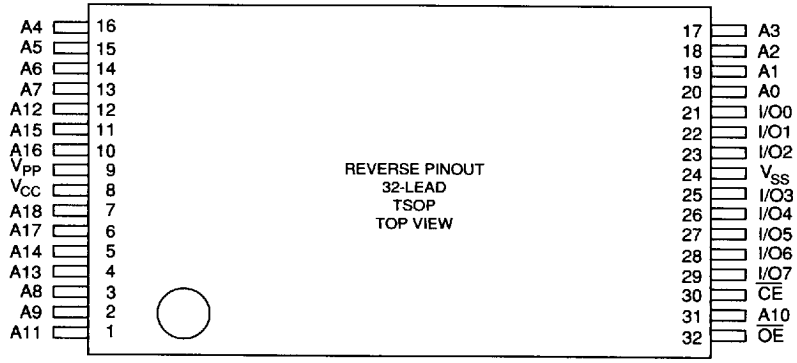
■ PIN ARRANGEMENT (continued)

HN29C4001T Series



(PinT132.HN28F4001T)

HN29C4001R Series



(PinT132.HN28F4001R)

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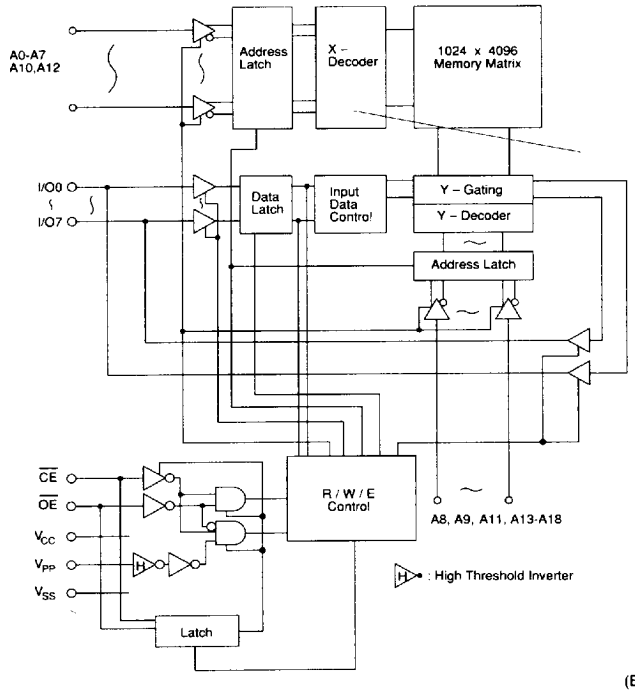
■ BLOCK DIAGRAM



(BD.HN28F4001)

■ MODE SELECTION

Mode		CE	OE	A_9	A_0	V_{PP}	I/O_0 to I/O_7
Read	Read	V_{IL}	V_{IL}	A_9	A_0	V_{cc} [6]	D_{OUT}
	Output Disable	V_{IL}	V_{IH}	X	X	V_{cc}	High-Z
	Standby	V_{IH}	X	X	X	V_{cc}	High-Z
	Identifier [1]	V_{IL}	V_{IL}	V_H [2]	V_{IL}	V_{cc}	Code"07"
		V_{IL}	V_{IL}	V_H [2]	V_{IH}	V_{cc}	Code"08"
Command	Read [3,5]	V_{IL}	V_{IL}	A_9	A_0	V_{PP}	D_{OUT}
Program	Standby	V_{IH}	X	X	X	V_{PP}	High-Z
	Write [4]	V_{IL}	V_{IH}	A_9	A_0	V_{PP}	D_{IN}

Notes:
1. Device Identifier Code can be output in Command Program Mode. Refer to Command Address and Data Input Table.
2. $11.4\ V \leq V_H \leq 12.6\ V$
3. Data can also be read when 12 V is applied to V_{PP}. Device Identifier Code can be output by Command Inputs. See Device Identifier Mode Description Table for more details.
4. Refer to Command Address and Data Input Table. Data is programmed, erased, or verified after inputting Commands.
5. Status of Programming and Erase can be verified in this mode. Status Outputs on I/O_7. I/O_0 to I/O_6 are in high impedance states.
6. X = Don't Care. $V_{PP} = 0V$ to V_{CC}.

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■ COMMAND ADDRESS AND DATA INPUT

Command	Bus Cycles Required	First Cycle			Second Cycle		
		Operation Mode [1]	Address [2]	Data [3]	Operation Mode [1]	Address [2]	Data [3]
Read (Memory) [4]	1	Write	X	00H	Read	RA	D_{OUT}
Read Identifier Codes	2	Write	X	90H	Read	IA	ID
Set-up Chip Erase/ Chip Erase [5]	2	Write	X	20H	Write	X	20H
Reserved [8]	2	Write	X	60H	Write	X	60H
Erase Verify [5]	2	Write	EVA	A0H	Read	X	EVD
Reserved [8]	2	Write	X	30H	Write	X	30H
Reserved [8]	2	Write	X	20H	Write	X	D0H
Setup Program/Program [6]	2	Write	X	40H	Write	PA	PD
Program Verify [6]	2	Write	PA	C0H	Read	X	PVD
Reserved [8]	2	Write	X	10H	Write	X	X
Reset	1 or 2	Write	X	FFH	Write[7]	X	FFH[11]

Notes:
1. Refer to Command Program Mode in Mode Selection about operation mode.
2. Refer to Device Identifier Mode. IA = Identifier Address, PA = Programming Address, EVA = Erase Verify Address, RA = Read Address. Addresses are latched on the rising edge of chip-enable pulse.
3. Refer to Device Identifier Mode. PA are latched by Programming Command. ID = Identifier Output Code, PD = Programming Data, PVD = Programming Verify Output Data, EVD = Erase Verify Output Data.
4. Command latch default value when applying 12 V to V_{PP} is "00H". Device is in Read Mode after V_{PP} is set to 12 V (before other Command is input).
5. All data in the chip is erased. Erase data according to the Manual Chip Erase Flowchart.
6. Program data according to the Manual Programming Flowchart.
7. Write Reset Command twice to exit from program setup state or auto verify program setup state. Write it once to exit from others.
8. Do not write the following Command sequences to the device: 60H + 60H, 30H + 30H, 20H + D_{IN}, 10H + D_{IN}. Data may be destroyed if these Commands are written.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +14.0	V
A_9 Voltage [1,2]	V_{ID}	-0.6 to +13.5	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range [3]	T_{STG}	-65 to +125	°C
Storage Temperature Under Bias	T_{BIAS}	-10 to +80	°C

Notes:
1. Relative to V_{SS}.
2. V_{IN}, V_{OUT} and V_{ID} min = -2.0V for pulse width ≤ 20 ns.
3. Device storage temperature range before programming.

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■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0 V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = V_{SS} to V_{CC}
Operating V_{CC} Current	I_{CC1}	-	-	30	mA	I_{OUT} = 0 mA, f = 1 MHz
	I_{CC2}	-	-	50	mA	I_{OUT} = 0 mA, f = 8 MHz
Standby V_{CC} Current	I_{SB1}	-	-	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	-	-	20	µA	$\overline{CE}$ = V_{CC} ± 0.3V
V_{PP} Current	I_{PP1}	-	-	20	µA	V_{PP} = 5.5 V
Input Voltage [3]	V_{IL}	-0.5 [1]	-	0.8	V	
	V_{IH}	2.2 [3]	-	V_{CC} + 0.5 [2]	V	
Output Voltage	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes:
1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns. V_{IL} min = -2.0 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns. If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.
3. Only defined for DC and long cycle function test. V_{IL} max = 0.4 V, V_{IH} min = 3.0 V for AC function test.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	HN29C4001-15 Min.	HN29C4001-15 Max.	HN29C4001-17 Min.	HN29C4001-17 Max.	Unit	Test Conditions
Address Access Time	t_{ACC}	-	150	-	170	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	150	-	170	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	70	-	70	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	50	0	60	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	5	-	5	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

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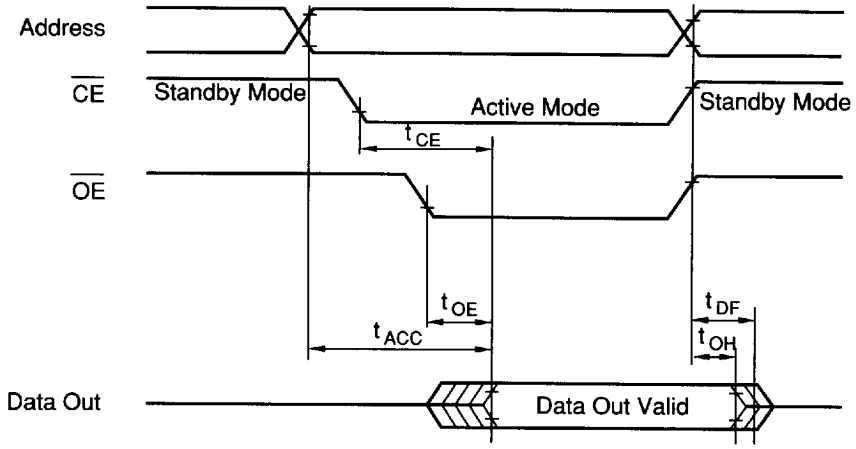
■ **READ TIMING WAVEFORM**



(TD.R.HN28F4001)

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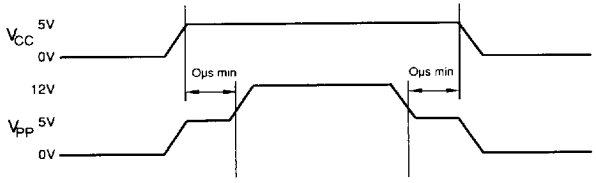
■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING AND ERASE OPERATIONS

(V_{CC} = 5V ± 10%, V_{PP} = 12.0 V ± 0.6 V, T_a = 0 to +70°C)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Leakage Current		I_{LI}	-	-	2	µA	V_{IN} = V_{SS} to V_{CC}
Output Leakage Current		I_{LO}	-	-	2	µA	V_{OUT} = V_{SS} to V_{CC}
Operating V_{CC} Current	Read	I_{CC1}	-	-	30	mA	I_{OUT} = 0 mA, f = 1 MHz
		I_{CC2}	-	-	50	mA	I_{OUT} = 0 mA, f = 8 MHz
	Program	I_{CC3}	-	-	30	mA	Programming
	Erase	I_{CC4}	-	-	30	mA	Erasing
	Program Verify	I_{CC5}	-	-	15	mA	Programming Verify
	Erase Verify	I_{CC6}	-	-	15	mA	Erase Verify
Standby V_{CC} Current		I_{SB1}	-	-	1	mA	$\overline{CE}$ = V_{IH}
		I_{SB2}	-	-	200	µA	$\overline{CE}$ = V_{CC} ± 0.3 V
V_{PP} Current	Read	I_{PP1}	-	-	200	µA	V_{PP} = 12.6 V
	Program	I_{PP2}	-	-	50	mA	Programming
	Erase	I_{PP3}	-	-	80	mA	Erasing
	Program Verify	I_{PP4}	-	-	10	mA	Program Verify
	Erase Verify	I_{CC5}	-	-	10	mA	Erase Verify
Input Voltage		V_{IL}	-0.5 [5]	-	0.8	V	
		V_{IH}	2.2[7]	-	V_{CC} + 0.5[6]	V	
Output Voltage		V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA
		V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. V_{CC}/V_{PP} power on/off timing: V_{CC} must be applied before or simultaneously with V_{PP}, and removed after or simultaneously with V_{PP}. These conditions must be satisfied at power on and off caused by power failure to the device.



2. V_{PP} must not exceed 14 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12 V.
4. When $\overline{CE}$ = V_{IL} do not change V_{PP} from V_{IL} to 12 V or 12 V to V_{IL}.
5. V_{IL} min = -1.0 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.
7. Only defined for DC and long cycle function test. V_{IL} max = 0.4 V, V_{IH} min = 3.0 V for AC function test.

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■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING AND ERASE OPERATIONS

(V_{CC} = 5V ± 10%, V_{PP} = 12.0 v ± 0.6 V, T_a = 0 to 70°C)

Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0V

Item	Symbol	HN29C4001-15		HN29C4001-15		Unit	
		Min.	Max.	Min.	Max.		
V_{PP} Setup Time	t_{VPS}	100	-	100	-	ns	
Output Enable Setup Time	t_{OES}	100	-	100	-	ns	
$\overline{OE}$ Setup after Command	t_{OESA}	6	-	6	-	µs	
$\overline{CE}$ Setup after Command	t_{CESA}	6	-	6	-	µs	
Chip Enable Hold Time	t_{CEH}	60	-	60	-	ns	
Chip Enable Pulse Width	t_{CEP}	60	-	60	-	ns	
Address Setup Time	t_{AS}	50	-	50	-	ns	
Address Hold Time	t_{AH}	20	-	20	-	ns	
Data Setup Time	t_{DS}	50	-	50	-	ns	
Data Hold Time	t_{DH}	20	-	20	-	ns	
Chip Enable Setup Time before Command Write	t_{CESC}	100	-	100	-	ns	
$\overline{CE}$ Setup before Verify	t_{CESV}	6	-	6	-	µs	
$\overline{OE}$ Setup before Verify	t_{OESV}	6	-	6	-	µs	
V_{PP} Hold Time	t_{VPH}	100	-	100	-	ns	
Standby Time Before Programming	t_{PPW}	25	-	25	-	µs	
Erase Standby Time	t_{ET}	0.95	-	0.95	-	ms	

Notes: 1. $\overline{CE}$ and $\overline{OE}$ must be fixed high during V_{PP} transition from 5 V to 12 V or from 12 V to 5 V.
2. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

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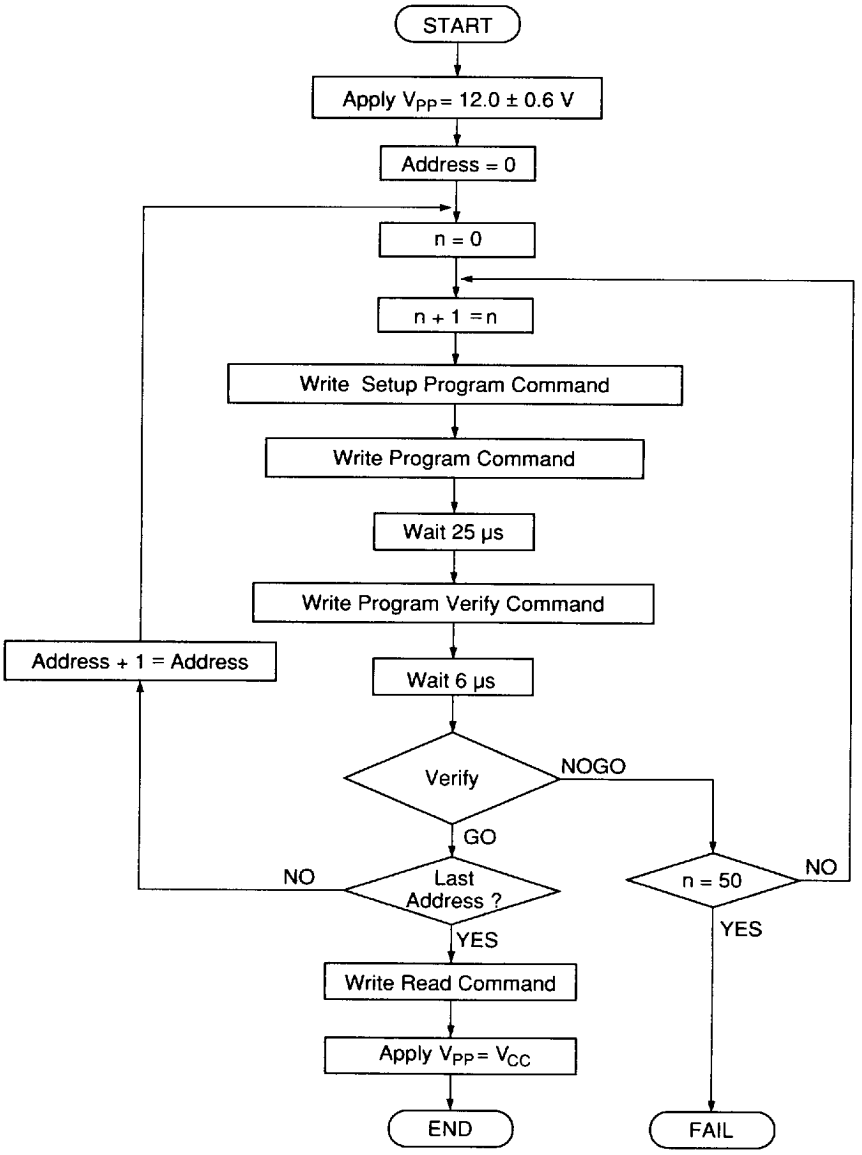
■ MANUAL PROGRAMMING FLOWCHART

The HN29C4001 can be programmed with the fast, high-reliability programming algorithm shown in the following flowchart. This algorithm provides fast programming time without any voltage stress to the device or deterioration in reliability of programmed data.



(FC.P.HN29C4001)

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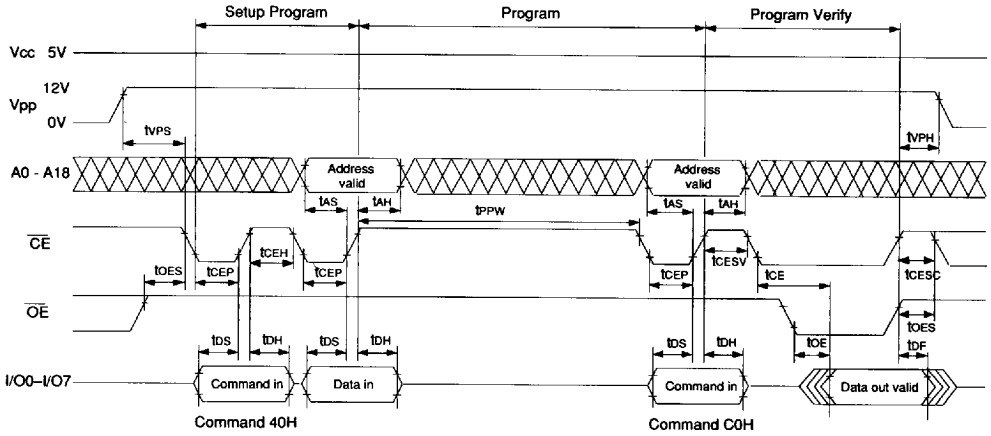
■ MANUAL PROGRAMMING TIMING WAVEFORM



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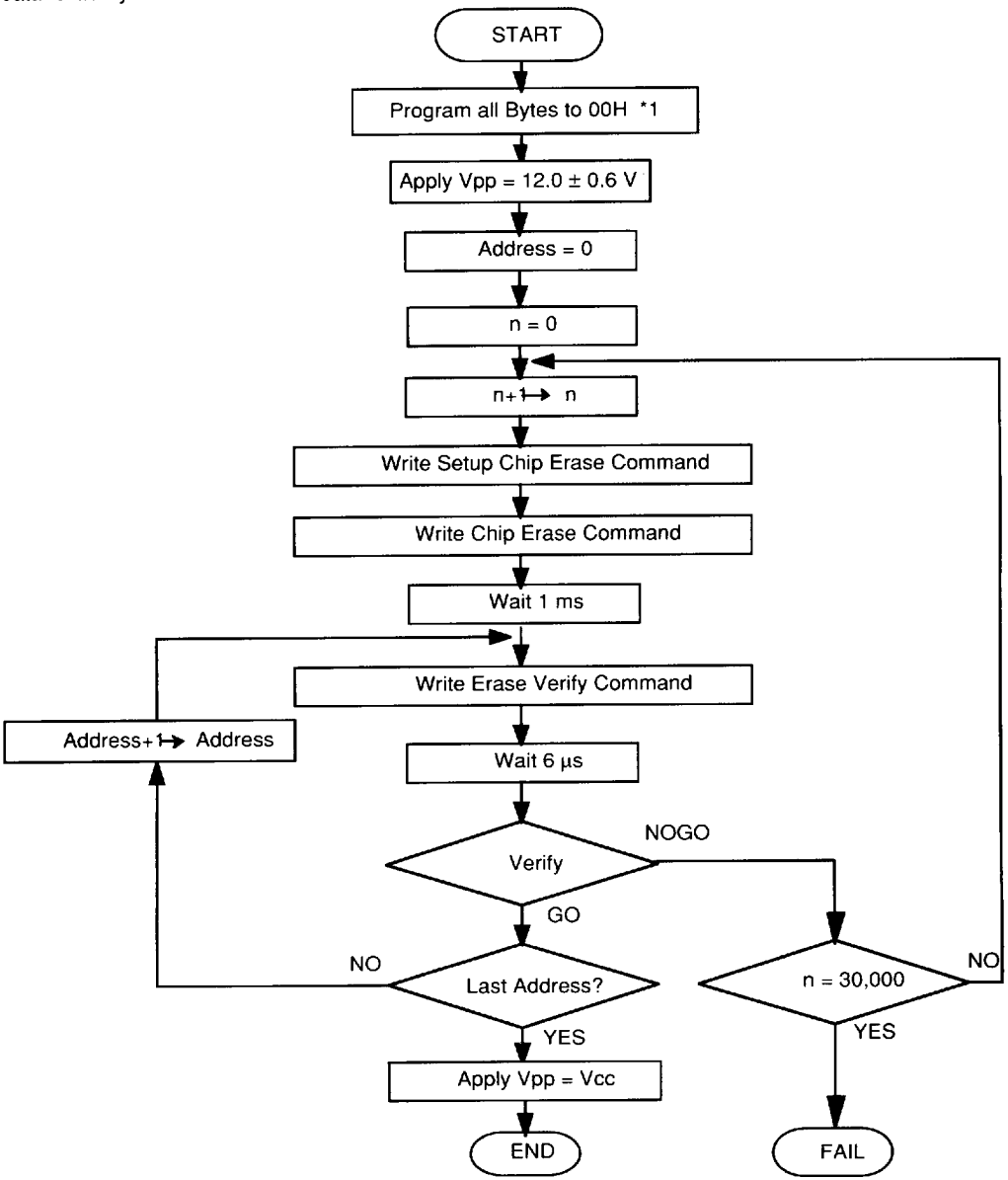
■ MANUAL CHIP ERASE FLOWCHART

The HN29C4001 can be erased with the fast, high-reliability chip erase algorithm shown in the following flowchart. This algorithm provides a fast erase time without any voltage stress to the device or deterioration in data reliability.



*1. Refer to Manual Programming Flowchart

(FC.CE.HN29C4001)

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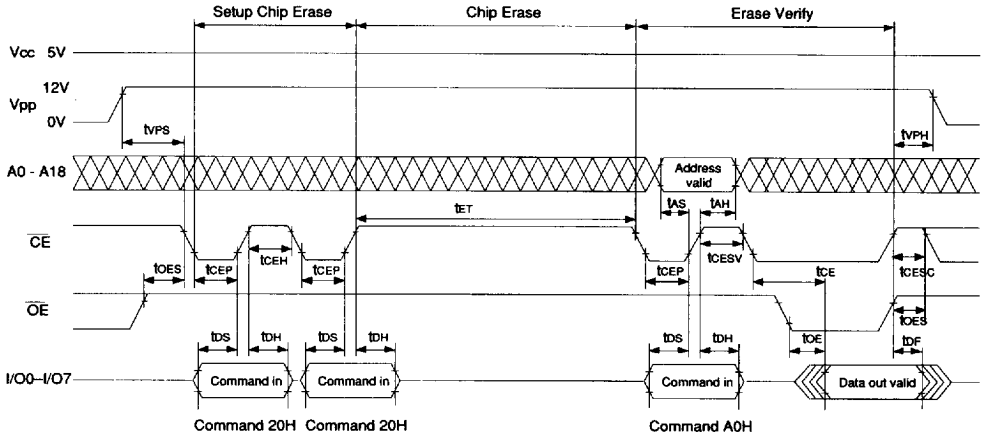
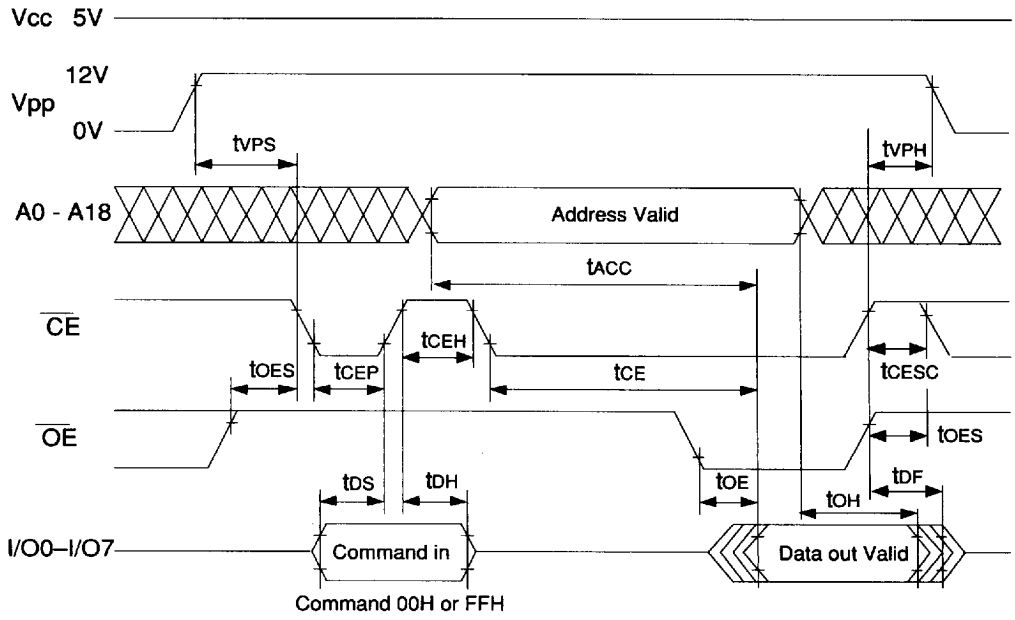
■ MANUAL CHIP ERASE TIMING WAVEFORM



(TD.CE.HN28F4001)

■ READ TIMING WAVEFORM (V_{PP} APPLIED)



(TD.RTW.HN28F4001)

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■ DEVICE IDENTIFIER MODE DESCRIPTION

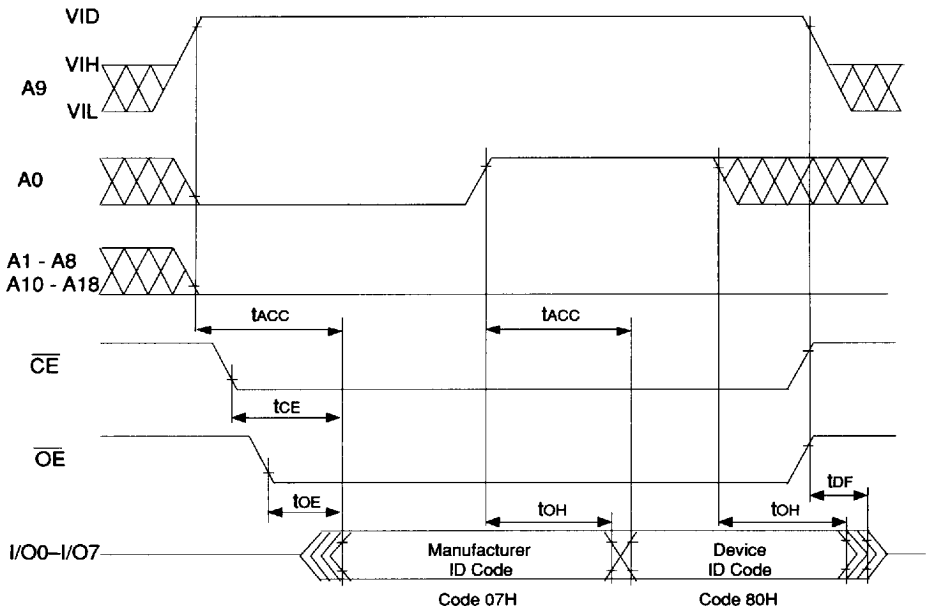
The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

■ HN28F4001 SERIES IDENTIFIER CODE

Identifier	A_0	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	1	0	0	0	0	0	0	0	80

Notes:
1. Device identifier code can be read out by applying 12.0 V ± 0.5 V to A9 when V_{PP}=V_{CC}, or inputting command while V_{PP}=12 V.
2. V_{CC} = V_{PP}=5.0 V ± 10% when applying 12 V to A9.
   V_{CC} =5.0 V ± 10% and V_{PP}=12.0 V ± 0.6 V in command inputs.
3. A1 to A8, A10 to A18, $\overline{CE}$, and $\overline{OE}$ = V_{IL}.

■ IDENTIFIER CODE READ TIMING WAVEFORM (V_{PP} = V_{SS} to V_{CC})



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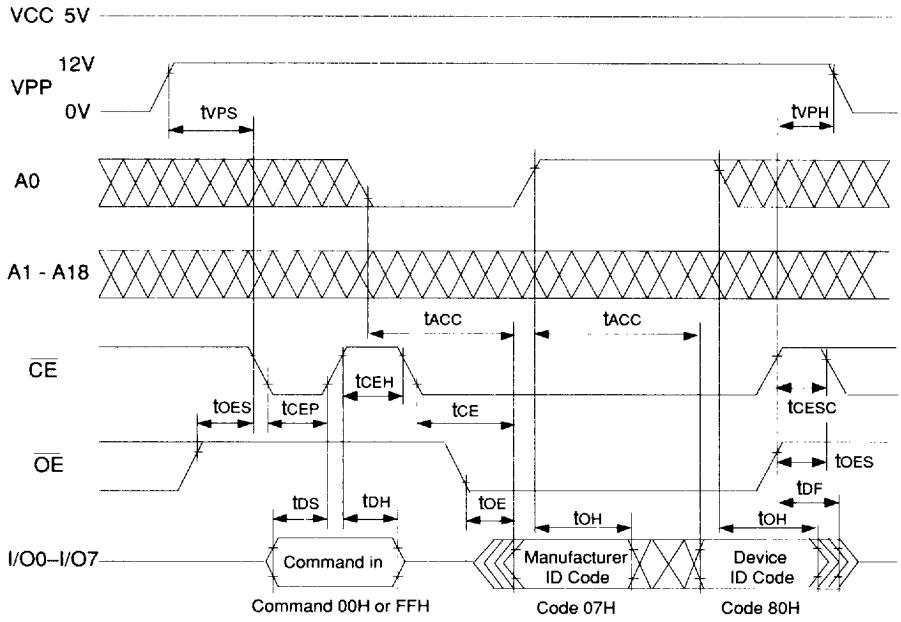
■ IDENTIFIER CODE READ TIMING WAVEFORM (V_{PP} = 12V)



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