MSM51V18160F

1,048,576-Word x 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The MSM51V18160F is a 1,048,576-word × 16-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM51V18160F achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM51V18160F is available in a 42-pin plastic SOJ or 50/44-pin plastic TSOP.

FEATURES

- 1,048,576-word × 16-bit configuration
- Single 3.3V power supply, ±0.3V tolerance
- Input : LVTTL compatible, low input capacitance
- Output : LVTTL compatible, 3-state
- Refresh : 1024 cycles/16ms
- Fast page mode, read modify write capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, hidden refresh, $\overline{\text{RAS}}$-only refresh capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self-refresh capability
- Package options:

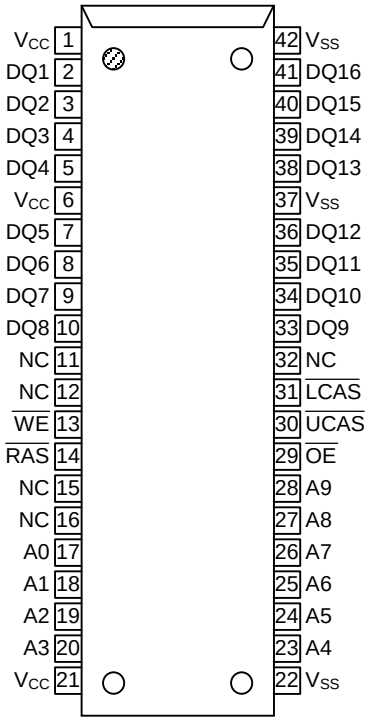
42-pin 400mil plastic SOJ	(SOJ42-P-400-1.27)	(Product : MSM51V18160F-xxJS)
50/44-pin 400mil plastic TSOP	(TSOPII50/44-P-400-0.80-K)	(Product : MSM51V18160F-xxTS-K)
	(TSOPII50/44-P-400-0.80-L)	(Product : MSM51V18160F-xxTS-L)

xx indicates speed rank.

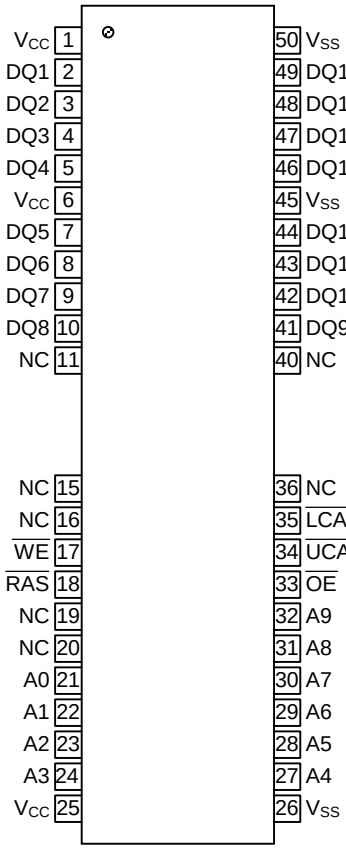
PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM51V18165F	50ns	25ns	13ns	13ns	90ns	450mW	1.8mW
	60ns	30ns	15ns	15ns	110ns	414mW	
	70ns	35ns	20ns	20ns	130ns	378mW	

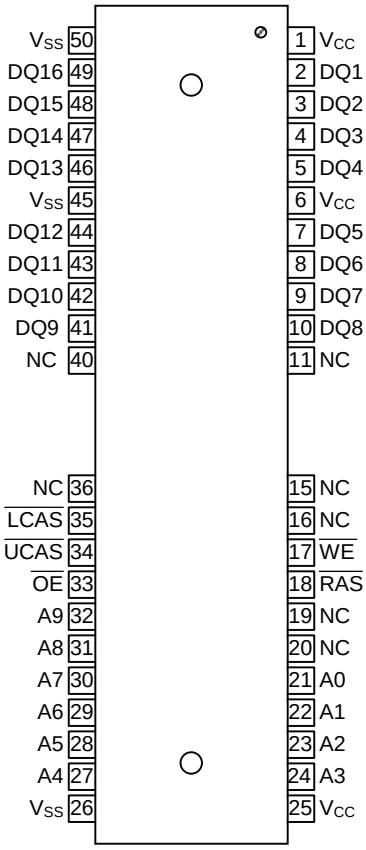
PIN CONFIGRATION (TOP VIEW)



42-Pin Plastic SOJ



55/44-Pin Plastic TSOP
(K Type)

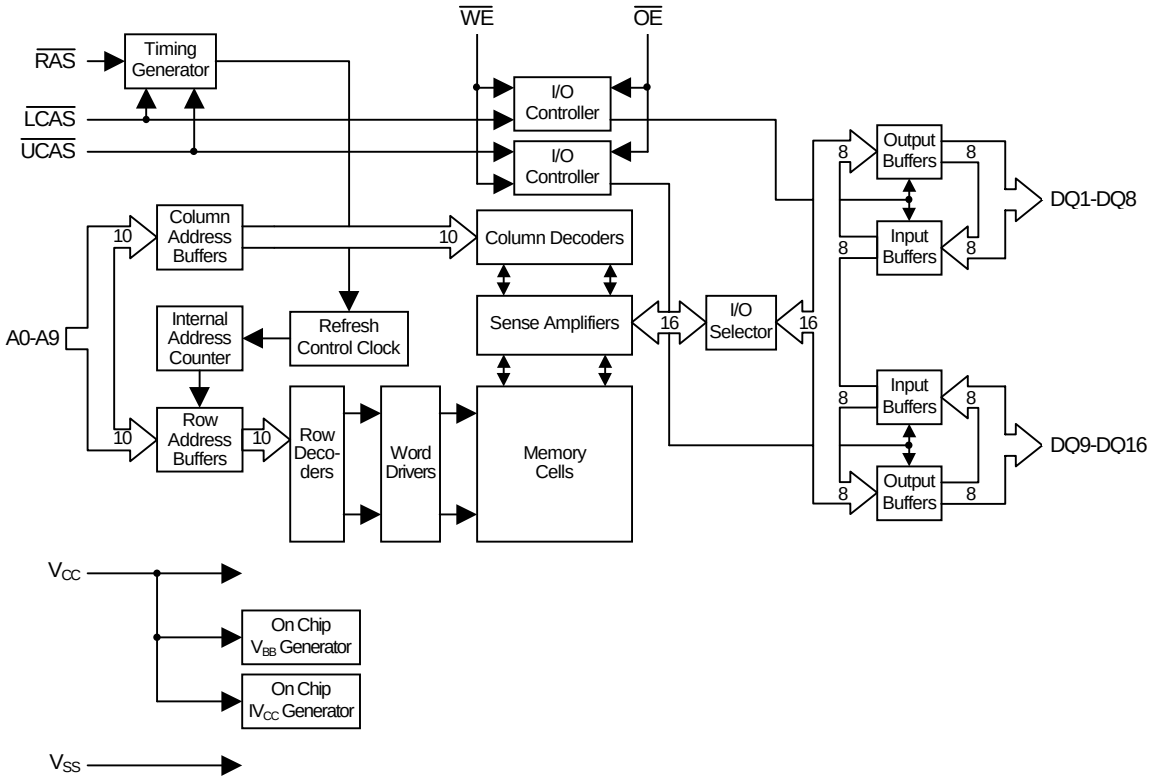


55/44-Pin Plastic TSOP
(L Type)

Pin Name	Function
A0–A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$	Lower Byte Column Address Strobe
$\overline{UCAS}$	Upper Byte Column Address Strobe
DQ1–DQ16	Data Input/Data Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (3.3V)
V_{SS}	Ground (0V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQ Pin		Function Mode
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	DQ1-DQ8	DQ9-DQ16	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D_{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D_{OUT}	Upper Byte Read
L	L	L	H	L	D_{OUT}	D_{OUT}	Word Read
L	L	H	L	H	D_{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D_{IN}	Upper Byte Write
L	L	L	L	H	D_{IN}	D_{IN}	Word Write
L	L	L	H	H	High-Z	High-Z	—

* : "H" or "L"

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	− 0.5 to V_{CC} + 0.5	V
Voltage V_{CC} Supply relative to V_{SS}	V_{CC}	− 0.5 to 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_{D*}	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	− 55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0 °C to 70 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3[*1]	V
Input Low Voltage	V_{IL}	− 0.3[*2]	—	0.8	V

Notes: *1. The input voltage is V_{CC} + 1.0V when the pulse width is less than 20ns (the pulse width is with respect to the point at which V_{CC} is applied).

*2. The input voltage is V_{SS} − 1.0V when the pulse width is less than 20ns (the pulse width respect to the point at which V_{SS} is applied).

Capacitance

(V_{CC} = 3.3V ± 0.3V, Ta = 25°C, f=1MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9)	C_{IN1}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ16)	$C_{I/O}$	—	7	pF

DC Characteristics

(V_{CC} = 3.3V ± 0.3V, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	MSM51V18160 F-50		MSM51V18160 F-60		MSM51V18160 F-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = –2.0mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0V ≤ V_I ≤ V_{CC}+0.3V; All other pins not under test = 0V	– 10	10	– 10	10	– 10	10	μA	
Output Leakage Current	I_{LO}	DQ disable 0V ≤ V_O ≤ V_{CC}	– 10	10	– 10	10	– 10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min.	—	80	—	70	—	60	mA	1,2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	2	—	2	—	2	mA	1
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2V	—	0.5	—	0.5	—	0.5		
Average Power Supply Current ($\overline{RAS}$-only Refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = Min.	—	80	—	70	—	60	mA	1,2
Power Supply Current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ = cycling, $\overline{CAS}$ before $\overline{RAS}$	—	80	—	70	—	60	mA	1,2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = Min.	—	80	—	70	—	60	mA	1,3

Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.

2. The address can be changed once or less while $\overline{RAS}$ = V_{IL}.

3. The address can be changed once or less while $\overline{CAS}$ = V_{IH}.

AC Characteristic (1/2)

(V_{CC} = 3.3V ± 0.3V, Ta = 0°C to 70°C) Note1,2,3

Parameter	Symbol	MSM51V18160 F-50		MSM51V18160 F-60		MSM51V18160 F-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	90	—	110	—	130	—	ns	
Read Modify Write Cycle Time	t_{RWC}	131	—	155	—	185	—	ns	
Fast Page Mode Cycle Time	t_{HPC}	35	—	40	—	45	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRWC}	76	—	85	—	100	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	50	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	13	—	15	—	20	ns	4,5
Access Time from Column Address	t_{AA}	—	25	—	30	—	35	ns	4,6
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	30	—	35	—	40	ns	4,12
Access Time from $\overline{OE}$	t_{OEA}	—	13	—	15	—	20	ns	4
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	ns	4
$\overline{CAS}$ to Data Output Buffer Turn-off Delay Time	t_{OFF}	0	13	0	15	0	20	ns	7
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	13	0	15	0	20	ns	7
Transition Time	t_T	3	50	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	30	—	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	50	100,000	60	100,000	70	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	13	—	15	—	20	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	t_{ROH}	13	—	15	—	20	—	ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	7	—	10	—	10	—	ns	14
$\overline{CAS}$ Pulse Width	t_{CAS}	13	10,000	15	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	50	—	60	—	70	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	5	—	ns	12
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	30	—	35	—	40	—	ns	12

AC Characteristic (2/2)

(V_{CC} = 3.3V ± 0.3V, Ta = 0°C to 70°C) Note1,2,3

Parameter	Symbol	MSM51V18160 F-50		MSM51V18160 F-60		MSM51V18160 F-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	17	37	20	45	20	50	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	12	25	15	30	15	35	ns	6
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	7	—	10	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	11
Column Address Hold Time	t_{CAH}	7	—	10	—	15	—	ns	11
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	25	—	30	—	35	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	11
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	8,11
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	8
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	9,11
Write Command Hold Time	t_{WCH}	7	—	10	—	15	—	ns	11
Write Command Pulse Width	t_{WP}	7	—	10	—	10	—	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	13	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	13	—	15	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	13	—	15	—	20	—	ns	13
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	10,11
Data-in Hold Time	t_{DH}	7	—	10	—	15	—	ns	10,11
$\overline{OE}$ to Data-in Delay Time	t_{OED}	13	—	15	—	20	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	36	—	40	—	50	—	ns	9
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	48	—	55	—	65	—	ns	9
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	73	—	85	—	100	—	ns	9
$\overline{CAS}$ Precharge $\overline{WE}$ Delay Time	t_{CPWD}	53	—	60	—	70	—	ns	9
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	5	—	5	—	5	—	ns	11
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	10	—	10	—	ns	11
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	10	—	10	—	10	—	ns	12

Notes:

1. A start-up delay of 200μs is required after power-up, followed by a minimum of eight initialization cycles($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.

2. The AC characteristics assume t_T = 5ns.

3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL}.

4. This parameter is measured with a load circuit equivalent to 1 TTL load and 100pF.
The output timing reference levels are V_{OH} = 2.0V and V_{OL} = 0.8V.

5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met.
t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC}.

6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met.
t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA}.

7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieved the open circuit condition and are not referenced to output voltage levels.

8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$(Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.

10. These parameters are referenced to the $\overline{UCAS}$ and $\overline{LCAS}$, leading edges in an early write cycle, and to the $\overline{WE}$ leading edge in an $\overline{OE}$ control write cycle, or a read modify write cycle.

11. These parameters are determined by the falling edge of either $\overline{UCAS}$ or $\overline{LCAS}$, whichever is earlier.

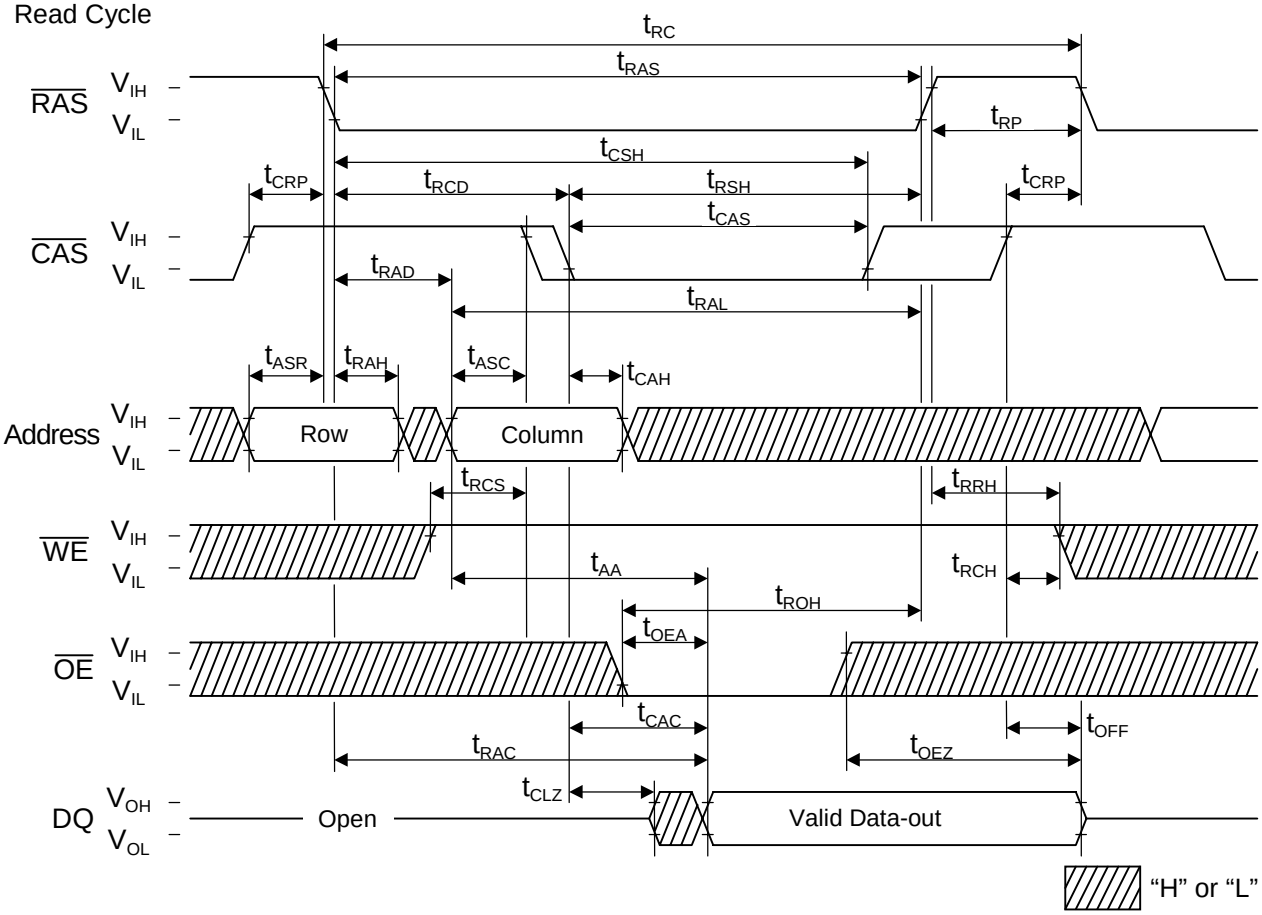
12. These parameters are determined by the rising edge of either $\overline{UCAS}$ or $\overline{LCAS}$, whichever is later.

13. t_{CWL} should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.

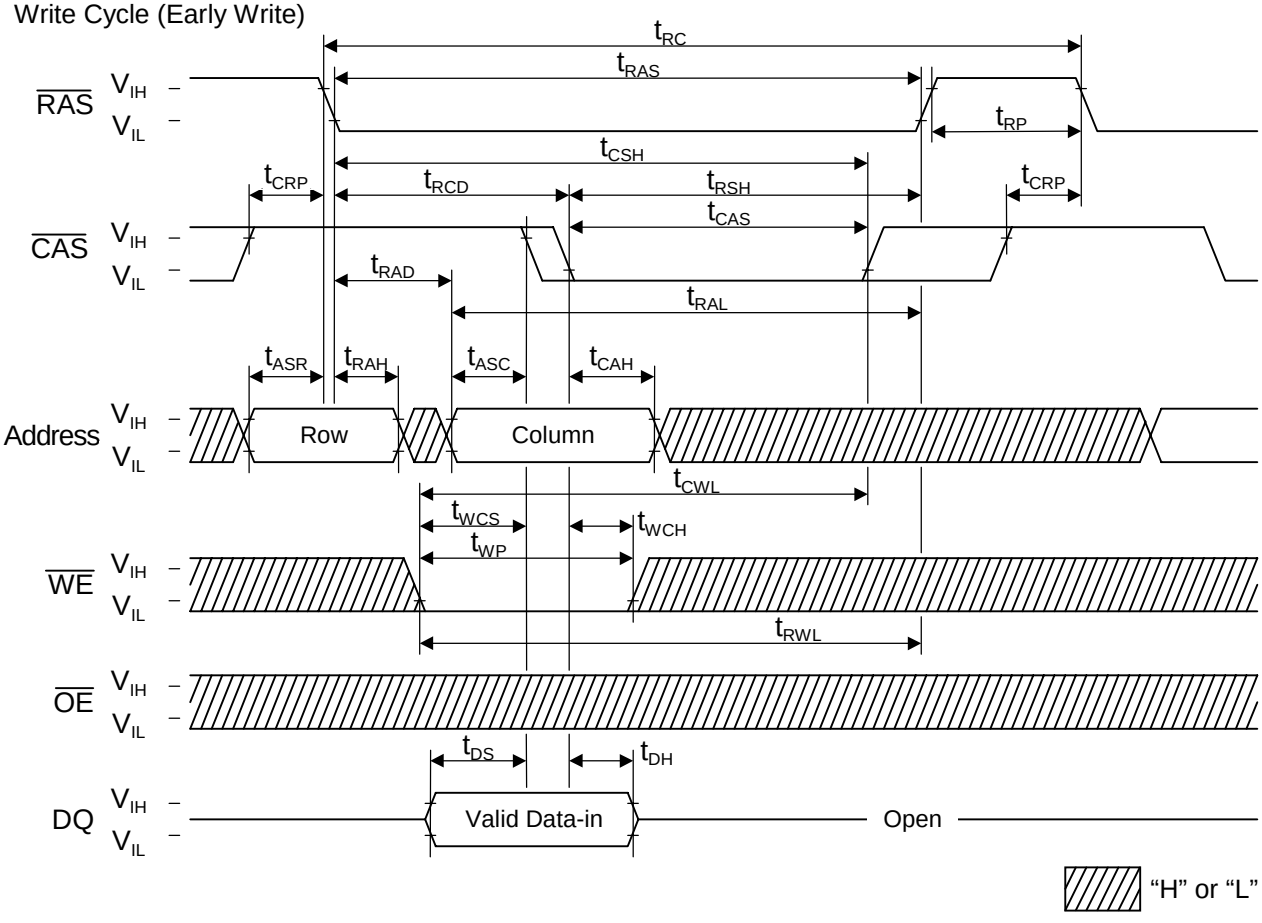
14. t_{CP} is determined by the time both $\overline{UCAS}$ and $\overline{LCAS}$ are high.

Timing Chart

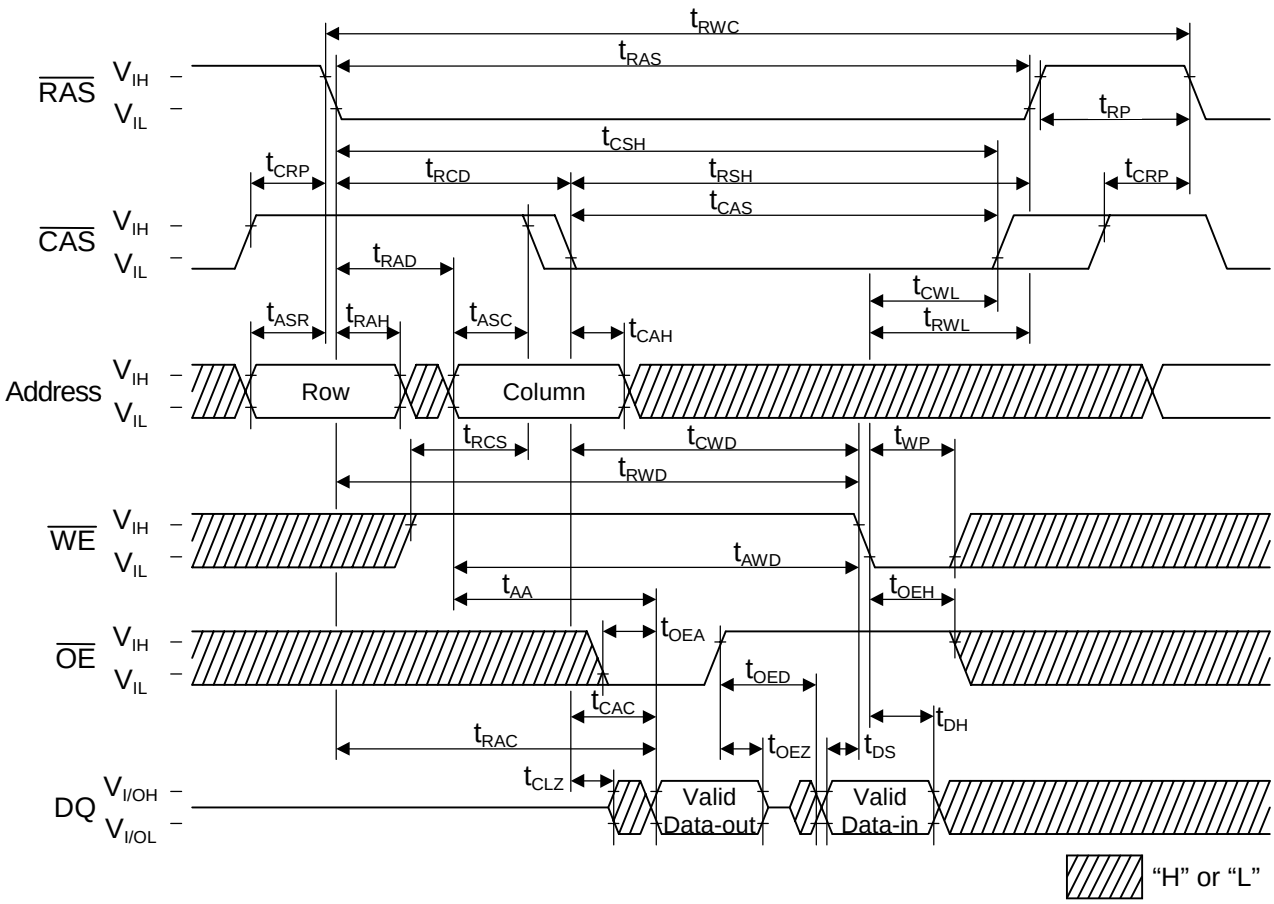
- Read Cycle



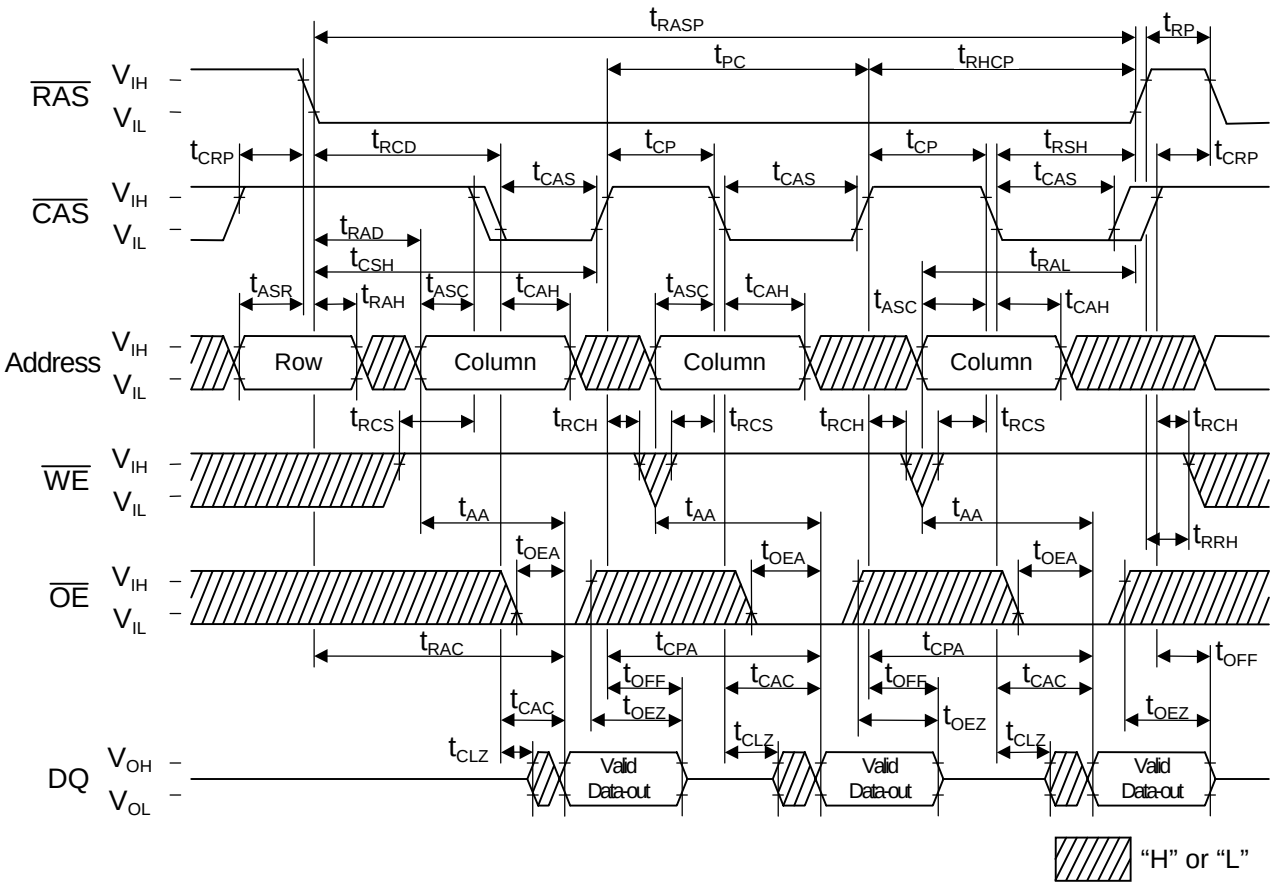
- Write Cycle (Early Write)



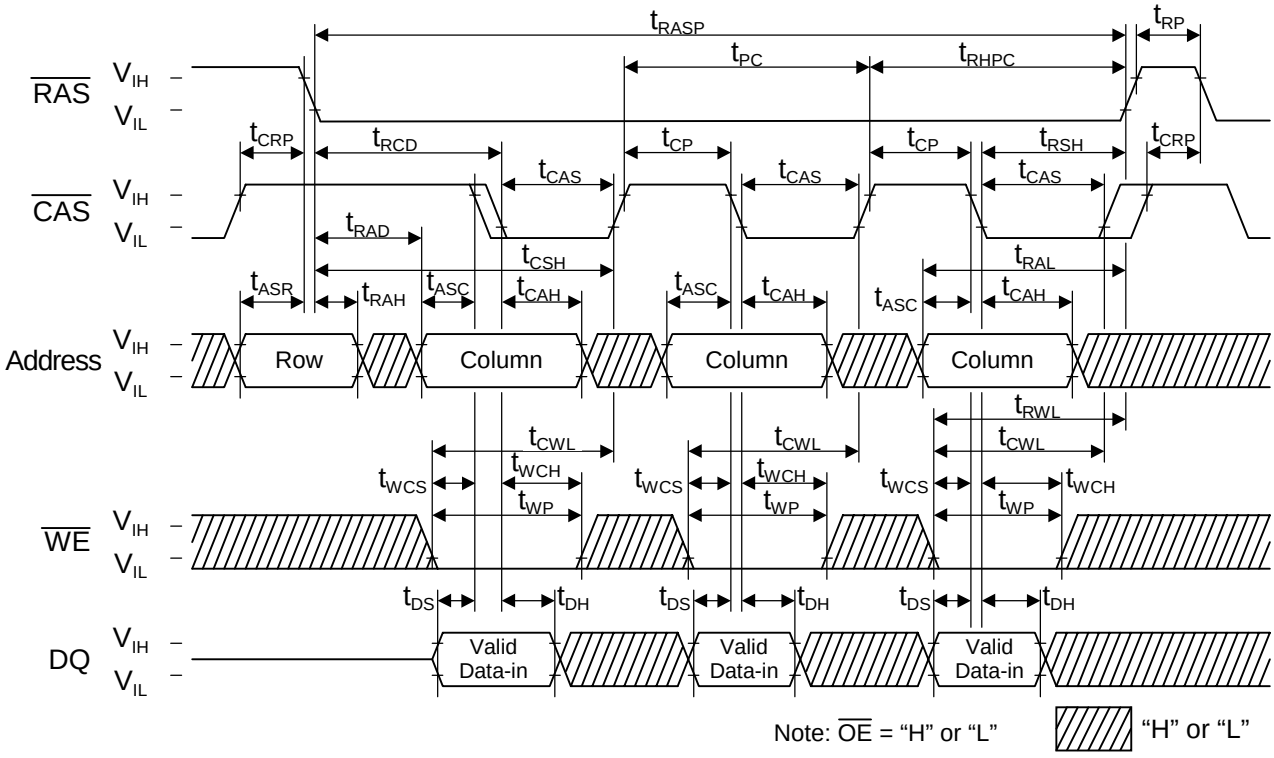
- Read Modify Write Cycle



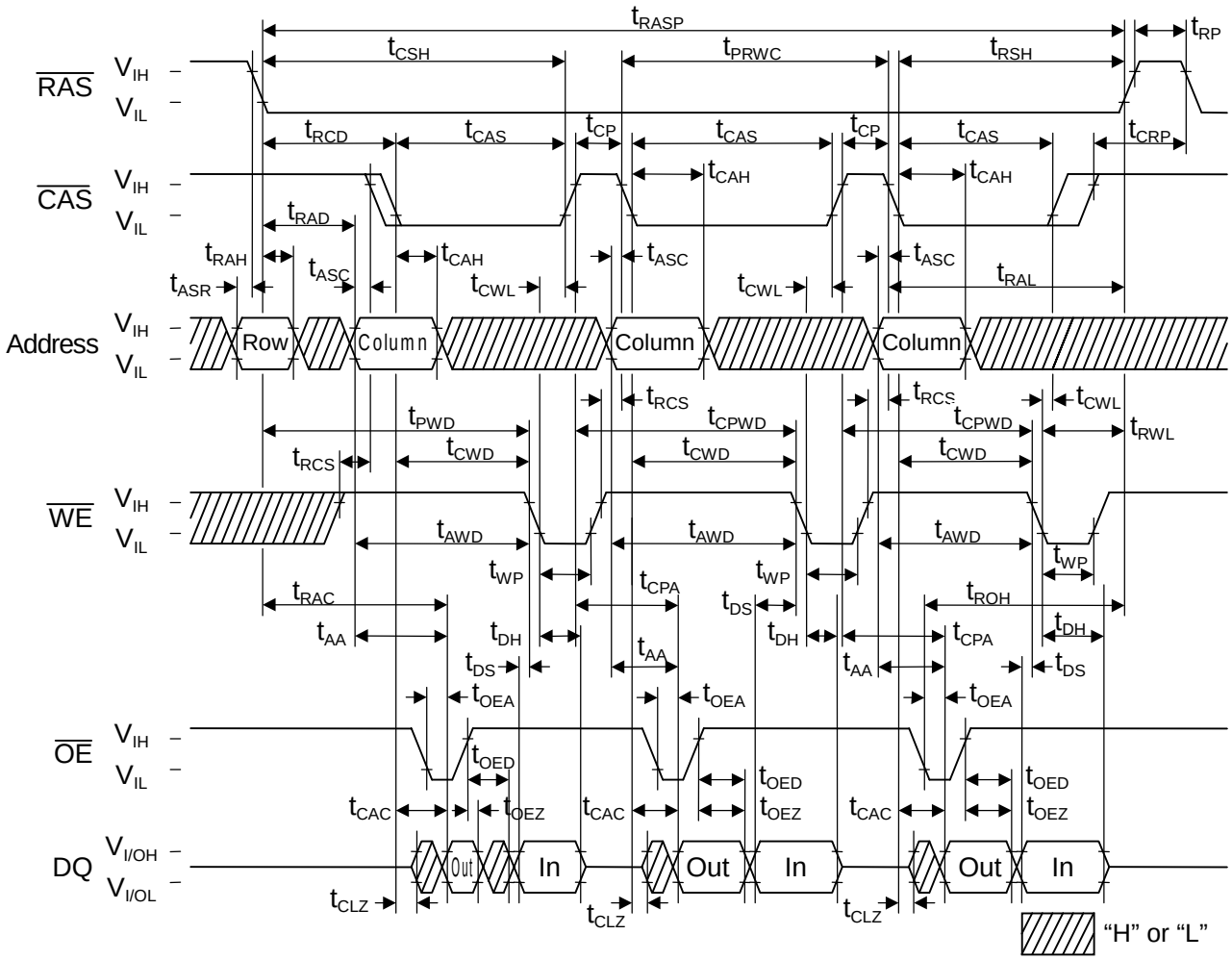
- Fast Page Mode Cycle



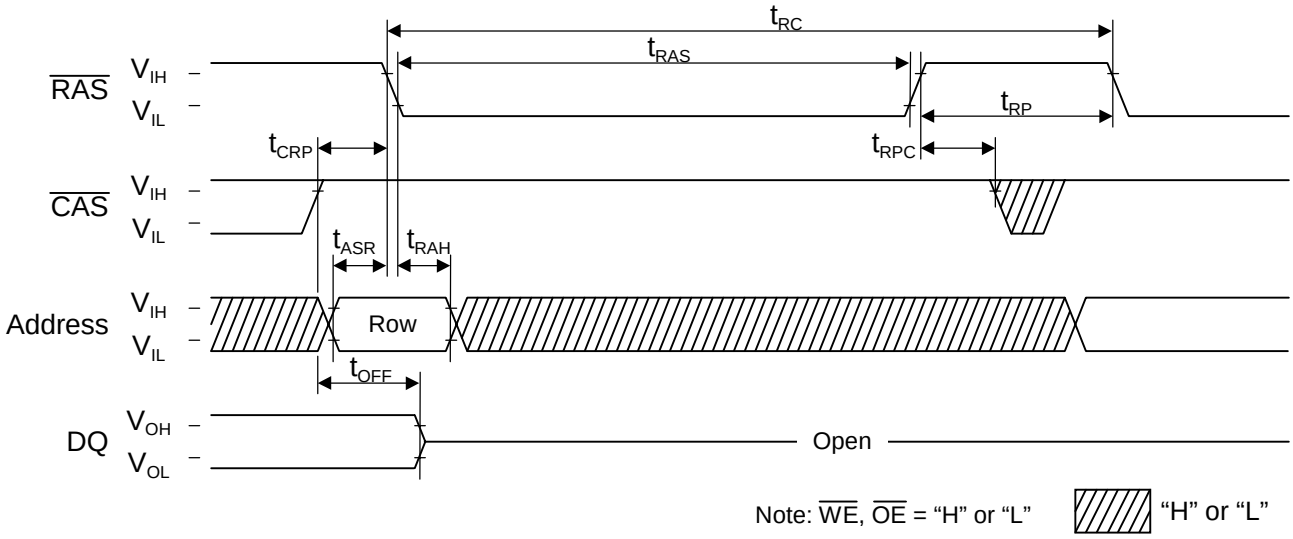
- Fast Page Mode Write Cycle (Early Write)



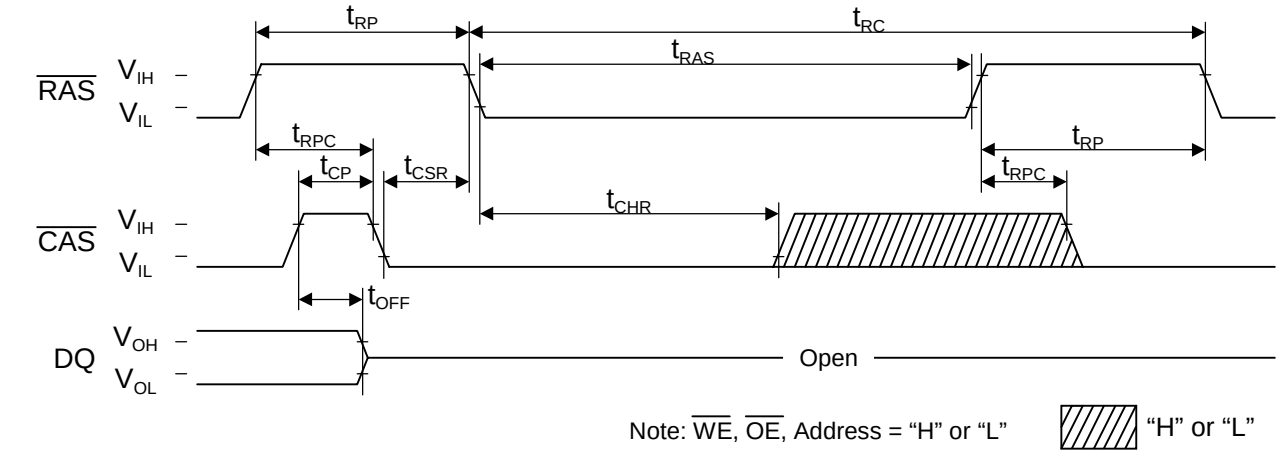
- Fast Page Mode Read Modify Write Cycle



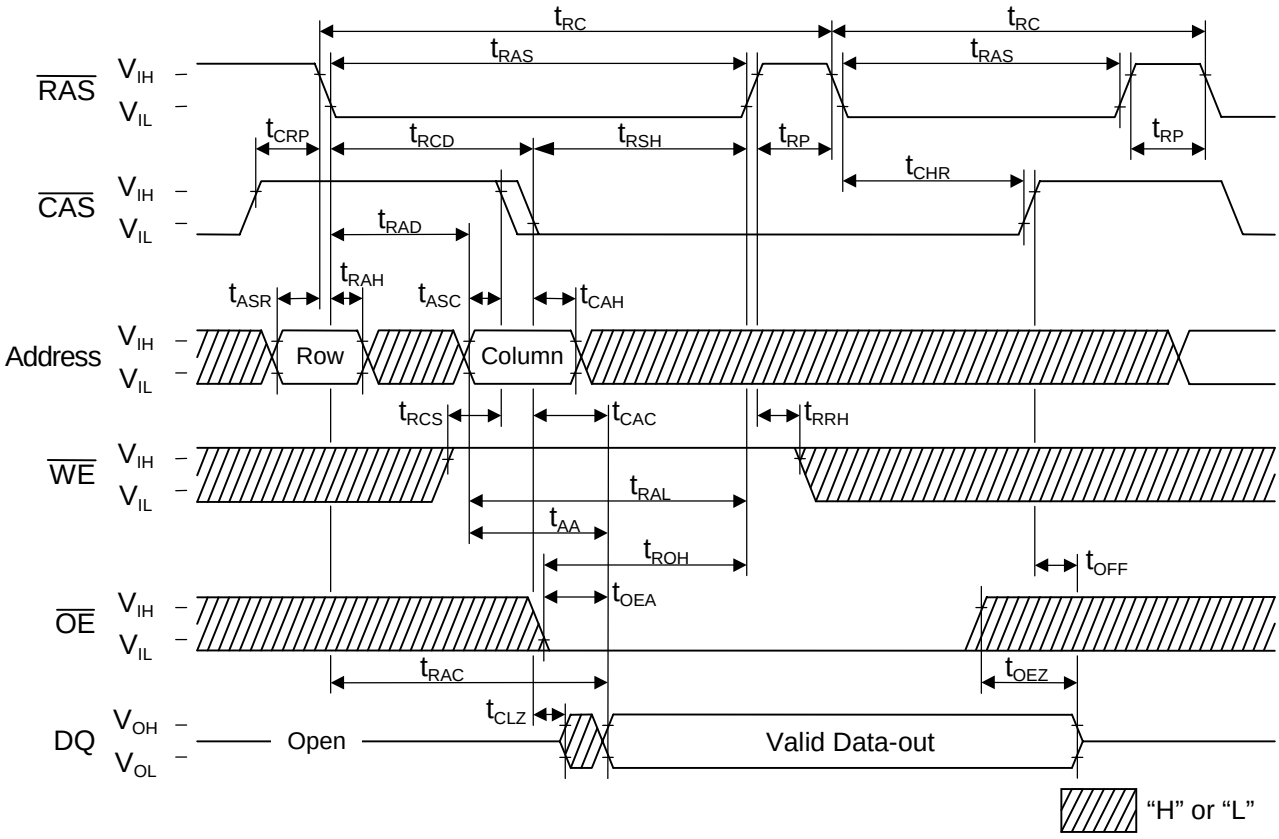
- $\overline{\text{RAS}}$-only Refresh Cycle



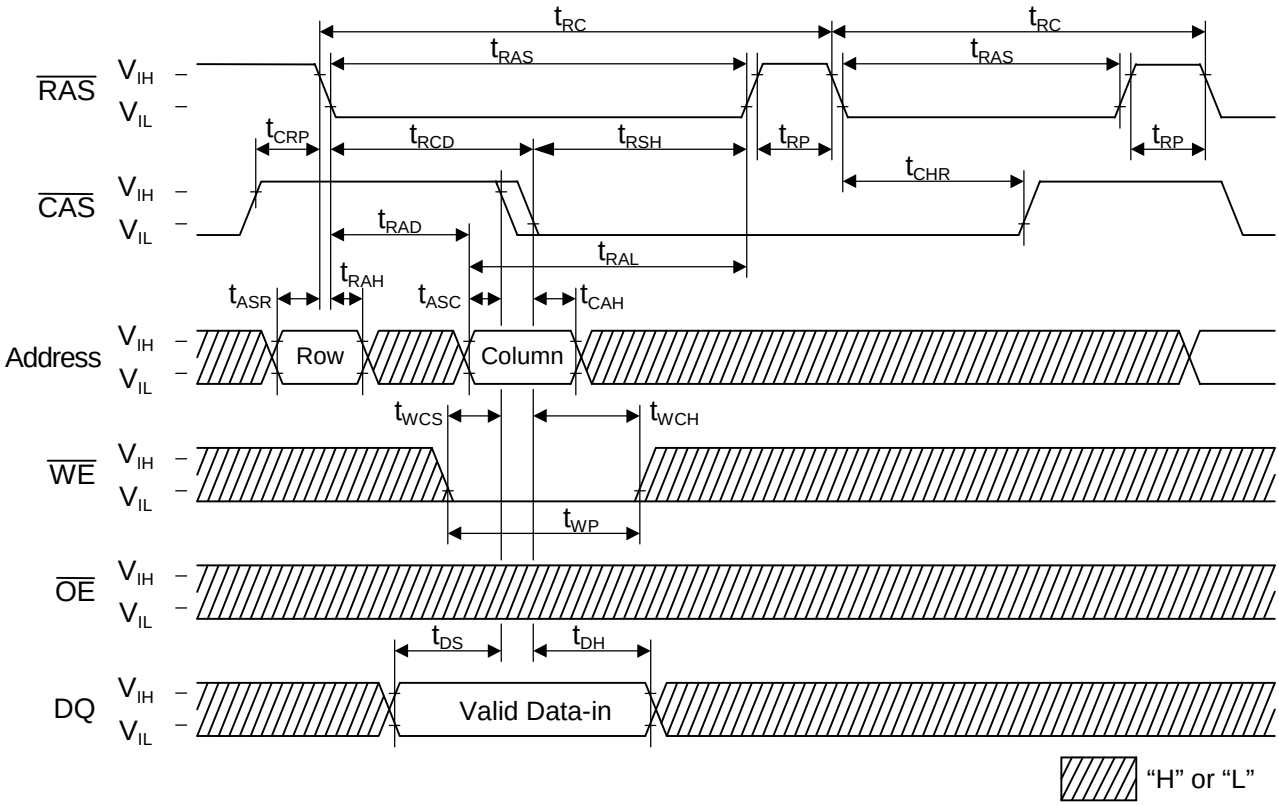
- $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



- Hidden Refresh Read Cycle



Hidden Refresh Write Cycle



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