

# DATA SHEET

## **74LVC11**

### **Triple 3-input AND gate**

Product specification  
Supersedes data of 1998 Apr 28

2004 Jan 13

## Triple 3-input AND gate

## 74LVC11

## FEATURES

- Wide supply voltage range from 1.2 to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output capability: standard
- I<sub>CC</sub> category: SSI
- In accordance with JEDEC standard no. 8-1A
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.

## DESCRIPTION

The 74LVC11 is a high-performance, low power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC11 provides the 3-input AND function.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> ≤ 2.5 ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB, nC to nY	C <sub>L</sub> = 50 pF; V <sub>CC</sub> = 3.3 V	3.7	ns
C <sub>I</sub>	input capacitance		5.0	pF
C <sub>PD</sub>	power dissipation capacitance per gate	notes 1 and 2	26	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in Volts;

N = total switching outputs;

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

2. The condition is V<sub>I</sub> = GND to V<sub>CC</sub>.

## ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74LVC11D	-40 to +85 °C	14	SO14	plastic	SOT108-1
74LVC11DB	-40 to +85 °C	14	SSOP14	plastic	SOT337-1
74LVC11PW	-40 to +85 °C	14	TSSOP14	plastic	SOT402-1
74LVC11BQ	-40 to +85 °C	14	DHVQFN14	plastic	SOT762-1

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**FUNCTION TABLE**

See note 1.

INPUT			OUTPUT
nA	nB	nC	nY
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

**Note**

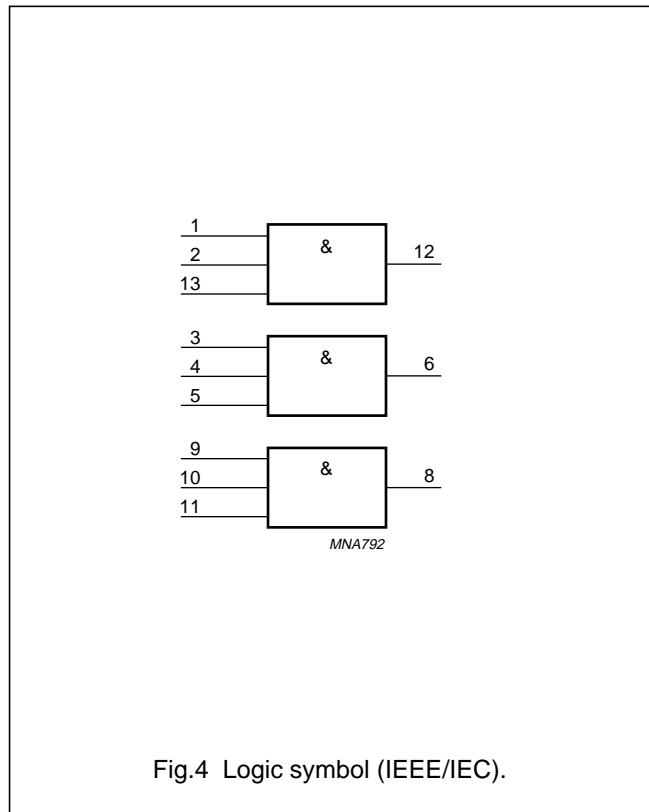
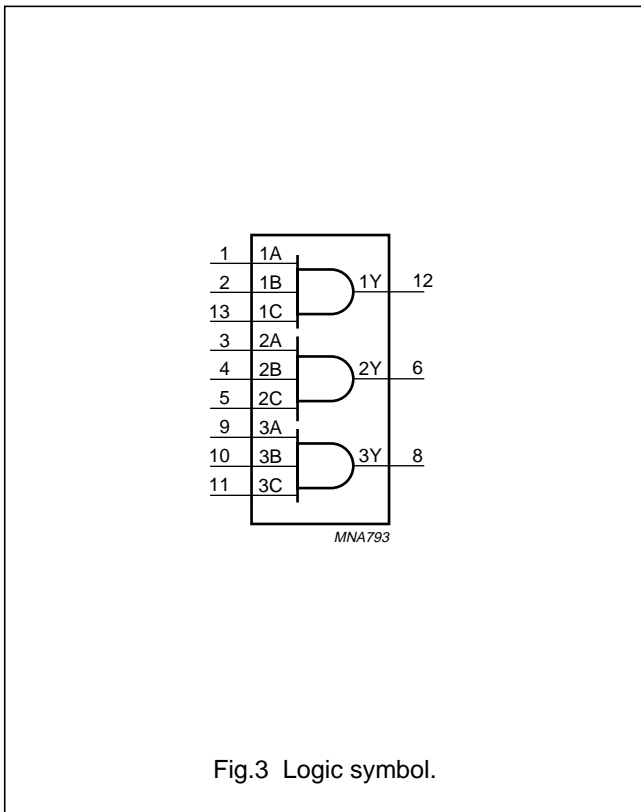
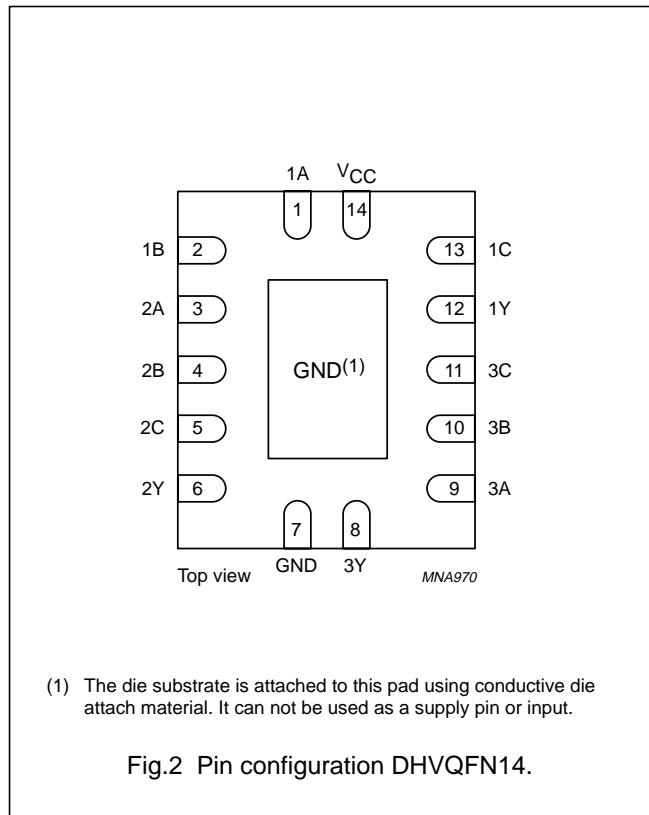
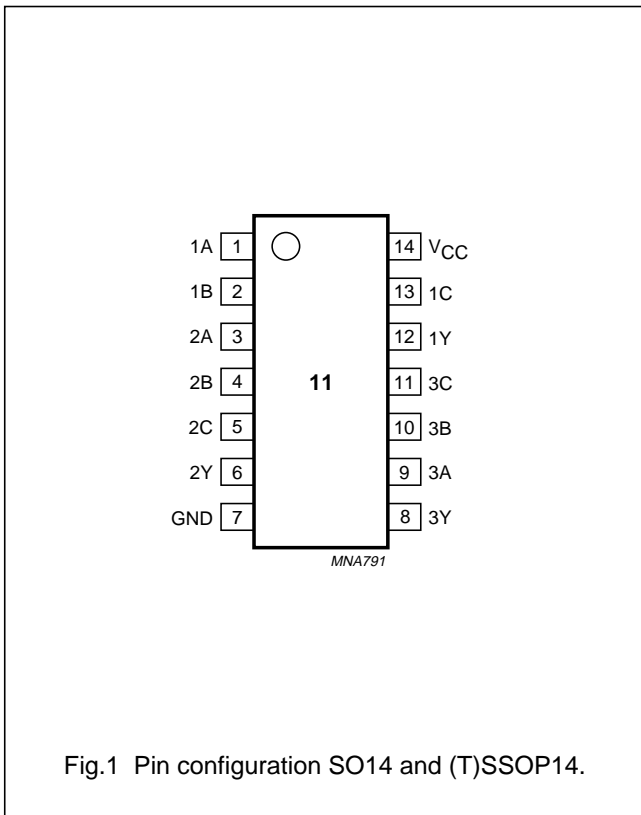
1. H = HIGH voltage level.  
L = LOW voltage level.

**PINNING**

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1B	data input
3	2A	data input
4	2B	data input
5	2C	data input
6	2Y	data output
7	GND	ground (0 V)
8	3Y	data output
9	3A	data input
10	3B	data input
11	3C	data input
12	1Y	data output
13	1C	data input
14	V <sub>CC</sub>	positive supply voltage

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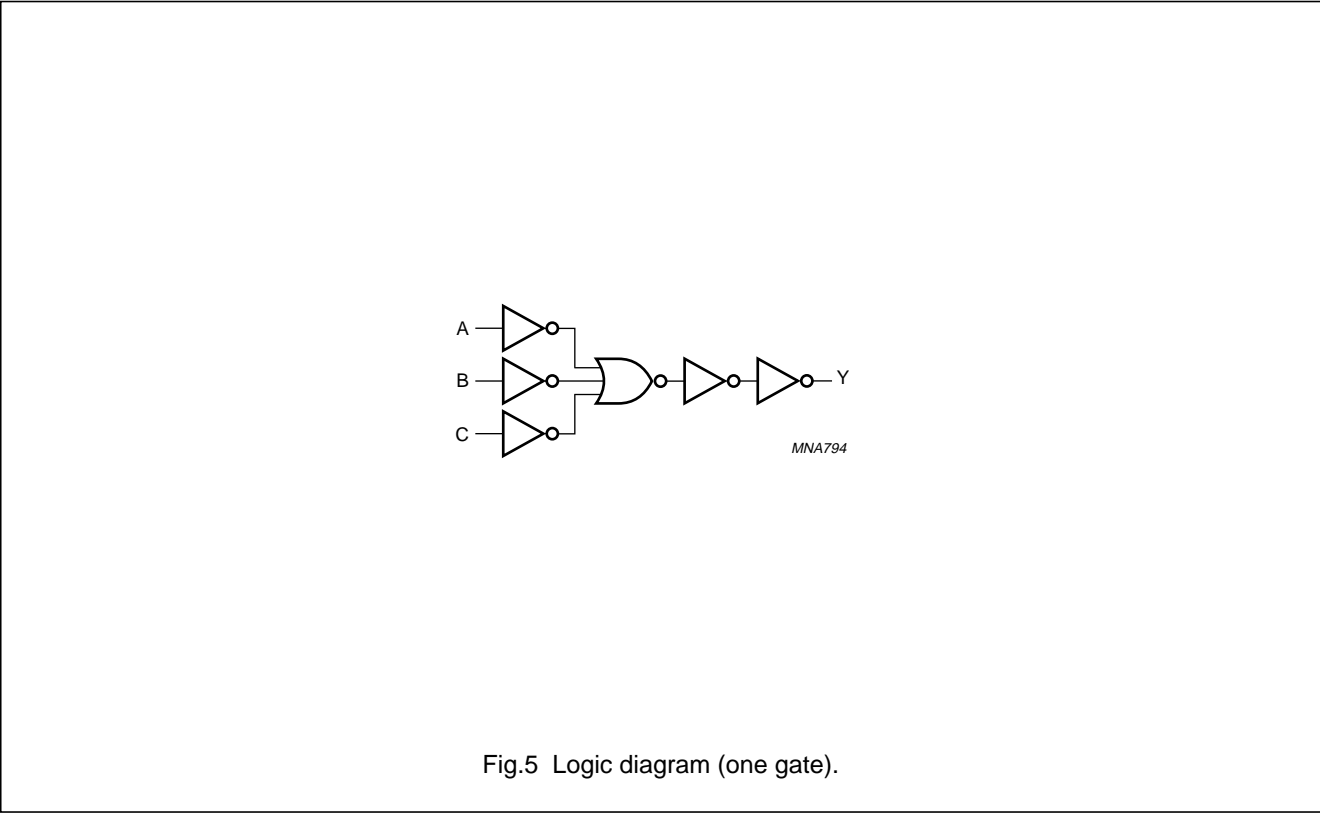


Fig.5 Logic diagram (one gate).

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage		0	$V_{CC}$	V
$T_{amb}$	operating ambient temperature		-40	+85	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 1.2$ to $2.7$ V	0	20	ns/V
		$V_{CC} = 2.7$ to $3.6$ V	0	10	ns/V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input diode current	$V_I < 0$	-	-50	mA
$V_I$	input voltage	note 1	-0.5	+6.5	V
$I_{OK}$	output diode current	$V_O > V_{CC}$ or $V_O < 0$	-	±50	mA
$V_O$	output voltage	note 1	-0.5	$V_{CC} + 0.5$	V
$I_O$	output source or sink current	$V_O = 0$ to $V_{CC}$	-	±50	mA
$I_{GND}, I_{CC}$	$V_{CC}$ or GND current		-	±100	mA
$T_{stg}$	storage temperature range		-65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40$ to $+125$ °C; note 2	-	500	mW

## Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO14 packages: above 70 °C the value of  $P_D$  derates linearly with 8 mW/K.  
For (T)SSOP14 packages: above 60 °C the value of  $P_D$  derates linearly with 5.5 mW/K.  
For DHVQFN14 packages: above 60 °C the value of  $P_D$  derates linearly with 4.5 mW/K.

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**DC CHARACTERISTICS**

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>							
V <sub>IH</sub>	HIGH level input voltage		1.2	V <sub>CC</sub>	-	-	V
			2.7 to 3.6	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		1.2	-	-	GND	V
			2.7 to 3.6	-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -12 mA	2.7	V <sub>CC</sub> - 0.5	-	-	V
		I <sub>O</sub> = -100 µA	3.0	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
		I <sub>O</sub> = -12 mA	3.0	V <sub>CC</sub> - 0.6	-	-	V
		I <sub>O</sub> = -24 mA	3.0	V <sub>CC</sub> - 1.0	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 12 mA	2.7	-	-	0.40	V
		I <sub>O</sub> = 100 µA	3.0	-	GND	0.20	V
		I <sub>O</sub> = 24 mA	3.0	-	-	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	-	±0.1	±5	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	-	0.1	10	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	-	5	500	µA

**Note**

- All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

**AC CHARACTERISTICS**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> ≤ 2.5 ns; C<sub>L</sub> = 50 pF; R<sub>L</sub> = 500 Ω.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay	see Figs 6 and 7	2.7	-	-	7.0	ns
			3.0 to 3.6	-	3.7	6.2	ns

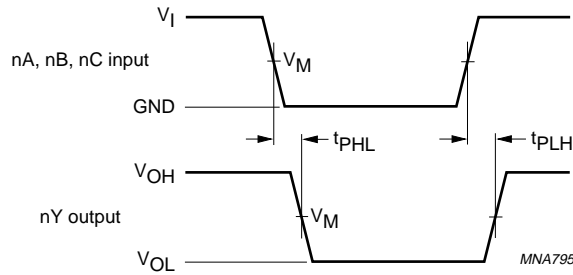
**Note**

- Typical value is measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

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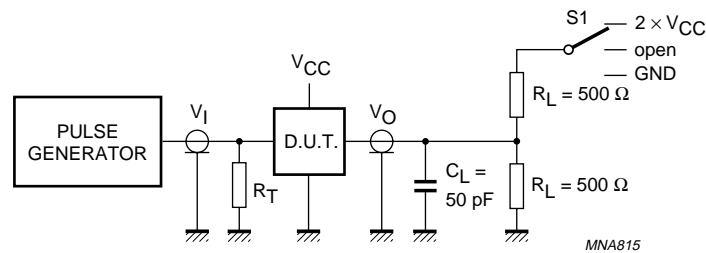
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AC WAVEFORMS



$V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ .  
 $V_M = 0.5V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ .  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

Fig.6 Input (nA, nB and nC) to output (nY) propagation delays.



SWITCH POSITION	
TEST	S1
$t_{PLH}/t_{PHL}$	open

$V_{CC}$	$V_I$
$< 2.7\text{ V}$	$V_{CC}$
$2.7\text{ to }3.6\text{ V}$	$2.7\text{ V}$

Definitions for test circuit:  
 $R_L$  = load resistor.  
 $C_L$  = load capacitance including jig and probe capacitance.  
 $R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Fig.7 Load circuitry for switching times.



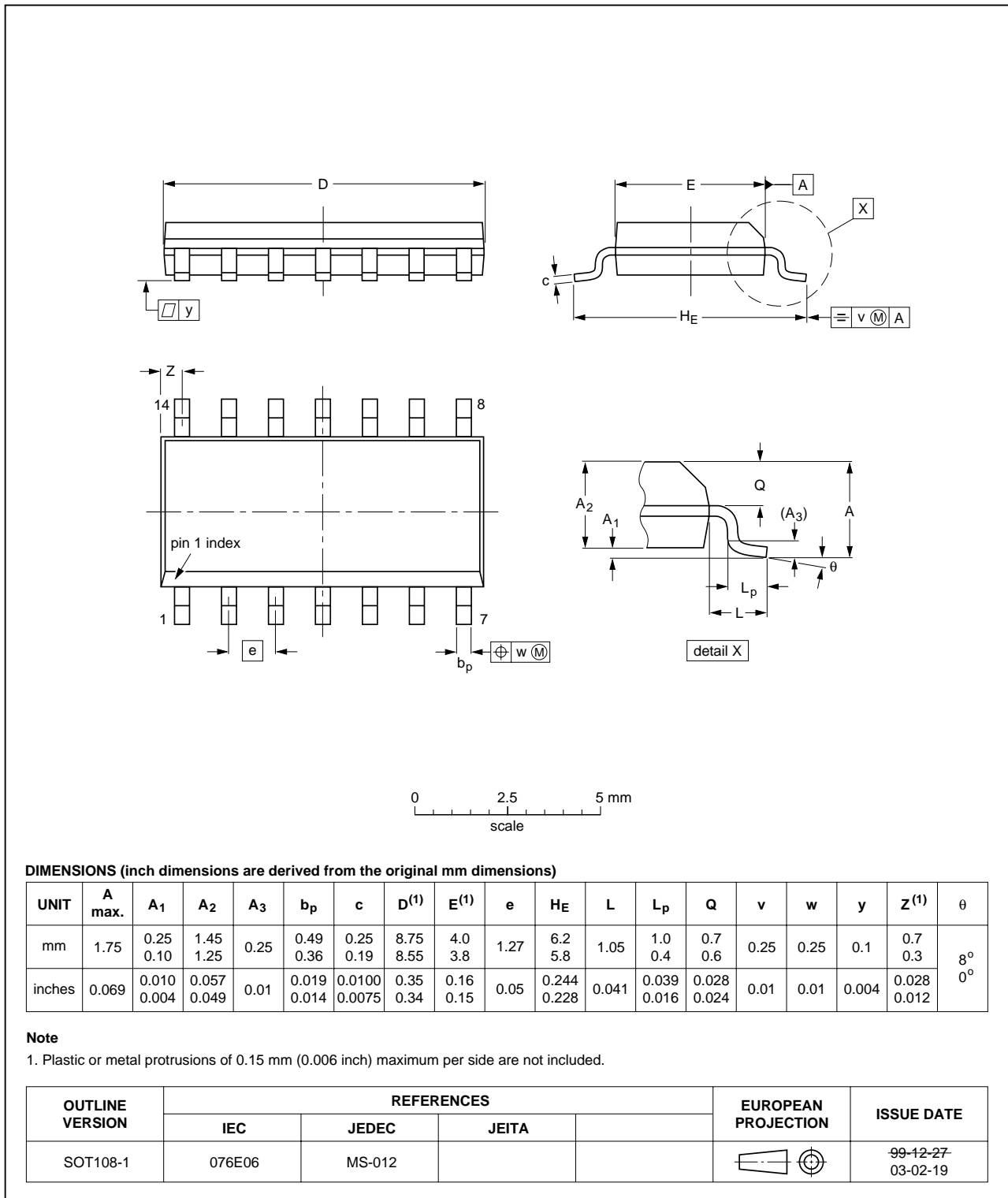
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## PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

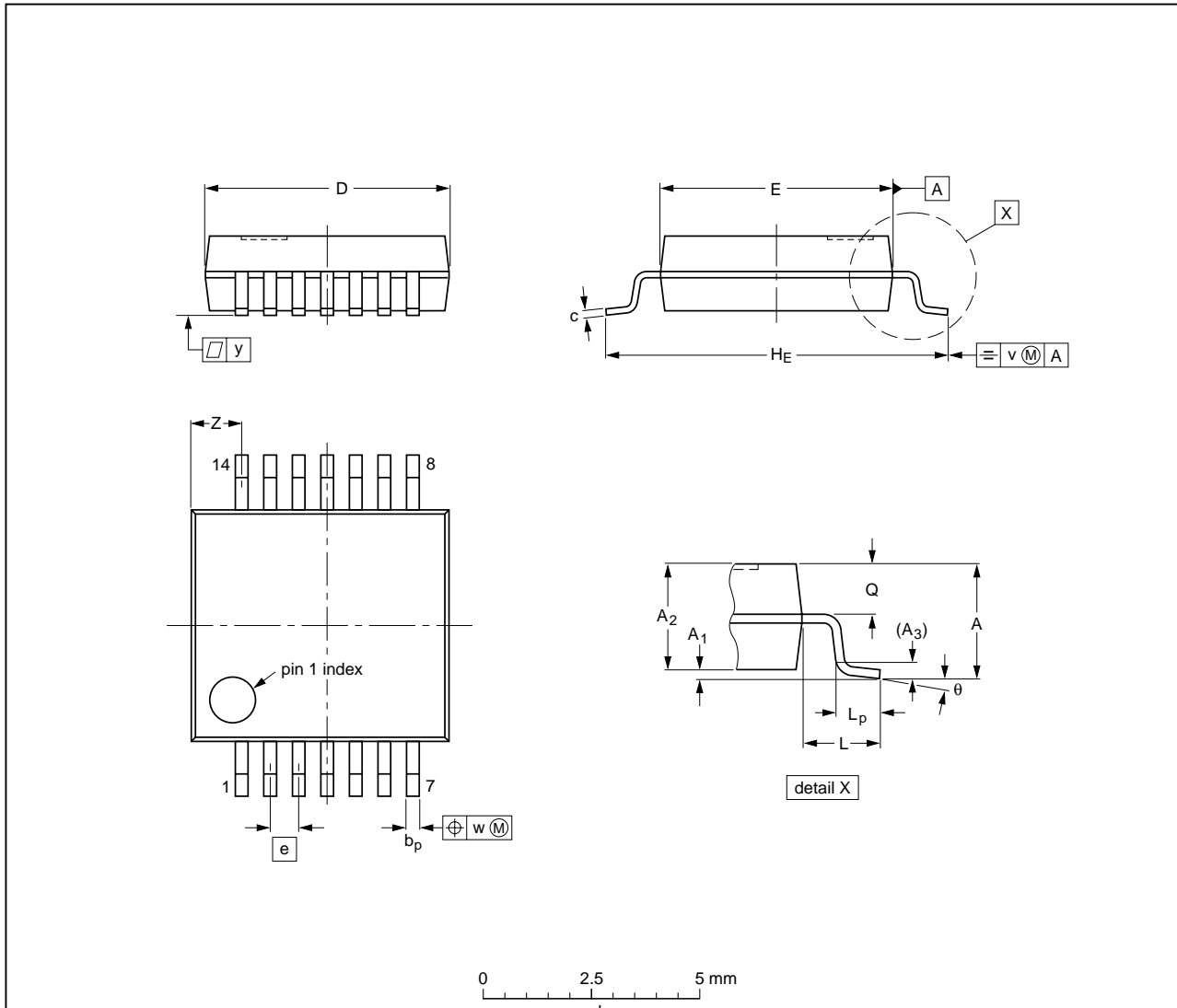


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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

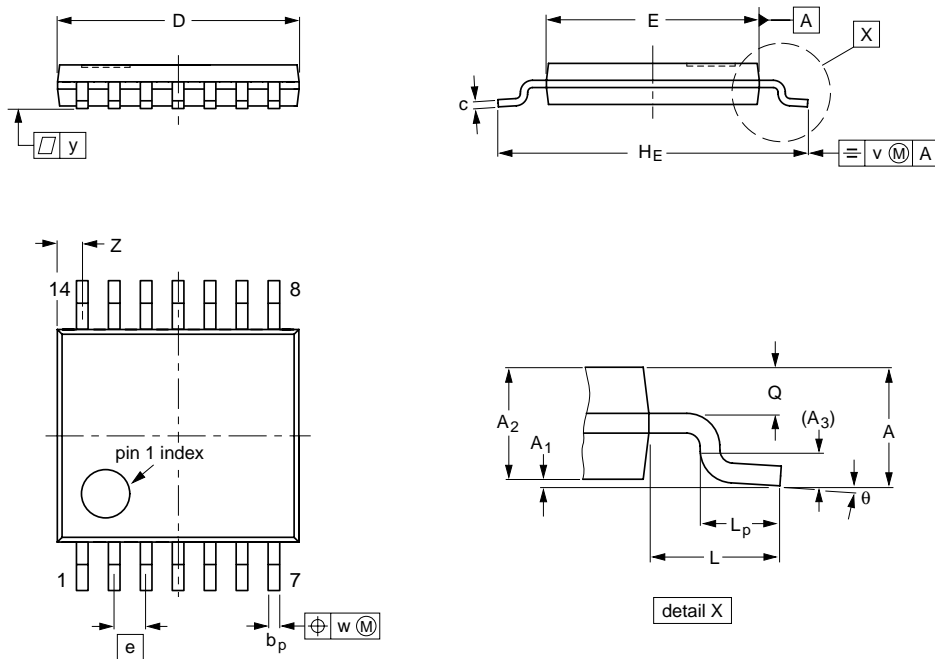
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				99-12-27 03-02-19

Triple 3-input AND gate

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

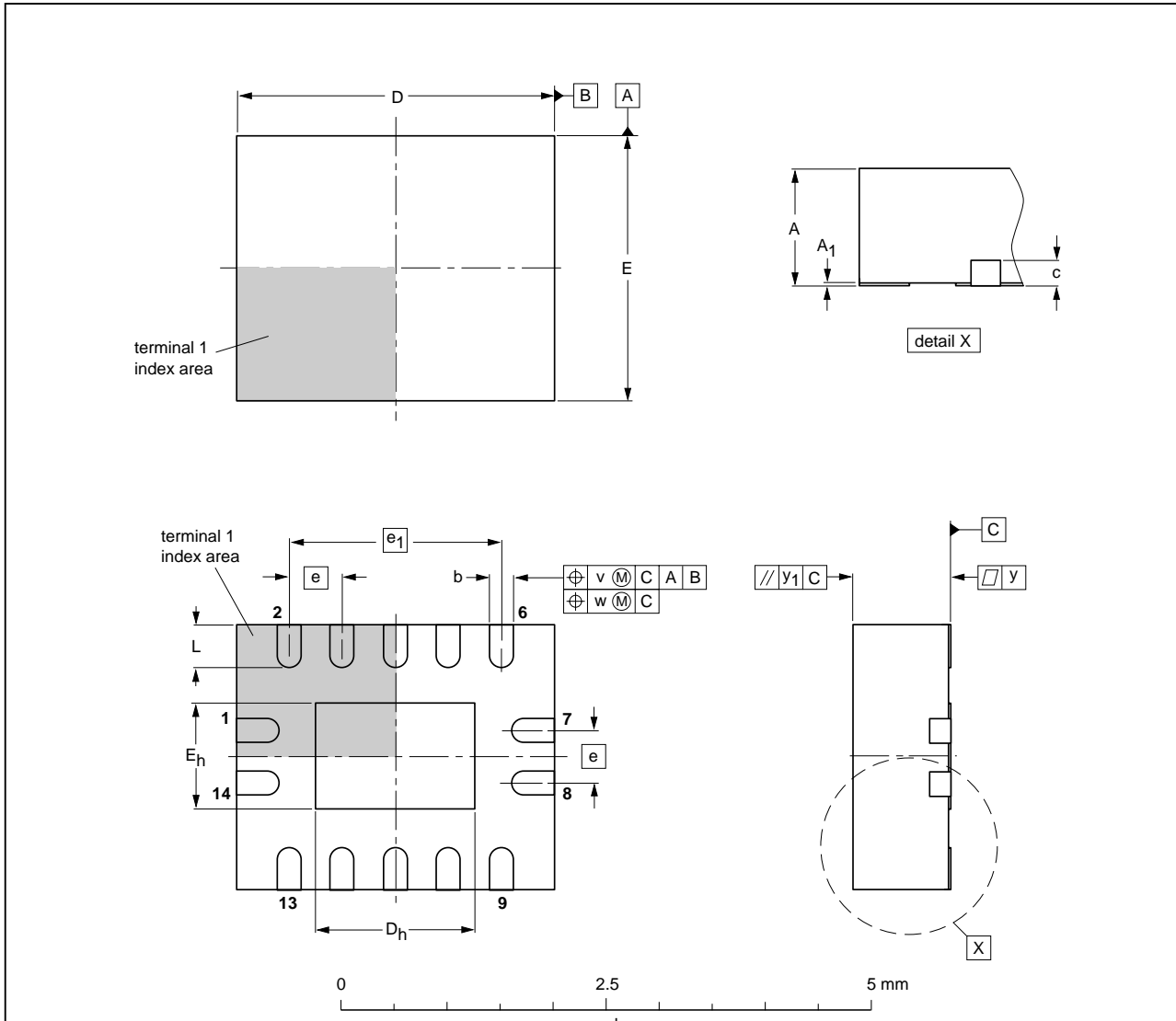
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT402-1		MO-153			99-12-27 03-02-18

# Triple 3-input AND gate

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**DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm**

**SOT762-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A <sup>(1)</sup> max.	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	L	v	w	y	y <sub>1</sub>
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT762-1	---	MO-241	---		02-10-17 03-01-27

## Triple 3-input AND gate

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