HT447K0/447P0 SPECIFICATION

Features

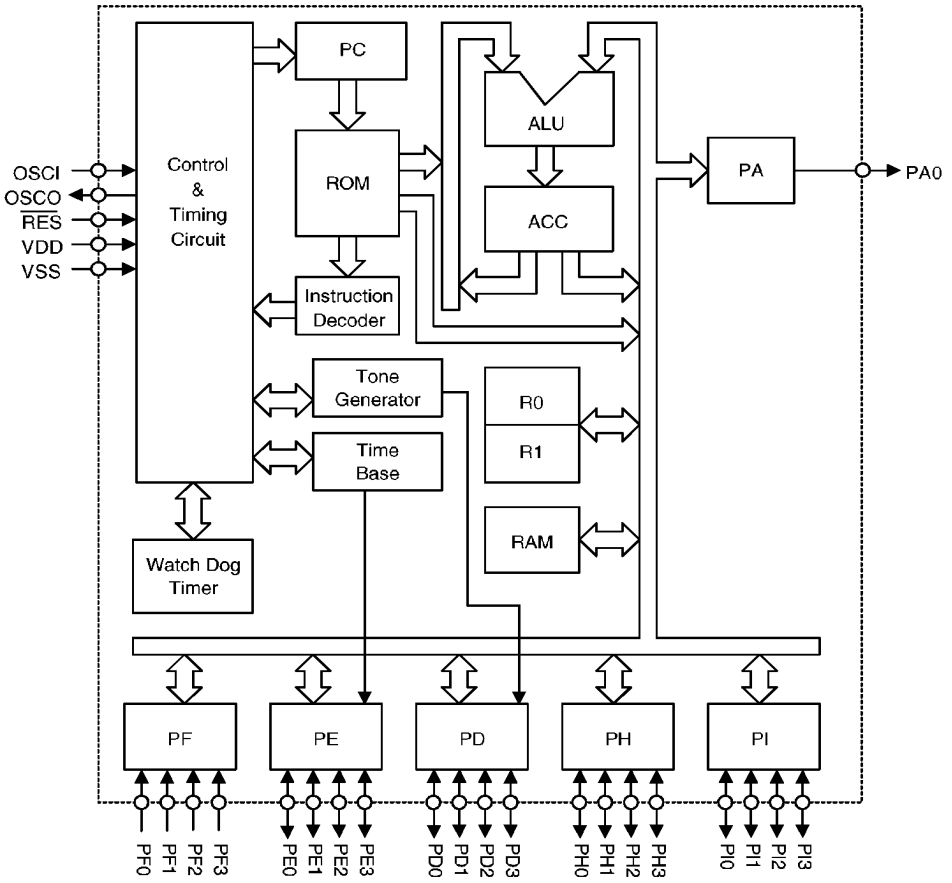
- Operating voltage: 2.4V~5V
- RC or crystal oscillator circuit as system clock
- A high driving output line with or without carriers
- An input port with latch capability
- 3 bidirectional I/O ports for HT447K0
- 4 bidirectional I/O ports for HT447P0
- 2 working registers
- Program memory ROM
  1K × 8 size for HT447K0
  2K × 9 size for HT447P0
- Data memory RAM
  32 × 4 size for HT447K0
  64 × 4 size for HT447P0
- Halt function to reduce power consumption and wake-up feature
- Watch dog timer
- Up to 1μs instruction cycle (4MHz system clock), at VDD=5V
- All instructions in 1 or 2 machine cycles
- 8–bit table read instruction
- Bit manipulation instruction

General Description

The HT447K0/447P0 are two processors from Holtek's 4-bit stand alone single chip microcontroller range specifically designed for multiple I/O products. The two devices are similar in most ways apart from size of ROM, RAM and I/O ports.

Both devices are ideally suited for multiple I/O low power applications, such as remote controllers, fan/light controllers, washing machine controllers, scalers, toys etc.

Block Diagram



Note:

ACC: Accumulator

PC: Program counter

R0,R1: Working registers

PA0: Output line with or without carriers

PD,PE,PH: I/O ports

PI: I/O port - for the HT447P0 only

PF: Input port

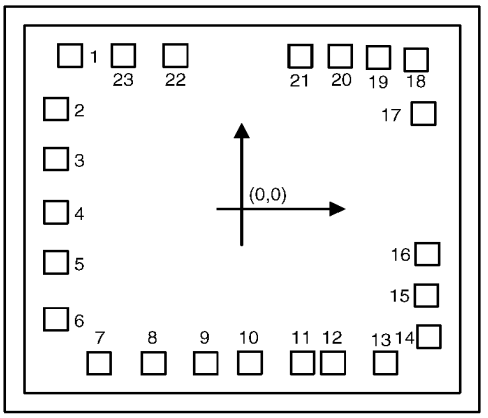
Pad Description HT447K0

Pad No.	Pad Name	I/O	Mask Option	Function
4~1	PD0~PD3	I/O	CMOS open drain pull-high single tone	4-bit bidirectional I/O port. The port can be configurated as a bidirectional I/O by instructions. PD2, PD3 can drive a pair of inverted single tone signals (by mask option).
8~5	PE0~PE3	I/O	CMOS open drain pull-high wake-up PE3 timebase	4-bit bidirectional I/O port. The port can be configurated as a bidirectional I/O by instructions. Also, it can be used as a wake-up microcomputer from the halt mode. PE3 has an additional time-base option.
16, 23 9, 22	PH0~PH3	I/O	CMOS open drain pull-high wake-up	4-bit bidirectional I/O port. The port can be configurated as a bidirectional I/O by instructions. Also, it can be used as a wake-up microcomputer from the halt mode.
10~13	PF0~PF3	I	Pull-high latch wake-up	4-bit input port
14	PA0	O	Level output or carrier output carrier 1/2 or 1/4 duty cycle	1-bit latch for output only, with high driving capacity and carrier output capability
15	VDD	I	—	Positive power supply
17 18	OSCO OSCI	O I	RC crystal	OSCI and OSCO are connected to a resistor or crystal for generating the system clock.
19	VSS	I	—	Negative power supply (GND)
20	$\overline{\text{RES}}$	I	—	Input for resetting the LSI inside with a pull-up resistor. It is used to initialize the processor and is activated on the low-going edge.
21	NC	—	—	Test pad This pad must be left open when the HT447K0 is in normal operation.

Pad Description HT447P0

Pad No.	Pad Name	I/O	Mask Option	Function
4~1	PD0~PD3	I/O	CMOS open drain pull-high single tone	4-bit bidirectional I/O port. The port can be configurated as a bidirectional I/O by instructions. PD2, PD3 can drive a pair of inverted single tone signals (by mask option).
8~5	PE0~PE3	I/O	CMOS open drain pull-high wake-up PE3 timebase	4-bit bidirectional I/O port. The port can be configurated as a bidirectional I/O by instructions. Also, it can be used as a wake–up microcomputer from the halt mode. PE3 has an additional time-base option.
18 27 9 26	PH0~PH3	I/O	CMOS open drain pull-high wake-up	4-bit bidirectional I/O port. The port can be configurated as a bidirectional I/O by instructions. Also, it can be used as a wake-up microcomputer from the halt mode.
11~10 23~24	PI0~PI3	I/O	CMOS open drain pull-high	4-bit bidirectional I/O port. The port can be configurated as a bidirectional I/O by instructions.
12~15	PF0~PF3	I	Pull-high latch wake-up	4-bit input port
16	PA0	O	Level output or carrier output carrier 1/2 or 1/4 duty cycle	1-bit latch for output only, with high driving capacity and carrier output capability
17	VDD	I	—	Positive power supply
19 20	OSCO OSCI	O I	RC crystal	OSCI and OSCO are connected to a resistor or crystal for generating the system clock.
21	VSS	I	—	Negative power supply (GND)
22	$\overline{\text{RES}}$	I	—	Input for resetting the LSI inside with a pull-up resistor. It is used to initialize the processor and is activated on the low-going edge.
25	NC	—	—	Test pad This pad must be left open when the HT447P0 is in normal operation.

Pad Coordinates & Position HT447K0



Chip size: $2620 \times 2390\ (\mu m)^2$

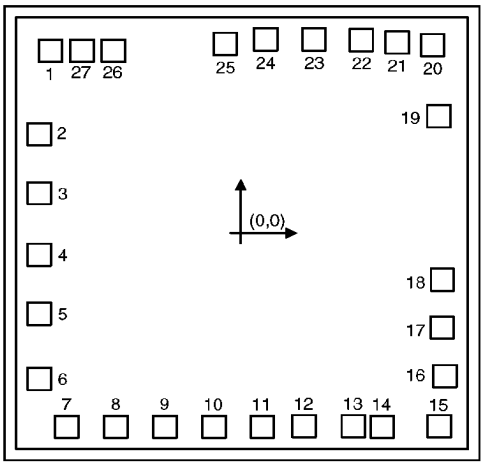
* The IC substrate should be connected to VSS in the PCB layout artwork.

Unit: μm

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1*	PD3	–1033	974.75	13	PF3	870.5	–969.75
2*	PD2	–1122.5	635.25	14*	PA0	1132.5	–805.75
3*	PD1	–1122.5	318.25	15*	VDD	1117.5	–544.75
4*	PD0	–1122.5	–18.25	16	PH0	1122.5	–283.75
5*	PE3	–1122.5	–336.25	17*	OSCO	1099.5	605.25
6*	PE2	–1122.5	–696.25	18*	OSCI	1053.5	946.25
7*	PE1	–862	–974.75	19*	VSS	826.5	959.25
8*	PE0	–531.5	–974.75	20*	$\overline{\text{RES}}$	596.5	969.25
9	PH2	–217.5	–974.75	21	NC	356	969.75
10*	PF0	49.5	–969.75	22	PH3	–399.5	974.75
11*	PF1	367.5	–969.75	23	PH1	–715	974.75
12	PF2	552.5	–969.75				

* These pins must be bonded out for functional testing.

Pad Coordinates & Position HT447P0



Chip size: 2980×2550 $(\mu m)^2$

* The IC substrate should be connected to VSS in the PCB layout artwork.

Unit: μm

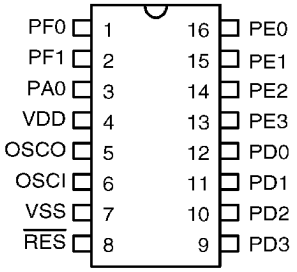
Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1*	PD3	–1224.25	988.5	15*	PF3	1277.25	–1045
2*	PD2	–1296.25	535.5	16*	PA0	1312.25	–774
3*	PD1	–1296.25	217.5	17*	VDD	1295.75	–513
4*	PD0	–1296.25	–119	18	PH0	1296.25	–252
5*	PE3	–1296.25	–437	19*	OSCO	1273.25	635
6*	PE2	–1296.25	–789.5	20*	OSCI	1234.75	1018
7*	PE1	–1120.25	–1050	21*	VSS	1007.75	1034.5
8*	PE0	–804.75	–1050	22*	$\overline{\text{RES}}$	777.75	1045
9	PH2	–490.75	–1050	23	PI2	470.75	1050
10	PI1	–175.25	–1050	24	PI3	162.75	1050
11	PI0	139.25	–1050	25	NC	–101.25	1024.5
12*	PF0	407.25	–1045	26	PH3	–819.25	988.5
13*	PF1	725.25	–1045	27	PH1	–1023.25	988.5
14*	PF2	910.25	–1050				

* These pins must be bonded out for functional testing.

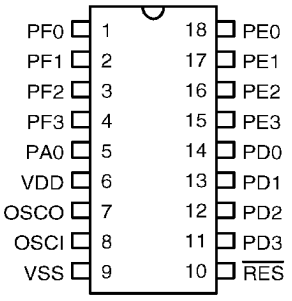
Package & Pin Assignment

HT447K0

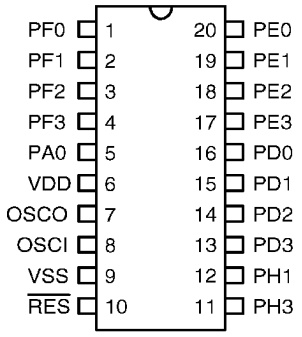
16 Pin DIP/SOP package



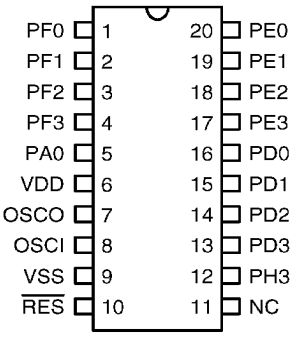
18 Pin DIP package



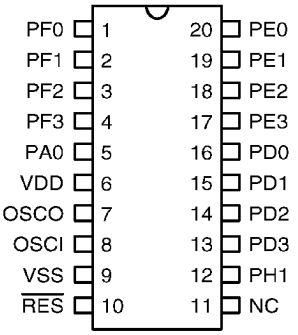
20 Pin DIP/SOP-A package



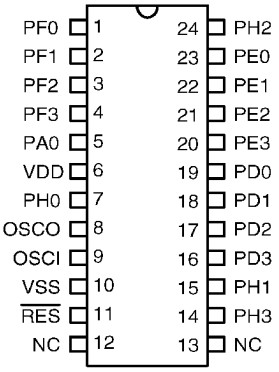
20 Pin DIP/SOP-B package



20 Pin DIP/SOP-C package

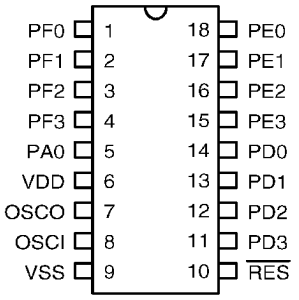


24 Pin SOP/SKINNY package

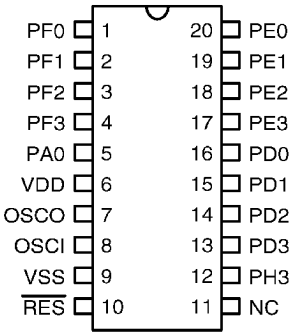


HT447P0

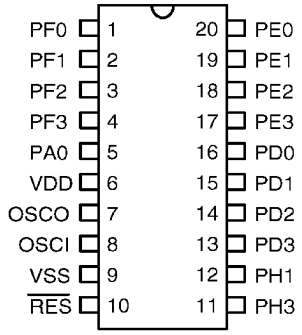
18 Pin DIP package



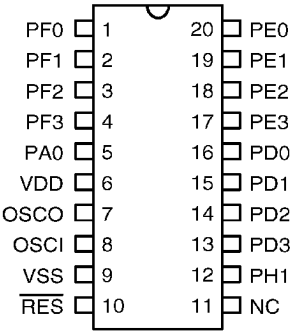
20 Pin DIP/SOP-B package



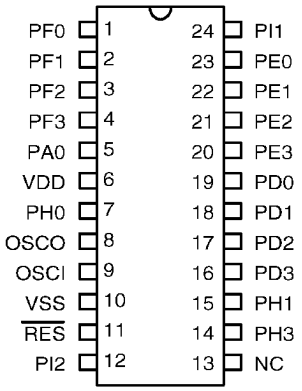
20 Pin DIP/SOP-A package



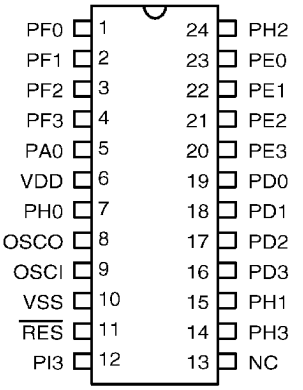
20 Pin DIP/SOP-C package



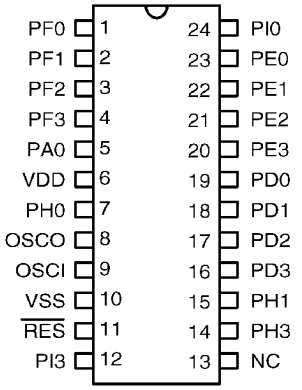
24 Pin SOP/SKINNY-A package



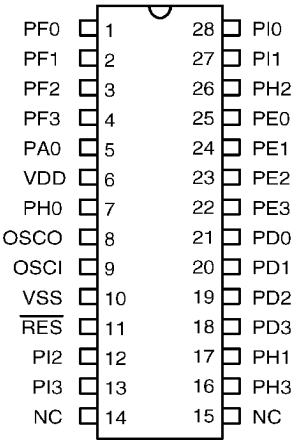
24 Pin SOP/SKINNY-C package



24 Pin SOP/SKINNY-B package



28 Pin SOP/SKINNY package



Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Supply Voltage	V_{DD}	–0.3	6	V
Input Voltage	V_I	V_{SS}–0.3	V_{DD}+0.3	V
Storage Temperature	T_{STG}	–50	125	°C
Operating Temperature	T_{OP}	–25	75	°C

A.C. Characteristics

(Ta=25°C)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
f_{SYS}	System clock	3V	RC oscillator	20	—	800	KHz
		5V		20	—	2000	KHz
		3V	Crystal oscillator	20	—	4000	KHz
		5V		20	—	4000	KHz
t_{CY}	Cycle time	—	f_{SYS}=4MHz	—	1.0	—	μs
t_{RES}	Reset pulse width	—	—	5	—	—	ms

D.C. Characteristics

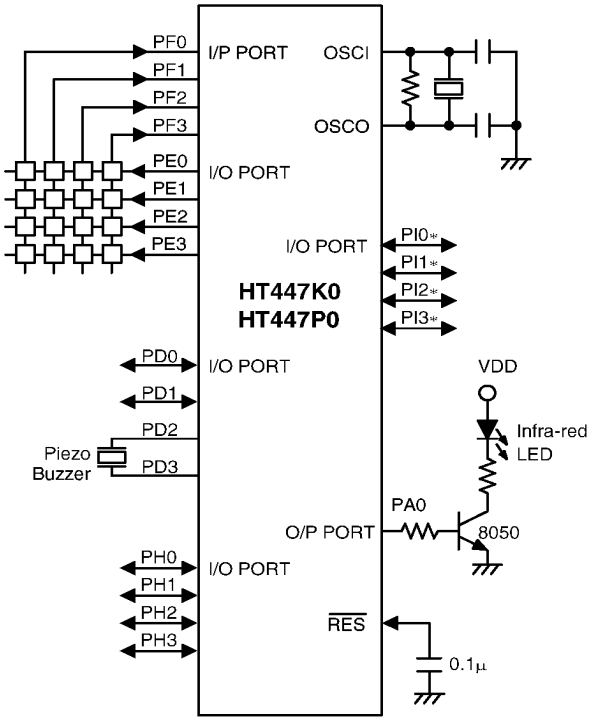
(Ta=25°C)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating voltage	—	—	2.4	—	5	V
I_{DD}	Operating current	3V	No load, f_{SYS}=2MHz	—	1	2	mA
		5V		—	1.5	3	mA
I_{STB}	Stand-by current	3V	No load, HALT mode	—	—	1	μA
		5V		—	—	2	μA
V_{IL1}	Input low voltage	3V	PD, PE, PF, PH, PI*	0	—	0.6	V
		5V		0	—	1	V
V_{IH1}	Input high voltage	3V	PD, PE, PF, PH, PI*	2.4	—	3	V
		5V		4	—	5	V
V_{IL2}	Input low voltage	3V	$\overline{RES}$	—	1.5	—	V
		5V		—	2.5	—	V
V_{IH2}	Iuput high voltage	3V	$\overline{RES}$	—	2.4	—	V
		5V		—	4.0	—	V
I_{OL1}	Port PA0 output sink current	3V	V_{OL}=0.3V	2	—	—	mA
		5V	V_{OL}=0.5V	5	—	—	mA
I_{OH1}	Port PA0 output source current	3V	V_{OH}=2.7V	–1	—	—	mA
		5V	V_{OH}=4.5V	–2.5	—	—	mA
I_{OL2}	PD, PE, PH, PI* output sink current	3V	V_{OL}=0.3V	1.5	—	—	mA
		5V	V_{OL}=0.5V	4.0	—	—	mA
I_{OH2}	PD, PE, PH, PI* output source current	3V	V_{OH}=2.7V	–0.8	—	—	mA
		5V	V_{OH}=4.5V	–2.0	—	—	mA
R_{PH}	Pull-high resistance	3V	PD, PE, PF, $\overline{RES}$, PH, PI*	20	—	100	KΩ
		5V		10	—	50	KΩ

* PI is available only in the HT447P0.

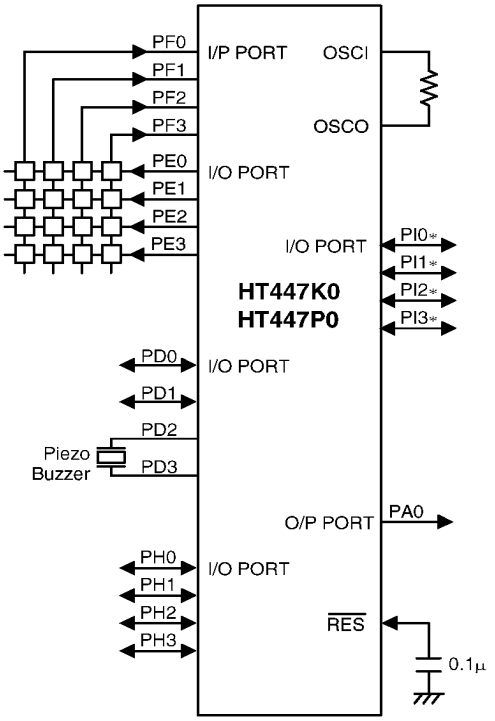
Application Diagram

Crystal system clock for remote controller applications



*: For the HT447P0 only

RC system clock for multiple I/O applications



*: For the HT447P0 only

SYSTEM ARCHITECTURE

Program Counter - PC

This is a binary counter which addresses the program memory (ROM). For the HT447K0 it is organized into 10 bits from PC0 to PC9 and is capable of specifying a maximum of 1024 addresses. For the HT447P0 it is organized into 11 bits from PC0 to PC10 and can specify a maximum of 2048 addresses.

The program counter (PC) is incremented by 1 or 2 with each execution of an instruction.

When executing the jump instruction (JMP, JNZ, JC, JZ...) or initial reset, the program counter (PC) will be loaded with the corresponding address data.

For jump and branch instructions, the address space is capable of specifying 1024(HT447K0)/ 2048(HT447P0) addresses directly (jump bit instructions are excluded).

Note: P0~P9/P10: Program location, defined by instructions
@: Current page number

Program Memory - ROM

The program memory is used to store the executed program and non-volatile data. It is organized into 1024×8 bits, from 000H to 3FFH for the HT447K0. For the HT447P0 there are 2048×9 bits, from 000H to 7FFH. It is addressed by the program counter. There are some special locations in the program memory as described below:

Location 0
Activating the $\overline{\text{RES}}$ pin of the processor causes the first instruction to be fetched from location 0.

Table location
The look-up table can locate in any position of the ROM. The instruction "READn MA" will read the table and transfer the table data to the ACC and data memory addressed by the register pair R1,R0. For the HT447P0 the bit 8 of the table data cannot be accessed by the table read instruction.

Working Registers - R1,R0

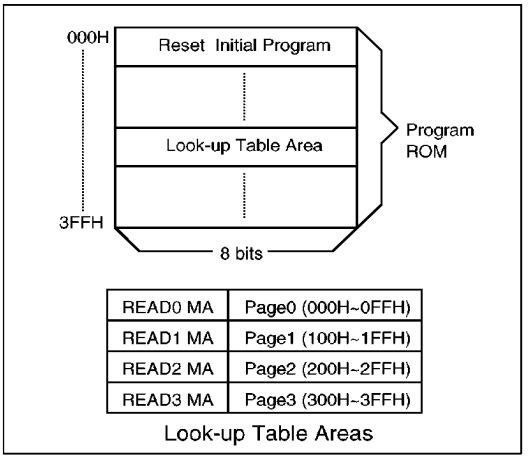
The working registers consist of register R0 which is of 4 bits wide, and register R1 which is of 1 bit wide in the HT447K0 and of 2 bits wide in the HT447P0. Their usual purpose is to store the frequently accessed intermediate results. The working register R0 can operate incremention (+1) or decremention (–1). The register pair R1,R0 can be used as the data

Mode	Program Counter									
	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Initial reset	0	0	0	0	0	0	0	0	0	0
Jump, Jump carry, Jump zero	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
Jump bit	@	@	P7	P6	P5	P4	P3	P2	P1	P0

Program Counter HT447K0

Mode	Program Counter										
	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Initial reset	0	0	0	0	0	0	0	0	0	0	0
Jump, Jump carry, Jump zero	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
Jump bit	@	@	@	P7	P6	P5	P4	P3	P2	P1	P0

Program Counter HT447P0



Program Memory HT447K0

memory, or used effectively as the data memory pointer when the data memory transfer instruction is executed.

Data Memory - RAM

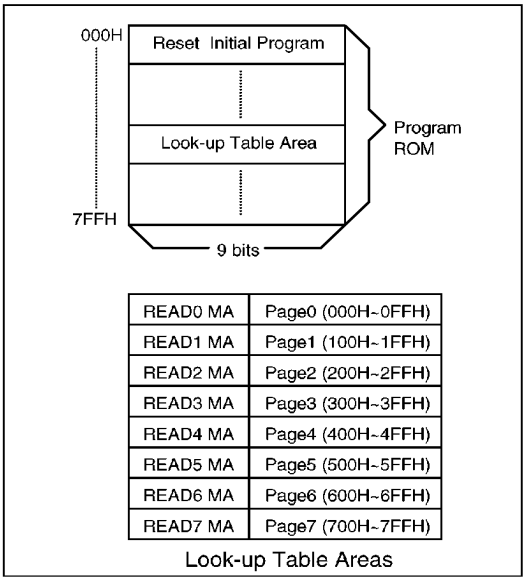
The static data memory is used to store data and is organized into 32×4 bits for the HT447K0 and 64×4 bits for the HT447P0. The data memory can be directly accessed by "MOV A,[XXH]", "MOV [XXH],A" and be indirectly addressed through the working register pair R1,R0.

Each bit of the data memory can be set or reset by instructions, and it is helpful in data manipulation.

The data memory may be affected by binary addition, logical operation, increment and decrement operation, data memory movement and bit manipulation.

Accumulator - ACC

The accumulator is the most important data register for data operation and control. It is one of the sources of inputs to the ALU and one of the result destinations of operations performed in the ALU. Data transfers between the I/O ports and memory may also pass through the accumulator.



Program Memory HT447P0

Arithmetic and Logic Unit - ALU

This circuit performs both arithmetic and logical operations. The ALU provides the following functions:

- Add with or without carry
- AND, OR, Exclusive OR
- Increment, Decrement
- Data transfer
- Branch decision

The ALU not only outputs the results of data operations but also sets the status of the carry flag (CF) and zero flag (ZF) in certain instructions.

Initial Reset

Both devices are provided with an $\overline{RES}$ pin for system initialization. This reset pin has an internal pull-high resistor. For all internal circuits to be reset it is combined with an external 0.1μF capacitor for providing an internal reset pulse. If the reset pulse is generated externally, the $\overline{RES}$ pin must be held low for 5ms at least.

The reset performs the following functions when the reset pulse is low ...

- The watchdog timer will be reset and stop counting
- Port PA0 will be in a low condition

The following situations will happen after the reset pulse returns high ...

- The program counter is set to 000H
- All the bidirectional pins are either floating or high depending upon the mask option
- PA0 contains no carriers but is set high or low depending upon the mask option
- The watch dog timer starts counting

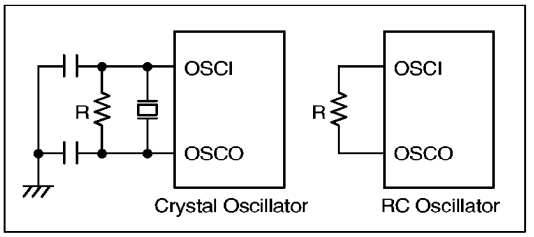
Oscillator Circuit

The system clock oscillation circuit can be either a crystal/resonator or an RC oscillator decided by mask option.

For the crystal oscillator, a crystal or ceramic resonator connected across the OSCI and OSCO provides the feedback and phase shift, both of which are required for oscillation. However the capacitor values will vary with the type and frequency chosen.

If an accurate frequency is not required a ceramic resonator may be used in place of the crystal one. For the RC oscillator, only a resistor across the OSCI and OSCO is required since a capacitor is already fabricated on the IC.

The system clock can be derived from the oscillator circuit. The oscillator circuit drives a 6 stage counter whose outputs can all be used as a system clock. Of the 6 stages, the first stage is different from the others for it includes a division by 2 or division by 3 option which depends upon the value of the carrier frequency. A division by 2 and a division by 3 will give k a value of 1.0 and 1.5, respectively, as shown in the following system clock equation. Note that n is the counter stage number.



Oscillator Configurations

$$\text{System clock} = \frac{\text{XTAL (RC)}}{2^{(6-n)} * ko}$$

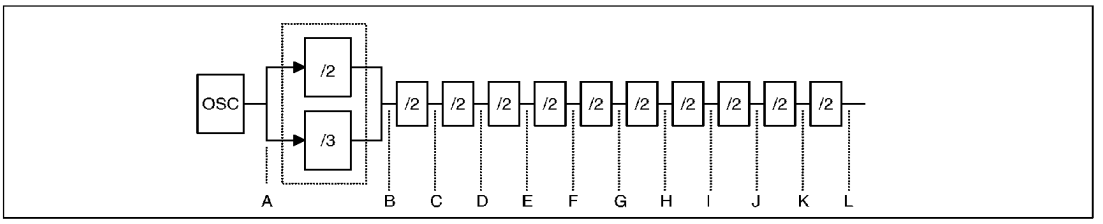
... where n ranges from 0 to 6; XTAL(RC) is the oscillator frequency; the value of ko is equal to the value of k of the prescaler. Note that if n is selected to be the value 6, ko will be changed to the value 1.

A machine cycle consists of a sequence of 4 states numbered T1 to T4. Each state lasts for an oscillator period. The system oscillator frequency ranges from 20KHz to 4MHz. The machine cycle turns out to be 1μs if the system frequency is 4MHz.

Prescaler

There is a prescaler for the HT447K0/447P0 to generate the system clock, carrier signal, WDT's clock and single tone signal.

The first stage of the prescaler is determined by the carrier's frequency. If the division by 3 option is chosen, the vaule of k is 1.5. Nonetheless,



Prescaler

k turns out to be 1 if division by 2 is chosen instead.

The system clock may come from A to G. The clock of WDT is derived from J to L. However, the single tone signal may come from H to L.

Output Line - PA0

PA0 is bit 0 of the port PA and is configured as a high driving capability CMOS output. Its additional carrier driving capability allows for easy interfacing to an infra-red diode.

The "carrier" option can be active depending on mask option. The carrier frequency is closely related to the system clock. Different system clock frequencies will result in different carrier frequencies. In addition, a 1/2 or 1/4 duty cycle can be selected.

The carrier frequency equation is as follows...

$$\text{Carrier frequency} = \frac{\text{XTAL (RC)}}{2^{(6-n)} * \text{kc}}$$

... where n ranges from 0 to 6. XTAL (RC) is the oscillator frequency. The value of kc is equal to the value of k of the prescaler. Note that if n is selected to be the value 6, kc will be change to the value 1.

If the "carrier" option is selected, writing a "0" to the PA0 latch (OUT PA,A where bit 0 of ACC=0) results in a carrier output. Writing a "1" to the PA0 latch keeps the state of PA0 at normal low level.

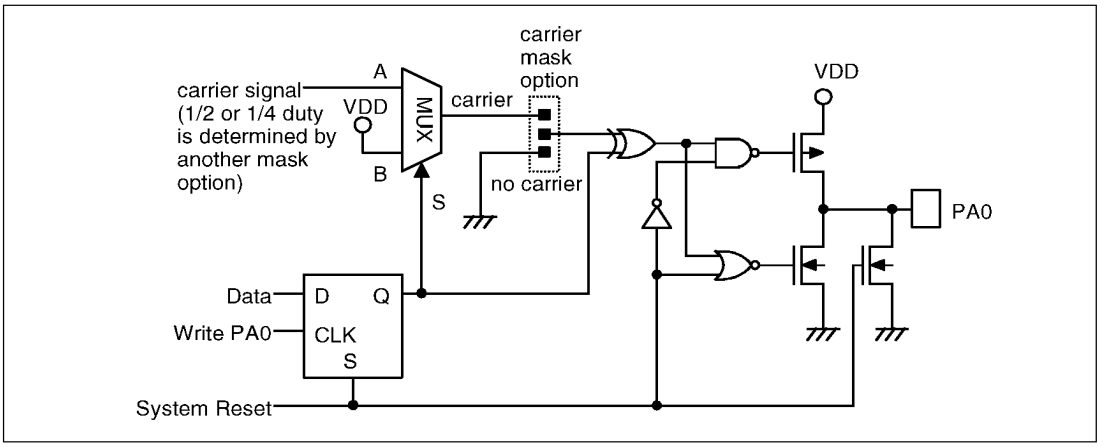
If the "no carrier" option is selected, it functions as a normal output line. Writing a "0" to the PA0 latch results in a low output. Otherwise, writing a "1" to the PA0 latch will keep a high output.

This line will be in a low condition during the time when the reset pulse is active. Once the reset pulse ends, it will assume a high or low state depending upon mask option. If the "carrier" option is selected the PA0 will stay at a low level. On the contrary, the PA0 will stay at a high level if the "no carrier" option is chosen.

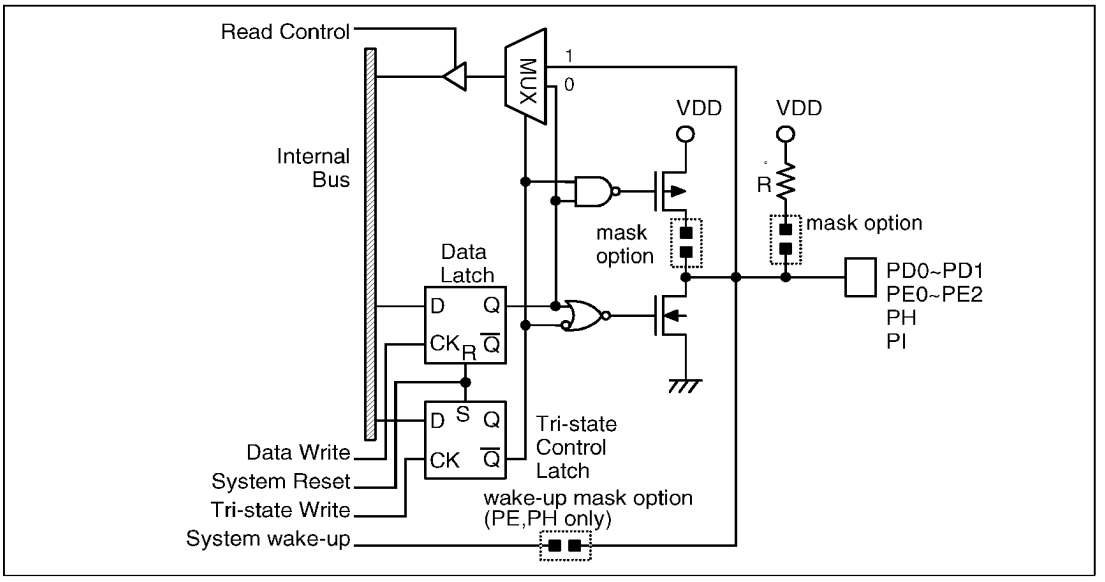
Input/Output Ports - PD,PE,PH,PI

There are four physical I/O ports (PD, PE, PH, PI) for the HT447P0 and three I/O ports for the HT447K0. All of these ports have the same basic structure, open drain NMOS output, CMOS output and internal pull-high resistor. Nonetheless, each line may have different configuration and mask options.

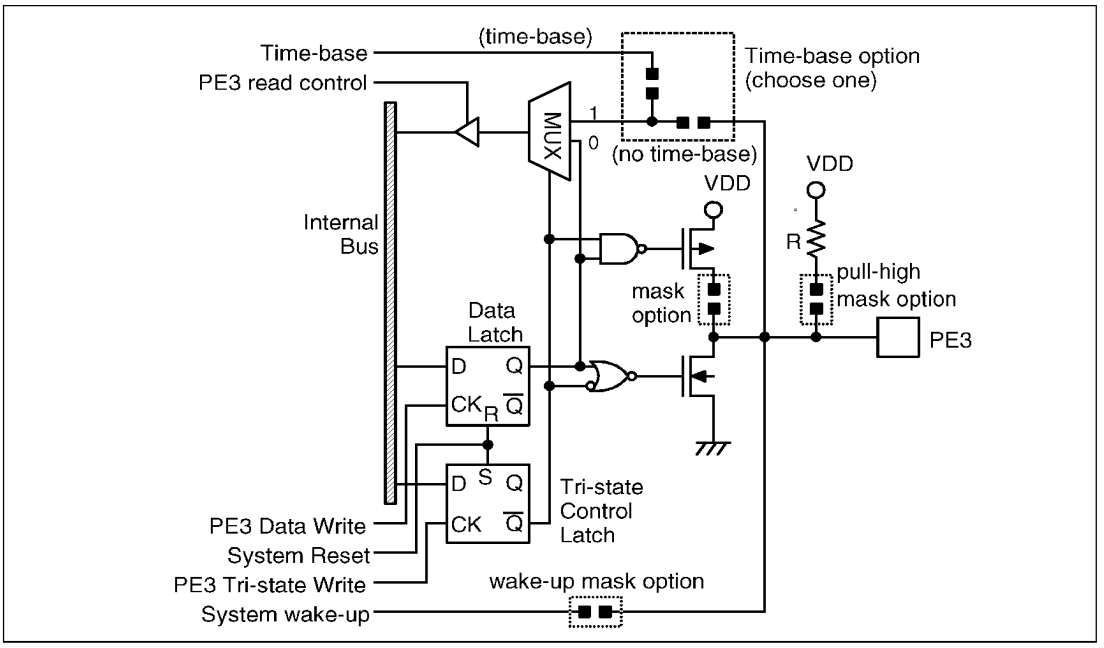
With this basic configuration, if a line performs an input function, a "TRI" instruction can be invoked (writing a "1" to the corresponding Tri-state control latch), which makes the output part of the input/output port exhibit a floating



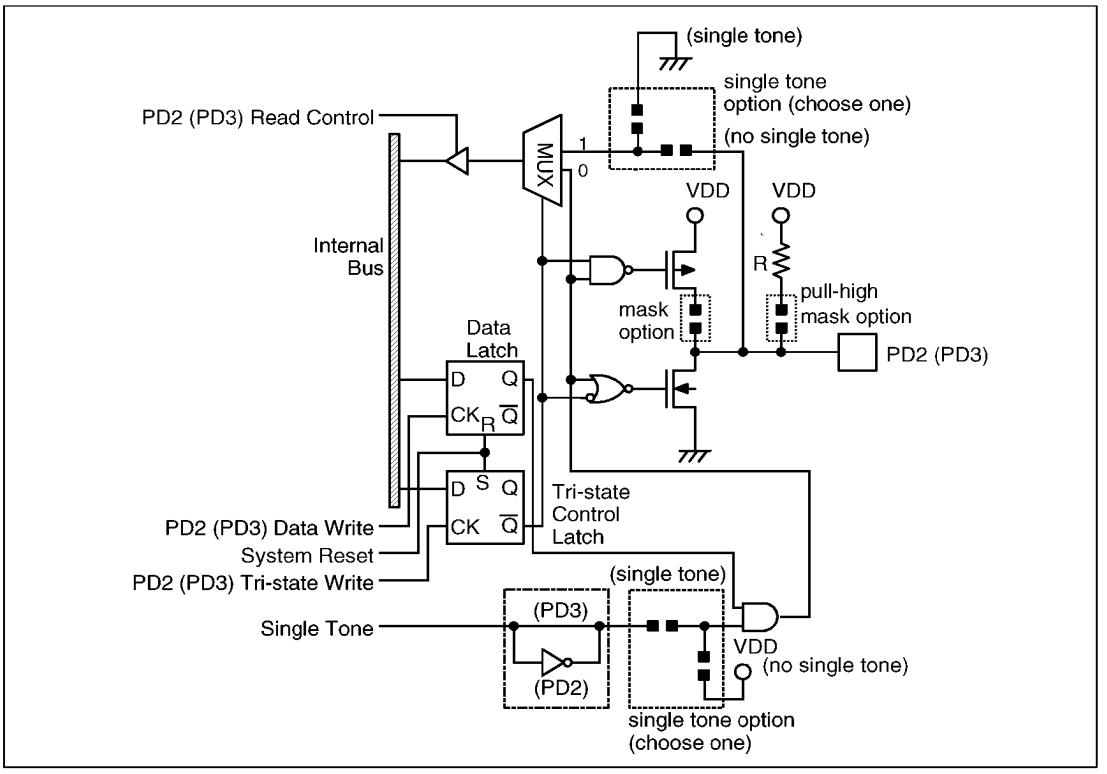
PA0 Output Line



Basic Structure of Input/Output Ports



Input/Output Ports - PE3



Input/Output Ports - PD2,PD3

state (in the case of no pull-high resistor option) to minimize the loading effect.

When the tri-state control latch is "1", the input operation is directly read from the pad. However, the input data comes from the internal data latch if the related tri-state control latch is "0". This feature is important when the ports apply the read-modify-write instructions.

After the power on is reset, the tri-state control latch will be "1". It implies that all the I/O lines are floating (or high level if they have pull-high resistors).

In the output application, three configurations can be selected; CMOS, NMOS open drain output with or without pull-high resistors. They can also drive the open-collector or open drain outputs without the need for additional external pull-high resistors. In the situation where pull-high resistors are selected and interfaced with an external output circuit, a "1" must be written to the data latch to turn off the NMOS. This is to avoid logical conflict.

Bit 0 to bit 2 of the PE port is a normal type configuration. PE3 has the time-base option and if that option is selected, the input function will differ from other I/O line(s). The "SET PE.3" and "CLR PE.3" are read-modify-write instructions whose operation may get different results from those intended if the time-base option is selected. PE also has a wake-up option (by forcing the low level at the terminal) which may make the HT447K0/447P0 escape the HALT state and resume operation.

The CPU can be used as an S/W timer by polling the time-base signal to measure its width or period.

Bit 2 and bit 3 of PD have single tone options. If the single tone is selected, writing a "1" to the related latch will drive the output stage according to the internal single tone signal. The single tone in bit 2 is the inverse of bit 3, which is a useful feature in differential drive applications. Reading these two bits will get "0" if the single tone option is selected. The set-bit or clear-bit instructions will lose their original specific functions. They can still be executed but no results can be derived.

Input Port - PF

There are 3 options available for this port, namely pull-high resistor, wake-up and latch type.

If the wake-up mask option is chosen a low level input will force the device to resume operation and leave the HALT mode.

The input port is available in both normal and latch type. When a normal type input is desired the input type control mask option must select VSS. On the other hand, if the latch type input is used the PF CLEAR option must be selected. A normal type input polls the state of input port by using a CPU instruction. A latch input on the other hand uses a hardware latch to store the port data which can then be read at any time by the processor. This option allows input pulses to be detected and reduces the processor loading time.

There are 4 phases in a machine cycle. If the port is configured as a latch type, the processor will read the data in the latch port at the second phase T2 by executing the instruction "IN A,PF". During the 4th phase of the same cycle, the processor will clear the latch port by setting PF CLEAR to 0. Attention must be paid to two improper operations which may occur with latch type configurations. The first is the occurrence of a low going input after the T2 phase and the end of that low going input before the end of the T4 phase. In this instance the pulse will not be seen by the processor. The other is if the low level duration extends to the end of the the input instruction's machine cycle, the processor will not clear the latch and the data will still be held in the latch giving a false reading the next time the input latch is read. The diagram gives more details.

Tone Generator

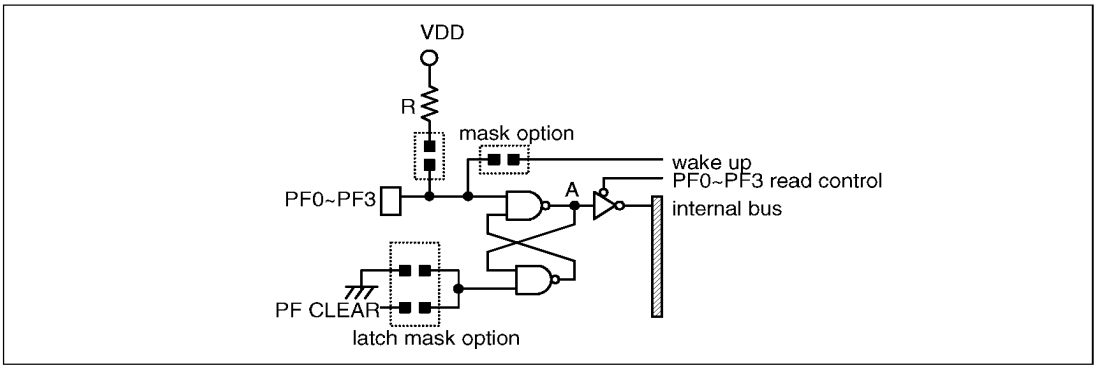
The HT447K0/447P0 provides a single tone generator.

The frequency of the tone signal is shown below:

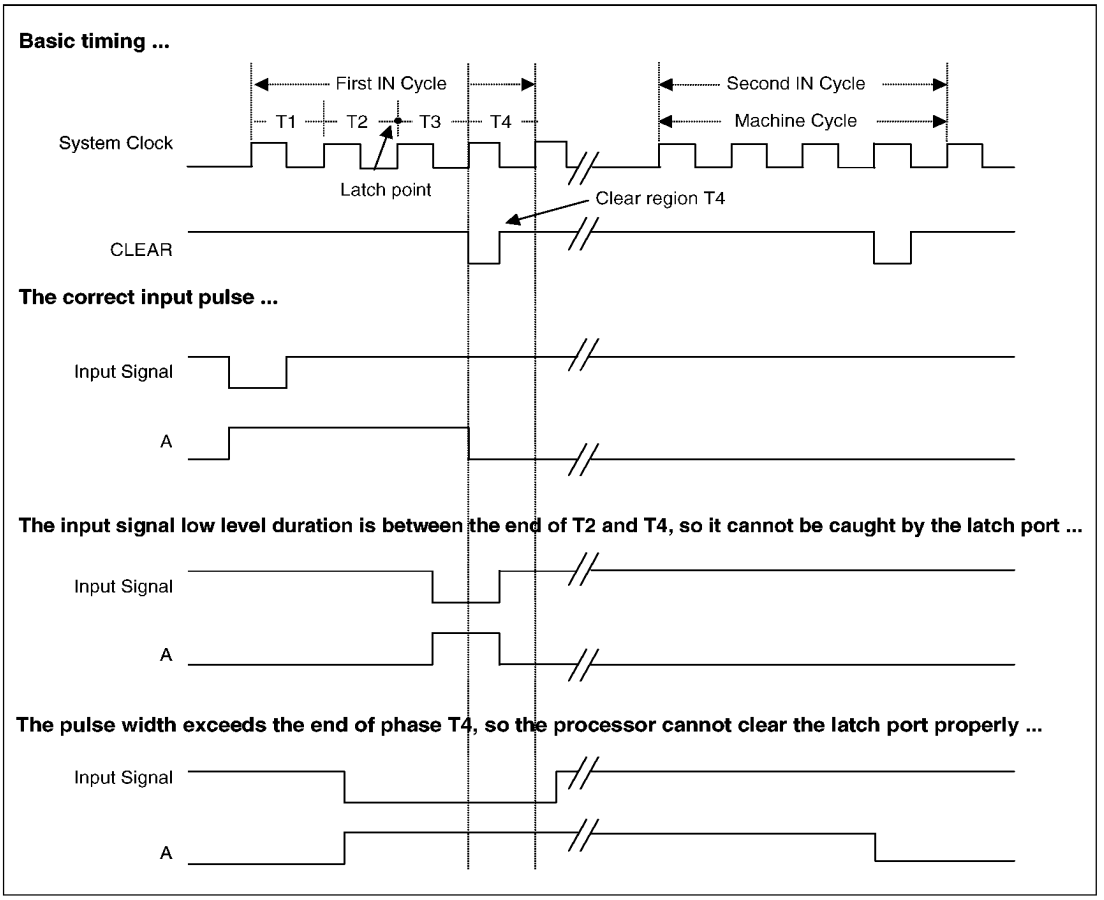
$$\text{Tone frequency} = \frac{\text{XTAL (RC)}}{2^{(11-n)} * k}$$

where n ranges from 0 to 4 by mask option. Since the tone signal and the carrier signal use the same prescaler, the value of k is determined by the prescaler. XTAL (RC) is the oscillator frequency.

The output terminal(s) of the tone generator depends upon the mask option. Bit 3 of port PD (PD3) can be optioned as an output of the tone



Input Port - PF



Input Port PF Timing

generator and bit 2 of port PD (PD2) can be optioned as an inverted output of the tone generator. These can be chosen only by PD3 or both PD2 and PD3. Once PD3 or PD2 is configured as the tone output, the input/output and set/clear operation in PD will not function as they are in the original spec, which is optioned as a tone output, and reading the corresponding bit will get a "0".

If PD2 and PD3 are configured as the tone output, writing "1" to PD3 will enable the tone output and writing "0" to PD3 will disable the tone output, and writing "0" or "1" to PD2 will not affect the tone output.

Watch Dog Timer - WDT

This timer is composed of an 8-stage count-up counter designed to prevent the program from jumping to an unknown or unwanted location. This prevents the application circuit from losing of control with unpredictable results.

The timer clock comes from the prescaler, and the carrier frequency option also affects the clock. The watch dog clock equation is as follows ...

The frequency of watch dog clock =

$$\frac{\text{XTAL (RC)}}{2^{(11-n)} * k}$$

... where n ranges from 0 to 2 by mask option. XTAL(RC) is the oscillator frequency. The value of k is determined by the prescaler.

In normal operation, the application program will reset this timer (by issuing a "CLEAR WDT" instruction) before the timer overflows. If timer overflow occurs, it implies that the operation is not under control. The HT447K0/447P0 will then perform a system reset to initialize the system. It has another option regarding the "CLEAR WDT" instruction - the clearing stage. The two or four stages in the MSB side or all the eight stages can be optioned to be cleared whenever the "CLEAR WDT" is performed. In other words, the remaining stage(s) will maintain its/their content(s) even if "CLEAR WDT" is executed.

During the power on reset period, the WDT will be cleared (no matter what kind of the clearing stage option is). After that, the WDT will start counting to function as a watch dog.

The user may disable the WDT by mask option. The time base uses the same stage of the WDT, so restraining the WDT function occurs in the synchronization stage.

Time Base

The time base is used to generate the regular time base signal. Since it utilizes the same counter with WDT, the clearing stage option of WDT will affect the time base option selection.

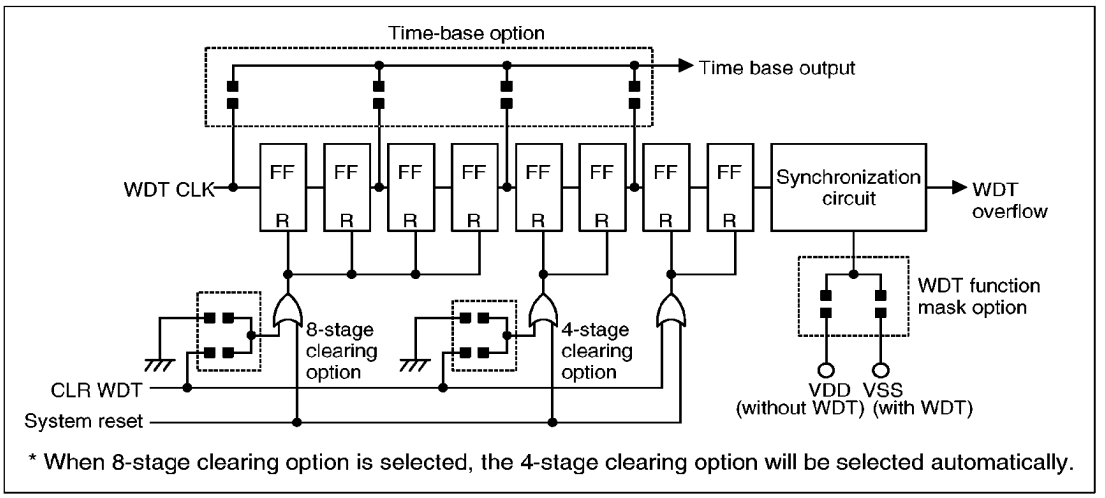
Normally, the frequency of the time base is the following:

The frequency of the time base =

$$\frac{\text{CLOCK of WDT}}{2^{(6-n)}}$$

If 2 clearing stages of the WDT option are selected, the lower 6 stages still operate, and n can be any value 0,2,4, or 6. If 4 clearing stages of the WDT option are adopted, the lower 4 stages operate well, and the value of n can be 0,2 or 4. If 8 clearning stages of the WDT option are chosen, n can only be 0.

The time base signal can be polled in bit 3 of port PE by mask option. With the importing of the PE operation the user can check the status of the time base signal. In that way, bit 3 of port PE can no longer reflect the state of PE3. Only the output function is available and bit set/clear



Witch Dog Timer - WDT

is useless. If the PE3 operates in the output mode, the time base signal will not be read.

Halt

When the instruction "HALT" is executed, the system clock will be stopped and the system is driven to a low power consumption state. The contents of the on-chip RAM and registers remain unchanged. The halt state can be terminated by a low level input to PE, PF and PH if these lines are configured to have the wake -up option by the appropriate mask option. A hardware reset will also wake up the processor and resume normal operation.

It should be noted that when the halt state is terminated by a low level input of PE, PF or PH the system will resume and execute the instruction right after the "HALT" instruction.

Mask Options

Oscillator	Crystal or RC
	The system clock equation: System clock = $\frac{\text{XTAL (RC)}}{2^{(6-n)} * \text{ko}}$ where n ranges from 0 to 6 by mask option ko is equal to the k value of the prescaler if n = 6 then ko=1, and XTAL(RC)=oscillator frequency
PD, PE, PH, PI* (PI is available only for the HT447P0)	CMOS or NMOS open drain
	Pull-high resistor or no pull-high resistor
	Wake-up (PE,PH); each line of PE and PH can be selected to wake-up the microcomputer from the HALT state.
	Time-base input (PE3); the time-base signal will substitute the input line.
	Single tone output (PD2,PD3); the single tone signal will drive the output stage.
PF	Pull-high resistor or no pull-high resistor latch type
	Latch type
	Wake-up; each line of PF can be selected to wake-up the microcomputer from the HALT mode.
PA0	Carrier frequency eauation: Carrier frequency = $\frac{\text{XTAL (RC)}}{2^{(6-n)} * \text{kc}}$ where n ranges from 0 to 6 by mask option kc is equal to the k value of the prescaler if n=6 then kc=1, and XTAL(RC)= oscillator frequency
	With or without a carrier option
	Carrier signal can be selected as a 1/2 or 1/4 duty cycle.

Watch dog timer	No watch dog timer
	The frequency of WDT's clock = $\frac{\text{XTAL (RC)}}{2^{(11-n)} * k}$ where n ranges from 0 to 2 by mask option XTAL(RC)= oscillator frequency
	Clearing stage option; 2,4,8 can be selected.
Time-base	The frequency of time base = $\frac{\text{CLOCK of WDT}}{2^{(6-n)}}$ where n can be 0,2,4 or 6, which is also determined by the clearing stage option of WDT.
	PE3 input option; the time-base signal can be monitored in the PE3 input.
Tone	The frequency of tone = $\frac{\text{XTAL (RC)}}{2^{(11-n)} * k}$ where n ranges from 0 to 4 by mask option XTAL (RC)= oscillator frequency
	PD2 and PD3 output option; the tone signal can be exhibited in PD2 or PD3 with different phases.

Software Tools

To ease the programming task and to reduce development time Holtek supplies a development system for the HT447K0/HT447P0. The system runs under an IBM PC-XT/AT environment and consists of both a hardware emulation board and a suite of programs including powerful debug functions. The user can download the code from the PC to the emulation board for verification. The main features of the system are as follows.

- Can incorporate the user's text editor or word processor with Holtek's cross assembler to form an integrated development system
- Supports mouse functions with its window based human interface
- Performs stand-alone operation for demonstration purposes
- Auto-executes self test function at every power on reset
- Provides symbolic debugging capabilities
- User defined mask options
- RC with variable resistor or crystal system clock provided
- Displays and modifies registers, carry flag, timer, port output level and internal RAM
- Single instruction stepping
- Jumps unconditionally to any address and halts anytime during execution
- Provides up to 8 breakpoint settings
- Real time 255 forward step or 256 backward step trace

After program verification on the emulation board the customer supplies Holtek with the verified code prior to manufacture.

INSTRUCTION SET

Instruction Set Summary

The following tables gives a complete list of instructions for the two processors. Note that the machine codes of the two devices may differ. This is because the HT447P0 posseses instructions of 9-bit width but the HT447K0 has 8 bits only. Note that in some cases the operation code may differ as a result of different internal resources, and this is also indicated where applicable.

Mnemonic	Description	Word	Cycle	CF	ZF
Arithmetic					
ADD A,M	Add data memory to ACC	1	1	√	√
ADD M,A	Add ACC to data memory	1	1	√	√
ADC A,M	Add data memory with carry to ACC	1	1	√	√
ADC M,A	Add ACC with carry to data memory	1	1	√	√
ADD A,XH	Add immediate data to ACC	1	1	√	√
ANC A,XH	Add immediate data to ACC with CF not affected	2	2	—	√
CPL A	Complement ACC	1	1	—	√
CPL R1	Complement R1	1	1	—	√
Logic operation					
AND A,M	AND data memory to ACC	1	1	—	√
AND M,A	AND ACC to data memory	1	1	—	√
AND A,XH	AND immediate data to ACC	2	2	—	√
OR A,M	OR data memory to ACC	1	1	—	√
OR M,A	OR ACC to data memory	1	1	—	√
OR A,XH	OR immediate data to ACC	2	2	—	√
XOR A,M	Exclusive-OR data memory to ACC	1	1	—	√
XOR M,A	Exclusive-OR ACC to data memory	1	1	—	√
XOR A,XH	Exclusive-OR immediate data to ACC	2	2	—	√
Increment & Decrement					
INC R0	Increment register R0	1	1	—	√
INC M	Increment data memory	1	1	√	√
DEC R0	Decrement register R0	1	1	—	√
DEC M	Decrement data memory	1	1	√	√
Rotate					
RLC A	Rotate ACC left through the carry	1	1	√	—
RRC A	Rotate ACC right through the carry	1	1	√	—
Input & Output					
IN A,Pi	Input port-i to ACC, port-i=PD,PE,PF,PH,PI*	1	1	—	√
OUT Po,A	Output ACC to port-o, port-o=PD,PE,PH,PI*	1	1	—	—
TRI Pn,A	Output ACC to tri-state latch of port-n, port-n=PD,PE,PH,PI*	1	1	—	—
OUT PA,A	Output ACC0 to port A	1	1	—	—

Mnemonic	Description	Word	Cycle	CF	ZF
Data Move					
MOV A,R0	Move R0 to ACC	1	1	—	√
MOV R0,A	Move ACC to R0	1	1	—	—
MOV A,R1	Move R1 to ACC	1	1	—	√
MOV R1,A	Move ACC to R1	1	1	—	—
MOV A,M	Move data memory to ACC	1	1	—	√
MOV M,A	Move ACC to data memory	1	1	—	—
MOV A,XH	Move immediate data to ACC	1	1	—	—
MOV R1R0,XXH	Move immediate data to R1 and R0	1	1	—	—
MOV R0,M	Move data memory to R0	1	1	—	—
MOV A,[XXH]	Move data memory to ACC directly	1	1	—	√
MOV [XXH],A	Move ACC to data memory directly	1	1	—	—
Branch					
JMP addr	Jump unconditionally	2	2	—	—
JC addr	Jump on carry=1	2	2	—	—
JNC addr	Jump on carry=0	2	2	—	—
JZ addr	Jump on zero flag=1	2	2	—	—
JB A.i,addr	Jump on A.i=1	2	2	—	—
JB Pm.i,addr	Jump on Pm.i=1, Pm=PE	2	2	—	—
JB M.i,addr	Jump on M(R1,R0).i=1	2	2	—	—
JNZ addr	Jump on zero flag=0	2	2	—	—
JNB A.i,addr	Jump on A.i=0	2	2	—	—
JNB M.i,addr	Jump on M(R1,R0).i=0	2	2	—	—
Miscellaneous					
HALT	Enter power down mode	1	2	—	—
NOP	No operation	1	1	—	—
Flag					
CLR C	Clear carry flag	1	1	0	—
SET C	Set carry flag	1	1	1	—
Table Read					
READn MA	Read page 0~3 of ROM code to M(R1,R0) & ACC - HT447K0 only Read page 0~7 of ROM code to M(R1,R0) & ACC - HT447P0 only	1	2	—	√
Bit Set/Reset					
SET M.i	Set bit of data memory	1	1	—	—
CLR M.i	Clear bit of data memory	1	1	—	—
SET Pn.i	Set bit of Pn.i, Pn=PD,PE,PI*	1	1	—	—
CLR Pn.i	Clear bit of Pn.i, Pn=PD,PE,PI*	1	1	—	—
Watch Dog					
CLEAR WDT	Clear watch dog timer	1	1	—	—

* PI is available only for the HT447P0.

Instruction Definitions

ADC A,M Add data memory content and carry to accumulator

Machine code 0 0 1 0 0 0 0 0 - for the HT447K0

0 0 0 1 0 0 0 0 0 - for the HT447P0

Description The content of the data memory addressed by the register pair "R1,R0", the carry flag and the accumulator are added simultaneously. The result is stored in the accumulator. The carry and zero flags are affected.

Operation ACC ← ACC+M(R1,R0)+CF

ADC M,A Add accumulator and carry to data memory

Machine code 0 0 0 0 0 0 0 0 - for the HT447K0

0 0 0 0 0 0 0 0 0 - for the HT447P0

Description The content of the data memory addressed by the register pair "R1,R0", the carry flag and the accumulator are added simultaneously. The result is stored in the data memory. The carry and zero flags are affected.

Operation M(R1,R0) ← ACC+M(R1,R0)+CF

ADD A,M Add data memory to accumulator

Machine code 0 0 1 1 0 0 0 0 - for the HT447K0

0 0 0 1 1 0 0 0 0 - for the HT447P0

Description The content of the data memory addressed by the register pair "R1,R0" and the accumulator are added. The result is stored in the accumulator. The carry and zero flags are affected.

Operation ACC ← ACC+M(R1,R0)

ADD A,XH Add immediate data to accumulator

Machine code 0 1 1 1 d d d d - for the HT447K0

0 0 1 1 1 d d d d - for the HT447P0

Description The immediate data and the accumulator content are added. The result is stored in the accumulator. The carry and zero flags are affected.

Operation ACC ← ACC+XH

ADD M,A Add accumulator to data memory

Machine code 0 0 0 1 0 0 0 0 - for the HT447K0

0 0 0 0 1 0 0 0 0 - for the HT447P0

Description The content of the data memory addressed by the register pair "R1,R0", and the accumulator content are added. The result is stored in the data memory. The carry and zero flags are affected.

Operation M(R1,R0) ← ACC+M(R1,R0)

ANC A,XH Add immediate data to ACC with CF not affected

Machine code 0 0 0 0 d d d d 0 0 0 0 0 0 1 1 - for the HT447K0

0 0 0 0 0 d d d d 0 0 0 0 0 0 0 1 1 - for the HT447P0

Description The immediate data and the accumulator content are added. The result is stored in the accumulator. The zero flag is affected.

Operation ACC ← ACC+XH

AND A,M Logical AND data memory to accumulator

Machine code 0 0 0 1 0 0 1 1 - for the HT447K0

0 0 0 0 1 0 0 1 1 - for the HT447P0

Description Data in the accumulator and the data memory addressed by the register pair "R1,R0" perform the bitwise logical-AND operation and the result is stored in the accumulator. The zero flag is affected.

Operation ACC ← ACC "AND" M(R1,R0)

AND A,XH Logical AND accumulator with immediate data

Machine code 0 0 0 0 0 0 1 1 0 0 1 0 d d d d - for the HT447K0

0 0 0 0 0 0 0 1 1 0 0 0 1 0 d d d d - for the HT447P0

Description Data in the accumulator and the specified data perform the bitwise logical-AND operation and the result is stored in the accumulator. The zero flag is affected.

Operation ACC ← ACC "AND" XH

AND M,A Logical AND accumulator to data memory

Machine code 1 1 0 0 0 0 0 0 - for the HT447K0

0 1 1 0 0 0 0 0 0 - for the HT447P0

Description Data in the accumulator and the data memory addressed by the register pair "R1,R0" perform the bitwise logical-AND operation and the result is stored in the data memory. The zero flag is affected.

Operation M(R1,R0) ← ACC "AND" M(R1,R0)

CLEAR WDT Clear watch dog timer

Machine code 1 1 1 0 0 0 0 1 - for the HT447K0

0 1 1 1 0 0 0 0 1 - for the HT447P0

Description The watch dog timer is cleared. The zero and carry flags are not affected.

CLR C Clear carry flag

Machine code 1 1 1 0 0 0 1 0 - for the HT447K0

0 1 1 1 0 0 0 1 0 - for the HT447P0

Description The carry is reset to zero.

Operation CF ← 0

CLR M.i Clear bit of data memory

Machine code 0 0 1 1 i3 i2 i1 i0 - for the HT447K0

0 0 0 1 1 i3 i2 i1 i0 - for the HT447P0

i0~i3 are determined by operand i. The corresponding bit will be "0" if i is reset.Otherwise the bit is set to 1. For example, if i=0 then i3~i0=1110.

Description The specified bit of data memory addressed by register pair "R1,R0" is reset to zero.

Operation M(R1,R0).i ← 0

CLR Pn.i Clear bit of port

Machine code
PD 0 0 1 0 i3 i2 i1 i0 - for the HT447K0
0 0 0 1 0 i3 i2 i1 i0 - for the HT447P0
PE 0 0 0 0 i3 i2 i1 i0 - for the HT447K0
0 0 0 0 0 i3 i2 i1 i0 - for the HT447P0
PI 1 0 0 1 0 i3 i2 i1 i0 - for the HT447P0 only

i0~i3 are determined by operand i. The corresponding bit will be "0" if i is reset. Otherwise the bit is set to 1. For example, if i=0 then i3~i0=1110.

Description The specified bit of port "Pn" is reset to zero. Pn can be PD,PE,PI.

Operation Pn.i ← 0; Pn=PD,PE,PI

CPL A Complement accumulator

Machine code
0 0 1 1 1 1 1 1 - for the HT447K0
0 0 0 1 1 1 1 1 1 - for the HT447P0

Description Each bit of the accumulator is logically complemented. The zero flag is affected.

Operation $ACC \leftarrow \overline{ACC}$

CPL R1 Complement R1

Machine code
1 1 1 1 0 0 0 1 - for the HT447K0
1 1 1 1 1 0 0 0 1 - for the HT447P0

Description Each bit of the register R1 is logically complemented. The zero flag is affected.

Operation $R1 \leftarrow \overline{R1}$

DEC M Decrement data memory

Machine code
0 0 0 0 1 1 1 1 - for the HT447K0
0 0 0 0 0 1 1 1 1 - for the HT447P0

Description Data in the data memory specified by the register pair "R1,R0" is decremented by one. The carry and zero flags are affected. Carry is set if a borrow does not take place in DEC M operation; otherwise carry is cleared.

Operation M(R1,R0) ← M(R1,R0)–1

DEC R0 Decrement register R0

Machine code 0 0 0 1 1 1 1 1 - for the HT447K0

0 0 0 0 1 1 1 1 1 - for the HT447P0

Description Data in the working register R0 is decremented by one. Only the zero flag is affected.

Operation R0 ← R0–1

HALT Enter halt state

Machine code 0 0 1 1 0 1 0 1 - for the HT447K0

0 0 0 1 1 0 1 0 1 - for the HT447P0

Description HALT stops instruction execution and places the controller in the power down mode. Reset or an active signal in the "PE,PF,PH" ports (by mask option) will resume execution. No flags are affected.

IN A,Pi Input port to accumulator

Machine code

PD	0 0 1 0 1 0 0 1 - for the HT447K0
	0 0 0 1 0 1 0 0 1 - for the HT447P0
PE	0 0 0 0 1 0 0 1 - for the HT447K0
	0 0 0 0 0 1 0 0 1 - for the HT447P0
PF	0 0 1 0 1 1 0 0 - for the HT447K0
	0 0 0 1 0 1 1 0 0 - for the HT447P0
PH	0 0 1 0 0 1 0 1 - for the HT447K0
	0 0 0 1 0 0 1 0 1 - for the HT447P0
PI	1 0 0 1 0 1 0 0 1 - for the HT447P0 only

Description The data on port "Pi" is transferred to the accumulator. The zero flag is affected.

Operation ACC ← Pi; Pi=PD,PE,PF,PH - for the HT447K0
ACC ← Pi; Pi=PD,PE,PF,PH,PI -for the HT447P0

INC M Increment data memory

Machine code 1 1 0 0 0 0 0 1 - for the HT447K0

0 1 1 0 0 0 0 0 1 - for the HT447P0

Description Data in the data memory specified by the register pair "R1,R0" is incremented by one. The carry and zero flags are affected. Carry is set if the operation results in a carry out; otherwise the carry is cleared.

Operation M(R1,R0) ← M(R1,R0)+1

INC R0 Increment register R0

Machine code 1 1 0 1 0 0 0 1 - for the HT447K0

0 1 1 0 1 0 0 0 1 - for the HT447P0

Description Data in the working register "R0" is incremented by one. The zero flag is affected.

Operation R0 ← R0+1

JB A.i,address Jump if bit of the accumulator is set

Machine code 1 1 0 0 0 1 i1 i0 a a a a a a a a - for the HT447K0

0 1 1 0 0 0 1 i1 i0 0 a a a a a a a a - for the HT447P0

i0,i1 indicate which bit of the accumulator is detected. For example, that i0=i1=0 means that if bit 0 of the accumulator=1, the jump instruction will be executed.

Description If the indicated bit of the accumulator is set to 1, control passes to the specified address; otherwise it proceeds with the next instruction. Note that the branch destination is available only in the current page. (only bits 0~7 of the program counter will be replaced by the destination address.)

Operation PC ← address, if bit i of ACC=1
PC ← PC+2, if bit i of ACC=0

JB Pm.i,address Jump if bit of the I/O port is set

Machine code PE 1 1 0 0 1 1 i1 i0 a a a a a a a a - for the HT447K0

0 1 1 0 0 1 1 i1 i0 0 a a a a a a a a - for the HT447P0

i0,i1 indicate which bit of port PE is detected. For example, that i0=i1=0 means that if bit 0 of port Pm=1, the jump instruction will be executed.

Description If the indicated bit of port PE is set to 1, control passes to the specified address; otherwise it proceeds with the next instruction. Note that the branch destination is available only in the current page. (Only bits 0~7 of the program counter will be replaced by the destination address.)

Operation PC ← address, if bit i of Pm=1, Pm=PE
PC ← PC+2, if bit i of Pm=0, Pm=PE

JB M.i,address Jump if bit of the data memory is set

Machine code 1 1 1 0 0 1 i1 i0 a a a a a a a a - for the HT447K0

0 1 1 1 0 0 1 i1 i0 0 a a a a a a a a - for the HT447P0

i0,i1 indicate which bit of the data memory is detected. For example, that i0=i1=0 means that if bit 0 of the data memory is equal to 1, the jump instruction will be executed.

Description If the indicated bit of the data memory addressed by register pair "R1,R0" is set to 1, control passes to the specified address; otherwise it proceeds with the next instruction. Note that the branch destination is available only in the current page. (Only bits 0~7 of the program counter is replaced by the destination address.)

Operation PC ← address, if bit i of M(R1,R0)=1
PC ← PC+2, if bit i of M(R1,R0)=0

JC address Jump if the carry flag is set

Machine code 1 1 1 0 1 0 a a a a a a a a a - for the HT447K0

a 1 1 1 0 1 0 a a 0 a a a a a a a a - for the HT447P0

Description If the carry flag is set to one, control passes to the specified address; otherwise it proceeds with the next instruction.

Operation PC ← address, if CF=1
PC ← PC+2, CF=0

JMP address Direct jump

Machine code 1 1 1 1 1 1 a a a a a a a a a a - for the HT447K0

a 1 1 1 1 1 1 a a 0 a a a a a a a a a - for the HT447P0

Description All bits of the program counter are replaced with the directly specified address, and control passes to the destination.

Operation PC ← address

JNB A.i,address Jump if bit of the accumulator is not set.

Machine code 1 1 0 1 0 1 i1 i0 a a a a a a a a a - for the HT447K0

0 1 1 0 1 0 1 i1 i0 0 a a a a a a a a a - for the HT447P0

i0,i1 indicate which bit of the accumulator is detected. For example, that i0=i1=0 means that if bit 0 of the accumulator =0, the jump instruction will be executed.

Description If the indicated bit of the accumulator is reset to 0, control passes to the specified address; otherwise it proceeds with the next instruction. Note that the branch destination is available only in the current page. (Only bits 0~7 of program counter is replaced by the destination address.)

Operation PC ← address, if bit i of ACC=0
PC ← PC+2, if bit i of ACC=1

JNB M.i,address Jump if bit of the data memory is not set

Machine code 1 1 1 1 0 1 i1 i0 a a a a a a a a a - for the HT447K0

0 1 1 1 1 0 1 i1 i0 0 a a a a a a a a a - for the HT447P0

i0,i1 indicate which bit of the data memory is detected. For example, that i0=i1=0 means that if bit 0 of the data memory =0, the jump instruction will be executed.

Description If the indicated bit of the data memory addressed by register pair "R1,R0" is reset to 0, control passes to the specified address; otherwise it proceeds with the next instruction. Note that the branch destination is available only in the current page. (Only bits 0~7 of program counter is replaced by the destination address.)

Operation PC ← address, if bit i of M(R1,R0)=0
PC ← PC+2, if bit i of M(R1,R0)=1

JNC address Jump if the carry flag is not set

Machine code 1 1 1 1 1 0 a a a a a a a a a a - for the HT447K0

a 1 1 1 1 1 0 a a 0 a a a a a a a a a - for the HT447P0

Description If the carry flag is reset to zero, control passes to the specified address; otherwise it proceeds with the next instruction.

Operation PC ← address, if CF=0
PC ← PC+2, if CF=1

JNZ address Jump if the zero flag is not set

Machine code 1 1 0 1 1 0 a a a a a a a a a a - for the HT447K0

a 1 1 0 1 1 0 a a 0 a a a a a a a a a - for the HT447P0

Description If the zero flag is reset to zero, control passes to the specified address; otherwise it proceeds with the next instruction.

Operation PC ← address, if ZF=0
PC ← PC+2, if ZF=1

JZ address Jump if the zero flag is set

Machine code 1 1 0 0 1 0 a a a a a a a a a a - for the HT447K0

a 1 1 0 0 1 0 a a 0 a a a a a a a a a - for the HT447P0

Description If the zero flag is set to one, control passes to the specified address; otherwise it proceeds with the next instruction.

Operation PC ← address, if ZF=1
PC ← PC+2, if ZF=0

MOV A,M Move the data memory to the accumulator

Machine code 0 0 1 1 1 0 0 1 - for the HT447K0

0 0 0 1 1 1 0 0 1 - for the HT447P0

Description The content of the data memory addressed by the register pair "R1,R0" is moved to the accumulator. If the contents of the data memory is zero, the zero flag will be set.

Operation ACC ← M(R1,R0)

MOV A,R0 Move the register R0 content to the accumulator

Machine code 0 0 0 0 0 1 0 1 - for the HT447K0

0 0 0 0 0 0 1 0 1 - for the HT447P0

Description The content of register R0 is moved into the accumulator. If the content of register R0 is zero, the zero flag will be set.

Operation ACC ← R0

MOV A,R1 Move the register R1 content to the accumulator

Machine code 0 0 0 0 0 1 1 0 - for the HT447K0

0 0 0 0 0 0 1 1 0 - for the HT447P0

Description The content of register R1 is moved into the bit 0 and 1 of the accumulator. The bit 2 and 3 of the accumulator are reset to 0 for the HT447P0, but for HT447K0 the bit 1 of the accumulator is also reset to 0. If the content of register R1 is zero, the zero flag will be set.

Operation ACC ← R1

MOV A,XH Move the immediate data to the accumulator

Machine code 0 1 1 0 d d d d - for the HT447K0

0 0 1 1 0 d d d d - for the HT447P0

Description The 4-bit data specified by code is loaded in the accumulator. No flags are affected.

Operation ACC ← XH

MOV A,[XXH] Move the data memory to the accumulator directly

Machine code 1 0 0 m4 m3 m2 m1 m0 - for the HT447K0

m5 1 0 0 m4 m3 m2 m1 m0 - for the HT447P0

m4~m0: address of data memory for the HT447K0

m5~m0: address of data memory for the HT447P0

Description The content of the data memory directly addressed by code is moved to the accumulator. The zero flag is affected. If the content of the data memory is zero, the zero flag will be set.

Operation ACC ← M(m4~m0) for the HT447K0
ACC ← M(m5~m0) for the HT447P0

MOV M,A Move the accumulator to the data memory

Machine code 0 0 1 1 1 0 1 0 - for the HT447K0

0 0 0 1 1 1 0 1 0 - for the HT447P0

Description The content of the accumulator is moved to the data memory addressed by register pair "R1,R0".

Operation M(R1,R0) ← ACC

MOV R0,A Move the accumulator to the register R0

Machine code 0 0 0 1 0 1 0 1 - for the HT447K0

0 0 0 0 1 0 1 0 1 - for the HT447P0

Description The content of the accumulator is moved into the register "R0".

Operation R0 ← ACC

MOV R1,A Move the accumulator to the register R1

Machine code 0 0 0 1 0 1 1 0 - for the HT447K0

0 0 0 0 1 0 1 1 0 - for the HT447P0

Description The bit 0 and 1 of the accumulator are moved into the register "R1" for the HT447P0, but for the HT447K0 only the bit 0 of the accumulator is moved into the register "R1".

Operation R1 ← ACC

MOV R0,M Move the data memory to register R0

Machine code 0 0 1 0 0 1 1 0 - for the HT447K0

0 0 0 1 0 0 1 1 0 - for the HT447P0

Description The content of the data memory addressed by the register pair "R1,R0" is moved to the register "R0".

Operation R0 ← M(R1,R0)

MOV R1R0,XXH Move the immediate data to register R0 and R1

Machine code 0 1 0 d d d d d - for the HT447K0

d 0 1 0 d d d d d - for the HT447P0

Description The 6-bit data specified by code is loaded in the register pair "R1,R0" for the HT447P0, but for the HT447K0 only 5-bit data are specified by code. No flags are affected.

Operation R1 ← XH (high nibble)
R0 ← XH (low nibble)

MOV [XXH],A Move the accumulator to the data memory directly

Machine code 1 0 1 m4 m3 m2 m1 m0 - for the HT447K0

m5 1 0 1 m4 m3 m2 m1 m0 - for the HT447P0

m4~m0:address of the data memory for the HT447K0

m5~m0:address of the data memory for the HT447P0

Description The content of the accumulator is directly moved to the data memory addressed by code. No flags are affected.

Operation M (m4~m0) ← ACC for the HT447K0
M (m5~m0) ← ACC for the HT447P0

NOP No operation

Machine code 1 1 1 1 0 0 0 0 - for the HT447K0

0 1 1 1 1 0 0 0 0 - for the HT447P0

Description No operation is performed. Execution continues with the next instruction.

Operation PC ← PC+1

OR A,M Logical OR data memory to the accumulator

Machine code 0 0 1 0 0 0 1 1 - for the HT447K0

0 0 0 1 0 0 0 1 1 - for the HT447P0

Description Data in the accumulator is logically ORed with the data memory addressed by register pair "R1,R0". The result is stored in the accumulator. The zero flag is affected.

Operation ACC ← ACC "OR" M(R1,R0)

OR A,XH Logical OR accumulator with the immediate data

Machine code 0 0 0 0 0 0 1 1 0 0 0 1 d d d d - for the HT447K0

0 0 0 0 0 0 0 1 1 0 0 0 1 d d d d - for the HT447P0

Description Data in the accumulator is logically ORed with the immediate data. The result is stored in the accumulator and the zero flag is affected.

Operation ACC ← ACC "OR" XH

OR M,A Logical OR accumulator to the data memory

Machine code 1 1 0 1 0 0 0 0 - for the HT447K0

0 1 1 0 1 0 0 0 0 - for the HT447P0

Description Data in the accumulator is logically ORed with the data memory addressed by register pair "R1,R0". The result is stored in the data memory. The zero flag is affected.

Operation M(R1,R0) ← ACC "OR" M(R1,R0)

OUT PA,A Output the accumulator data to port A

Machine code 0 0 1 1 1 1 0 0 - for the HT447K0

0 0 0 1 1 1 1 0 0 - for the HT447P0

Description The bit 0 of the accumulator is transferred to the output port PA0 for no carrier option. If carrier output option is selected, writing "0" to the PA0 will result in a carrier output, and writing "1" to the PA0 will keep the state of PA0 at normal low level.

Operation PA0 ← ACC0 (no carrier option).
ACC=0, PA0: carrier (carrier output option).
ACC=1, PA0: 0 (carrier output option).

OUT Po,A Output the accumulator data to the port

Machine code
PD 0 0 1 0 1 0 1 0 - for the HT447K0
0 0 0 1 0 1 0 1 0 - for the HT447P0
PE 0 0 0 0 1 0 1 0 - for the HT447K0
0 0 0 0 0 1 0 1 0 - for the HT447P0
PH 0 0 1 1 0 1 1 0 - for the HT447K0
0 0 0 1 1 0 1 1 0 - for the HT447P0
PI 1 0 0 1 0 1 0 1 0 - for the HT447P0 only

Description The data on the accumulator is transferred to the "Po" port.

Operation
Po ← ACC; Po=PD,PE,PH - for the HT447K0
Po ← ACC; Po=PD,PE,PH,PI - for the HT447P0

READn MA Read the ROM code to the data memory and accumulator

Machine code
1 1 1 0 1 1 n n - for the HT447K0
n 1 1 1 0 1 1 n n - for the HT447P0
nn: page number (0~3) for the HT447K0
nnn: page number (0~7) for the HT447P0

Description The 8 bits of the ROM code addressed by ACC and M(R1,R0) in page n are moved to the data memory addressed by register pair "R1,R0" and the accumulator. The high nibble of the ROM code is loaded to the data memory and the low nibble of the ROM code is loaded to the accumulator. If the ACC is zero, and the zero flag will be set. The address of the ROM code are specified by the following description:

ROM code address bit 9~8 ← Page "nn" for the HT447K0
ROM code address bit 7~4 ← ACC
ROM code address bit 3~0 ← M(R1,R0)

ROM code address bit 10~8 ← Page "nnn" for the HT447P0
ROM code address bit 7~4 ← ACC
ROM code address bit 3~0 ← M(R1,R0)

Operation
M(R1,R0) ← ROM code (high nibble)
ACC ← ROM code (low nibble)

RLC A Rotate the accumulator left through the carry

Machine Code 1 1 1 1 0 0 1 1 - for the HT447K0

0 1 1 1 1 0 0 1 1 - for the HT447P0

Description The contents of the accumulator are rotated left one bit. Bit 3 replaces the carry bit; the carry bit is rotated to the bit 0 position.

Operation An+1 ← An; An: Accumulator bit n (n=0,1,2)
A0 ← CF
CF ← A3

RRC A Rotate the accumulator right through the carry

Machine Code 1 1 1 1 0 0 1 0 - for the HT447K0

0 1 1 1 1 0 0 1 0 - for the HT447P0

Description The contents of the accumulator are rotated right one bit. Bit 0 replaces the carry bit; the carry bit is rotated to the bit 3 position.

Operation An ← An+1; An: Accumulator bit n (n=0,1,2)
A3 ← CF
CF ← A0

SET C Set carry flag

Machine code 1 1 1 0 0 0 1 1 - for the HT447K0

0 1 1 1 0 0 0 1 1 - for the HT447P0

Description The carry flag is set to one.

Operation CF ← 1

SET M.i Set bit of the data memory

Machine code 0 0 1 1 i3 i2 i1 i0 - for the HT447K0

0 0 0 1 1 i3 i2 i1 i0 - for the HT447P0

i0~i3 are determined by operand i. The corresponding bit will be "1" if the bit i of the memory is set to 1. For example, if i=0 then i3~i0=0001.

Description The bit of memory addressed by "R1,R0" is set to one.

Operation M(R1,R0).i ← 1

SET Pn.i Set bit of the I/O port

Machine code
PD 0 0 1 0 i3 i2 i1 i0 - for the HT447K0
0 0 0 1 0 i3 i2 i1 i0 - for the HT447P0
PE 0 0 0 0 i3 i2 i1 i0 - for the HT447K0
0 0 0 0 0 i3 i2 i1 i0 - for the HT447P0
PI 1 0 0 1 0 i3 i2 i1 i0 - for the HT447P0 only

i0~i3 are determined by operand i. The correponding bit will be "1" if i is set. For example, if i=0 then i3~i0=0001

Description The specified bit i of port "Pn" is set to one. For the HT447K0 Pn may be PD,PE. But for the HT447P0 Pn represents PD,PE,PI.

Operation
Pn.i ← 1; Pn=PD,PE for the HT447K0
Pn.i ← 1; Pn=PD,PE,PI for the HT447P0

TRI Po,A Output the accumulator to the tri-state latch

Machine code
PD 0 0 0 0 1 1 0 0 - for the HT447K0
0 0 0 0 0 1 1 0 0 - for the HT447P0
PE 0 0 0 1 1 1 0 0 - for the HT447K0
0 0 0 0 1 1 1 0 0 - for the HT447P0
PH 0 0 1 0 1 1 1 1 - for the HT447K0
0 0 0 1 0 1 1 1 1 - for the HT447P0
PI 1 0 0 0 0 1 1 0 0 - for the HT447P0 only

Description Data in the accumulator is transferred to the tri–state latch of port "Po". The "1" written to the tri-state latch makes the corresponding output part become floating. Writing "0" to the tri-state latch will force the related I/O bit to operate in output mode.

Operation
Po ← ACC ; Po=PD,PE,PH for the HT447K0
Po ← ACC ; Po=PD,PE,PH,PI for the HT447P0

XOR A,M Logical Exclusive-OR data memory to the accumulator

Machine code 0 0 1 1 0 0 1 1 - for the HT447K0

0 0 0 1 1 0 0 1 1 - for the HT447P0

Description Data in the accumulator is Exclusive-ORed with the data memory addressed by register pair "R1,R0". The result is stored in the accumulator. The zero flag is affected.

Operation ACC ← ACC "XOR" M(R1,R0)

XOR A,XH Logical Exclusive-OR accumulator with the immediate data

Machine code 0 0 0 0 0 0 1 1 0 0 1 1 d d d d - for the HT447K0

0 0 0 0 0 0 0 1 1 0 0 0 1 1 d d d d - for the HT447P0

Description Data in the accumulator is Exclusive-ORed with the immediate data specified by code. The result is stored in the accumulator. The zero flag is affected.

Operation ACC ← ACC "XOR" XH

XOR M,A Logical Exclusive-OR accumulator to the data memory

Machine code 1 1 1 0 0 0 0 0 - for the HT447K0

0 1 1 1 0 0 0 0 0 - for the HT447P0

Description Data in the accumulator is Exclusive-ORed with the data memory addressed by register pair "R1,R0". The result is stored in the data memory. The zero flag is affected.

Operation M(R1,R0) ← ACC "XOR" M(R1,R0)