

FEATURES

- v Avalanche Rugged Technology
- v Rugged Gate Oxide Technology
- v Lower Input Capacitance
- v Improved Gate Charge
- v Extended Safe Operating Area
- v Lower Leakage Current : 10 μ A (Max.) @ $V_{DS} = -250V$
- v Lower $R_{DS(ON)}$: 3.15 Ω (Typ.)

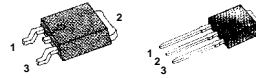
$$BV_{DSS} = -250 V$$

$$R_{DS(on)} = 4.0 \Omega$$

$$I_D = -1.53 A$$

D-PAK

I-PAK



1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	-250	V
I_D	Continuous Drain Current ($T_C=25^\circ C$)	-1.53	A
	Continuous Drain Current ($T_C=100^\circ C$)	-0.97	
I_{DM}	Drain Current-Pulsed ①	-6.1	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy ②	110	mJ
I_{AR}	Avalanche Current ①	-1.53	A
E_{AR}	Repetitive Avalanche Energy ①	1.9	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-4.8	V/ns
P_D	Total Power Dissipation ($T_A=25^\circ C$) *	2.5	W
	Total Power Dissipation ($T_C=25^\circ C$)	19	W
	Linear Derating Factor	0.15	W/ $^\circ C$
T_J, T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8 " from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	6.58	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient *	--	50	
$R_{\theta JA}$	Junction-to-Ambient	--	110	

* When mounted on the minimum pad size recommended (PCB Mount).

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Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV _{DSS}	Drain-Source Breakdown Voltage	-250	--	--	V	V _{GS} =0V, I _D =-250μA
ΔBV/ΔT _J	Breakdown Voltage Temp. Coeff.	--	-0.21	--	V/°C	I _D =-250μA See Fig 7
V _{GS(th)}	Gate Threshold Voltage	-2.0	--	-4.0	V	V _{DS} =-5V, I _D =-250μA
I _{GSS}	Gate-Source Leakage , Forward	--	--	-100	nA	V _{GS} =-30V
	Gate-Source Leakage , Reverse	--	--	100		V _{GS} =30V
I _{DSS}	Drain-to-Source Leakage Current	--	--	-10	μA	V _{DS} =-250V
		--	--	-100		V _{DS} =-200V, T _C =125°C
R _{DS(on)}	Static Drain-Source On-State Resistance	--	--	4.0	Ω	V _{GS} =-10V, I _D =-0.77A ④
g _{fs}	Forward Transconductance	--	1.0	--	S	V _{DS} =-40V, I _D =-0.77A ④
C _{iss}	Input Capacitance	--	225	295	pF	V _{GS} =0V, V _{DS} =-25V, f=1MHz See Fig 5
C _{oss}	Output Capacitance	--	35	55		
C _{rss}	Reverse Transfer Capacitance	--	13	20		
t _{d(on)}	Turn-On Delay Time	--	10	30	ns	V _{DD} =-125V, I _D =-1.6A, R _G =24Ω See Fig 13 ④ ⑤
t _r	Rise Time	--	18	45		
t _{d(off)}	Turn-Off Delay Time	--	24	60		
t _f	Fall Time	--	11	30		
Q _g	Total Gate Charge	--	9	11	nC	V _{DS} =-200V, V _{GS} =-10V, I _D =-1.6A See Fig 6 & Fig 12 ④ ⑤
Q _{gs}	Gate-Source Charge	--	2.0	--		
Q _{gd}	Gate-Drain("Miller ") Charge	--	4.6	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I _S	Continuous Source Current	--	--	-1.53	A	Integral reverse pn-diode in the MOSFET
I _{SM}	Pulsed-Source Current ①	--	--	-6.1		
V _{SD}	Diode Forward Voltage ④	--	--	-4.0	V	T _J =25°C, I _S =-1.53A, V _{GS} =0V
t _{rr}	Reverse Recovery Time	--	130	--	ns	T _J =25°C, I _F =-1.6A
Q _{rr}	Reverse Recovery Charge	--	0.61	--	μC	di _F /dt=100A/μs ④

Notes ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② L=75mH, I_{AS}=-1.53A, V_{DD}=-50V, R_G=27Ω*, Starting T_J=25°C
- ③ I_{SD} ≤ 1.6A, di/dt ≤ 250A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J=25°C
- ④ Pulse Test : Pulse Width = 250μs, Duty Cycle ≤ 2%
- ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

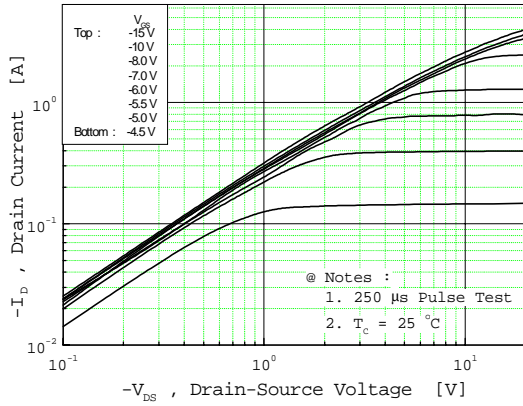


Fig 2. Transfer Characteristics

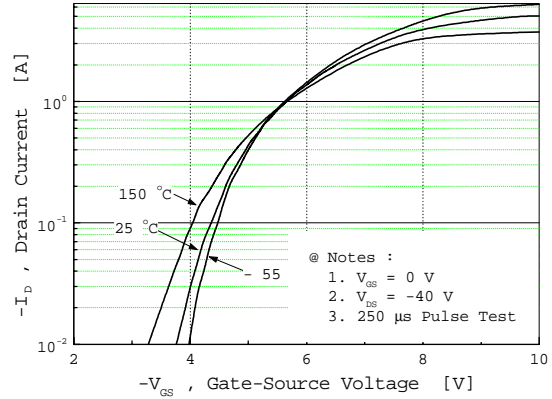


Fig 3. On-Resistance vs. Drain Current

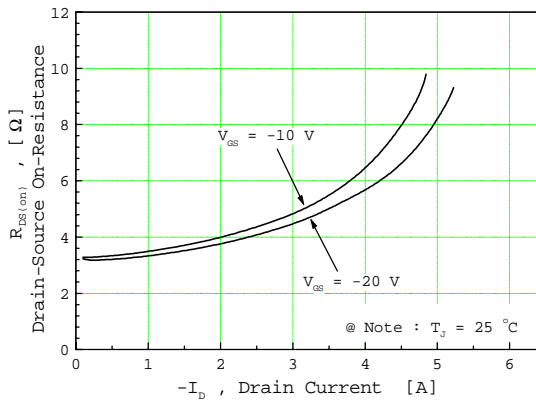


Fig 4. Source-Drain Diode Forward Voltage

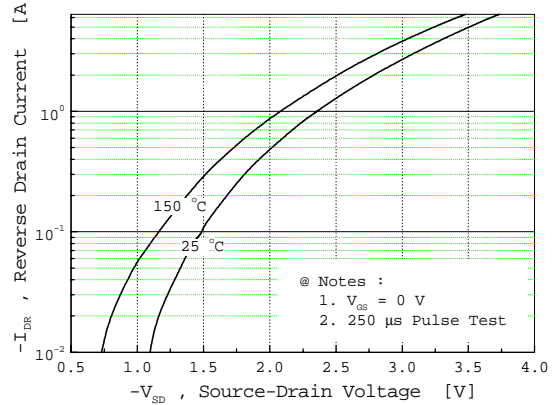


Fig 5. Capacitance vs. Drain-Source Voltage

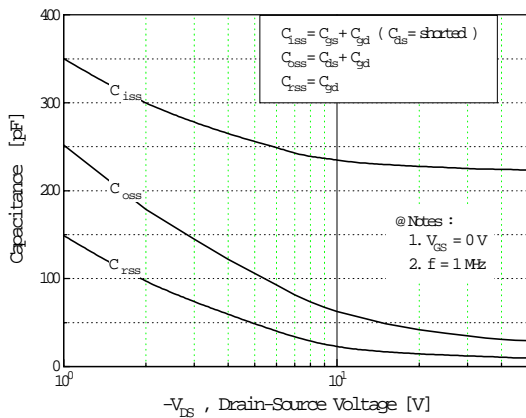


Fig 6. Gate Charge vs. Gate-Source Voltage

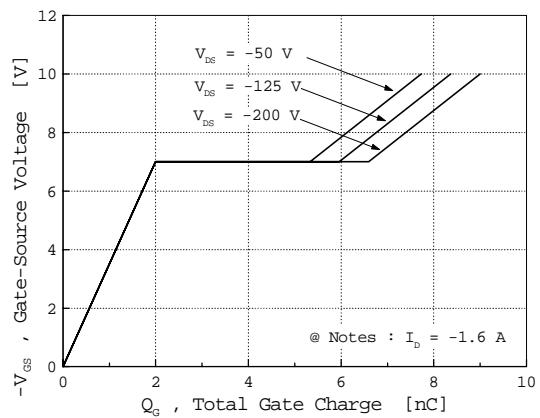


Fig 7. Breakdown Voltage vs. Temperature

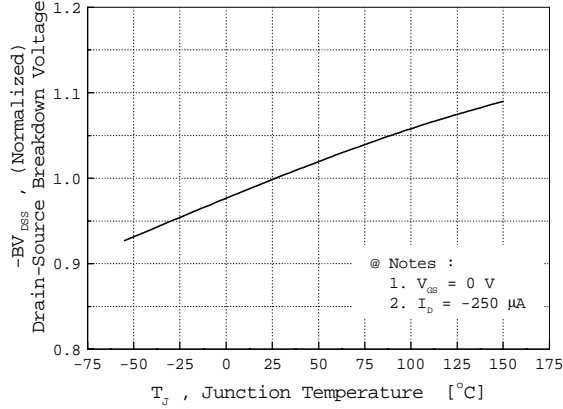


Fig 8. On-Resistance vs. Temperature

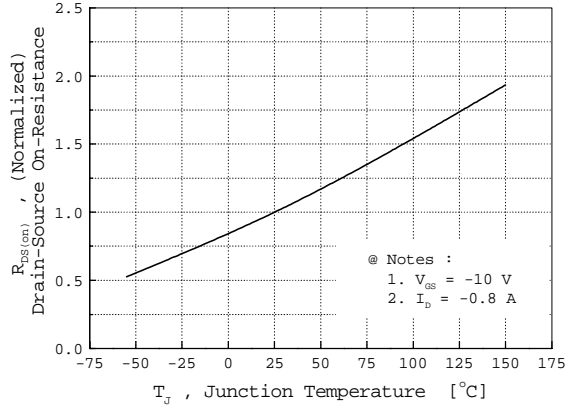


Fig 9. Max. Safe Operating Area

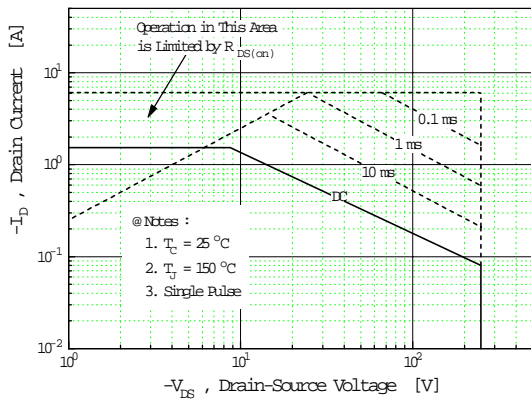


Fig 10. Max. Drain Current vs. Case Temperature

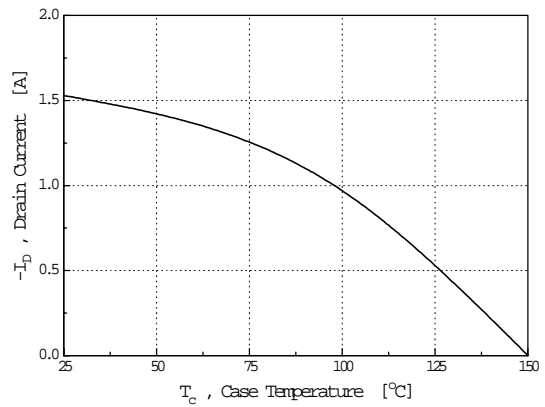


Fig 11. Thermal Response

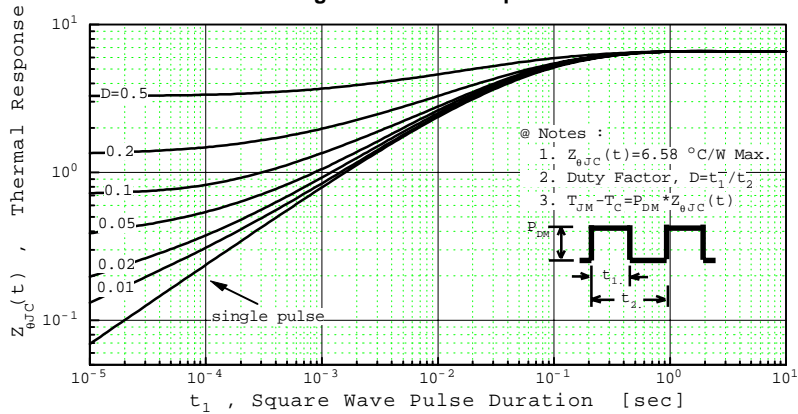


Fig 12. Gate Charge Test Circuit & Waveform

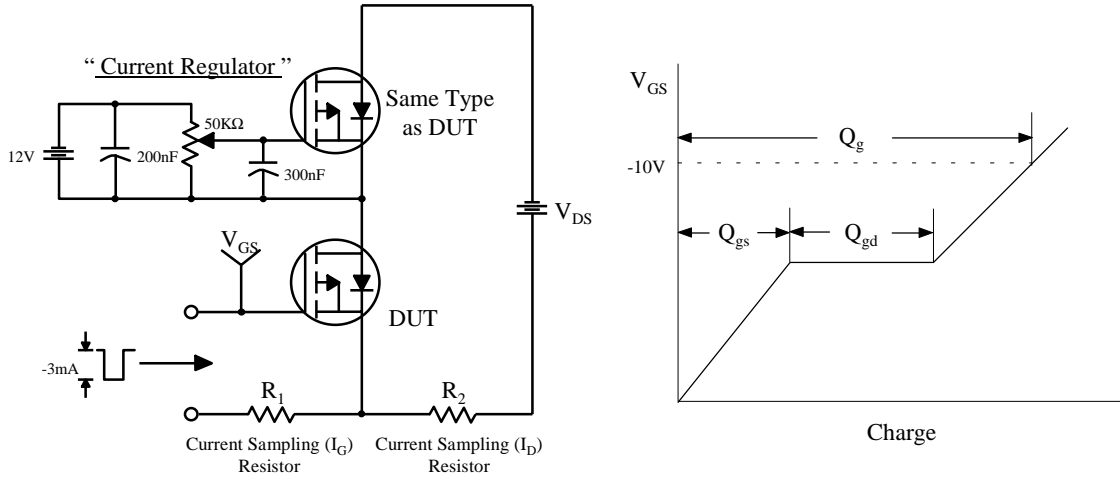


Fig 13. Resistive Switching Test Circuit & Waveforms

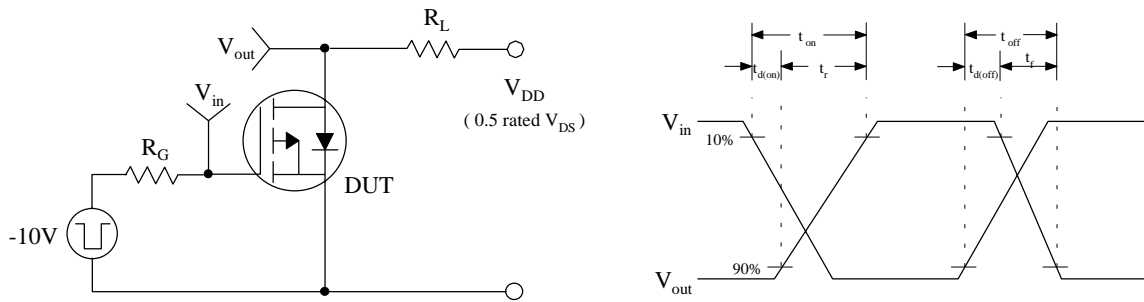


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

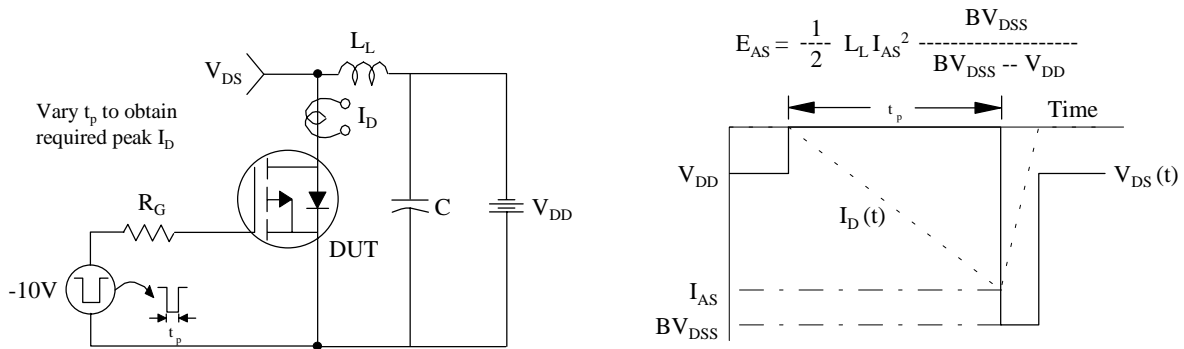
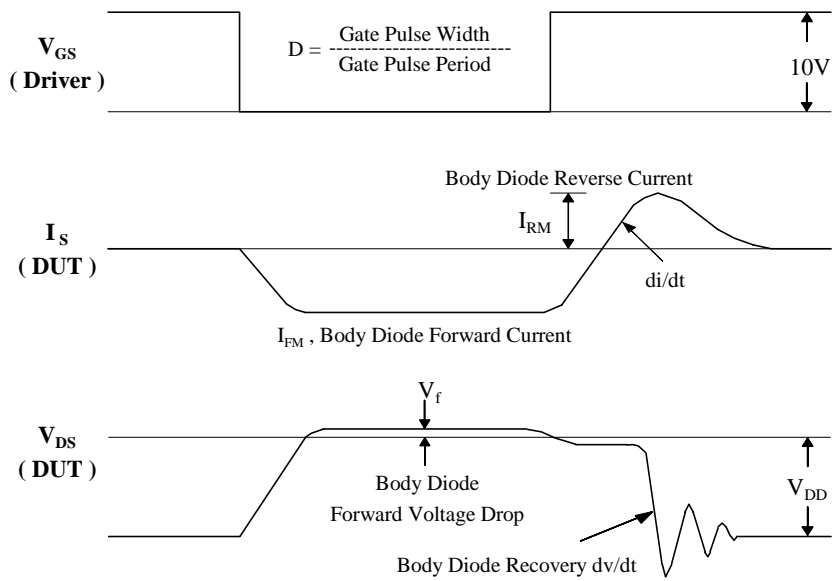
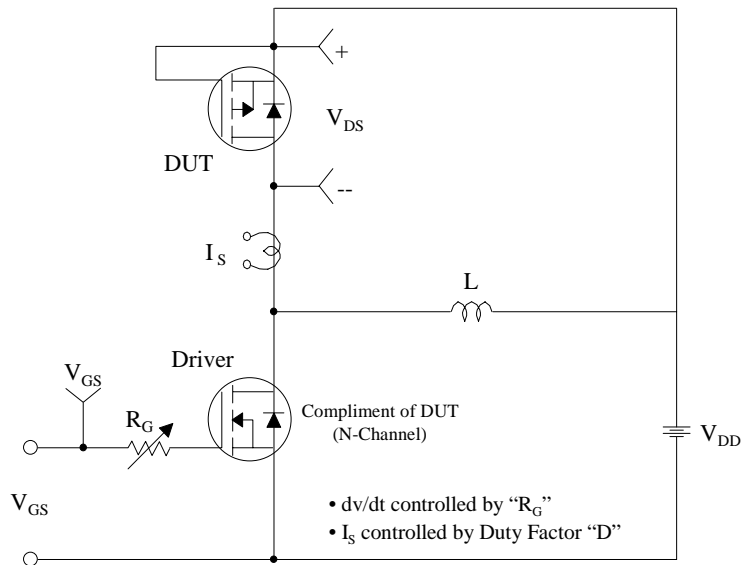


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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