DESCRIPTION

The M58990P,-1 is used to convert analog signals to 8-bit digital values.

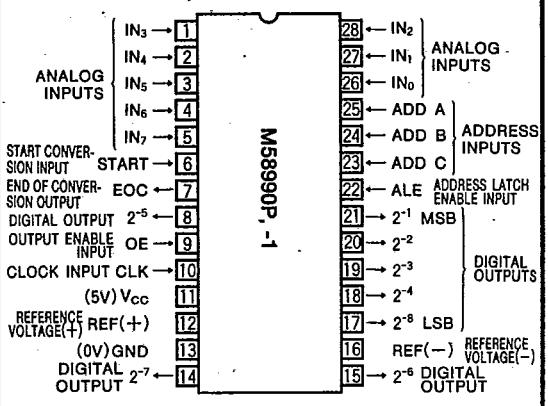
The M58990P,-1 is fabricated using silicon-gate CMOS technology. The M58990P,-1 can select multiplex 8 channels of analog input.

FEATURES

Type No.	Linearity error (Max) (LSB)	Absolute accuracy (Max) (LSB)
M58990P	±½	±1
M58990P-1	±1	±1½

- Single 5V supply voltage
- TTL compatible
- Conversion resolution of 8 bits
- Multiplex 8 channels of analog input
- Broad range of analog input voltages: 0V~V_{CC}
- Conversion time: 60μs
- Conversion by successive approximation
- Can be used online through the data bus of a microprocessor

PIN CONFIGURATION (TOP VIEW)



Outline 28P4

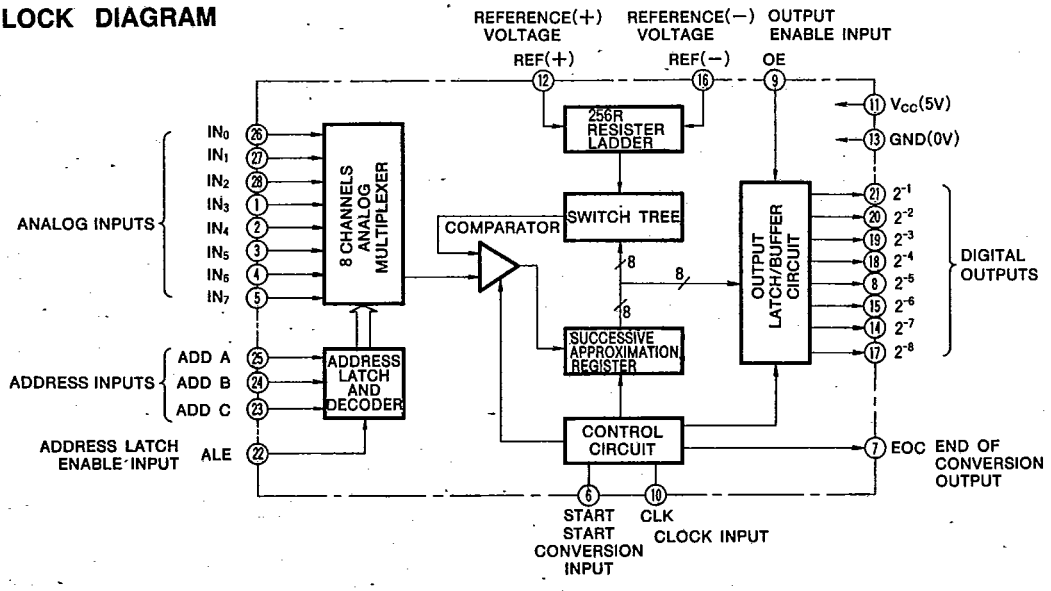
APPLICATION

Used with microcomputers to control analog systems

FUNCTION

The M58990P,-1 has eight analog input terminals that are selected by the input signals to the 3 address terminals (ADD A~ADD C). The address signals of these terminals are read and latched in the internal address latches by the ALE signal. When the OE terminal is at low-level, the output terminals 2^{-1}~2^{-8} are in a floating state so they can be connected directly to the data bus of a microcomputer. The input terminal START is used to call for the start of an analog to digital conversion and a signal is output through terminal EOC when the conversion is completed.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin	Name	Input or Output	Functions
IN_0 ∫ IN_7	Analog signal	Input	These are analog signal input pins. Which of the 8 inputs is selected, is determined by ADD A~ADD C. An analog voltage applied at the selected pin is converted to a digital value in the range of 2^{-1}~ 2^{-8} and output.
ADD A ∫ ADD C	Address signal	Input	The input is used for selecting which of the 8 terminals IN_0~IN_7 is to be converted from analog to digital. The address input through ADD A~ADD C is read to the address latch by the rising edge of ALE.
ALE	Address latch enable signal	Input	This is the strobe signal which causes the address signal input through ADD A~ADD C to be read and latched for use as an internal address.
REF(+)	Reference voltage(+)	Input	This is one of the input terminals for the réference voltage that is applied to the 256R resistor ladder circuit. The other terminal is REF(−) and the voltage levels of these two inputs must meet the condition: REF(+) >REF(−).
REF(−)	Reference voltage(−)	Input	This is one of the input terminals for the reference voltage that is applied to the 256R resistor ladder circuit. The other terminal is REF(+) and the voltage levels of these two inputs must meet the condition: REF(+) >REF(−).
OE	Output enable signal	Input	The signal at this pin controls the digital output. When the signal is low-level, pins 2^{-1}~ 2^{-8} are in a floating state. When it is high-level , the data is output.
2^{-1} ∫ 2^{-8}	Digital signal	Output	The analog signal, which was input through IN_0~IN_7, is converted to digital data and is output from these terminals. When OE is low-level, these terminals are floating. When OE is high-level, the converted digital data is output. The MSB is 2^{-1} and the LSB is 2^{-8}.
EOC	End of conversion signal	Output	This terminals is used to indicate the completion of an analog to digital conversion. It is reset by a START signal (high-level to low-level) and is set on completion of the conversion (low-level to high-level). This output is normally used to generate an interrupt request for the CPU.
START	Start conversion signal	Input	The input signal at this terminal is used to start a conversion cycle by setting the successive approximation register. The successive approximation register is reset by rising from low-level to high-level and conversion is started after being set by falling from high-level to low-level.
CLK	Clock input	Input	The signal at this terminal is the basic clocking signal used to determine internal timing.

BASIC FUNCTION BLOCKS

8-channel Multiplexer

The M58990P,-1 has eight input pins ($IN_0 \sim IN_7$) used for entering analog signals. When analog signals are present at $IN_0 \sim IN_7$, the 8-channel multiplexer selects one of those signals and converts it into a digital signal.

The address decoder contains an input latch circuit which functions to hold the input signal present at pins ADD A~ ADD C. This circuit is illustrated in Fig. 1, while timing of the address latch is shown in Fig. 2.

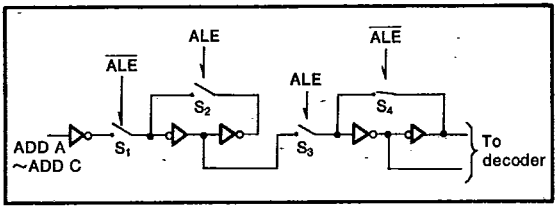


Fig.1 Address latch circuit

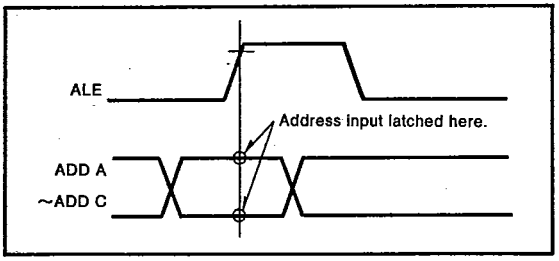


Fig.2 Address latch timing

When the ALE signal is "L", S_1 and S_4 (Fig. 1) are closed, and S_2 and S_3 are open. At this time, external input is inhibited at S_3, and the previous data is sent to the decoder. When ALE transits from "L" to "H", S_1 and S_4 open, and S_2 and S_3 close. This simultaneously latches the address data, and enables output to the decoder. At this point, the new data arriving at ADD A~ADD C is blocked at S_1. Subsequent transition of ALE from "H" to "L" does not produce a change; the latched data remains held.

The method for determining selection of the analog input at $IN_0 \sim IN_7$ is by reading the value of the latched address signal. Value allocations are shown in Table 1.

Table 1 Address signals as related to selected analog signal pin

ADD C	ADD B	ADD A	Analog input
0	0	0	IN_0
0	0	1	IN_1
0	1	0	IN_2
0	1	1	IN_3
1	0	0	IN_4
1	0	1	IN_5
1	1	0	IN_6
1	1	1	IN_7

256R Ladder Network And Switch Tree

Fig. 3 shows the 256R resistor ladder and switch tree circuit. The 256R ladder network is created in the diffusion process by forming 256 individual resistors into the substrate. 254 of these resistors have the same value R, while the resistor on each end of the ladder carries the value 3/2R and 1/2R respectively. The reference voltage source is applied to both ends of the ladder, and the reference voltage used to compare analog input voltages is output at each of the steps.

The reason for using different resistance values on the ends of the ladder network is illustrated in Fig. 9 (a) showing the I/O characteristics of the A-D converter. The different resistance values provide symmetry between the zero point and full scale point in the output characteristics transfer curve. As noted in this diagram, the width of the horizontal axis of each step is determined by the potential difference created by each ladder resistor. The step widths for the zero and full scale points are respectively 1/2 and

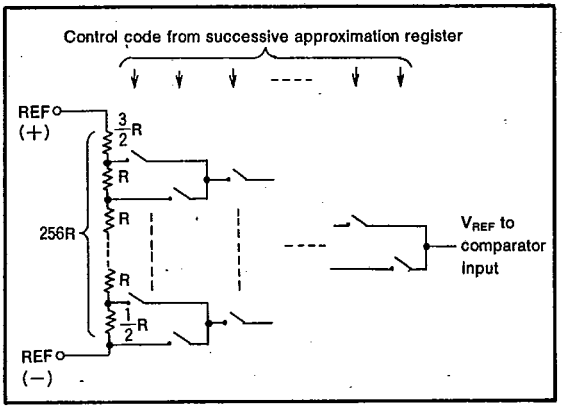


Fig.3 256R ladder network and switch tree

3/2-times that of the intermediate steps.

The switch tree is an analog switch network made up of 510 MOSFETs, and is used to output the ladder step voltage selected by successive approximation register (S.A.R.) code to the comparator. The output voltage obtained from the 256R ladder and switch tree is increased or decreased in accordance with the S. A. R. code, with the monotonicity of the 256R ladder.

Comparator

The comparator used in M58990P,-1 has a chopper type amplifier used to minimize input offset voltage and drift. This circuit is illustrated in Fig. 4. Fig. 6 shows the operational timing of the comparator.

At the start of the comparing cycle, S_0 and S_1 close on the positive edge of ϕ_0 and ϕ_1. Analog input voltage V_{IN} is then sent to the comparator. At the same time, the input of the AC amplifier is biased at point A shown in the I/O characteristics curve of Fig. 6.

When S_0 and S_1 open, S_2 closes on the positive edge of ϕ_2, and the difference voltage ΔV derived from comparing analog input voltage V_{IN} and reference voltage V_{REF} from the ladder appears at AC amplifier input. Amplification of this difference voltage causes a voltage saturated at "H" or "L" level to appear at output. (This is shown as point B or C in Fig. 5.)

Offset and drift are blocked by the AC amplifier. The comparator results are stored in the successive approximation register at the end of the comparing cycle.

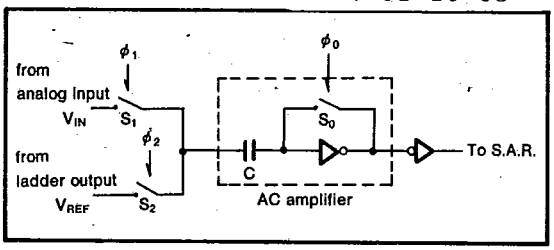


Fig.4 Comparator

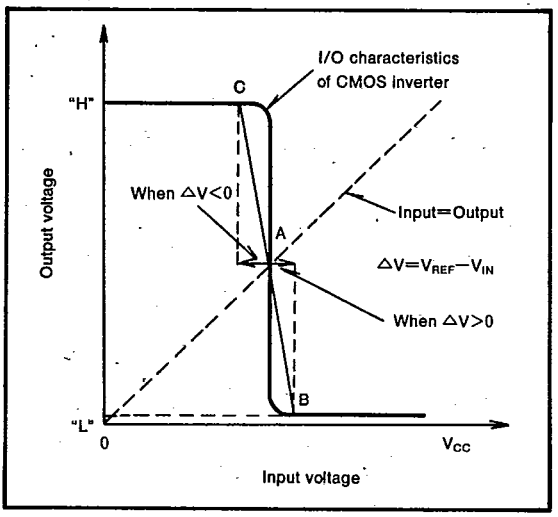


Fig.5 AC amplifier I/O characteristics

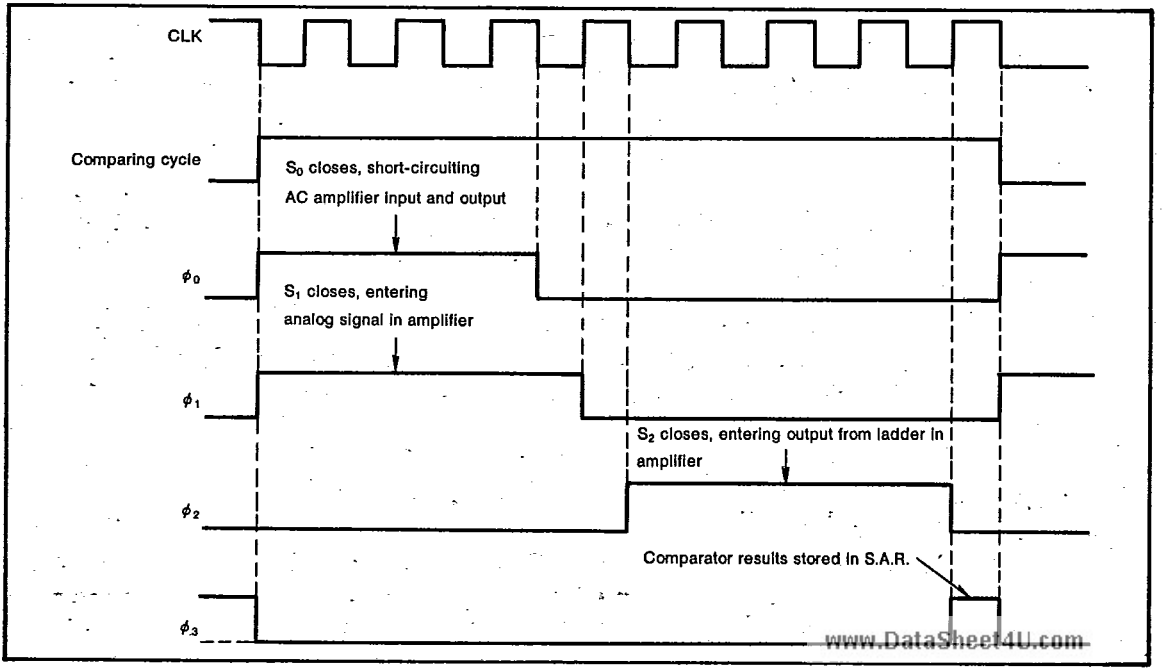


Fig.6 Comparing cycle timing

Successive Approximation Register (S.A.R.)

The S.A.R. takes the results from the comparator and converts them to an 8-bit binary code for use in determining the reference voltage value that should be used in the next input comparison. The relationship between reference voltage V_{REF} and the binary code is as follows:

$$V_{REF} = (2^7C_7+2^6C_6+\cdots 2^0C_0) \times \frac{V_{FSR}}{256} + REF(-) - \frac{V_{FSR}}{512} \cdots\cdots (1)$$

Where $C_7+C_6+\cdots+C_0 \neq 0$.

When $C_7=C_6=\cdots=C_0=0$, $V_{REF}=REF(-)$

Here, V_{FSR} stands for full scale range of analog voltage, which indicates the range between minimum and maximum value, or $V_{FSR}=REF(+)-REF(-)\cdots(2)$

C_7, $C_6 \cdots C_0$ are each represented by a 0 or 1 digit in the binary code, with C_7 the MSB and C_0 the LSB. Consequently, from equation (1), we have:

$$V_{REF} = (\frac{1}{2}C_1+\frac{1}{2^2}C_6+\cdots+\frac{1}{2^8}C_0) \times V_{FSR} + REF(-) - \frac{V_{FSR}}{512} \cdots\cdots (3)$$

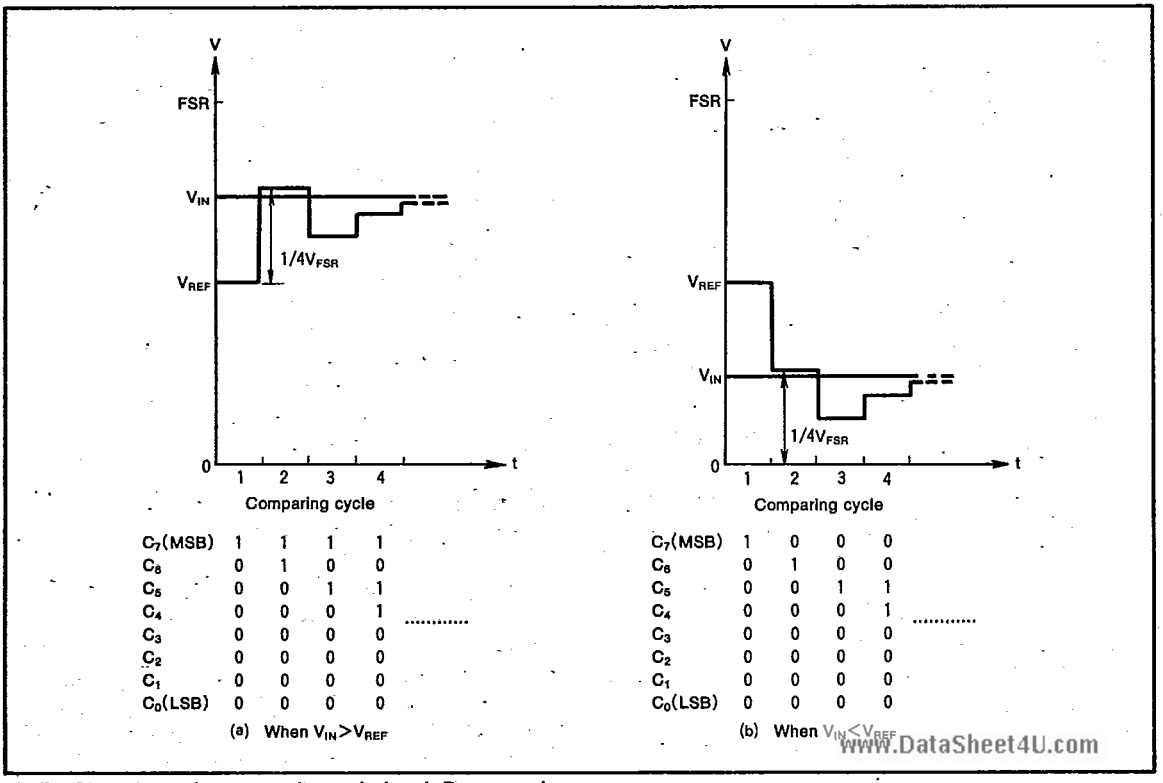
When each digit (bit) in the right half of equation (3) is weighted from 1/2 to $1/2^8$, the value relative to full scale can be obtained. With the successive comparator method, successive approximations are made from MSB to LSB until reference voltage V_{REF} is as close to V_{IN} as it can get. The following explanation provides more specifics.

When the start pulse entered at the START pin transitions from "L" to "H", the S.A.R. sets only the MSB "1", the other bits being reset to "0". As a result, the voltage selected for reference voltage V_{REF} is approximately one-half of V_{FSR}, and this is used to compare with analog input V_{IN}.

The conversion is started when the start pulse transition from "H" to "L", and the first comparing cycle is entered. At this time, should V_{IN} be smaller than V_{REF}, MSB will be reset to "0". If larger, the MSB will remain "1" and the next comparing cycle will be entered. For this cycle, the bit next to MSB, C_6 will be set, and the previous results will be carried up. In other words, taking the next selected reference voltage as V_{REF}', when

$V_{IN}>V_{REF}$, then:

$$V_{REF}' = (\frac{1}{2}+\frac{1}{4}) V_{FSR} - \frac{V_{FSR}}{512} + REF(-)$$



C_7(MSB)	1	1	1	1
C_6	0	1	0	0
C_5	0	0	1	1
C_4	0	0	0	1
C_3	0	0	0	0
C_2	0	0	0	0
C_1	0	0	0	0
C_0(LSB)	0	0	0	0

(a) When $V_{IN}>V_{REF}$

C_7(MSB)	1	0	0	0
C_6	0	1	0	0
C_5	0	0	1	1
C_4	0	0	0	1
C_3	0	0	0	0
C_2	0	0	0	0
C_1	0	0	0	0
C_0(LSB)	0	0	0	0

(b) When $V_{IN}<V_{REF}$

Fig.7 Changing reference voltage during A-D conversion

And when $V_{IN} < V_{REF}$,

$$V_{REF}' = \frac{1}{4}V_{FSR} = \frac{V_{FSR}}{512}\,REF\,(-)$$

In the second comparing cycle, V_{IN} is compared with V_{REF}', and the results for C_6 are obtained. From there, the comparator cycles are repeated until the value for C_0 is obtained. This process is illustrated in Fig. 7.

There are eight comparing cycles for each conversion cycle, and one comparing cycle requires eight clocks. This means that each conversion cycle requires 64 clocks, and since clock frequency is 640kHz, each conversion cycle requires 100μs. (Note 1)

When the comparison has been made, results are latched in the output circuit, and the EOC signal is sent. The EOC signal is reset to "L" by the start pulse, then set "H" when the conversion is completed.

The EOC signal has interrupt capability with regards to the CPU, and can be tied to the start pulse for continuous conversion.

If a new start signal is entered during conversion, the S.A.R. is reset and starts over from that point.

Note 1 : Conversion time t_C, a characteristics value that will be convered later, is defined as the time between the positive edge of the start pulse and the positive eage of EOC. Consequently, t_C is a combination value of conversion cycle time, EOC delay time (1 to 8 clocks), and latch cycle time applied to the output circuit (1 clock).

EOC delay time is determined by the state of the internal circuit and start pulse timing. Consequently, if continuous conversions are to be run at a fixed conversion time, the start pulse must be applied synchronized with the positive edge of EOC.

Output Circuit

As illustrated in Fig. 8, the output circuit consists of a D latch and a 3-state buffer. At the end of a conversion cycle, the converted data is latched in the D latch. Then when OE transits "H", the latched data is output to pins $2^{-1}\sim2^{-8}$. When OE is "L", pins $2^{-1}\sim2^{-8}$ are in a floating state.

During the conversion cycle, the previous data is held in the D latch.

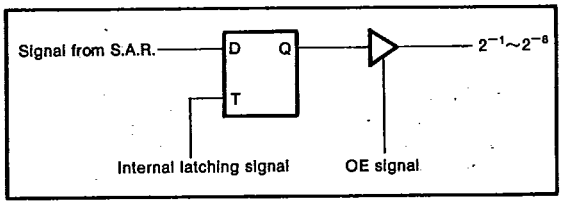


Fig.8 Output circuit

ERRORS AND ACCURACY OF THE A-D CONVERTER

Resolution

The analog input voltage range over which conversion operations are possible is referred to as the full scale range (FSR), and resolution defines the number of "steps" that FSR can be broken down into. In general, n-bits of resolution indicates that FSR can be resolved into $1/2^n$ steps. Also, resolution can be arrived at by taking FSR divided by 2^n as the size of the LSB.

Consequently, for 8-bits, FSR is divided into 256 steps, and if FSR is referenced to 5.12V, then the LSB will be 20mV.

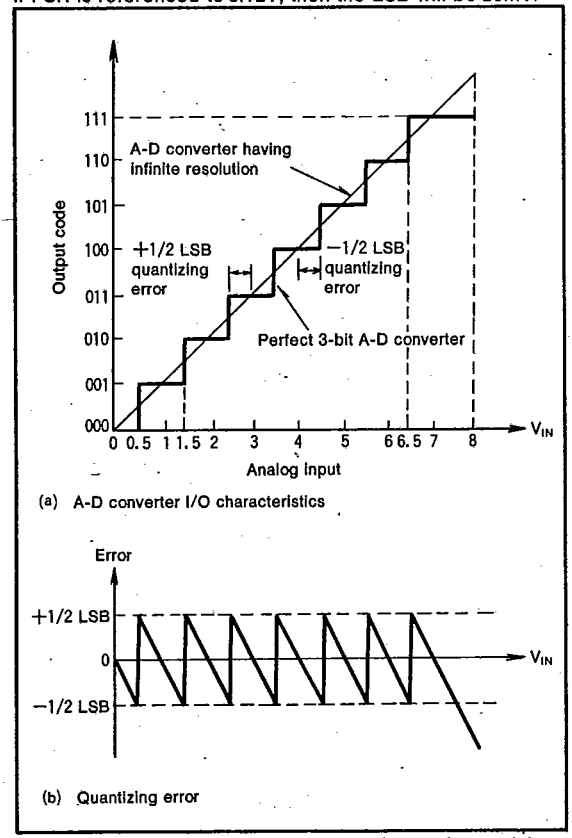


Fig.9 A-D converter I/O characteristics and quantizing errors

Quantizing Error

An inherent error in the A-D conversion process develops due to the fact that analog input values of less than the LSB must be rounded off. Figure 9 shows the quantizing errors occurring in a 3-bit A-D converter. The I/O characteristics of a perfect 3-bit A-D converter are illustrated in Fig. 9 (a). Where FSR is 8 and LSB is 1, as shown in the diagram, analog input voltage V_{IN} is rounded off to n in the range of

$$n-\frac{1}{2}LSB \leqq V_{IN} < n+\frac{1}{2}LSB\ (0<n\leqq 7).$$

In this case, a quantizing error of ±1/2 LSB is produced on one of the two ends of the step.

Fig. 9 (b) shows how quantizing errors are produced. Each step is shown like the tooth of a saw, centered on 0. An input of full scale becomes −1 LSB. This is because output codes can only be produced up to $111_2 = 7_{10}$, so when using the converter near full scale should be took care. In order to reduce quantizing errors, resolution must be increased.

Non-linearity Errors

Non-linearity error is the portion of A-D converter I/O characteristics that indicate the amount of deviation from the ideal line. These errors can be expressed as total linearity, or for only a portion of the scale, as differential nonlinearity. This is shown in Fig. 10.

Linearity indicates the amount of deviation from a straight line drawn from the start to the end of a step. Differential linearity indicates the amount that an actual step differs from 1 LSB of perfect step width. Monotonicity is the term used to express the fact that rises and falls in output follow rises and falls in input, and monotonicity cannot be assured unless differential nonlinearity is less than 1/2 LSB.

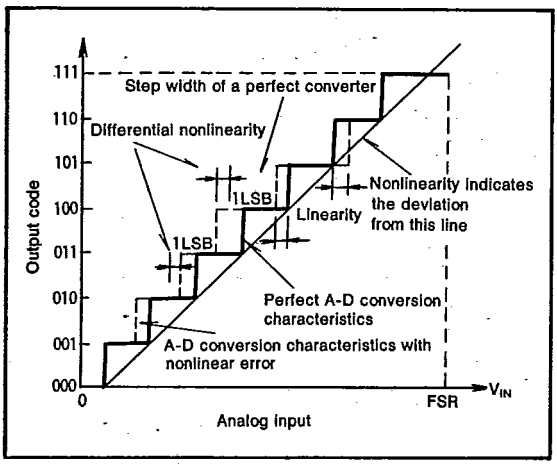


Fig.10 Nonlinearity in A-D conversion characteristics

Zero Error And Full Scale Error

Zero error is the error relative to the input voltage required to bring the output code to all "0"s, and full scale error is the error relative to the input voltage required to bring the output code to all "1"s. These errors are expressed as the amount of deviation from the perfect A-D conversion curve, and are illustrated in Fig. 11.

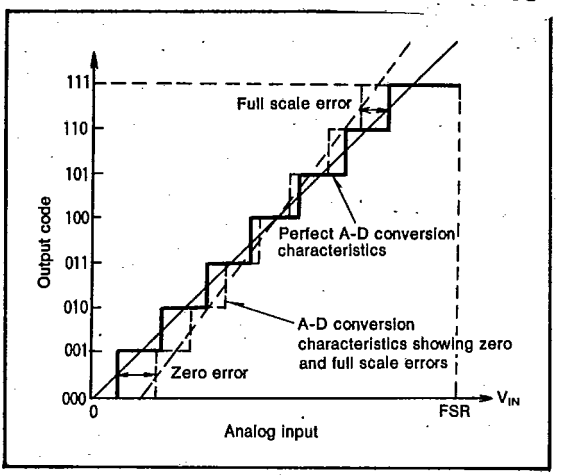


Fig.11 Zero and full scale error

Absolute Accuracy

Absolute accuracy accounts for the various errors occurring in the A-D conversion, and indicate how closely the output code represents the analog input. Where the output code is N;

$$\text{absolute accuracy} = N - \frac{V_{IN}}{LSB}$$

This is shown in Fig. 12.

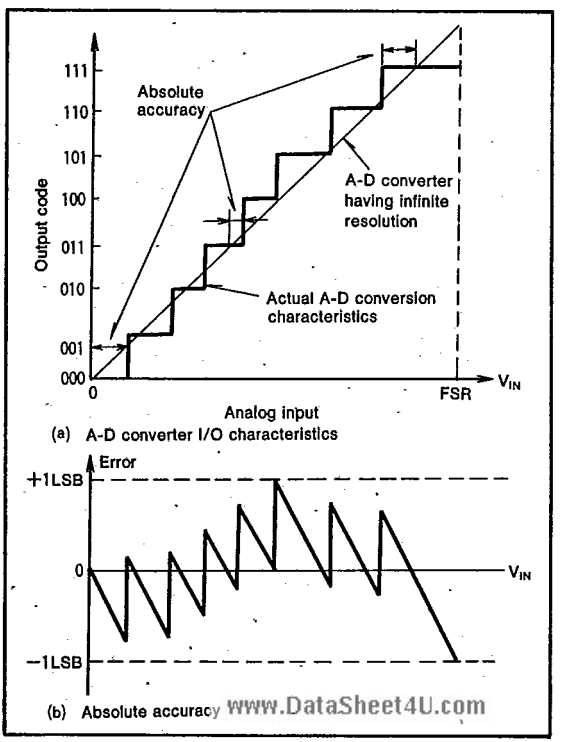


Fig.12 A-D converter absolute accuracy

PRECAUTIONS REGARDING REFERENCE VOLTAGE POWER SUPPLIES

Fig. 13 shows a portion of the 256R ladder network and switch tree, and Fig. 14 illustrates the turn-on resistance characteristics for MOSFETs.

As Fig. 14 shows, where drain potential V_D approaches V_{CC}, the turn-on resistance of n-channel MOSFETs increases. On the other hand, when V_D approaches GND, turn-on resistance for p-channel MOSFETs increases.

Where threshold voltage for the two transistor types is taken as V_{thN} and V_{thP} respectively, when V_D is between GND and V_{thN}, p-channel MOSFETs will not turn on, and when V_D is in the range $V_{CC} - V_{thP} \sim V_{CC}$, n-channel MOSFETs will not turn on. Due to this fact, the border formed by $(REF(+) + REF(-))/2$ in the switch tree of Fig. 13 is an operating limit for MOSFETs. Above this line, p-channel devices are used, and below this line n-channel devices are used.

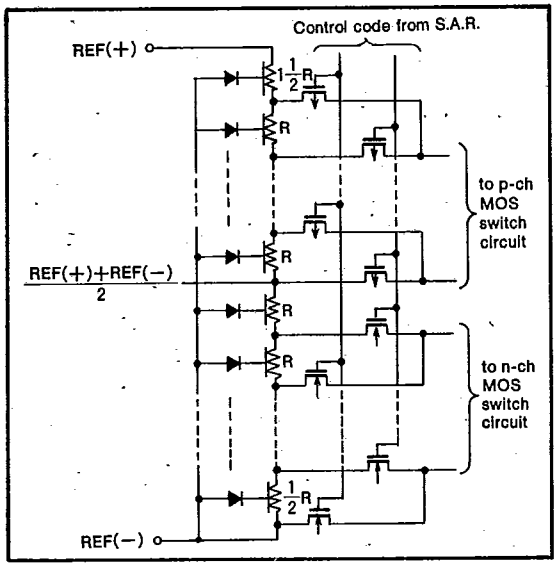


Fig.13 256R ladder network and switch tree

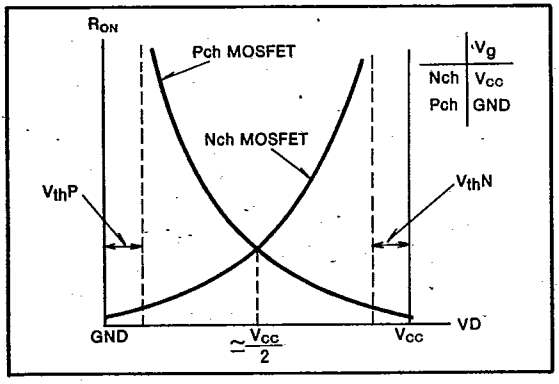


Fig.14 MOS switch turn-on resistance

For ladder network and switch tree structures like this, the following precautions should be observed in the design of the reference voltage supply.

1. REF (+) potential must not exceed V_{CC}.
2. REF (−) potential must not go below GND.
3. The value for $(REF(+) + REF(-))/2$ must not differ greatly from the value of $V_{CC}/2$.
4. $REF(+) > REF(-)$ must be observed.

The reason for 1 and 2 is that for MOS switches located near the V_{REF} pin, their souces and substate PN junctions are likely to forward bias, with the resulting current flow changing ladder potentials.

In 3, $(REF(+) + REF(-))/2$ is the potential for the center of the ladder, and as shown in Fig. 13, this is the borderline between p-channel and n-channel switch operations. Consequently, if this potential varies greatly from $V_{CC}/2$, turn-on resistance of the n-channel swiches near the center of the ladder will increase. (See Fig. 14.) On the other hand, if this value is smaller than $V_{CC}/2$, the turn-on resistance of the p-channel switches will increase.

Where turn-on resistance is high, the required settling time after fully charging the comparator's input capacitor becomes too long, and accuracy cannot be maintained.

In 4, if $REF(+) < REF(-)$, the up-down transients of the control signals from the S.A.R. will be reversed relative to the up-down transients of the reference voltage from ladder to comparator. In this case, instead of the approximations converging, the bits will diverge all "0"s or all "1"s. Also, as noted previously, where REF (+) and REF (−) approach GND and V_{CC} respectively, the switches will not turn on.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3~7	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Maximum power dissipation	T_a=25℃	500	mW
T_{opr}	Operating free-air temperature range		0~70	℃
T_{stg}	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=0~70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
GND	Supply voltage		0		V
$V_{REF(+)}$	Max of reference voltage(+)		V_{CC}	V_{CC}+0.1	V
$V_{REF(-)}$	Min of reference voltage(−)	−0.1	0		V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$		$\frac{V_{CC}}{2}$−0.1	$\frac{V_{CC}}{2}$	$\frac{V_{CC}}{2}$+0.1	V
$\triangle V_{REF}$	Defferential of reference voltage		5.12	5.25	V
$V_{I(IN)}$	Analog input voltage	0		$V_{REF(+)}$	V

ELECTRICAL CHARACTERISTICS (T_a=0~70℃, V_{CC}=5V ±5%, unless otherwise noted)

Symbol	Parameter		Alternative symbol	Test conditions	Limits			Unit
					Min	Typ	Max	
V_{IH}	High-level input voltage		$V_{IN(1)}$		2		V_{CC}	V
V_{IL}	Low-level input voltage		$V_{IN(0)}$		−0.3		0.8	V
V_{OH}	High-level output voltage		$V_{OUT(1)}$	I_{OH}=−360μA, T_a=70℃	V_{CC}−0.4			V
V_{OL}	Low-level output voltage, 2^{-1}~2^{-8} output		$V_{OUT(0)}$	I_{OL}=1.6mA			0.45	V
$V_{OL(EOC)}$	Low-level output voltage, EOC output		$V_{OUT(0)}$	I_{OL}=1.2mA			0.45	V
I_{IH}	High-level input current		$I_{IN(1)}$	V_{IH}=5.25V			1.0	μA
I_{IL}	Low-level input current		$I_{IN(0)}$	V_{IL}=0V			−1.0	μA
I_{OZH}	Off-state (high-impedance state) output current 2^{-1}~2^{-8} output		I_{OUT}	V_O=5V			3	μA
I_{OZL}	Off state (high-impedance state) output current, 2^{-1}~2^{-8} output		I_{OUT}	V_O=0V			−3	μA
I_{CC}	Supply current from V_{CC} input			$f_{C(\phi)}$=500kHz, T_a=70℃			1000	μA
I_{IZ}	Off-state input current, (IN_0~IN_7 input)		$I_{OFF(+)}$	V_{CC}=5V, V_I=5V			200	nA
I_{IZ}	Off-state input current, (IN_0~IN_7 input)		$I_{OFF(-)}$	V_{CC}=5V, V_I=0V			−200	nA
—	Conversion resolution				8			Bits
—	Linearity error	M58990P		V_{CC}=$V_{REF(+)}$=5.12V, $V_{REF(-)}$=GND		±¼	±½	LSB
		M58990P-1				±½	±1	
—	Zero error					±¼	±½	LSB
—	Full-scale error					±¼	±½	LSB
—	Absolute accuracy	M58990P					±1	LSB
		M58990P-1					±1½	
R_{LADDER}	Ladder resistances			V_{CC}=5V	1			kΩ
C_I	Input capacitance		C_{IN}	V_I=GND, V_O=25mVrms, f=1MHz			15	pF
C_O	Output capacitance		C_{OUT}	V_O=GND, V_O=25mVrms, f=1MHz			12	pF

Note 1 : Current flowing into an IC is positive, and Min and Max show the absolute limit.

TIMING REQUIREMENTS (T_a=25℃, V_{CC}=$V_{REF(+)}$=5V, $V_{REF(-)}$=GND unless otherwise noted)

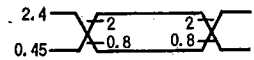
Symbol	Parameter	Alternative Symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{W(START)}$	Start pulse width	t_{WS}		200			ns
$t_{W(ALE)}$	ALE pulse width	t_{WALE}		200			ns
$t_{SU(A)}$	Address setup time	ts		50			ns
$t_{h(A)}$	Address hold time	t_H		50			ns
$f_{C(\phi)}$	Clock frequency	fc		10	640	1200	kHz
$t_{C(\phi)}$	Clock cycle	—		100	1.56	0.83	μs

SWITCHING CHARACTERISTICS (T_a=25℃, V_{CC}=$V_{REF(+)}$=5V, $V_{REF(-)}$=GND, unless otherwise noted)

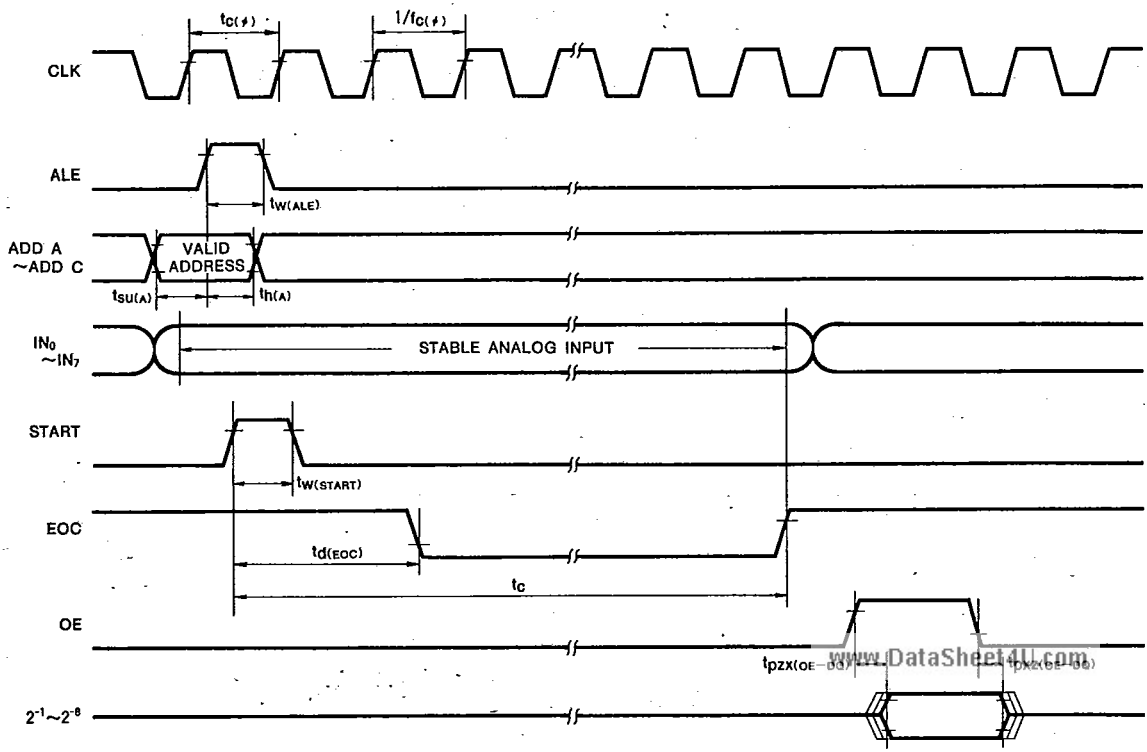
Symbol	Parameter	Alternative Symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{PZX(OE-DQ)}$	Propagation time from OE to output	t_{HI}, t_{HO}	C_L=50pF			250	ns
$t_{PXZ(OE-DQ)}$	Propagation time from OE to output floating	t_{IH}, t_{OH}				250	ns
t_C	Cycle time	tc	$f_{C(\phi)}$=640kHz			114	ns
$t_{d(EOC)}$	EOC delay time	t_{EOC}		1		8	Clock cycle time

Note 2 : A. C Testing waveform

Input pulse level	0.45~2.4V
Input pulse rise time	10ns
Input pulse fall time	10ns
Reference level Input	V_{IH}=2V, V_{IL}=0.8V
output	V_{OH}=2V, V_{OL}=0.8V



TIMING DIAGRAM



APPLICATION EXAMPLE