DPS512S8AA3

HIGH SPEED CERAMIC 512K X 8
BUFFERED/DECODED CMOS SRAM MODULE

Dense-Pac Microsystems, Inc.

PRELIMINARY

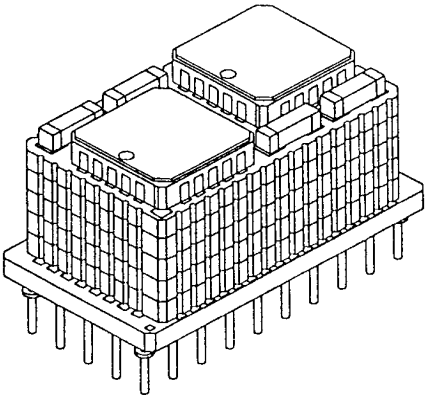
DESCRIPTION:

The DPS512S8AA3 "DENSE-STACK" module is a revolutionary new high speed memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC) along with memory interface logic and capacitors mounted on a co-fired ceramic substrate. The module packs 4-Megabits of low-power CMOS static RAM in an area of just over one half square inch (0.540 in^2), while maintaining a height of only 0.570 inches.

The DPS512S8AA3 contains four individual 128K x 8 SRAMs, packaged in their own hermetically sealed SLCCs plus an address decoder and data transceiver making the module suitable for commercial, industrial and military applications, with a minimum of external support logic.

The module is organized as 512K x 8 and features extremely low standby power making it suitable for battery backup.

By using SLCCs, the "Dense-Stack" family of modules offers a higher board density of memory than available with conventional through-hole, surface mount or hybrid techniques.

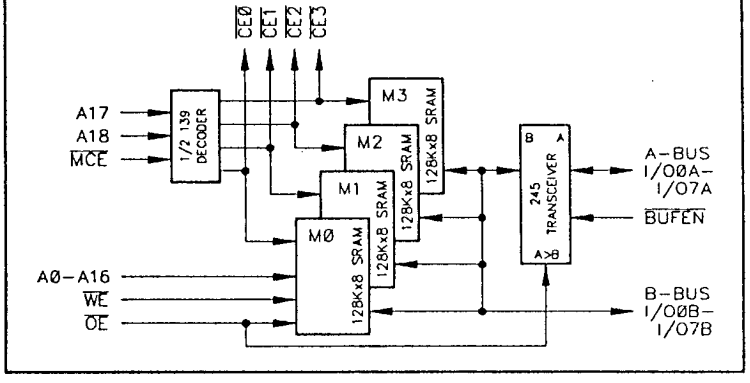


FEATURES:

- Organization Available: 512K x 8
- Access Times: 55*, 70, 85ns
- Fully Static Operation - No clock or refresh required
- Single +5V Power Supply, ±10% Tolerance
- TTL Compatible
- Common Data Inputs and Outputs
- Low Power Dissipation:
  200mW (typ.) Standby
  475mW (typ.) Operating
- 2 Volt Data Retention: 2.0µA (typ.)
- 50-Pin PGA Package

* Commercial only.

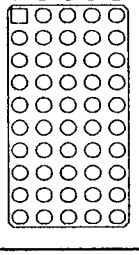
FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAM

	A	B	C	D	E
1	A17	$\overline{MCE}$	$\overline{CE3}$**	$\overline{CE2}$**	$\overline{CE1}$**
2	VSS	VSS	$\overline{BUFEN}$	N.C.**	VDD
3	A18	A16	$\overline{WE}$	N.C.**	A15
4	A14	A12	A7	A8	A13
5	A6	A5	$\overline{OE}$	A11	A9
6	A4	A3	A2	$\overline{CE0}$**	A10
7	A1	A0	I/O5A	I/O4A	I/O3A
8	I/O2A	I/O1A	I/O0A	I/O7A	I/O6A
9	VSS	I/O1B*	I/O3B*	I/O5B*	VDD
10	I/O0B*	I/O2B*	I/O4B*	I/O6B*	I/O7B*

(TOP VIEW)



PIN NAMES

A0 - A18	Address Inputs
I/O0A - I/O7A, I/O0B - I/O7B	Data Input/Output
$\overline{MCE}$	Master Chip Enable
$\overline{CE0}$ - $\overline{CE3}$	Low Chip Enables
$\overline{BUFEN}$	Buffer Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground

* Data I/O lines I/O0B - I/O7B are not buffered.
** Leave these output pins unconnected or use them to drive other modules.

PRELIMINARY

RECOMMENDED OPERATING RANGE[3]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.8	V
T_A	Operating Temp.	-55	+25	+125	°C

ABSOLUTE MAXIMUM RATINGS[3]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.5 to +7.0	V
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD} +0.5	V

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	40	pF	V_{IN}[2] = 0V
C_{MCE}	Master Chip Enable	25		
C_{BUF}	Buffer Enable	20		
C_{WE}	Write Enable	40		
C_{OE}	Output Enable	50		
$C_{I/O}$	Data Input/Output	20		

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH} = -12mA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL} = 48mA	-	0.4	V

TRUTH TABLE							
Standard Operating Modes	$\overline{MCE}$	$\overline{BUFEN}$	$\overline{WE}$	$\overline{OE}$	A-BUS	B-BUS	Supply Current
Not Selected	H	H	X	X	HIGH-Z	HIGH-Z	Standby
Read A to B	L	L	H	L	D_{OUT}	D_{OUT}	Active
Write A, A to B	L	L	L	H	D_{IN}	A-DATA	Active
Output Disable	L	H	H	H	HIGH-Z	HIGH-Z	Active
Other Operating Modes							
B to A	H	L	X	L	Output	Input	Active
A to B	H	L	X	H	Input	Output	Active
Read B	L	H	H	L	HIGH-Z	D_{OUT}	Active
Write B	L	H	L	X	HIGH-Z	D_{IN}	Active
A to B	L	L	H	H	Input	Output	Active
Write B, B to A	L	L	L	L	B-DATA	D_{IN}	Active

H = HIGH, L = LOW & X = Don't Care.

DC OPERATING CHARACTERISTICS: Over operating ranges										
Symbol	Characteristics	Test Conditions	TYP. (†)	C		I		M		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-	-8	+8	-8	+8	-8	+8	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{MCE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-	-15	+15	-15	+15	-15	+15	µA
I_{CC1}	Active Supply Current	$\overline{MCE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA	60		100		125		125	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA	90		140		165		165	mA
I_{SB1}	Full Standby Supply Current (CMOS)	V_{IN} ≥ V_{DD} -0.2V or V_{IN} ≤ V_{SS} +0.2V, $\overline{MCE}$ ≥ V_{DD} -0.2V	0.05		4		8		12	mA
I_{SB2}	Standby Current (TTL)	$\overline{MCE}$ = V_{IH}	25		40		60		60	mA
I_{DR3}	Data Retention Supply Current (3V)	V_{DR} = 3V, $\overline{MCE}$ ≥ V_{DR} -0.2V	40		480		800		2800	µA
I_{DR2}	Data Retention Supply Current (2V)	V_{DR} = 2V, $\overline{MCE}$ ≥ V_{DR} -0.2V	20		400		680		2000	µA
V_{OL}	Output Low Voltage	I_{OUT} = 48mA	-		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -12mA	-	2.4		2.4		2.4		V

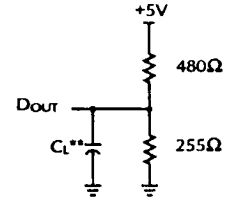
† Typical measurements made at +25°C, Cycle = min., V_{DD} = 5.0V.

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

* Transition between 0.8 and 2.2V.

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	30 pF	except t_{BLZ} and t_{BHZ}
2	5 pF	t_{BLZ} and t_{BHZ}

Figure 1. Output Load
** Including Probe and Jig Capacitance.



AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges									
No.	Symbol	Parameter	-55†		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	55		70		85		ns
2	t_{AA}	Address Access Time		55		70		85	ns
3	t_{CO}	Chip Enable to Output Valid		55		70		85	ns
4	t_{BV}	$\overline{BUFEN}$ to Output Valid		15		15		15	ns
5	t_{OE}	Output Enable to Output Valid		30		40		45	ns
6	t_{OSB}	Output Enable Setup Time to $\overline{BUFEN}$		10		10		10	ns
7	t_{OH}	Output Hold from Address Change	10		10		10		ns
8	t_{BLZ}***	$\overline{BUFEN}$ to Output in LOW-Z [4, 5]	1.5	-	1.5	-	1.5	-	ns
9	t_{BHZ}***	$\overline{BUFEN}$ to Output in HIGH-Z [4, 5]	1.5	15	1.5	15	1.5	15	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE [6]: Over operating ranges									
No.	Symbol	Parameter	-55†		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time	55		70		85		ns
11	t_{AW}	Address Valid to End of Write	45		60		75		ns
12	t_{CW}	$\overline{MCE}$ to End of Write	45		60		75		ns
13	t_{BW}	$\overline{BUFEN}$ to End of Write	35		45		45		ns
14	t_{OSB}	Output Enable Setup Time to $\overline{BUFEN}$	10		10		10		ns
15	t_{AS}***	Address Set-up Time	0		0		0		ns
16	t_{WP}	Write Pulse Width	40		55		65		ns
17	t_{WR}	Write Recovery Time	5		10		10		ns
18	t_{DW}	Data to Write Time Overlap	25		35		35		ns
19	t_{DH}	Data Hold from Write Time	0		0		0		ns

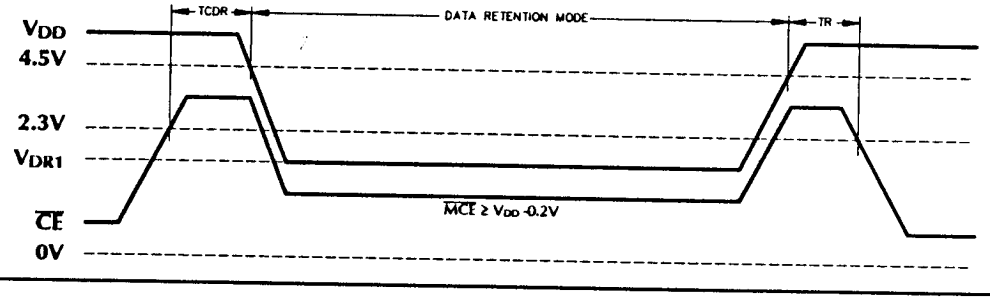
† Commercial grade only.
*** Valid for both Read and Write Cycles.

PRELIMINARY

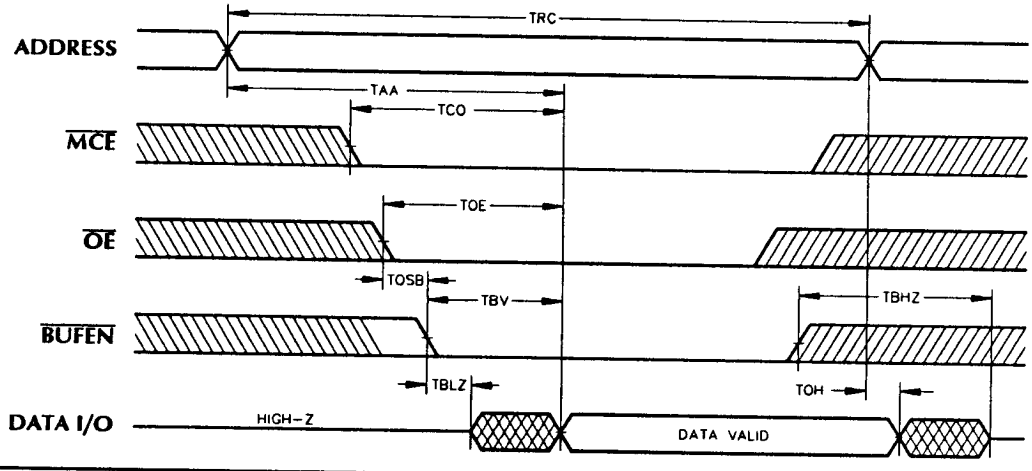
Data Retention AC Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	$\overline{MCE} \geq V_{DD}$ -0.2V	2.0	-	-	V
t_{CDR}	Chip Disable to Data Retention Time	See Data Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time	See Data Retention Waveform	5	-	-	ms

DATA RETENTION WAVEFORM: $\overline{CE}$ Controlled.



READ CYCLE: $\overline{MCE}$ Controlled. $\overline{WE}$ is High.

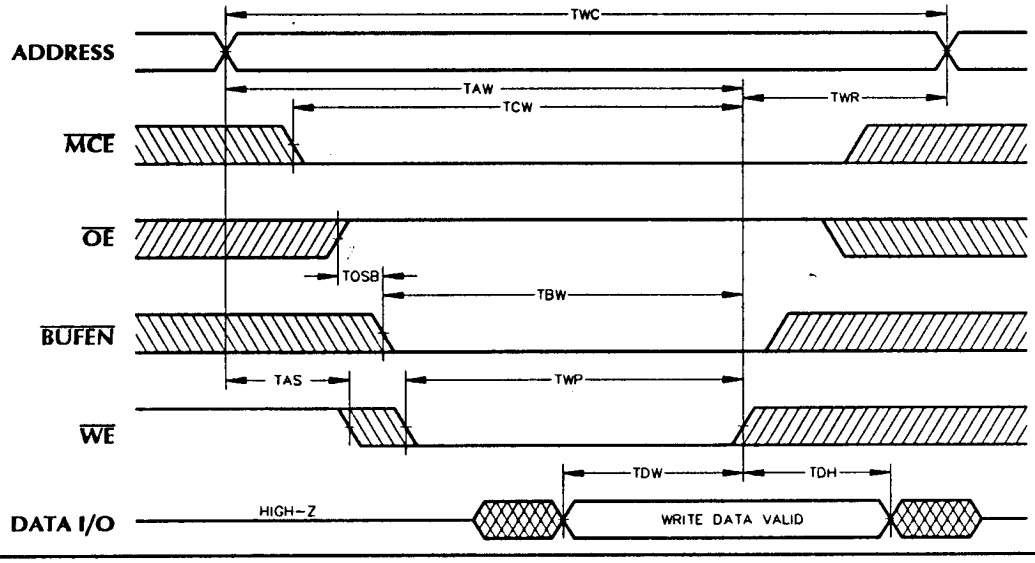


WAVEFORM KEY

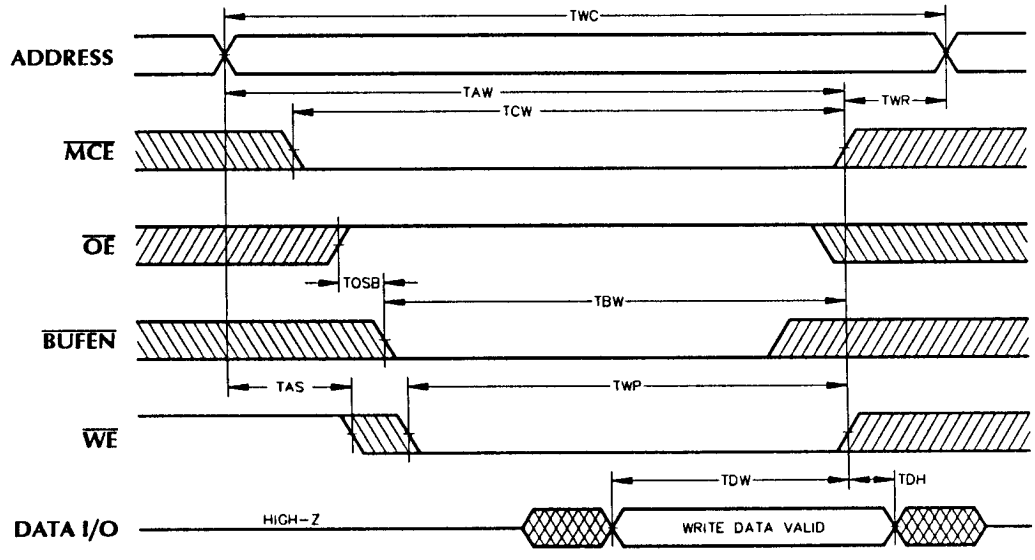
Data Valid	Transition from HIGH to LOW	Transition from LOW to HIGH	Data Undefined or Don't Care

PRELIMINARY

WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ Clocked.



WRITE CYCLE 2: $\overline{MCE}$ Controlled. $\overline{OE}$ Clocked.



PRELIMINARY

ORDERING INFORMATION

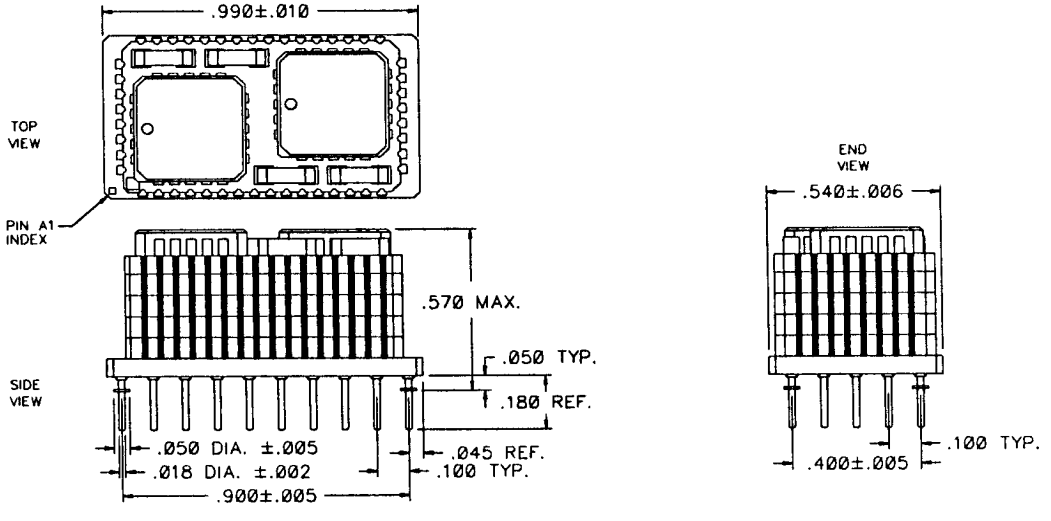
DP S 512 S 8 AA3 – XX X

PREFIX		
TYPE		
MEMORY DEPTH		
DESIG		
MEMORY WIDTH		
PACKAGE		
SPEED		
GRADE		
	C	COMMERCIAL 0°C to +70°C
	I	INDUSTRIAL -40°C to +85°C
	M	MILITARY -55°C to +125°C
	B	MIL-PROCESSED -55°C to +125°C
	55	55ns (COMMERCIAL ONLY)
	70	70ns
	85	85ns
		HIGH SPEED, CERAMIC PIN GRID ARRAY (PGA) (3-D) DENSE-STACK MODULE
		MODULE WITH SUPPORT LOGIC
		CMOS SRAM DEVICES

NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$, $\overline{MCE}$, and $\overline{BUFEN}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.

MECHANICAL DRAWING



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