MEMORY Mobile FCRAM™
CMOS
16M Bit (1 M word x 16 bit)
Mobile Phone Application Specific Memory

MB82DS01181E-70L-A

CMOS 1,048,576-WORD x 16 BIT
Fast Cycle Random Access Memory
with Low Power SRAM Interface

■ DESCRIPTION

The Fujitsu MB82DS01181E is a CMOS Fast Cycle Random Access Memory (FCRAM) with asynchronous Static Random Access Memory (SRAM) interface containing 16,777,216 storages accessible in a 16-bit format. This MB82DS01181E is suited for mobile applications such as Cellular Handset and PDA.

■ FEATURES

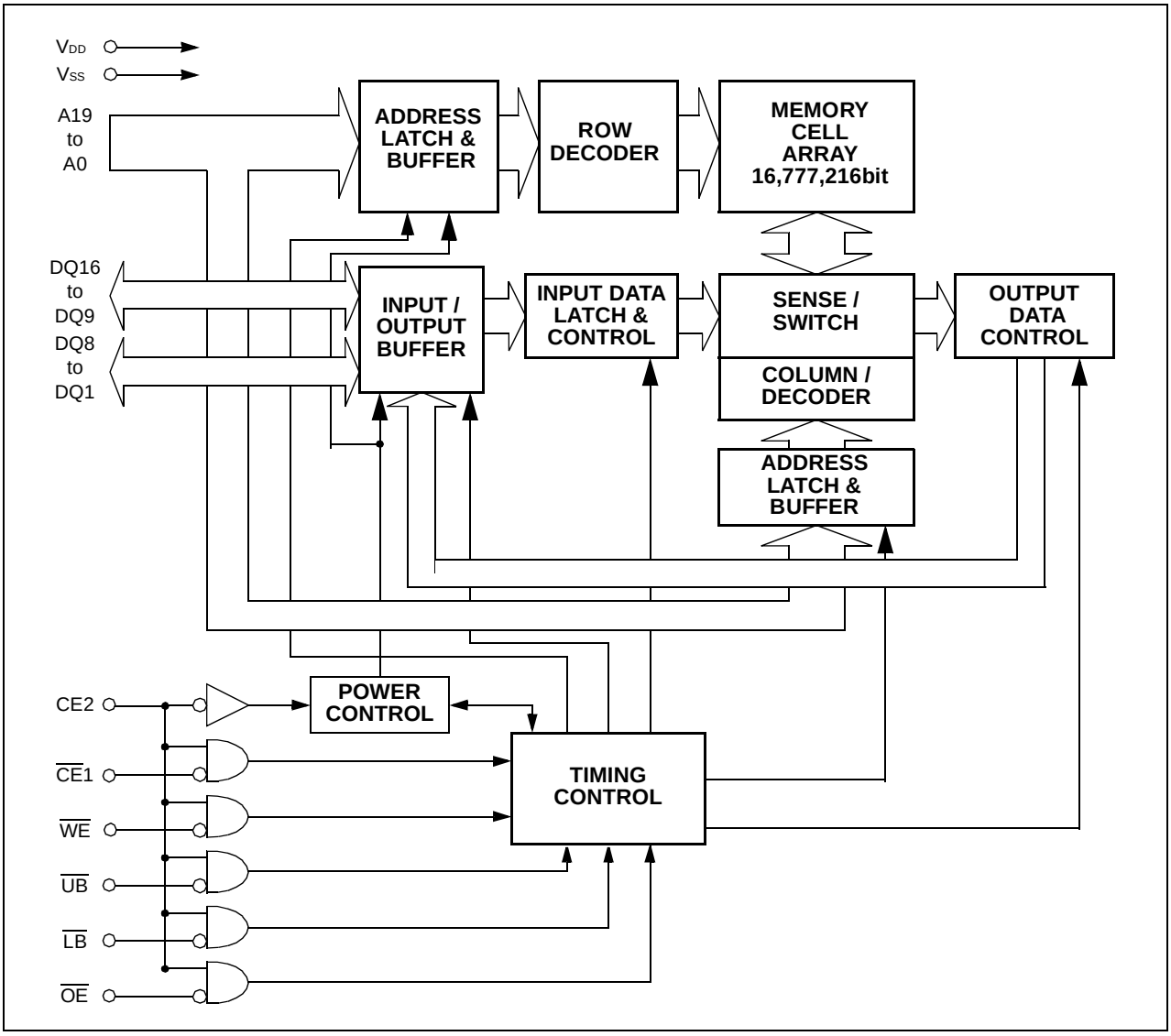
- Asynchronous SRAM Interface
- Fast Random Access Time
  t_{CE} = 70ns (-70)
- Low Voltage Operating Condition
  V_{DD} = +1.7V to +1.95V
- Wide Operating Temperature
  T_A = -30°C to +85°C
- Byte Control by $\overline{LB}$ and $\overline{UB}$
- Low Power Consumption
  I_{DDA1} = 20mA max
  I_{DDS1} = 100µA max
- Power Down mode

Notice: FCRAM is a trademark of Fujitsu Limited, Japan

■ PIN DESCRIPTION

Pin Name	Description
A_{19} to A_0	Address Input
$\overline{CE}1$	Chip Enable (Low Active)
CE2	Chip Enable (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{UB}$	Upper Byte Control (Low Active)
$\overline{LB}$	Lower Byte Control (Low Active)
DQ_{16-9}	Upper Byte Data Input/Output
DQ_{8-1}	Lower Byte Data Input/Output
V_{DD}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE

Mode	Note	CE2	$\overline{CE1}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	A19-0	DQ8-1	DQ16-9	I_{DD}	Data Retention
Standby (Deselect)		H	H	X	X	X	X	X	High-Z	High-Z	I_{DDS}	Yes
Output Disable	*1	H	L	H	H	X	X	*3	High-Z	High-Z	I_{DDA}	
Output Disable (No Read)				H	L	H	H	Valid	High-Z	High-Z		
Read (Upper Byte)						H	L	Valid	High-Z	Output Valid		
Read (Lower Byte)						L	H	Valid	Output Valid	High-Z		
Read (Word)						L	L	Valid	Output Valid	Output Valid		
No Write				L	H	H	H	Valid	Invalid	Invalid		
Write (Upper Byte)						H	L	Valid	Invalid	Input Valid		
Write (Lower Byte)						L	H	Valid	Input Valid	Invalid		
Write (Word)						L	L	Valid	Input Valid	Input Valid		
Power Down	*2	L	X	X	X	X	X	X	High-Z	High-Z	I_{DDP}	No

Notes L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High Impedance

*1: Should not be kept this logic condition longer than 1µs.
Please contact local FUJITSU representative for the relaxation of 1µs limitation.

*2: Power Down mode can be entered from Standby state and all DQ pins are in High-Z state.

*3: Can be either V_{IL} or V_{IH} but must be valid before Read or Write.

■ ABSOLUTE MAXIMUM RATINGS

(See WARNING below.)

Parameter	Symbol	Value	Unit
Voltage of V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 to +3.6	V
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +3.6	V
Short Circuit Output Current	I_{OUT}	±50	mA
Storage Temperature	T_{STG}	-55 to +125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

(See WARNING below.)

Parameter	Notes	Symbol	Min.	Max.	Unit
Supply Voltage		V_{DD}	1.7	1.95	V
		V_{SS}	0	0	V
High Level Input Voltage	*1	V_{IH}	V_{DD}*0.8	V_{DD}+0.2	V
Low Level Input Voltage	*2	V_{IL}	-0.3	V_{DD}*0.2	V
Ambient Temperature		T_A	-30	85	°C

(Referenced to V_{SS})

Notes *1: Maximum DC voltage on input and I/O pins are V_{DD}+0.2V. During voltage transitions, inputs may positive overshoot to V_{DD}+1.0V for periods of up to 5 ns.

*2: Minimum DC voltage on input or I/O pins are -0.3V. During voltage transitions, inputs may negative overshoot V_{SS} to -1.0V for periods of up to 5ns.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ PACKAGE PIN CAPACITANCE

Test conditions: T_A = 25°C, f = 1.0 MHz

Symbol	Description	Test Setup	Typ.	Max.	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0V	—	5	pF
C_{IN2}	Control Input Capacitance	V_{IN} = 0V	—	5	pF
C_{IO}	Data Input/Output Capacitance	V_{IO} = 0V	—	8	pF

■ DC CHARACTERISTICS

(Under Recommended Operating Conditions unless otherwise noted) Note *1,*2,*3

Parameter	Symbol	Test Conditions		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}		-1.0	+1.0	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{DD}, Output Disable		-1.0	+1.0	µA
Output High Voltage Level	V_{OH}	V_{DD} = V_{DD}(min), I_{OH} = –0.5mA		1.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 1mA		—	0.4	V
V_{DD} Power Down Current	I_{DDPS}	V_{DD} = V_{DD} max., V_{IN} = V_{IH} or V_{IL}, CE2 ≤ 0.2V		—	10	µA
V_{DD} Standby Current	I_{DDS}	V_{DD} = V_{DD} max., $\overline{V_{IN}}$ = V_{IH} or V_{IL} $\overline{CE1}$ = CE2 = V_{IH}		—	1	mA
	I_{DDS1}	V_{DD} = V_{DD} max., $\overline{V_{IN}}$ ≤ 0.2V or V_{IN} ≥ V_{DD} – 0.2V, $\overline{CE1}$ = CE2 ≥ V_{DD} – 0.2V		—	100	µA
V_{DD} Active Current	I_{DDA1}	V_{DD} = V_{DD} max., $\overline{V_{IN}}$ = V_{IH} or V_{IL}, $\overline{CE1}$ = V_{IL} and CE2= V_{IH}, I_{OUT}=0mA	t_{RC} / t_{WC} = minimum	—	20	mA
	I_{DDA2}		t_{RC} / t_{WC} = 1µs	—	3	mA

Notes *1: All voltages are referenced to Vss.
*2: DC Characteristics are measured after following POWER-UP timing.
*3: I_{OUT} depends on the output load conditions.

■ AC CHARACTERISTICS

(Under Recommended Operating Conditions unless otherwise noted)

READ OPERATION

Parameter	Symbol	Value		Unit	Notes
		Min.	Max.		
Read Cycle Time	t_{RC}	80	1000	ns	*1, *2
$\overline{CE}$1 Access Time	t_{CE}	—	70	ns	*3
$\overline{OE}$ Access Time	t_{OE}	—	45	ns	*3
Address Access Time	t_{AA}	—	70	ns	*3, *5
$\overline{LB}$ / $\overline{UB}$ Access Time	t_{BA}	—	30	ns	*3
Output Data Hold Time	t_{OH}	5	—	ns	*3
$\overline{CE}$1 Low to Output Low-Z	t_{CLZ}	5	—	ns	*4
$\overline{OE}$ Low to Output Low-Z	t_{OLZ}	0	—	ns	*4
$\overline{LB}$ / $\overline{UB}$ Low to Output Low-Z	t_{BLZ}	0	—	ns	*4
$\overline{CE}$1 High to Output High-Z	t_{CHZ}	—	20	ns	*3
$\overline{OE}$ High to Output High-Z	t_{OHZ}	—	20	ns	*3
$\overline{LB}$ / $\overline{UB}$ High to Output High-Z	t_{BHZ}	—	20	ns	*3
Address Setup Time to $\overline{CE}$1 Low	t_{ASC}	–5	—	ns	
Address Setup Time to $\overline{OE}$ Low	t_{ASO}	10	—	ns	
Address Invalid Time	t_{AX}	—	10	ns	*5
Address Hold Time from $\overline{CE}$1 High	t_{CHAH}	–5	—	ns	*6
Address Hold Time from $\overline{OE}$ High	t_{OHAH}	–5	—	ns	
$\overline{WE}$ High to $\overline{OE}$ Low Time for Read	t_{WHOL}	15	1000	ns	*7
$\overline{CE}$1 High Pulse Width	t_{CP}	15	—	ns	

Notes *1: Maximum value is applicable if $\overline{CE}$1 is kept at Low without any address change. If the relaxation is needed by system operation, please contact local FUJITSU representative for the relaxation of 1µs limitation.

*2: Address should not be changed within minimum t_{RC}.

*3: The output load 50pF with 50ohm termination to V_{DD}*0.5 V.

*4: The output load 5pF without any other load.

*5: Applicable when $\overline{CE}$1 is kept at Low.

*6: t_{RC}(min) must be satisfied.

*7: If actual value of t_{WHOL} is shorter than specified minimum values, the actual t_{AA} of following Read may become longer by the amount of subtracting actual value from specified minimum value.

■ AC CHARACTERISTICS (Continued)

WRITE OPERATION

Parameter	Symbol	Value		Unit	Notes
		Min.	Max.		
Write Cycle Time	t_{WC}	80	1000	ns	*1, *2
Address Setup Time	t_{AS}	0	—	ns	*2
$\overline{CE}1$ Write Pulse Width	t_{CW}	45	—	ns	*3
$\overline{WE}$ Write Pulse Width	t_{WP}	45	—	ns	*3
$\overline{LB}$ / $\overline{UB}$ Write Pulse Width	t_{BW}	45	—	ns	*3
$\overline{LB}$ / $\overline{UB}$ Byte Mask Setup Time	t_{BS}	–5	—	ns	*4
$\overline{LB}$ / $\overline{UB}$ Byte Mask Hold Time	t_{BH}	–5	—	ns	*5
Write Recovery Time	t_{WR}	0	—	ns	*6
$\overline{CE}1$ High Pulse Width	t_{CP}	15	—	ns	
$\overline{WE}$ High Pulse Width	t_{WHP}	15	1000	ns	
$\overline{LB}$ / $\overline{UB}$ High Pulse Width	t_{BHP}	15	1000	ns	
Data Setup Time	t_{DS}	20	—	ns	
Data Hold Time	t_{DH}	0	—	ns	
$\overline{OE}$ High to $\overline{CE}1$ Low Setup Time for Write	t_{OHCL}	–5	—	ns	*7
$\overline{OE}$ High to Address Setup Time for Write	t_{OES}	0	—	ns	*8
$\overline{LB}$ and $\overline{UB}$ Write Pulse Overlap	t_{BWO}	20	—	ns	

Notes *1: Maximum value is applicable if $\overline{CE}1$ is kept at Low without any address change. If the relaxation is needed by system operation, please contact local FUJITSU representative for the relaxation of 1µs limitation.

*2: Minimum value must be equal or greater than the sum of write pulse (t_{CW}, t_{WP} or t_{BW}) and write recovery time (t_{WRC}, t_{WR} or t_{BR}).

*3: Write pulse is defined from High to Low transition of $\overline{CE}1$, $\overline{WE}$, or $\overline{LB}$ / $\overline{UB}$, whichever occurs last.

*4: Applicable for byte mask only. Byte mask setup time is defined to the High to Low transition of $\overline{CE}1$ or $\overline{WE}$ whichever occurs last.

*5: Applicable for byte mask only. Byte mask hold time is defined from the Low to High transition of $\overline{CE}1$ or $\overline{WE}$ whichever occurs first.

*6: Write recovery is defined from Low to High transition of $\overline{CE}1$, $\overline{WE}$, or $\overline{LB}$ / $\overline{UB}$, whichever occurs first.

*7: If $\overline{OE}$ is Low after minimum t_{OHCL}, read cycle is initiated. In other word, $\overline{OE}$ must be brought to High within 5ns after $\overline{CE}1$ is brought to Low. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met.

*8: If $\overline{OE}$ is Low after new address input, read cycle is initiated. In other word, $\overline{OE}$ must be brought to High at the same time or before new address valid. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met.

■ AC CHARACTERISTICS (Continued)

POWER DOWN PARAMETERS

Parameter	Symbol	Value		Unit	Note
		Min.	Max.		
CE2 Low Setup Time for Power Down Entry	t_{CSP}	10	—	ns	
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	80	—	ns	
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit [SLEEP mode only]	t_{CHH}	300	—	µs	*1
$\overline{CE}$1 High Setup Time following CE2 High after Power Down Exit	t_{CHS}	0	—	ns	

Notes *1: Applicable also to power-up.

OTHER TIMING PARAMETERS

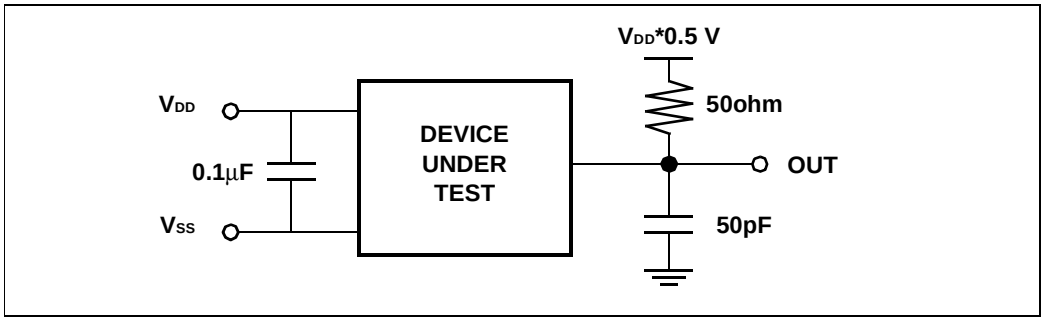
Parameter	Symbol	Value		Unit	Note
		Min.	Max.		
$\overline{CE}$1 High to $\overline{OE}$ Invalid Time for Standby Entry	t_{CHOX}	10	—	ns	
$\overline{CE}$1 High to $\overline{WE}$ Invalid Time for Standby Entry	t_{CHWX}	10	—	ns	*1
$\overline{CE}$1 High Hold Time following CE2 High after Power-up	t_{CHH}	300	—	µs	
Input Transition Time	t_T	1	25	ns	*2

Notes *1: Some data might be written into any address location if t_{CHWX}(min) is not satisfied.
*2: The Input Transition Time (t_T) at AC testing is 5ns as shown in below. If actual t_T is longer than 5ns, it may violate AC specification of some timing parameters.

AC TEST CONDITIONS

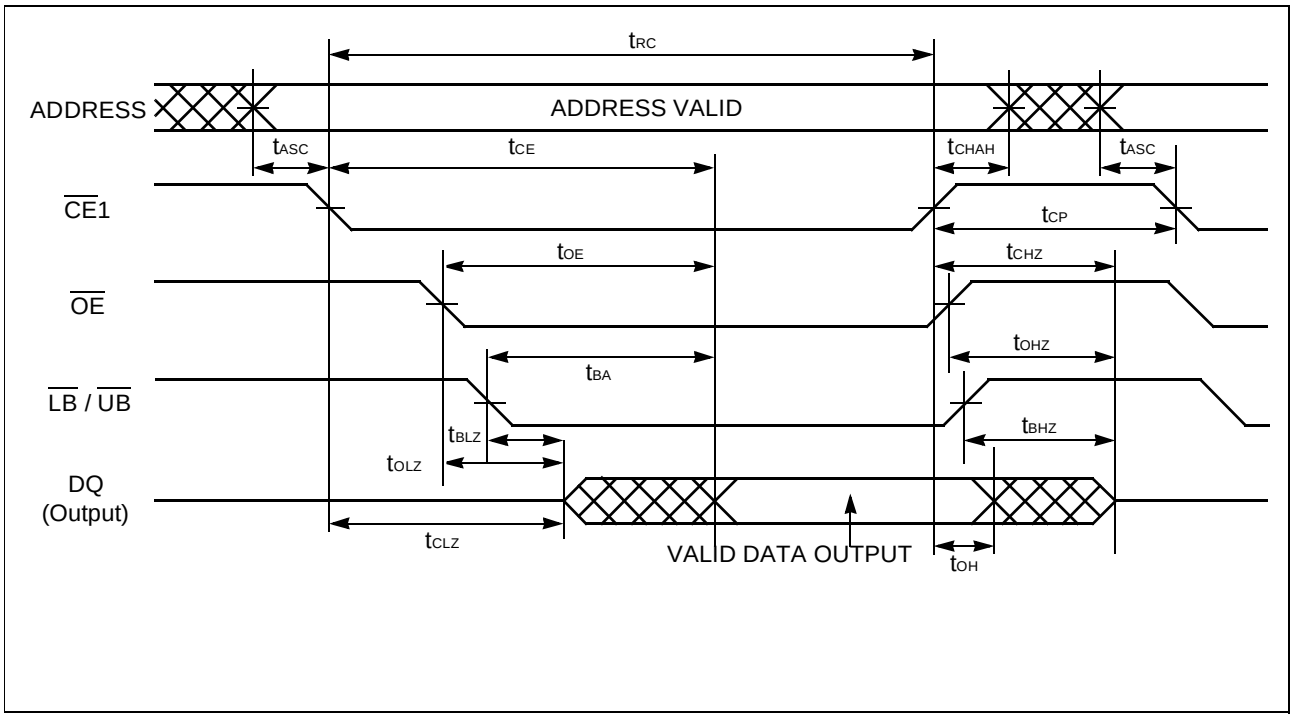
Symbol	Description	Test Setup	Value	Unit	Note
V_{IH}	Input High Level		V_{DD} * 0.8	V	
V_{IL}	Input Low Level		V_{DD} * 0.2	V	
V_{REF}	Input Timing Measurement Level		V_{DD} * 0.5	V	
t_T	Input Transition Time	Between V_{IL} and V_{IH}	5	ns	

AC MEASUREMENT OUTPUT LOAD CIRCUIT



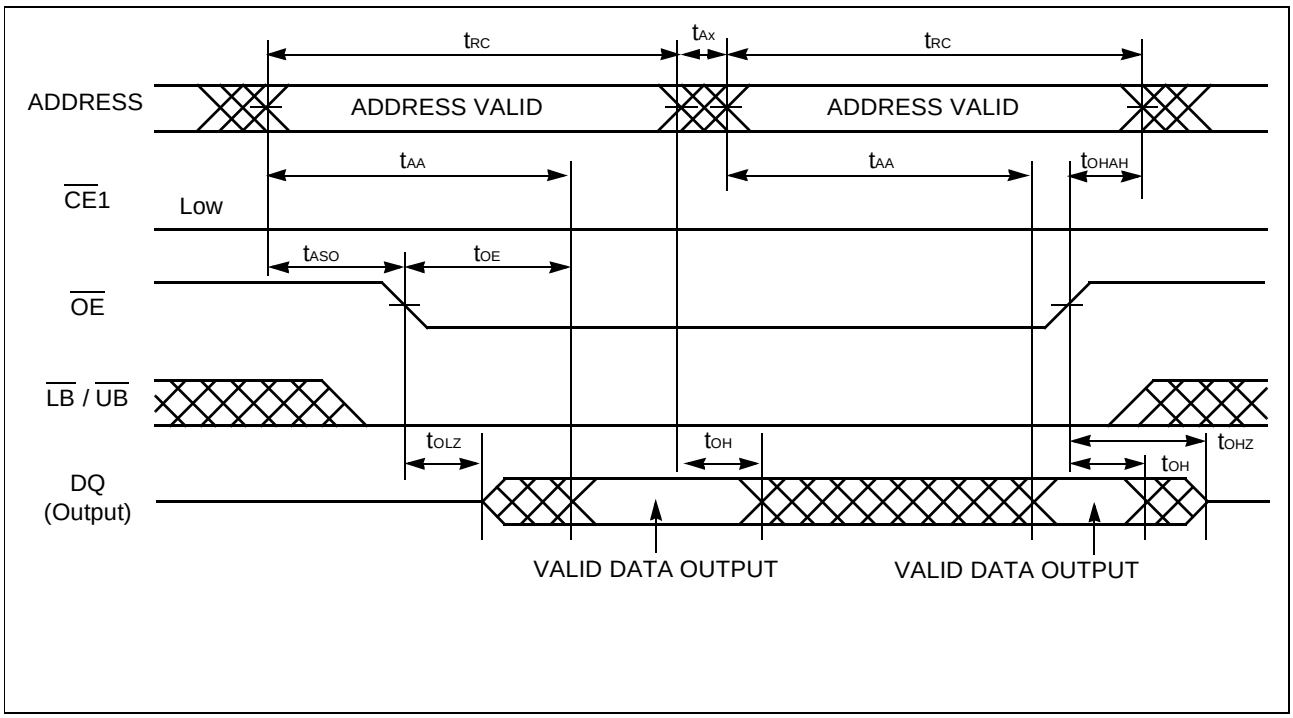
■ TIMING DIAGRAMS

READ Timing #1 (Basic Timing) See Note.



Note: This timing diagram assumes CE2=H and $\overline{WE}$=H.

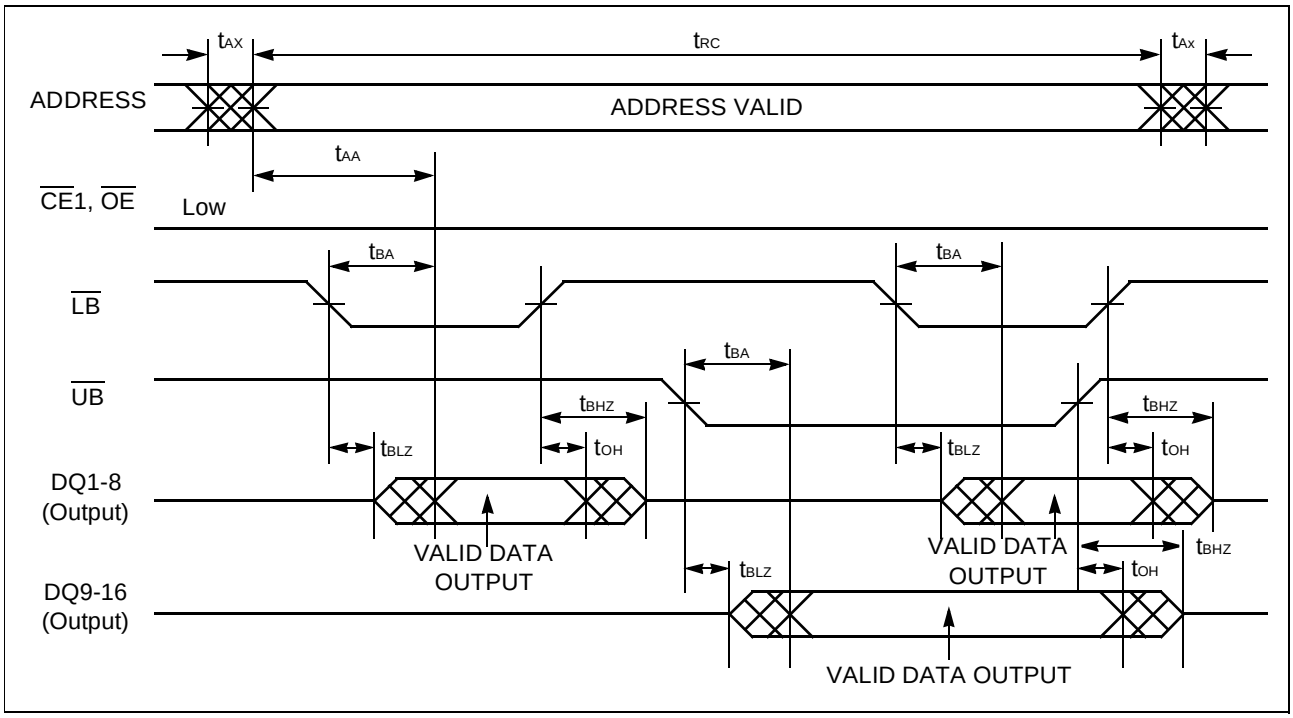
READ Timing #2 ($\overline{OE}$ & Address Access) See Note.



Notes: This timing diagram assumes CE2=H and $\overline{WE}$=H.

■ TIMING DIAGRAMS (Continued)

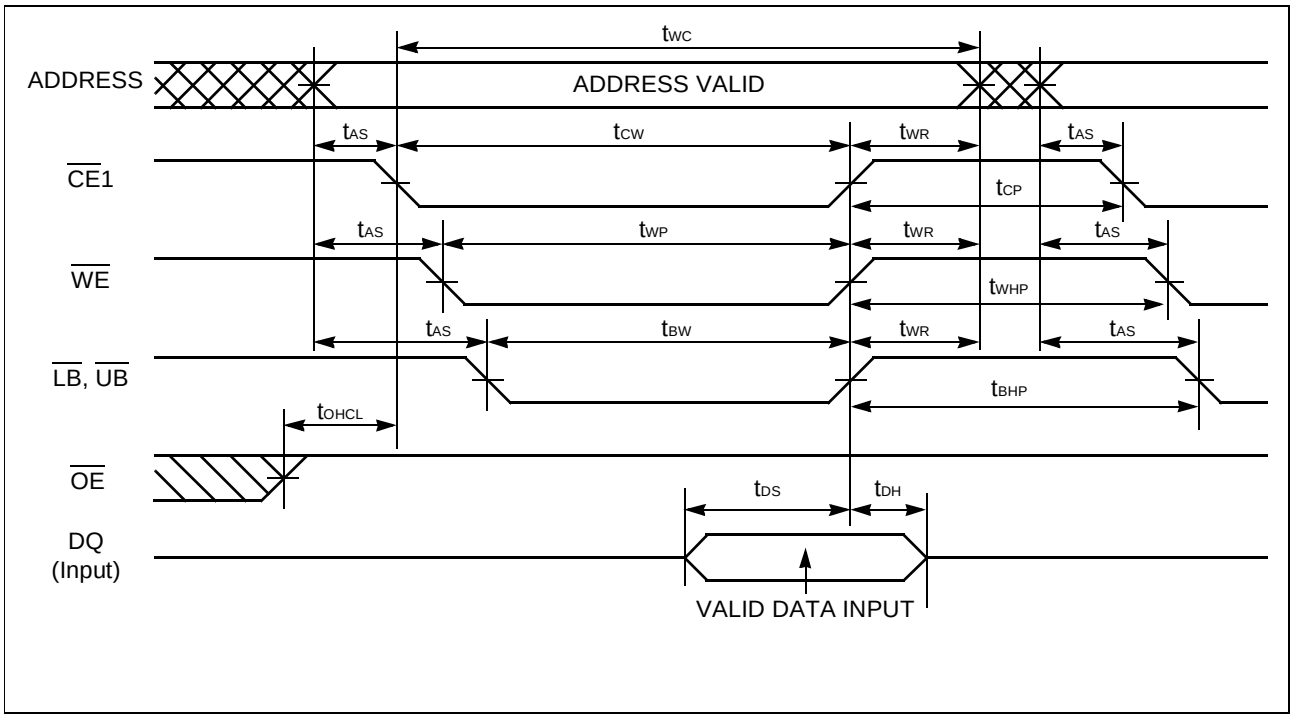
READ Timing #3 ($\overline{LB}$ / $\overline{UB}$ Byte Access) See Note.



Note: This timing diagram assumes CE2=H and $\overline{WE}$=H.

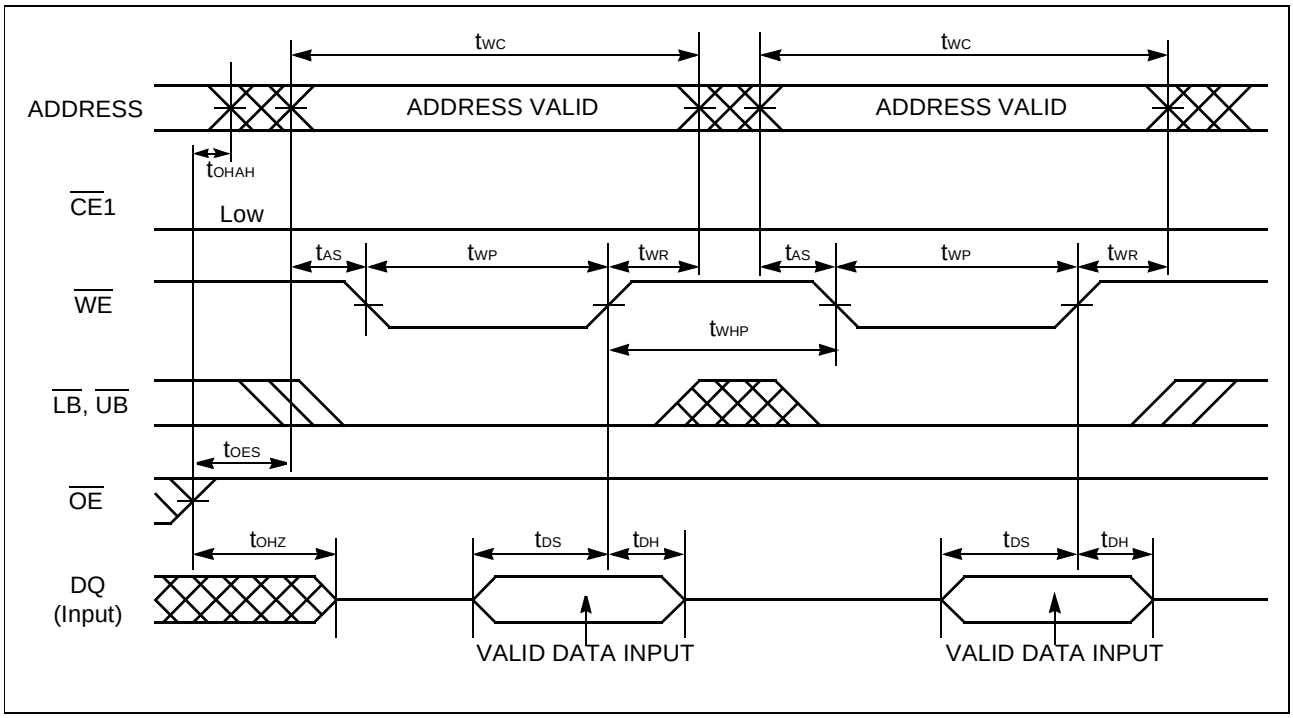
■ TIMING DIAGRAMS (Continued)

WRITE Timing #1 (Basic Timing) See Note.



Notes: This timing diagram assumes CE2=H.

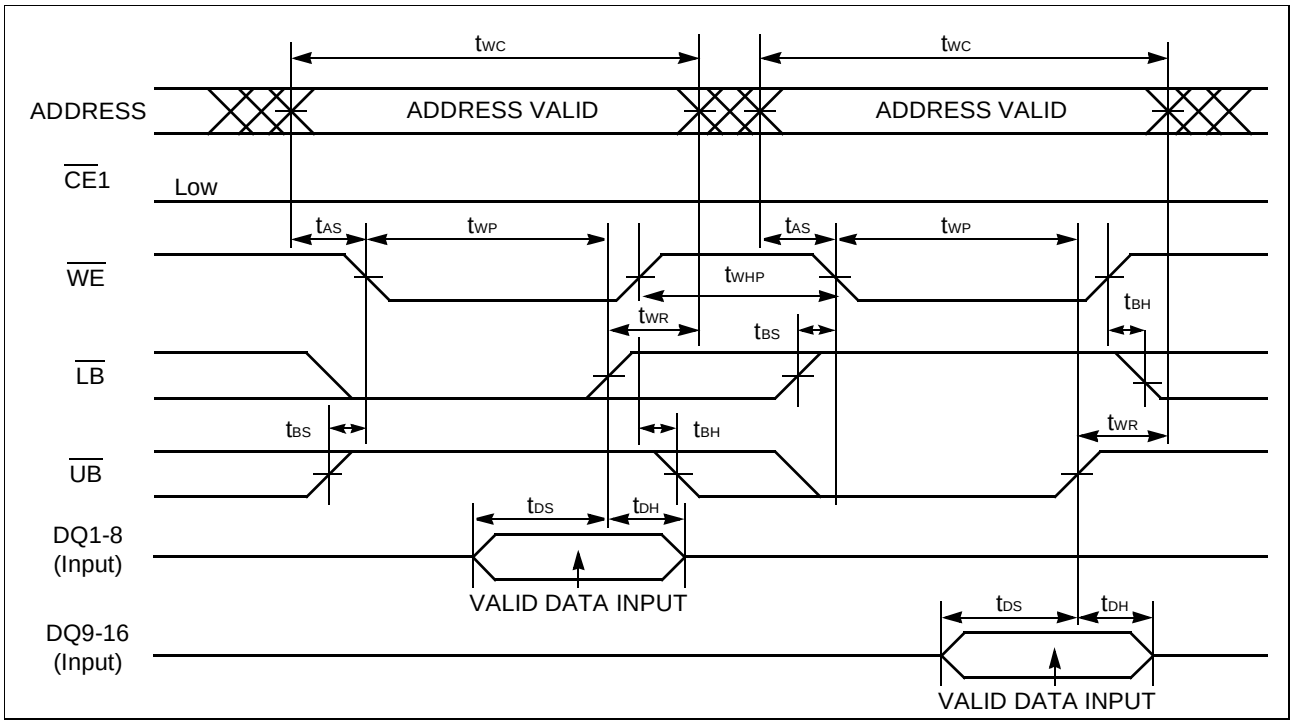
WRITE Timing #2 (WE Control) See Note.



Note: This timing diagram assumes CE2=H.

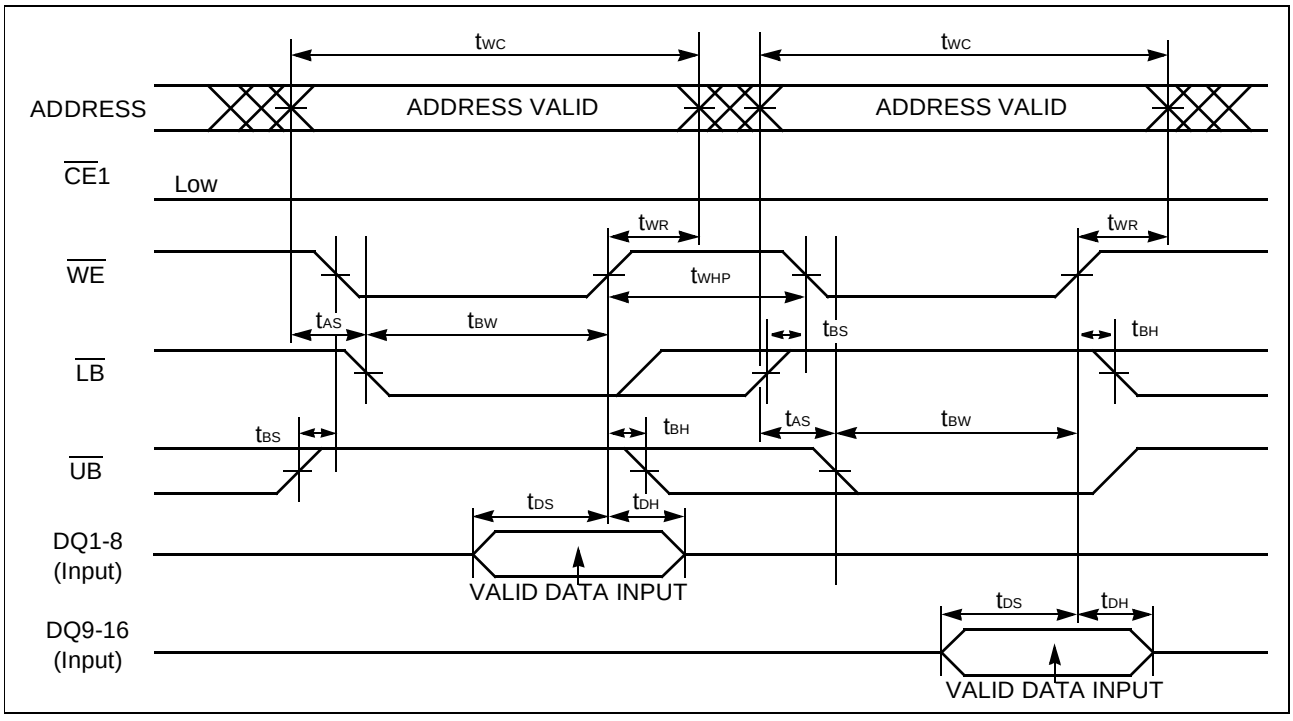
■ TIMING DIAGRAMS (Continued)

WRITE Timing #3-1 ($\overline{WE}$ / $\overline{LB}$ / $\overline{UB}$ Byte Write Control) See Note.



Note: This timing diagram assumes CE2=H and $\overline{OE}$=H.

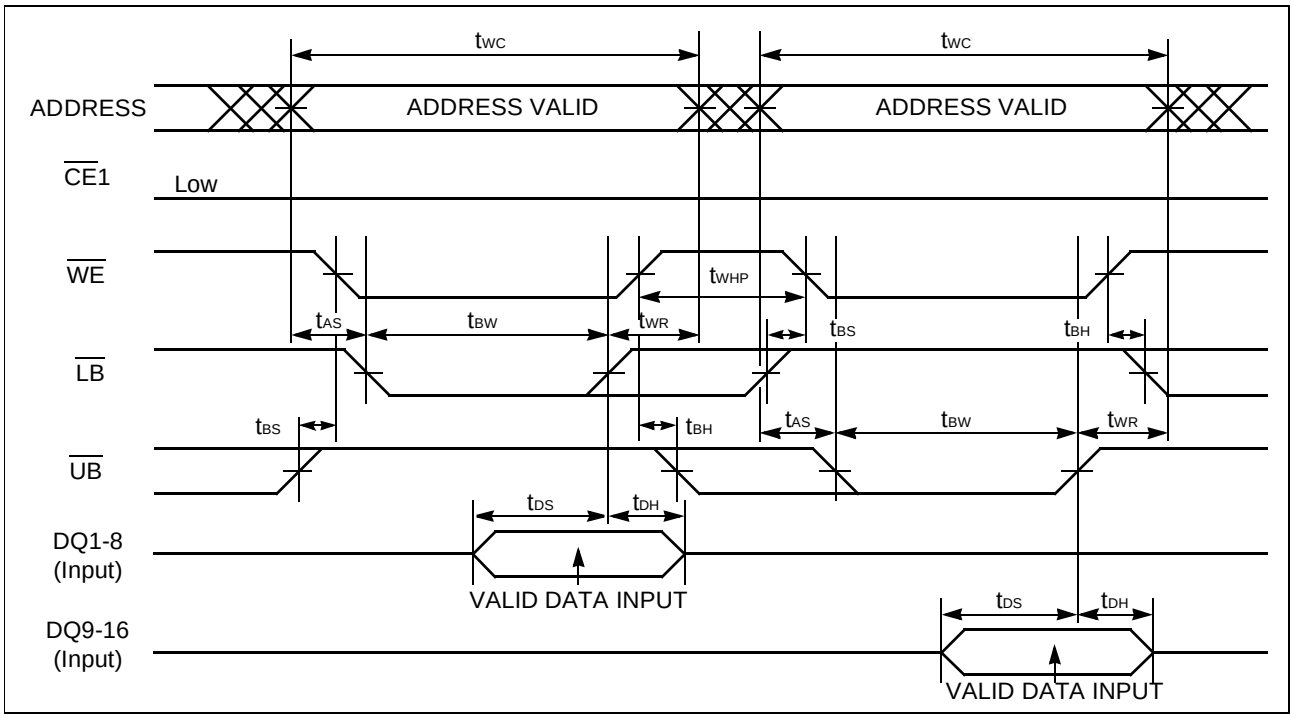
WRITE Timing #3-2 ($\overline{WE}$ / $\overline{LB}$ / $\overline{UB}$ Byte Write Control) See Note.



Note: This timing diagram assumes CE2=H and $\overline{OE}$=H.

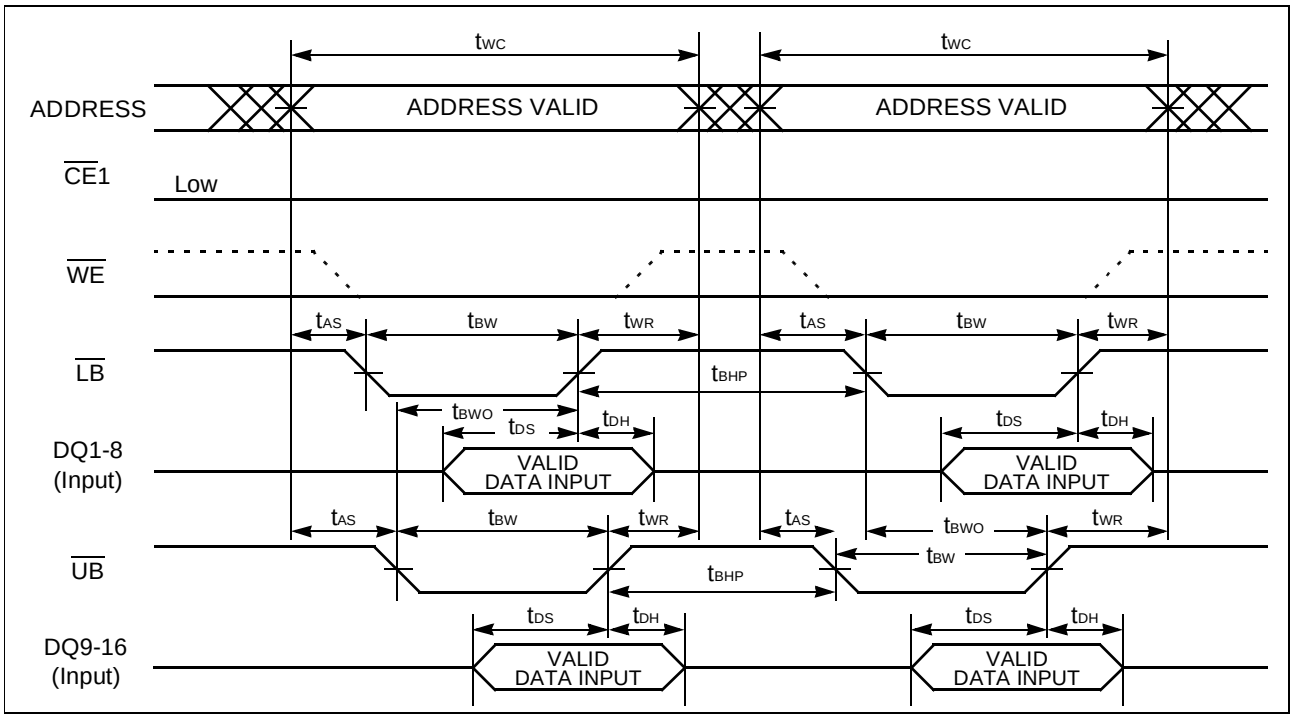
■ TIMING DIAGRAMS (Continued)

WRITE Timing #3-3 ($\overline{WE}$ / $\overline{LB}$ / $\overline{UB}$ Byte Write Control) See Note.



Note: This timing diagram assumes CE2=H and $\overline{OE}$=H.

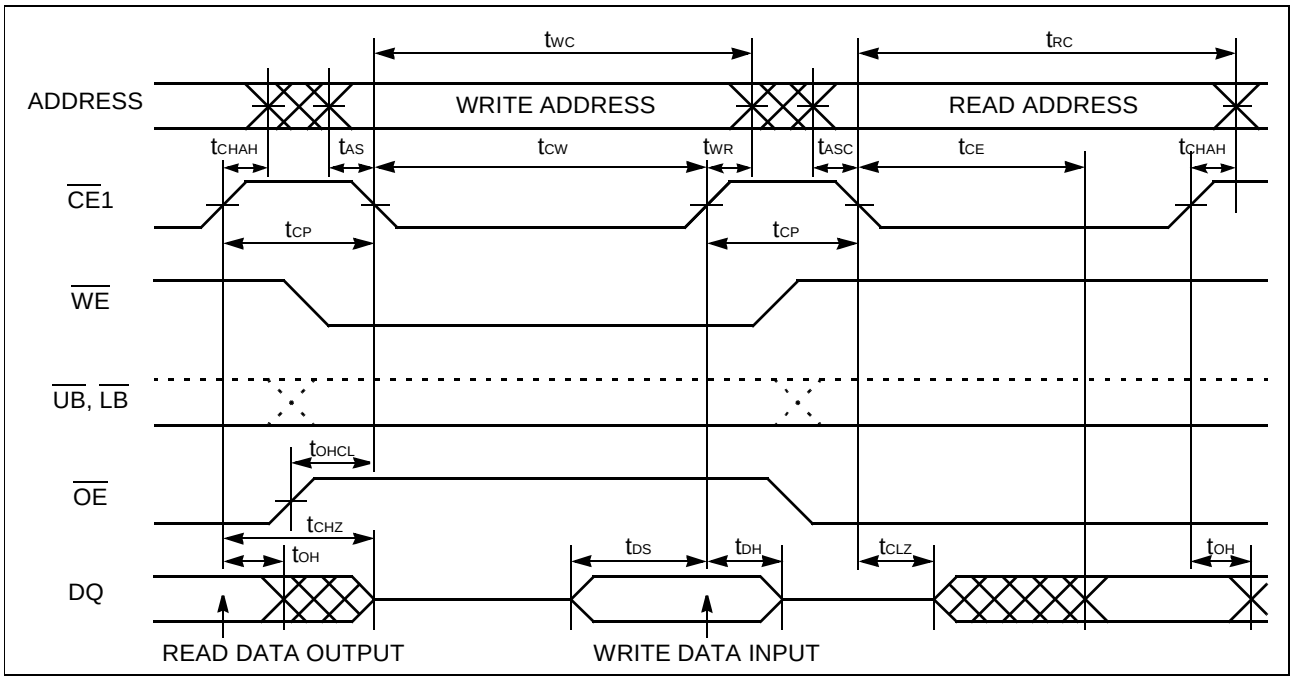
WRITE Timing #3-4 ($\overline{WE}$ / $\overline{LB}$ / $\overline{UB}$ Byte Write Control) See Note.



Note: This timing diagram assumes CE2=H and $\overline{OE}$=H.

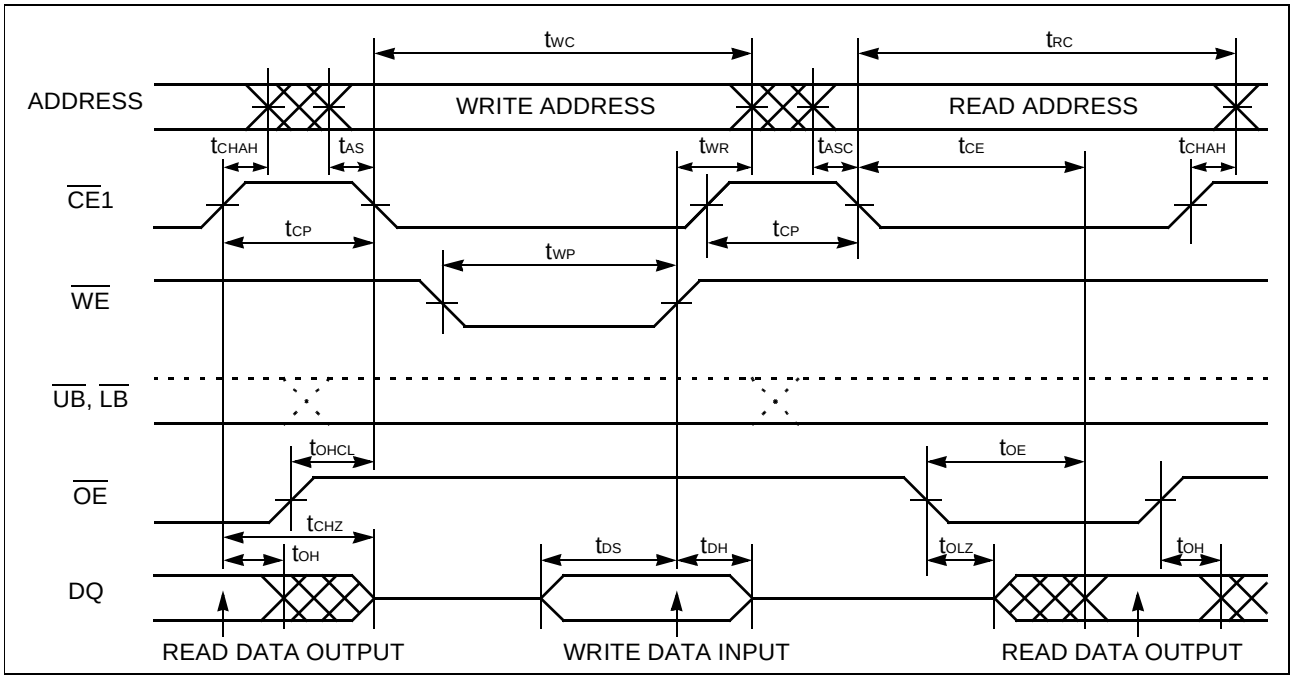
■ TIMING DIAGRAMS (Continued)

READ / WRITE Timing #1-1 ($\overline{CE}$1 Control) See Note.



Notes *1: This timing diagram assumes CE2=H.
*2: Write address is valid from either $\overline{CE}$1 or $\overline{WE}$ of last falling edge.

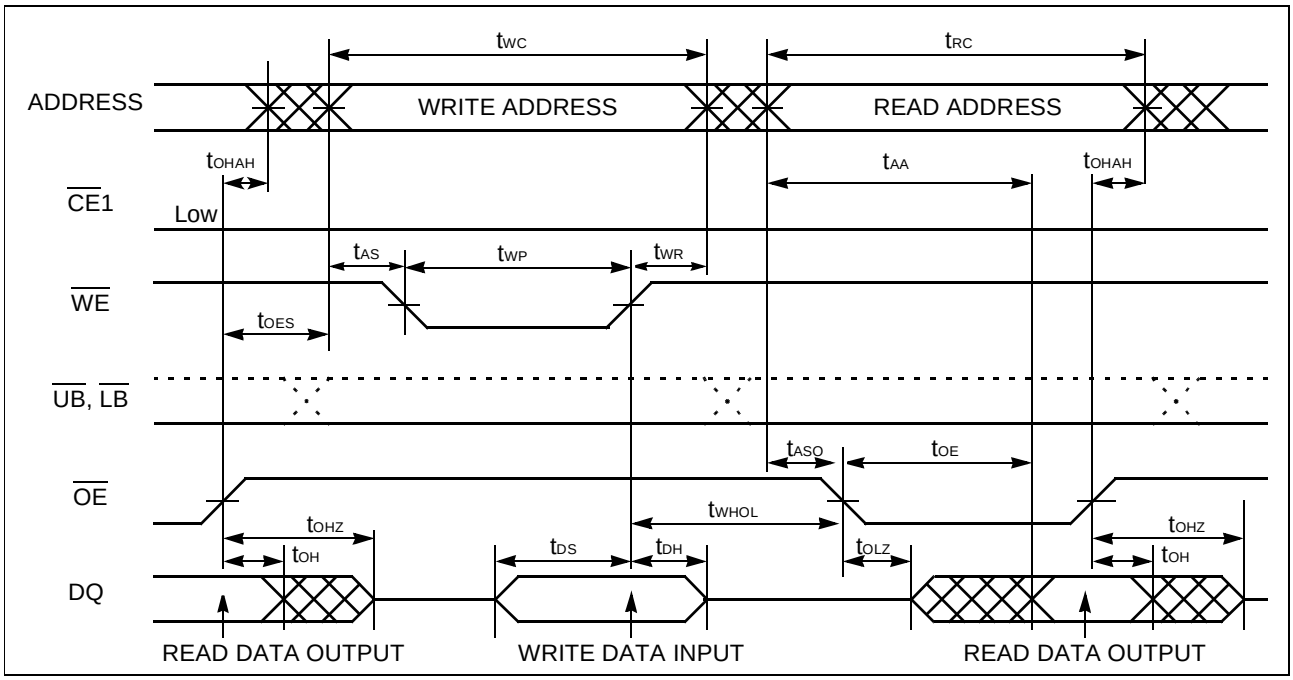
READ / WRITE Timing #1-2 ($\overline{CE}$1 / $\overline{WE}$ / $\overline{OE}$ Control) See Note.



Notes *1: This timing diagram assumes CE2=H.
*2: $\overline{OE}$ can be fixed Low during write operation if it is $\overline{CE}$1 controlled write at Read-Write-Read sequence.

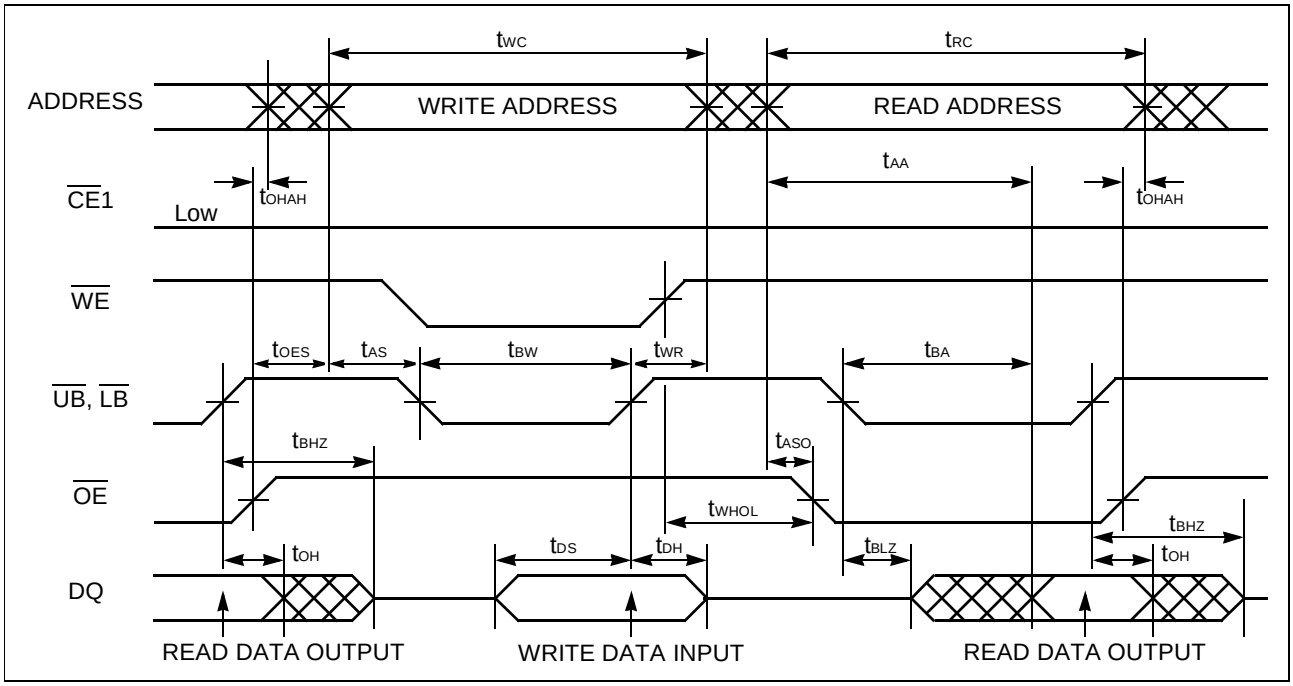
■ TIMING DIAGRAMS (Continued)

READ / WRITE Timing #2 ($\overline{OE}$, $\overline{WE}$ Control) See Note.



Notes *1: This timing diagram assumes CE2=H.
*2: $\overline{CE}$1 can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.

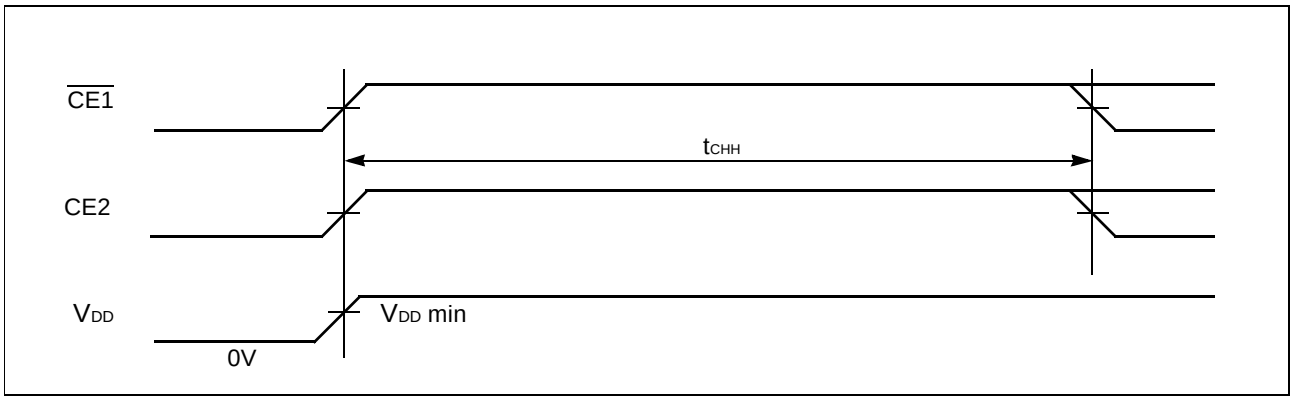
READ / WRITE Timing #3 ($\overline{OE}$, $\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Control) See Note.



Notes *1: This timing diagram assumes CE2=H.
*2: $\overline{CE}$1 can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.

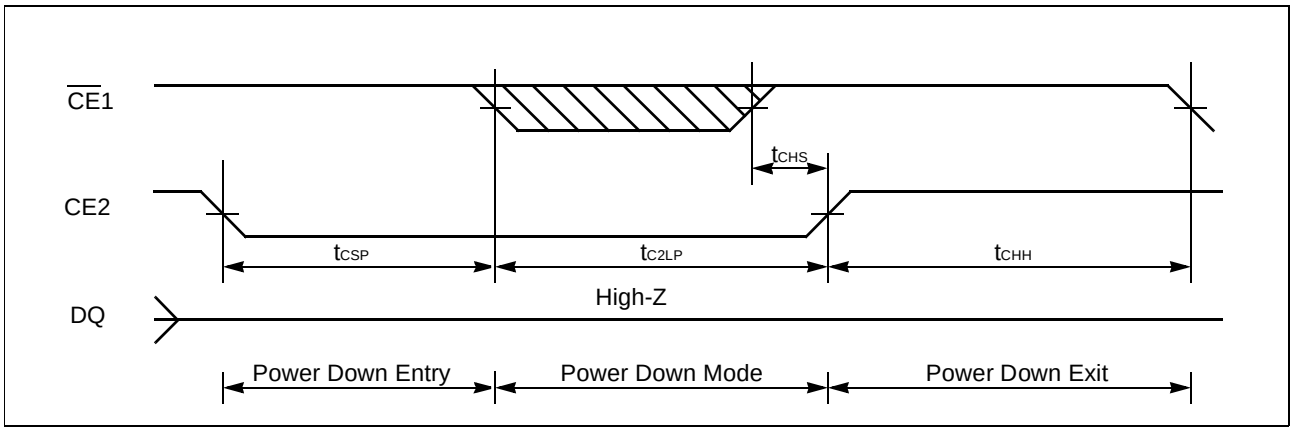
■ TIMING DIAGRAMS (Continued)

POWER-UP Timing See Note.



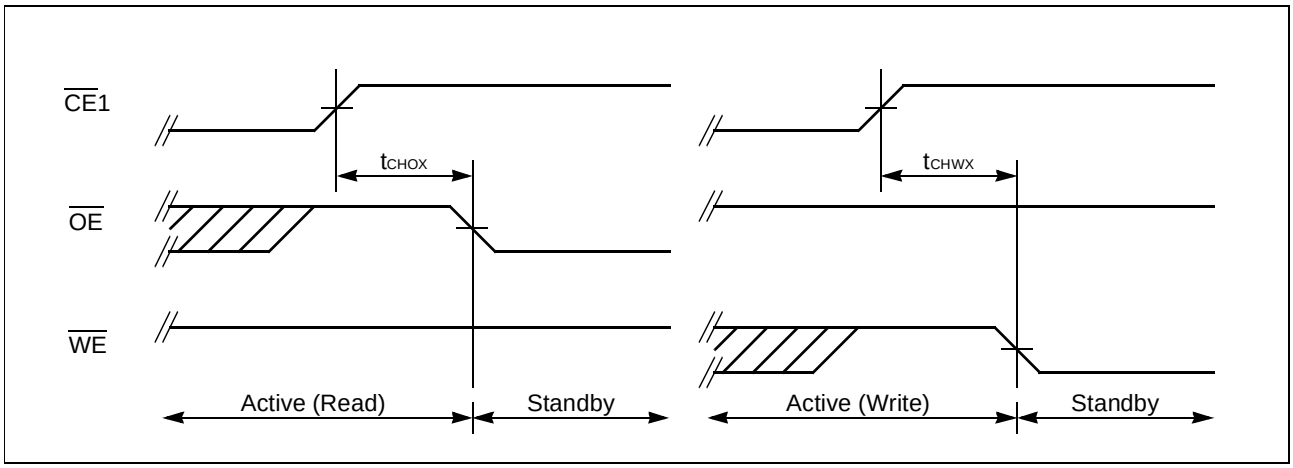
Note: The t_{CHH} specifies after V_{DD} reaches specified minimum level and applicable both $\overline{CE1}$ and CE2.

POWER DOWN Entry and Exit Timing See Note.



Note: This Power Down mode can be also used as a reset timing if POWER-UP timing above could not be satisfied and Power-Down program was not performed prior to this reset.

Standby Entry Timing after Read or Write See Note.



Note: Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode.
If either of timing is not satisfied, it takes t_{RC} (min) period for Standby mode from $\overline{CE1}$ Low to High transition.

■ BONDING PAD

Bonding Pad Layout

Please contact local FUJITSU representative for pad layout and pad coordinate information.

Bonding Pad Description

Pin Name	Description
A_{19} to A_0	Address Input
$\overline{CE}1$	Chip Enable (Low Active)
CE2	Chip Enable (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{UB}$	Upper Byte Control (Low Active)
$\overline{LB}$	Lower Byte Control (Low Active)
DQ_{16-9}	Upper Byte Data Input/Output
DQ_{8-1}	Lower Byte Data Input/Output
V_{DD}	Power Supply
V_{SS}	Ground
TEST/OPEN	Test/Open (This pad should be left open. Do not use.)

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