MOTOROLA
Semiconductor Technical Data

Order Number: MC33889/D
Rev. 5.0, 08/2001

Advance Information

System Basis Chip With Low Speed Fault Tolerant CAN Interface

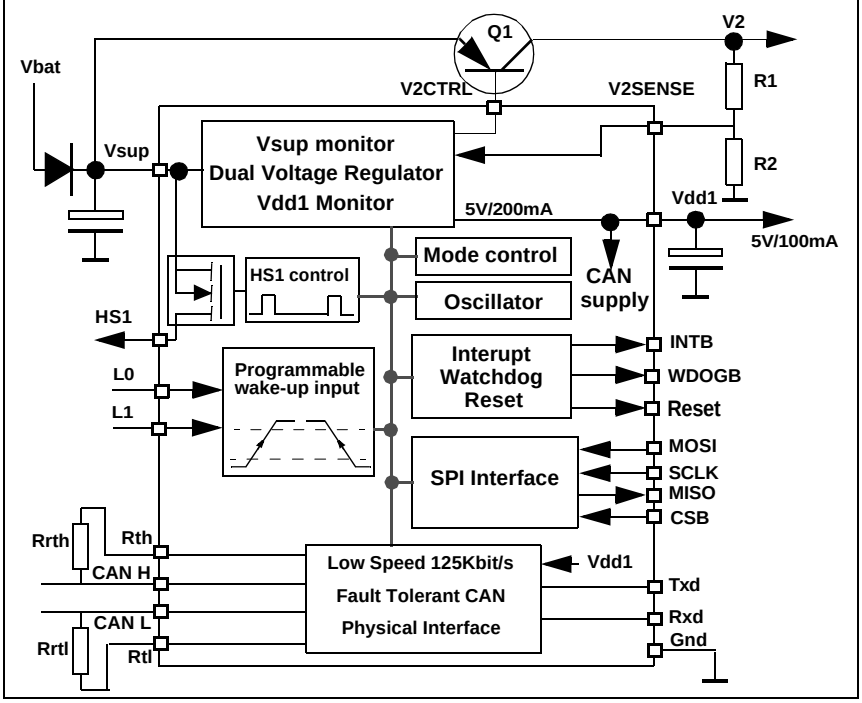
MC33889

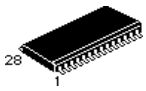
System Basis Chip

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC33889 is a monolithic integrated circuit combining many functions frequently used by automotive ECUs. It incorporates a low speed fault tolerant CAN physical inteface.

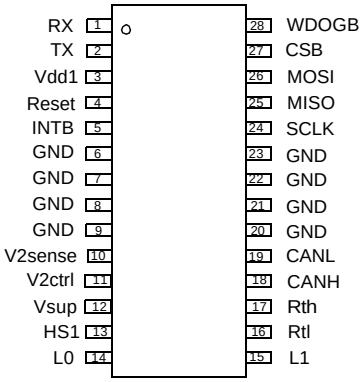
Main features:
• Vdd1: Low drop voltage regulator, current limitation, over temperature detection, monitoring and reset function. Total current capability 200mA (100mA for CAN current plus 100mA for MCU and external peripheral components).
• V2: control circuitry for external bipolar ballast transistor for high flexibility in choice of peripheral voltage and current supply.
• Four operational modes: normal, stand-by, stop and sleep modes.
• Low stand-by current consumption in stop and sleep modes
• Built in Low speed 125KBaud fault tolerant CAN physical interface, compatible with Motorola MC33388.
• External high voltage wake-up input, associated with HS1 Vbat switch
• 150mA output current capability for HS1 Vbat switch allowing drive of external switches pull up resistors or relays
• Vsup monitoring and failure detection
• DC Operating voltage from 5 to 27V
• 40V maximum transient voltage
• Programmable software time out and window watchdog
• Separate outputs for Watchdog time out signla (WDOGB) and Reset (Reset).
• Wake up capabilities: wake up input, programmable cyclic sense, forced wake up, CAN interface and SPI (CSB pin).
• Interface with MCU through 4 Mhz SPI.
• SO28WB package with thermal enhanced lead frame.





DW SUFFIX
PLASTIC PACKAGE
CASE
SO-28

PIN CONNECTIONS



(Top view)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
None	T_A = -40 to 125°C	SO-28

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA digital dna™

1 MAXIMUM RATINGS

Ratings	Symbol	Min	Typ	Max	Unit
ELECTRICAL RATINGS					
Supply Voltage at Vsup - Continuous voltage - Transient voltage (Load dump)	 Vsup Vsup	 -0.3		 27 40	V
Logic Inputs (Rx, Tx, MOSI, MISO, CSB, SCLK, Reset, WDOGB, INTB)	Vlog	- 0.3		Vdd1+0.3	V
Output current Vdd1	I		Internally limited		A
HS1 - voltage - output current	 V I	 -0.3	 Internally limited	 Vsup+0.3	 V A
ESD voltage (HBM 100pF, 1.5k) - CANL, CANH, Rtl, Rth, HS1, L0, L1 - All other pins	Vesdh	 -4 -2		 4 2	kV
ESD voltage (Machine Model) All pins	Vesdm	200		200	V
L0, L - DC Input voltage - DC Input current - Transient input current (according to ISO7637 specification) and with external component tbd.	Vwu DC	 -0.3 -2 tbd		 40 2 tbd	 V mA mA
CAN related pins: CANH, CANL, RTL, RTH, Tx, Rx (refer to CAN section)					
THERMAL RATINGS					
Junction Temperature	T_j	- 40		+150	°C
Storage Temperature	T_s	- 55		+165	°C
Ambient Temperature (for info only)	T_a	- 40		+125	°C
Thermal resistance junction pin	Rthj/p			20	°C/W

2 ELECTRICAL CHARACTERISTICS

(V_{sup} From 5.5V to 18V and T_j from -40°C to 150°C) unless otherwise noted. For all pins except can related pins

Description	Symbol	Characteristics			Unit	Conditions
		Min	Typ	Max		
Vsup pin (Device power supply)						
Nominal DC Voltage range	Vsup	5.5		18	V	
Extended DC Voltage range 1	Vsup-ex1	4.5		5.5	V	Reduced functionality (note 1)
Extended DC Voltage range 2	Vsup-ex2	18		27	V	(note 3)
Input Voltage during Load Dump	VsupLD			40	V	Load dump situation
Input Voltage during jump start	VsupJS			27	V	Jump start situation
Supply Current in Sleep Mode (note 2,4)	Isup (sleep1)		45	65	µA	Vdd1 & V2 off, Vsup<12V, oscillator running (note 5) excluding CAN current
Supply Current in Sleep Mode (note 2,4)	Isup (sleep2)		25	40	µA	Vdd1 & V2 off, Vsup<12V oscillator not running (note5) excluding CAN current,
Supply current in sleep mode (note 2,4)	Isup (sleep3)			150	µA	Vdd1 & V2 off, Vsup>12V oscillator running (note 5) excluding CAN current
Supply Current in Stand-by Mode (note 2,4)	Isup(stdby)			15	mA	Iout at Vdd1 =10mA, CAN recessive state or disabled
Supply Current in Normal Mode (note 2)	Isup(norm)			15	mA	Iout at Vdd1 =10mA, CAN recessive state or disabled
Supply Current in Stop mode (note 2,4) I out Vdd1 <2mA	Isup (stop1)			85	µA	Vdd1 on (note 6), Vsup<12V oscillator running (note 5) excluding CAN current,
Supply Current in Stop mode (note 2,4) Iout Vdd1 < 2mA	Isup (stop2)			60	µA	Vdd1 on (note 6), Vsup<12V oscillator not running (note 5) excluding CAN current
Supply Current in Stop mode (note 2,4) Iout Vdd1 < 2mA	Isup (stop2)			180	µA	Vdd on (note6), Vsup>12 oscillator running (note 5) excluding CAN current
Supply Fail Flag internal threshold	Vthresh	1.5	3	4	V	
Supply Fail Flag hysteresis	Vdet hyst		1		V	

note 1: Vdd1>4V, reset high, logic pin high level reduced, device is functional.
note 2: current measured at Vsup pin.
note 3: Device is fully functional. All modes available and operating, Watchdog, HS1 turn ON turn OFF, CAN cell operating, L0 and L1 input operating, SPI read write operation. Over temperature may occur.
note 4: Excluding the CAN cell current. An additional 30uA typical must be added to specified value.
note 5: Oscillator running means “Forced Wake Up” or “Cyclic Sense” or “Software Watchdog” timer activated.
note 6: Vdd is ON with2mA typical output current capability.

Vdd1 (external 5V output for MCU supply and internal CAN physical interface supply).
Idd1 is the total regulator output current. Iddcan is the internal CAN block supply current. Iout is Vdd1 external output current.
Idd1 = Iddcan + Iout.
Vdd specification with external capacitor C>1uF and ESR<1O ohm. No tantalum capacitor required.

Vdd1 Output Voltage	Vdd1out	4,9	5	5,1	V	Idd1 from 2 to 200mA 5.5V< Vsup <27V
Vdd1 Output Voltage	Vdd1out	4			V	Idd1 from 2 to 200mA 4.5V< Vsup <5.5V
Drop Voltage Vsup>Vddout	Vdd1drop		0.2	0,5	V	Idd1 = 200mA
Idd1 Current (Idd1 = Iddcan + Iout)	Idd1	200	270	350	mA	Internally limited Included Internal CAN current consumption
Vdd1 Output Voltage in stop mode	Vddstop	4,75	5,00	5,25	V	Iout < 2mA
Thermal Shutdown	Tsd	160		190	°C	

(V_{sup} From 5.5V to 18V and T_j from -40°C to 150°C) unless otherwise noted. For all pins except can related pins

Description	Symbol	Characteristics			Unit	Conditions
		Min	Typ	Max		
Over temperature pre warning	Tpw	130		160	°C	
Temperature Threshold difference	Tsd-Tpw	20		40	°C	
Reset threshold 1	Rst-th1	4.3	4.5 V	4.7		Selectable by SPI. Default value after reset.
Reset threshold 2	Rst-th2	3.6	3.8	4		Selectable by SPI
Reset duration	reset-dur	1		2	ms	
Vdd1 range for Reset Active	Vdd_r	1			V	
Reset Delay Time	t_d	5		20	µs	
Line Regulation	LR1		5	25	mV	9V<V_{sup}<18, I_{dd}=10mA
Line Regulation	LR2		10	25	mV	5.5V<V_{sup}<27V, I_{dd}=10mA
Load Regulation	LD		20	50	mV	1mA<I_{Idd}<200mA
Thermal stability	ThermS		5		mV	Vsup=13.5V, I=100mA

V2 adjustable output voltage regulator

note 8: V2 specification with external capacitor

- option 1: C>22uF and ESR<1O ohm, (no tantalum capacitor required)
- option2: C>1uF and ESR<10 ohm, (no tantalum capacitor required). In this case depending upon ballast transistor gain an additional resistor and capacitor network between emitter and base of PNP ballast transistor might be required (ex C=10nF).

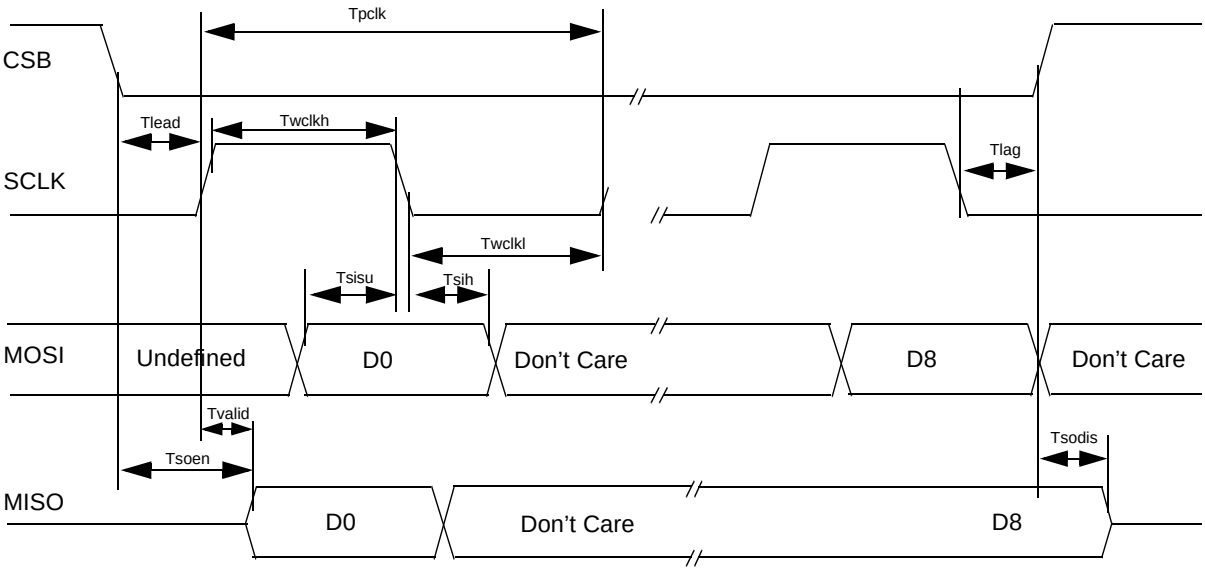
note 7 : Subject to external R1 and R2 resistors tolerances.

V2 Output Voltage (note 7)	V2	4,9	5	5,1	V	I2 from 2 to 200mA 5.5V< Vsup <27V
I2 output current (for information only)	I2	200			mA	Depending upon external ballast transistor
V2 sense reference voltage	V2sref		1.25		V	
V2 ctrl current	I2ctrl		10		mA	
Vdd2 to Vdd1 matching	Vmatch	0.5		0.5	%	excluding external component matching
Logic output pins (MISO)						
Low Level Output Voltage	Vol			1.0	V	I out = 1.5mA
High Level Output Voltage	Voh	Vdd1-0.9			V	I out = -250uA
Tristated MISO Leakage Current		-2		+2	µA	0V<V_{miso}<Vdd
Logic input pins (MOSI, SCLK, CSB)						
High Level Input Voltage	Vih	0.7Vdd1		Vdd1+0.3 V		
Low Level Input Voltage	Vil	-0.3		0.3Vdd1	V	
High Level Input Current on CSB	Iih	-20		-100	µA	V_i=4V
Low Level Input Current CSB	Iil	-20		-100	µA	V_i=1V
MOSI, SCLK Input Current	Iin	-10		10	µA	0<V_{IN}<Vdd
Reset Pin (output pin only)						
High Level Output current	Iol		-30		µA	0<V_{out}<0.7Vdd
Low Level Output Voltage (I_0=1.5mA)	Vol	0		0.9	V	1v<V_{sup}<27V
Reset pull down current	Ipdw	3		5	mA	
Reset Duration after Vdd High	reset-dur	1		2	ms	
Wdogb output pin						
Low Level Output Voltage (I_0=1.5mA)	Vol	0		0.9	V	1v<V_{sup}<27V
High Level Output Voltage (I_0=-250uA)	Voh	Vdd1-0.9				
INT Pin						
Low Level Output Voltage (I_0=1.5mA)	Vol	0		0.9	V	
High Level Output Voltage (I_0=-250uA)	Voh	Vdd1-0.9				
HS1: 150mA High side output pin						

(V_{sup} From 5.5V to 18V and T_j from -40°C to 150°C) unless otherwise noted. For all pins except can related pins

Description	Symbol	Characteristics			Unit	Conditions
		Min	Typ	Max		
Rdson at Tj=25°C, and Iout -150mA	Rdson25			2.5	Ohms	Vsup>9V
Rdson at Tj=150°C, and Iout -150mA	Rdson150			5	Ohms	Vsup>9V
Output current limitation	Ilim	200		500	mA	
Over temperature Shutdown	Ovt	155		190	°C	
Leakage current	Ileak			10	uA	
Output Clamp Voltage at Iout= -1mA	Vcl	-0.5		-2	V	no inductive load drive capability
Cyclic sense period (refer to SPI)	T1				ms	in sleep and stop modes
Cyclic sense On time (refer to SPI)	T2		300		us	in sleep and stop modes
Timing accuracy (cyclic sense peiord and on time)	Tacc	-30		+30	%	in sleep and stop mode
L0 and L1 inputs						
Negative Switching Threshold	Vthn	2.5	3	3.5	V	5.5V<Vsup<18V
Positive Switching Threshold	Vthp	3	3.7	4.5	V	5.5V<Vsup<18V
Hysteresis	Vhyst	0.7		1.3	V	5.5V<Vsup<18V
Input current	Iin	-10		10	uA	-0.3V < Vin < 40V
Wake up Filter Time		8	20	38	µs	
DIGITAL INTERFACE TIMING						
SPI operation frequency	Freq			4	MHz	
SCLK Clock Period	t_{pCLK}	250			ns	
SCLK Clock High Time	t_{wSCLKH}	125			ns	
SCLK Clock Low Time	t_{wSCLKL}	125			ns	
Falling Edge of CS to Rising Edge of SCLK	t_{lead}	100	50		ns	
Falling Edge of SCLK to Rising Edge of CS	t_{lag}	100	50		ns	
MOSI to Falling Edge of SCLK	t_{SISU}	40	25		ns	
Falling Edge of SCLK to MOSI	t_{SIH}	40	25		ns	
MISO Rise Time (CL = 220pF)	t_{rSO}		25	50	ns	
MISO Fall Time (CL = 220pF)	t_{fSO}		25	50	ns	
Time from Falling or Rising Edges of CS to: - MISO Low Impedance - MISO High Impedance	 t_{SOEN} t_{SODIS}			 50 50	ns	
Time from Rising Edge of SCLK to MISO Data Valid	t_{valid}			50		0.2 V1≤SO≥ 0.8V1, C_L=200pF

Figure 1. Timing Characteristics



3 CAN MODULE SPECIFICATION (COMPATIBLE WITH MC33388)

ELECTRICAL RATINGS

Ratings	Symbol	Min	Typ	Max	Unit
DC Voltage On Pins Tx, Rx	Vlogic	-0.3		V_{DD1} + 0.3	V
DC Voltage On Pins CANH, CANL	V_{BUS}	-20		+27	V
Transient Voltage At Pins CANH, CANL $0 < V_{DD} < 5.5V$; $V_{sup} \geq 0$; $T < 500ms$	V_{CANH}/V_{CANL}	-40		40	V
Transient Voltage On Pins CANH, CANL (Coupled Through 1nF Capacitor)	V_{tr}	-150		100	V
DC Voltage On Pins Rth, Rtl	V_{rtl}, V_{rth}	-0.3		+27	V
Transient Voltage At Pins RtH, RtL $0 < V_{DD} < 5.5V$; $V_{sup} \geq 0$; $T < 500ms$	V_{RtH}/V_{RtL}	-0.3		40	V
RTH, RTL Termination Resistance	R_t	500		16000	Ω

ELECTRICAL CHARACTERISTICS (V_{sup} From 5.5V to 18V and T_j from -40°C to 150°C unless otherwise noted).

Conditions	Symbol	Min	Typ	Max	Unit
Supply current described below are the CAN module internal supply current from VDd and Vsup					
Internal Vdd Supply Current (CAN and SBC in Normal Mode). TX= VDD, CAN in Recessive State	$I_{VDD1\text{-}int}$		2.3	3	mA
Internal Vdd Supply Current (CAN and SBC in Normal Mode). TX = 0V, No Load, CAN in Dominant State	$I_{VDD1\text{-}int}$		3.3	5	mA
Vsup Supply Current (CAN and SBC in Normal Mode). TX = VDD	$I_{sup\text{-}int}$		150	300	µA
Total Supply Current (CAN in Receive Only Mode, SBC in Normal mode). VDD = 5V ; V_{sup} = 12V	$I_{VDD1\text{-}int} + I_{BAT\text{-}int}$		0.85	1.2	mA
Total Supply Current (CAN in Bus Standby Mode, SBC in normal mode). VDD = 5V ; V_{sup} = 12V	$I_{VDD1\text{-}int} + I_{BAT\text{-}int}$		20	40	µA
Vbat Supply Current (CAN in Bus Standby mode) VDD = 0V ; V_{sup} = 12V	I_{BAT}		15	25	µA
TX Pin					
High Level Input Voltage	V_{ih}	$0.7*V_{DD1}$		V_{DD1}+0.3V	V
Low Level Input Voltage	V_{il}	-0.3		$0.3 * V_{DD}$	V
TX High Level Input Current (V_i = 4V)	I_{TX}	-25	-80	-200	µA
TX Low Level Input Current (V_i = 1V)	I_{TX}	-100	-320	-800	µA

Conditions	Symbol	Min	Typ	Max	Unit
RX Pin					
High Level Output Voltage RX (I_0 = -250µA)	V_{oh}	V_{DD1} - 0.9		V_{DD1}	V
Low Level Output Voltage (I_0 = 1.5mA)	V_{ol}	0		0.9	V
CANH, CANL Pins					
Differential Receiver, Recessive To Dominant Threshold (By Definition, V_{diff}=V_{CANH}-V_{CANL})	V_{diff1}	-3.2		-2.5	V
Differential Receiver, Dominant To Recessive Threshold (Bus Failures 1, 2, 5)	V_{diff2}	-3.2		-2.5	V
CANH Recessive Output Voltage TX = VDD ; $R_{(RTH)}$ < 4k	V_{CANH}			0.2	V
CANL Recessive Output Voltage TX = VDD ; $R_{(RTL)}$ < 4k	V_{CANL}	V_{DD1} - 0.2			V
CANH Output Voltage, Dominant TX = 0V; I_{CANH} = -40mA; Normal Operating Mode	V_{CANH}	V_{DD1} - 1.4			V
CANL Output Voltage, Dominant TX = 0V; I_{CANL} = 40mA; Normal Operating Mode	V_{CANL}			1.4	V
CANH Output Current (V_{CANH} = 0 ; TX = 0)	I_{CANH}	50	75	100	mA
CANL Output Current (V_{CANL} = 14V; TX = 0)	I_{CANL}	50	90	130	mA
Detection Threshold For Short-circuit To Battery Voltage (Normal Mode)	V_{CANH}, V_{CANL}	7.3	7.9	8.9	V
Detection Threshold For Short-circuit To Battery Voltage (Standby/Sleep Mode)	V_{CANH}	V_{BAT}/2 +3		V_{BAT} /2+5	V
CANH Output Current (Sleep Mode; V_{CANH} = 12V, Failure3)			5	10	µA
CANL Output Current (Sleep Mode ; V_{CANL} = 0V ; V_{BAT} = 12V, Failure 4)	I_{CANL}		0	2	µA
CANL Wake Up Voltage Threshold	$V_{wake,L}$	2.5	3.3	3.9	V
CANH Wake Up Voltage Threshold	$V_{wake,H}$	1.2	2	2.7	V
Wake Up Threshold Difference (Hysteresis)	V_{wakeL}-V_{wakeH}	0.2			V
CANH Single Ended Receiver Threshold (Failures 4, 6, 7)	$V_{SE, CANH}$	1.5	1.85	2.15	V
CANL Single Ended Receiver Threshold (Failures 3, 8)	$V_{SE, CANL}$	2.8	3.05	3.4	V
CANL Pull Up Current (Normal Mode, Failures 4, 6 and 7)	$I_{CANL,pu}$	45	75	90	µA
CANH Pull Down Current (Normal Mode, Failure 3)	$I_{CANH,pd}$	45	75	90	µA
Receiver Differential Input Impedance CANH / CANL	R_{diff}	100		180	kΩ
Differential Receiver Common Mode Voltage Range	V_{com}	-10		10	V
CANH To Ground Capacitance	C_{CANH}			50	pF
CANL To Ground Capacitance	C_{CANL}			50	pF
C_{CANL} to C_{CANH} Capacitor Difference (Absolute Value)	DC_{can}			10	pF
RTH, RTL Pins					

Conditions	Symbol	Min	Typ	Max	Unit
RTL to VDD Switch On Resistance (I_{out} < -10mA; Normal Operating Mode)	R_{rtl}	10	30	50	Ω
RTL to BAT Switch Series Resistance (VBAT Standby Mode Or Sleep Mode)	R_{rtl}	8	12.5	20	kΩ
RTH To Ground Switch On Resistance (I_{out} <10mA; Normal Operating Mode)	R_{rth}	10	25	50	Ω

Thermal Shutdown

CAN Module Thermal Shutdown	T_{sd}		165		°C

AC CHARACTERISTICS (V_{sup} From 5.5V to 18V and T_j from -40°C to 150°C unless otherwise noted)

CANL and CANH Slew Rates (10% to 90%). Rising or Falling Edges. NOTE2.	T_{sl}	3.5	5	10	V/µs
Propagation Delay TX to RX Low. NOTE2.	T_{pdlow}		1	2	µs
Propagation Delay TX to RX High. NOTE2.	T_{pdhigh}		1	2	µs
Min. Dominant Time For Wake-up On CANL or CANH (Vbat Standby And Sleep Modes ; V_{BAT} = 12V)	T_{wake}	8	16	30	µs
Min. WAKE Time For Wake-up (Vbat Standby And Sleep Modes ; V_{BAT}= 12V)	T_{wake}	6	15	30	µs
Failure 3 Detection Time (Normal Mode)	T_{df3}	10		60	µs
Failure 6 Detection Time (Normal Mode)	T_{df6}	50		400	µs
Failure 3 Recovery Time (Normal Mode)	T_{dr3}	10		60	µs
Failure 6 Recovery Time (Normal Mode)	T_{dr6}	150		1000	µs
Failure 4, 7, 8 Detection Time (Normal Mode)	T_{df478}	0.75		4	ms
Failure 4, 7, 8 Recovery Time (Normal Mode)	T_{dr478}	10		60	µs
Failure 3, 4, 7,8 Detection Time (Vbat Standby And Sleep Modes ; V_{BAT} = 12V)	T_{dr347}	0.8		8	ms
Failure 3, 4, 7,8 Recovery Time (Vbat Standby And Sleep Modes ; V_{BAT} = 12V)	T_{dr347}		2.5		ms
Minimum Hold Time For “Go To Sleep” Command	T_{gts}	4		38	µs
Edge Count Difference Between CANH and CANL for Failures 1, 2, 5 Detection (NERR Becomes Low), (Normal Mode)	E_{cdf}		3		
Edge Count Difference Between CANH And CANL For Failures 1, 2, 5 Recovery (Normal Mode)	E_{cdr}		3		
TX Permanent Dominant Timer Disable Time (Normal Mode And Failure Mode)	$t_{TX,d}$	0.75		4	ms
TX Permanent Dominant Timer Enable Time (Normal Mode And Failure Mode)	$t_{TX,e}$	10		60	µs

NOTE:
1. When VBAT is greater than 18V, the wake up thresholds remain identical to the wake up thresholds at 18V.
2. AC Characteristics measured according to schematic figure 2.

Figure 2. fDevice Signal Waveforms

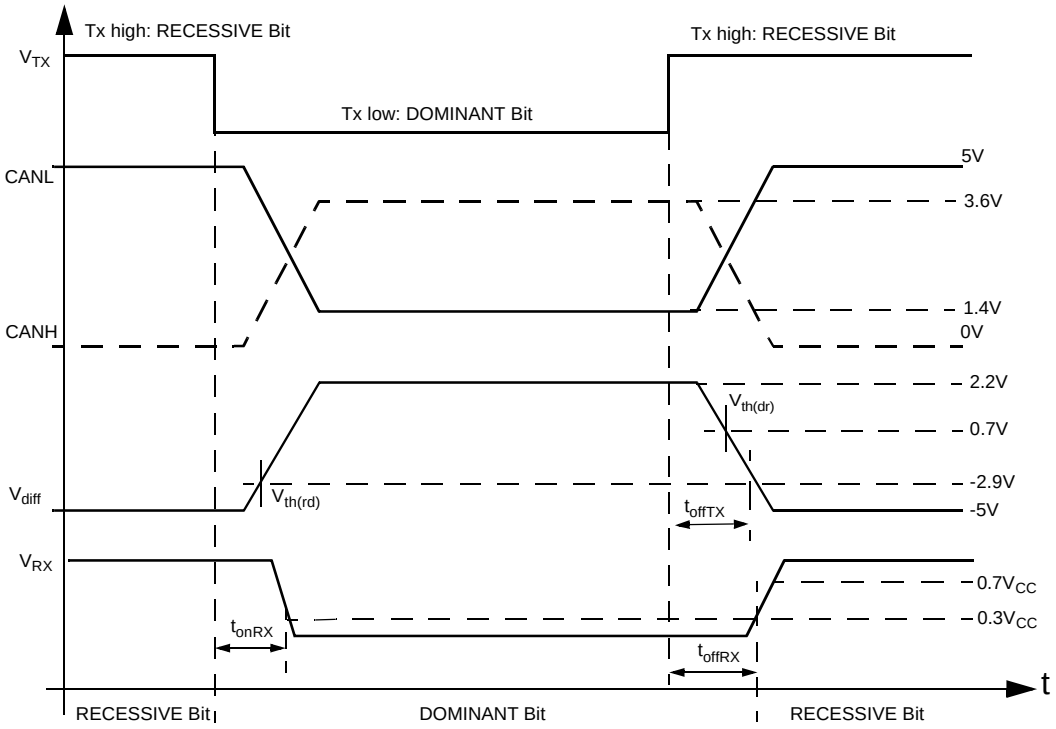
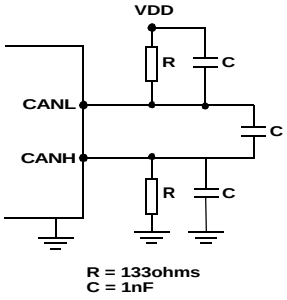


Figure 3. Test Circuit for AC Characteristics



4 DEVICE DESCRIPTION

Introduction:

The MC33889 is an integrated circuit dedicated to automotive applications. It includes the following functions:

- One full protected voltage regulator with 200mA total output current capability. Available output current is 100mA at Vdd1 external pin.
- Driver for external path transistor for V2 regulator function.
- Reset, programmable watchdog function
- Four operational modes
- Wake up capabilities: Forced wake up, cyclic sense and wake up inputs, CAN and SPI
- Can low speed fault tolerant physical interface, compatible with Motorola MC33388D.

4.1 Device Supply

The device is supplied from the battery line through the Vsup pin. An external diode is required to protect against negative transients and reverse battery. It can operate from 4.5V and under the jump start condition at 27V DC. This pin sustains standard automotive voltage conditions such as load dump at 40V. When Vsup falls below 3V typical the MC33989 detects it and store the information into the SPI register, in a bit called “BATFAIL”. This detection is available in all operation modes.

4.2 Vdd1 Voltage Regulator

Vdd1 Regulator is a 5V output voltage with total current capability of 200mA. As the V1 regulator supplies the CAN module, 100mA is available at the Vdd1 external outside the circuit. This Vdd1 regulator is normally used in the application for the main microcontroller supply. It includes a voltage monitoring circuitry associated with a reset function. The Vdd1 regulator is fully protected against over current, short-circuit and has over temperature detection warning flags and shutdown with hysteresis. Ouput current can be lower than 200mA due to limited thermal capability of the device once mounted on the printed circuit board.

4.3 V2 regulator

V2 Regulator circuitry is designed to drive an external path transistor in order to increase output current flexibility. Two pins are used: V2 sense and V2 ctrl. Output voltage can be adjusted by an external resistor bridge, in a range from 1.8 to 8V. Vsup must be greater than V2 regulator voltage + 1V.

Target ballast transistor is PNP MJD32C. Other PNP transistor might be used, however depending upon PNP gain an external resistor capacitor network might be connected between emitter and base of PNP.

4.4 HS1 Vbat Switch Output

HS1 output is a 2 ohms typical switch from Vsup pin. It allows the supply of external switches and their associated pull up or pull down circuitry, in conjunction with the wake up input pins for example. Output current is limited to 200mA and HS1 is protected against short-circuit and over temperature. HS1 output is controlled from the internal register and SPI. It can be activated at regular intervals in sleep mode thanks to internal timer. It can also be permanently turned on in normal or stand-by modes to drive external loads such as relays or supply peripheral components. In case of inductive load drice exetrnal clamp circuitry must be added.

4.5 Functional Modes

The device has four modes of operation, stand-by, normal, stop and sleep modes. All modes are controlled by the SPI. An additional temporary mode called “normal request mode” is automatically accessed by the device (refer to state machine) after wake up events. Special mode and configuration are possible for sofware application debug and flash memory programmation.

4.5.1 Normal mode:

In this mode both regulators are ON and this corresponds to the normal application operation. All functions are available in this mode (watchdog, wake up input reading through SPI, HS1 activation, CAN communication). The software watchdog is running and must be periodically cleared though SPI.

4.5.2 Standby mode:

Only the regulator 1 is ON. Regulator 2 is turned OFF by disabling the V2 ctrl pin. Same functions as in normal mode are available. The watchdog is running.

4.5.3 Sleep mode:

Regulators 1 and 2 are OFF. In this mode, the MCU is not powered. The sleep current from Vsup pin is less than 100uA (excluding CAN interface sleep current). In this mode, the device can be awakened internally by cyclic sense via the wake up inputs pins and HS1 output, from the forced wake function, the CAN physical interface, and SPI (CSB pin).

4.5.4 Stop mode

Regulator 2 is turned OFF by disabling the V2 ctrl pin. The regulator 1 is activated in a special low power mode which allow to deliver 2 mA. The objective is to maintain the MCU of the application supplied while it is turned into power saving condition (i.e stop or wait mode). In the stop mode, the device supply current from Vbat can be as low as 100uA (excluding CAN interface sleep current).

Stop mode is entered through SPI. Stop mode is dedicated to power the Microcontroller when it is in low power mode (stop, pseudo stop, wait etc.). In these mode the MCU supply current is less than 1mA. The MCU can restart its software application very quickly, without the complete power up and reset sequence.

When the application is in stop mode (both MCU and SBC), the application can wake up from the SBC side (ex cyclic sense, forced wake up, CAN message, wake up inputs) or the MCU side (key wake up etc.).

When Stop mode is selected by SPI, stop mode becomes active 20us after end of SPI message. The “go to stop” instruction must be the last instruction executed by the MCU before going to low power mode.

In stop mode the Software watchdog can be “running” or “not running” depending upon selection by SPI. Refer to SPI description, MCR register bit WDSTOP.

In stop mode, SBC wake up capability are identical as in sleep mode.

4.5.4.1 Stop mode: wake up from SBC side:

When application is in stop mode, it can wake up from the SBC side. When a wake up is detected by the SBC (ex CAN, Wake up input etc.) the SBC turns itself into Normal request mode. The wake up is signalled to the MCU through the INT pin. INT pin is pulled low for 10us and then returns high. Wake up event can be read through the SPI registers.

4.5.4.2 Stop mode: wake up from MCU side:

When application is in stop mode, the wake up event may come to the MCU. In this case the MCU has to signal to the SBC that it has to go into Normal mod in order for the Vdd1 regulator to be able to deliver full current capability. This is done by a low to high transisiton of the CSB pin. CSB pin low to high activation has to be done as soon as possible after the MCU.

Alternatively the L0 and L1 inputs can also be used as wake up from stop mode.

4.5.4.3 Software watchdog in stop mode:

If watchdog is enabled (register MCR, bit WDSTOP set), the MCU has to wake up independently of the SBC before the end of the SBC watchdog time. In order to do this the MCU has to signals the wake to the SBC through the SPI wake up (CSB pin low to high transition to activated SPI wake up). Then the SBC wakes up and jump into the normal request mode. MCU has to configured the SBC to go to either normal or standby mode. The MCU can then decide to go back again to stop mode.

If no MCU wakes up occurs within the watchdog timing, the SBC will activate the reset pin and jump into the normal request mode. The MCU can then be initialized.

4.5.5 Normal request mode:

This is a temporary mode automatically accessed by the device after a wake up event from sleep or stop mode or after device power up. In this mode the Vdd1 regulator is ON, V2 is off, the reset pin is high. As soon as the device enters the normal request mode an internal 400ms timer is started. During these 400ms the micro controller of the application must addressed the SBC via SPI and configure the watchdog register (TIM1 register). This is the condition for the SBC to leave the Normal request Mode and enter the Normal mode and to set the watchdog timer according to configuration done during the Normal Request mode.

If no SPI configuration occurs within the 400ms, two cases must be considered:

- The “BATFAIL flag” has not been cleared: in this case the SBC goes to reset mode for 1ms, then return to normal request mode. If no W/D configuration is done within 400ms, the SBC goes to reset again, then normal request etc.

- If the “BATFAIL flag” has been reset, the SBC will goes back to previous low power mode. For instance If SBC was in sleep mode prior to the wake up it returns to sleep mode and keep the same wake up event configuration.

If SBC was in stop mode, it return to stop mode and keep the same wake up event configuration.

After an SBC power up (Vsup rising from zero to nominal), and if BATFAIL flag is cleared (MCR register read) the default low power mode is sleep mode.

“BATFAIL flag” is a bit which is triggered when Vsup is below 3V. This bit is set into the MCR register. It is reset by MCR register read.

4.5.6 Reset and watchdog: mode1 and mode 2 (safe mode):

The watchdog and reset functions have two modes of operation: mode 1 and mode 2 (mode 2 is also called safe mode). These modes are independent of the SBC modes (Normal, stand-by, sleep, stop). Mode 1 or mode 2 selection is done through SPI (register MCR, bit SAFE). Default mode after reset is mode 1.

4.6 Internal Clock

The device has an internal clock used to generate all timings (reset, watchdog, cyclic wake up, filtering time etc....).

4.7 Reset pin

A reset output is available in order to reset the microcontroller. Two operation modes for the reset pin are available, mode 1 and mode 2 (refer to table for reset pin operation).

The reset cause when SBC is in mode 1 are:

- Vdd1 falling out of range: if Vdd1 fall below the reset threshold (parameter Rst-th), the reset pin is pull low until Vdd1 return to nominal voltage.

- Power on reset: at device power on or at device wake up from sleep mode, the reset is maintained low until Vdd1 is within its operation range.

- Watchdog time out: if the watchdog is not cleared the SBC will pull the reset pin low for the duration of the reset duration time (parameter: reset-dur).

In mode 2, the reset pin is not activated in case of watchdog time out. Refer to" table for reset pin operation"for mode detail.

For debug purposes at 25°C, reset pin can be shorted to 5V.

4.8 Software watchdog (selectable window or time out watchdog)

Software watchdog is used in the SBC normal and stand-by modes for the MCU monitoring. The watchdog can be either window or time out. This is selectable by SPI (register TIM, bit WDW). Default is window watchdog. The period for the watchdog is selectable by SPI from 5 to 400ms (register TIM, bits WDT0 and WDT1). When the window watchdog is selected, the closed window is the first half of the selected period, and the open window is the second half of the period. The watchdog can only be cleared within the open window time. An attempt to clear the watchdog in the closed window will generate a reset. Watchdog is cleared through SPI by addressing the TIM register.

Refer to" table for reset pin operation"for operation in mode 2.

4.9 Wake Up capabilities

Several wake-up capabilities are available for the device when it is in sleep or stop mode. When a wake up has occurred, the wake up event is stored into the WUR or CAN registers. The MCU can then access to the wake up source. The wake up options are selectable trough SPI while the device is in normal or standby mode and prior to go to enter low power mode (sleep or stop mode).

4.9.1 Wake up from wake up inputs (L0, L1) without cyclic sense:

The wake up lines are dedicated to sense external switches state and if changes occur to wake up the MCU (In sleep or stop modes). The wake up pins are able to handle 40V DC. The internal threshold is 3V typical and these inputs can be used as input port expander. The wake up inputs state can be read through SPI (register WUR).

4.9.2 Cyclic sense wake up (Cyclic sense timer and wake up inputs L0, L1)

The SBC can wake up upon state change of one of the wake up input lines (L0, L1) while the external pull up or pull down resistor of the switches associated to the wake up input lines are biased with HS1 Vsup switch. The HS1 switch is activated in sleep or stop mode from an internal timer. Cyclic sense and Forced wake up are exclusive. If Cyclic Sense is enabled the forced up can not be enabled.

4.9.3 Forced wake up

The SBC can wake up automatically after a pre determined time spent in sleep or stop mode. Forced wake up is enabled by setting bit FWU in LPC register. Cyclic sense and Forced wake up are exclusive. If Forced wake up is enabled the Cyclic Sense can not be enabled.

4.9.4 CAN wake up

The device can wake up from a CAN message. CAN wake up cannot be disabled.

4.9.5 SPI wake up

The device can wake up by the CSB pin in sleep or stop mode. Wake up is detetced by CSB pin transition from low to high level. In stop mode this correspond to the condition where MCU and SBC are both in Stop mode and when the application wake up events come through the MCU.

4.9.6 System power up

At power up the device automatically wakes up.

4.10 SPI

The complete device control as well as the status report is done through a 8 bits SPI interface. Refer to SPI paragraph.

4.11 CAN

The device incorporates a low speed fault tolerant CAN physical interface. Speed rate is up to 125kBauds. Its electrical parameters for the CANL, CANH, Rtl, Rth Rx and Tx pins are compatible with the MC33388D.

The state of the CAN interface is programmable through SPI.

4.12 Device power up

After device or system power up the SBC enter into "normal request mode".

4.13 Package and thermal consideration

The device is proposed in a standard surface mount SO28 package. In order to improve the thermal performances of the SO28 package, 8 pins are internally connected to the lead frame and are used for heat transfer to the printed circuit board.

4.14 Table 1: Reset and Wdogb operation. Mode1 and Mode2.

Table below is the reset and watchdog output mode of operation. Two modes (mode 1 and mode 2) are available and are selectable through the SPI, safe bit. Default operation after reset or power up is mode 1.

In both modes reset is active at device power up and wake up.

In mode 1: Reset is activated in case of Vdd1 fall or watchdog not triggered. Wdogb output is active low as soon as reset goes low and stays low as long as the watchdog is not properly re-activated by SPI.

In mode 2, safe mode: Reset in not activated in case of Watchdog failure. WDOGB output has same behavior as in mode 1.

The Wdogb output pin is a push pull structure than can drive external component of the application in order for instance to signal MCU wrong operation.
Even if it is internally turned on (low sate) the reset pins can be forced to 5V at 25°C only, thanks to its internal limited current drive capability (capability used in Flash programming modes).

Events	Mode	WDOGB output	Reset output
Device power up	1 or 2 (safe mode)	low	low to high
- Vdd1 normal - Watchdog properly triggered	1	high	high
Vdd1 < Rst-th	1	high	low
Watchdog time out reached	1	low (note1)	low
- Vdd1 normal - Watchdog properly triggered	2 (safe mode)	high	high
Vdd1 < Rst-th	2 (safe mode)	high	low
Watchdog time out reached	2 (safe mode)	low (note1)	high

note1: Wdogb stays low until the Watchdog register is properly addressed through SPI.

4.15 Application hardware and software debug with the SBC

When the SBC is mounted on the same printed circuit board as the mico contoller it supplies, both application software and SBC dedicated rouitne must be debugged. Following features allow the user to debug the software by allowing the possiblity to disable the SBC internal software watchdog timer.

4.15.1 First BSC power up, reset pin connected to Vdd1

At SBC power up, the Vdd1 voltage is provided, but if no SPI communication occurs to configure the device in normal mode, a reset occurs every 400ms. In order to allow software debug and avoid MCU reset the Reset pin can be connected directly to Vdd1 by a jumper.

4.15.2 Special debug mode with sowftare watchdog disabled though SPI

The software watchdog can be disabled through SPI. But in order to avoid unwanted watchdog disable and to limit the risk of disabling the watchdog during SBC normal operation the watchdog disable has to be done when the “bat fail flag” is set. The bat fail flag is set when the SBC supply voltage (Vsup) has been lower than 3V. This is the case at SBC power up.

When this is done, the watchdog of the SBC is disabled, SBC can be used without having to clear the W/D on a regular basis to facilitate software and hardware debug.

4.15.3 MCU flash programming configuration

In order to allow the possibility to download software into the application memory (MCU EEPROM or Flash) the SBC allow the following capabilities: The Vdd1 can be forced by an external power supply to 5V and the reset and Wdogb outputs by external signal sources to zero or 5V and this without damage. This allow for instance to supply the complete application board by external power supply and to apply the correct signal to reset pins.

4.16 Gnd Shift Detection

4.16.1 General

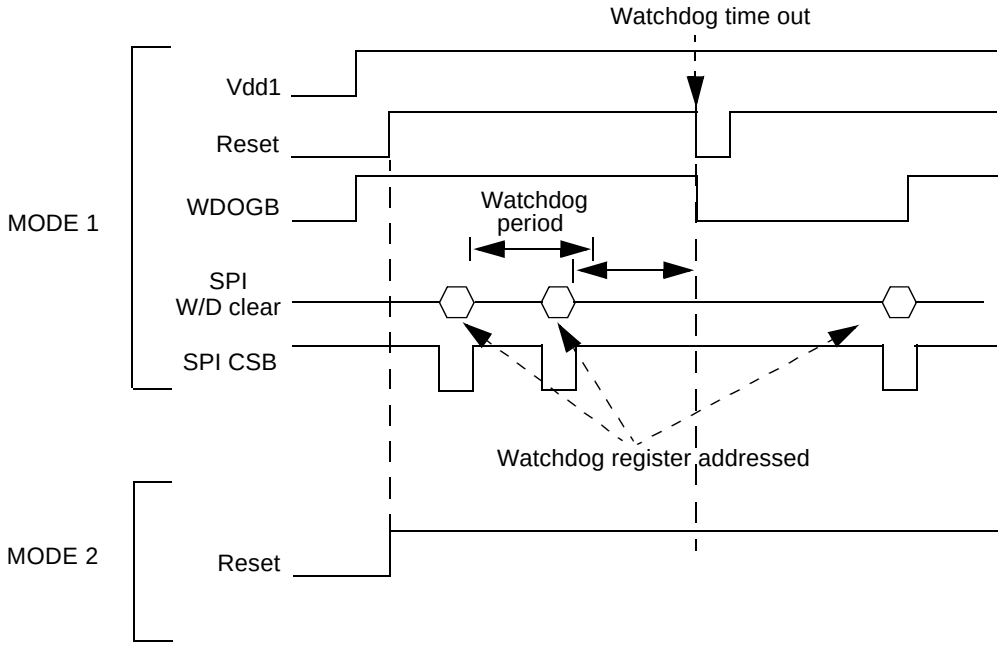
When normally working in two-wire operating mode, the CAN transmission can afford some ground shift between different nodes without trouble. Nevertheless, in case of bus failure, the transceiver switches to single-wire operation, therefore working with less noise margin. The affordable ground shift is decreased in this case.

The SBC provides a ground shift detection for diagnosis purpose. Four ground shift levels are selectable and the detection is stored in the IOR register which is accessible via the SPI.

4.16.2 Detection Principle

The gnd shift to detect is selected via the SPI out of 4 different vaues (-0.5V, -1V, -1.5V, -2V). At each TX falling edge (end of recessive state) CANH voltage is sensed. If it is detected to be below the selected gnd shift threshold, the bit SHIFT is set at 1 in IOR register. No filter is implemented. Required filtering for reliable detection should be done by software (e.g. several trials).

Figure 4. Reset and Wdogb function diagram in mode 1 and 2



5 TABLE OF OPERATION

The table below describe the SBC operation modes.

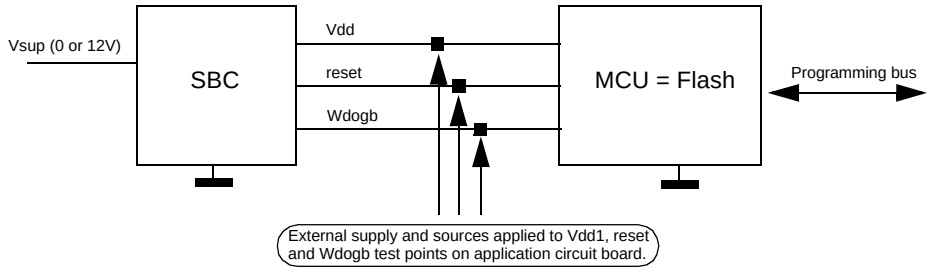
mode	Voltage Regulator HS1 switch	Wake up capabilities (if enabled)	Reset pin	INT	Software Watchdog	CAN cell
Normal Request	Vdd1: ON V2: OFF HS1: OFF		Low for 1ms, then high			term Vbat
Normal	Vdd1: ON V2: ON HS1 controllable		Normally high. Active low if W/D or Vdd1 under voltage occur (and mode 1 selected)	If enabled, signal failure (Vdd pre warning temp, CAN, HS1)	Running	Term Vbat Tx/Rx Rec only
Standby	Vdd1: ON V2: OFF HS1 controllable		Normally high. Active low if W/D or Vdd1 under voltage occur	If enabled, signal failure (Vdd temp, CAN, HS1)	Running	Term Vbat Tx/Rx Rec only
Stop	Vdd1: ON (2mA capability) V2: OFF HS1: OFF or cyclic	CAN (always enable) SPI and L0,L1 Cyclic sense or Forced Wake up	Normally high. Active low if W/D or Vdd1 under voltage occur	Signal SBC wake up (not maskable)	- Running if enabled - Not Running if disabled	Term Vbat.
Sleep	Vdd1: OFF V2: OFF HS1 OFF or cyclic	CAN (always enable SPI and L0,L1 Cyclic sense Forced Wake up	Low	Not active	No Running	Term Vbat.

Tableau 1 : table of operation

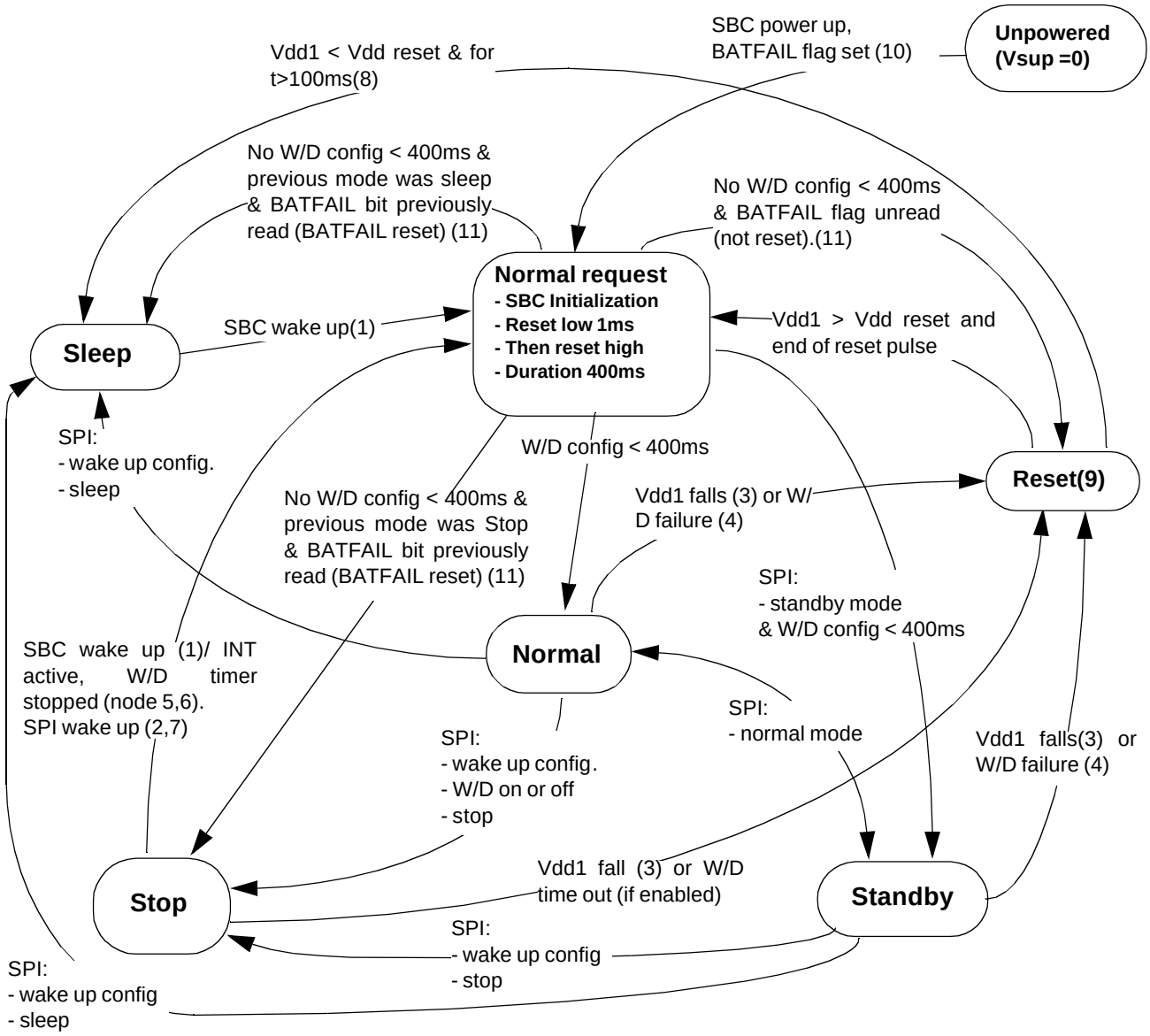
The table below describes the SBC special debug mode and flash programming configuration

mode	Voltage Regulator	Reset and Wdogb pins	Software Watchdog	Mode enter and comment
Debug	Vdd1: ON V2: ON	- Watchdog is normally high. Active only if Vdd1 under voltage occurs - Wdogb pin function identical as in other modes.	Not running	- Mode entered by SPI command, while BATFAIL flag is still set. - All SBC functions are available with the exception of the software watchdog which is disabled.
Flash programming	Forced externally	Forced externally	Not running	- Vsup pin can be power or unpowered. - Vdd1, reset and Wdogb pin are forced by external power supply or signal sources.

Simplified connection used in Flash programming mode



6 SIMPLIFIED STATE MACHINE

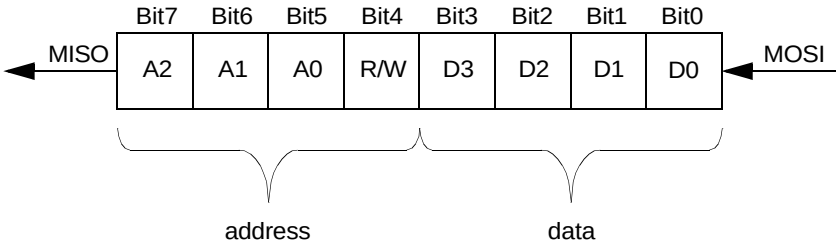


Comment:

(1): SBC wake up: wake up from CAN, Lx, Cyclic sense or forced wake up.
(2): SPI wake up: wake up from CSB pin (Wake up through MCU activity).
(3): Vdd1 falls: Vdd1 falls below Vdd1 reset threshold
(4): W/D failure: Watchdog not triggered before time out, or Watchdog trigger in the closed window.
(5): In stop mode when SBC wakes up, wake up is transmitted to MCU through INT pin activation. INT stays low until INT register is read (cleared).
(6): In stop mode, if W/D is enabled, when SBC goes out of stop mode before W/D time out, W/D timer is stopped. Then the normal request mode 400ms timer starts. If no SPI configuration occurs within the 400ms SBC goes back to Stop mode with same conditions (wake up, W/D enable etc.).
(7): In stop mode when MCU goes out of its low power mode, this event is transmitted to SBC through an SPI wake up (CSB pin activation).
(8): In case of short circuit or over load condition at Vdd. SBC goes to Sleep mode after 100ms.
(9): In reset mode Vdd1 is ON and can deliver full current capability (120mA). Reset pulse occurs at reset pin.
(10): BATFAIL bit is set to 1 when Vsup fall below 3V typical.
(11): BATFAIL is reset when MCR register is read.

7 SPI INTERFACE

7.1 Data format description



Read operation: R/W bit = 0

Write operation: R/W bit = 1

7.2 List of Registers:

Name	Adress	Description	Comment and usage
MCR	$ 0 0 0	Mode control register	Write: Control of normal, standby, sleep, stop, debug modes Read: BATFAIL flag and other status bits and flags
RCR	$ 0 0 1	Reset control register	Write: Configuration of reset voltage level and safe bit
CAN	$ 0 1 0	CAN control register	Write: CAN module control: Tx/Rx, Rec only, term Vbat, Normal and extended modes Read: CAN wake up and CAN failure status bits
IOR	$ 0 1 1	I/O control register	Write: HS1 (high side switch) control in normal and standby mode. Gnd shift register level selection Read: HS1 over temp bit SHIFT bit (gnd shift above selection)
WUR	$ 1 0 0	Wake up input register	Write: Control of wake up input polarity Read: Wake up input, and real time Lx input state
TIM	$ 1 0 1	Timing register	Write: TIM1, Watchdog timing control, window or Timeout mode. Write: TIM2, Cyclic sense and force wake up timing selection
LPC	$ 1 1 0	Low power mode control register	Write: HS1 periodic activation in sleep and stop modes Force wake up control
INTR	$ 1 1 1	Interrupt register	Write: Interrupt source configuration Read: INT source

Table 7-1.

7.3 Register description

7.3.1 MCR Register

MCR		D3	D2	D1	D0
$000b	W	WDSLEEP	MCTR2	MCTR1	MCTR0
	R	BATFAIL	VDDTEMP	GFAIL	WDRST
Reset		0	0	0	0

Table 7-2.

Control bits

BATFAIL	MCTR2	MCTR1	MCTR0	SBC mode	Description
X	automatically entered after reset			Normal Request	
0	0	0	1	Normal	
0	0	1	0	Standby	
X	0	1	1	Stop	
0	1	0	0	Sleep	
1	1	0	1	Normal	For debugging only, **watchdog is disabled**
1	1	1	0	Standby	

WDSTOP	Watchdog in stop mode
0	off
1	on

Status bits

Status bit	Description
GFAIL	Logic OR of CAN, HS1 failure
BATFAIL	Battery fail flag
VDDTEMP	Temperature pre-warning on VDD (latched)
WDRST	Watchdog reset occured

7.3.2 RCR register

RCR		D3	D2	D1	D0
$001b	W			SAFE	RSTTH
	R				
Reset				0	0

Table 7-3.

Control bits

Condition	SAFE	WDOGB	Reset
Device power up	0 1	0	0→1
V1 normal, WD is properly triggered	0 1	1	1 1
V1 drops below 4.5 volt	0 1	1 1	0 0
WD time out	0 1	0	0 1

Table 7-4.

RSTTH	Reset threshold voltage [V]			

7.3.3 CAN register

Some description.

CAN		D3	D2	D1	D0
$001b	W		CEXT	CCTR1	CCTR0
	R	CANWU	TXF	CANLF	CANHF
Reset			0	0	0

Table 7-5.

Fault tolerant CAN transceiver standard modes (light version only)

The CAN transceiver standard mode can be programmed by setting CEXT to 0. The transceiver cell will then be behave as known from MC33388..

CEXT	CCTR1	CCTR0	Mode
0	0	0	TermVBAT
0	0	1	
0	1	0	RxOnly
0	1	1	RxTx

Table 7-6.

Fault tolerant CAN transceiver extended modes (light version only)

By setting CEXT to 1 the transceiver cell supports sub bus communication.

CEXT	CCTR1	CCTR0	Mode
1	0	0	TermVBAT
1	0	1	TermVDD

Table 7-7.

CEXT	CCTR1	CCTR0	Mode
1	1	0	RxOnly
1	1	1	RxTx

Table 7-7.

Description.

CEXT	CCTR1	CCTR0	Mode

Status bits

Status bit	Description
CANWU	CAN wake-up occured
TXF	Permanent dominant TX*
CANLF	Failure on CANL (open wire, short circuit)*
CANHF	Failure on CANH (open wire, short circuit)*

*.light version only

7.3.4 IOR register

Some description.

IOR		D3	D2	D1	D0
$011b	W	HS1ON		GSLR1	GSLR0
	R	HS1OT	SHIFT		
Reset		0	0	0	0

Table 7-8.

Control bits

HS1ON	HS1
0	HS1 switch turn OFF
1	HS1 switch turn ON

Table 7-9.

Control bit for gnd shift detection)

GSLR1	GSLR0	typical gnd shift level
0	0	-0.5 V
0	1	-1 V
1	0	-1.5 V
1	1	-2 V

Table 7-10. gnd shift selection

Status bits

Status bit	Description
HS1OT	High side 1 overtemperature

Once the switch has been turned off because of over temperature, it can be turned on again by setting the appropriate control bit to “1”.

7.3.5 WUR register

The local wake-up inputs L0 and L1 can be used in both normal and standby mode as port expander and for waking up the SBC in sleep or stop mode.

WUR		D3	D2	D1	D0
$100b	W	LCTR3	LCTR2	LCTR1	LCTR0
	R		L1WU		L0WU
Reset		0	0	0	0

Table 7-11.

The wake-up inputs can be configured almost separetly, where L0 and L1 are independed configurable from L2 and L3.

Control bits:.

LCTR3	LCTR2	LCTR1	LCTR0	L0 configuration	L1 configuration
X	X	0	0	inputs disabled	
X	X	0	1	high level sensitive	
X	X	1	0	low level sensitive	
X	X	1	1	both level sensitive	
0	0	X	X		inputs disabled
0	1	X	X		high level sensitive
1	0	X	X		low level sensitive
1	1	X	X		both level sensitive

Table 7-12.

Status bits:

Status bit	Description
L0WU	Wake up occured at L0 (sleep or stop mode). Logic state on L0 (standby or normal mode)
L1WU	Wake up occured at L1 (sleep or stop mode). Logic state on L1 (standby or normal mode)

7.3.6 TIM register

Description.

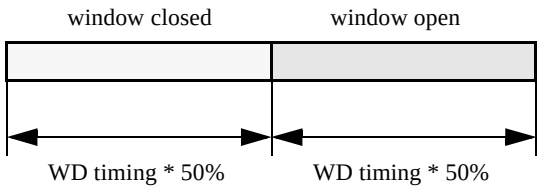
TIM1		D3	D2	D1	D0
$101b	W	0	WDW	WDT1	WDT0
	R				
Reset			0	0	0

Table 7-13.

Description

WDW	WDT1	WDT0	Watchdog timing [ms]	
0	0	0	10	no window watchdog
0	0	1	50	
0	1	0	100	
0	1	1	400	
1	0	0	10	window watchdog enabled (window lenght is half the watchdog timing)
1	0	1	50	
1	1	0	100	
1	1	1	400	

Table 7-14.



7.3.7 TIM2 register

The purpose of TIM2 register is to select an appropriate timing for sensing the wake-up circuitry or cyclically supplying devices by switching on or off HS1*.

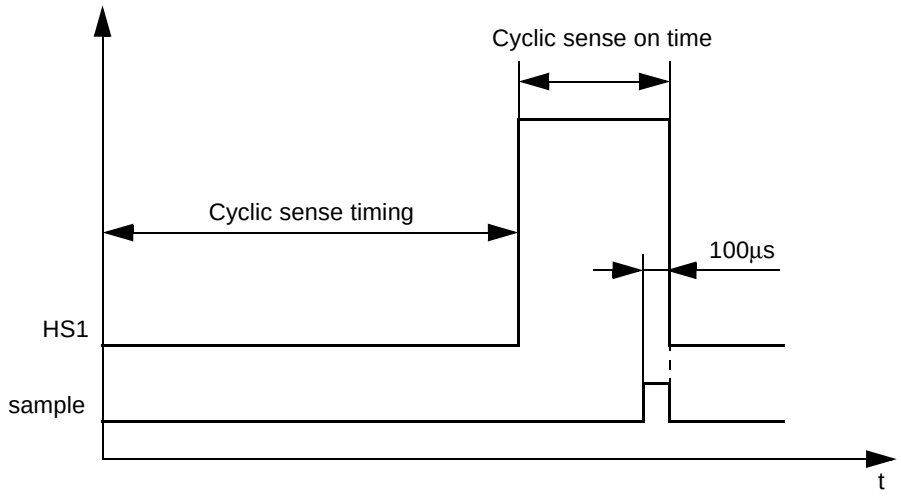
TIM2		D3	D2	D1	D0
$101b	W	1	CSP2	CSP1	CSP0
	R				
Reset			0	0	0

Table 7-15.

*only available on MC33890

CSP2	CSP1	CSP0	Cyclic sense timing [ms]
0	0	0	5
0	0	1	10
0	1	0	20
0	1	1	40
1	0	0	75
1	0	1	100
1	1	0	200
1	1	1	400

Table 7-16.



7.3.8 LPC register

LPC		D3	D2	D1	D0
$110b	W	LX2HS1	FWU	HS2AUTO	HS1AUTO
	R				
Reset		1	0	0	0

Table 7-17.

LX2HS1	HS2AUTO	HS1AUTO	Wake-up inputs supplied by HS1	Autotiming HS2	Autotiming HS1
X	X	0			off
X	X	1			on
X	0	X		off	
X	1	X		on	

Table 7-18.

LX2HS1	HS2AUTO	HS1AUTO	Wake-up inputs supplied by HS1	Autotiming HS2	Autotiming HS1
0	X	X	no		
1	X	X	yes		

Table 7-18.

7.3.9 INTR register

INTR		D3	D2	D1	D0
$111b	W		HS1OT	VDDTEMP	CANF
	R		HS1OT	VDDTEMP	CANF
Reset			0	0	0

Table 7-19.

Control bits:

Control bit	Description
CANF	Mask bit for CAN failures
VDDTEMP	Mask bit for VDD medium temperature
HS1OT	Mask bit for HS1 over temperature

When the mask bit has been set, INTB pin goes low if the appropriate condition occurs.

Status bits:

Status bit	Description
CANF	CAN failure
VDDTEMP	VDD medium temperature
HS1OT	HS1 over temperature

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1-303-675-2140 or 1-800-441-2447

Technical Information Center: 1-800-521-6274

HOME PAGE: http://www.motorola.com/semiconductors

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3-20-1, Minami-Azabu, Minato-ku, Tokyo 106-8573 Japan. 81-3-344-3569

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2, Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852-26668334