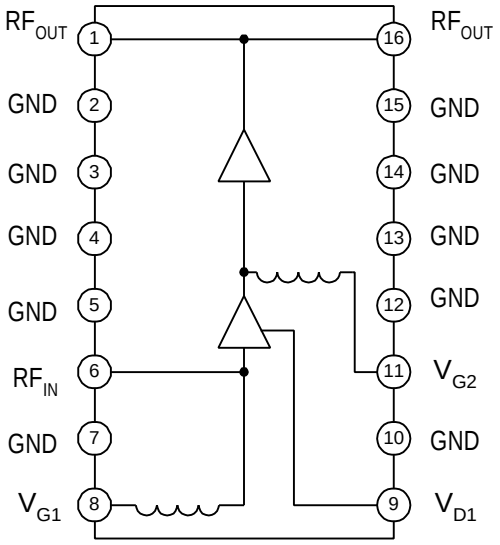
TriQuint SEMICONDUCTOR

WIRELESS COMMUNICATIONS DIVISION



TQ9147B

DATA SHEET

2-Stage AMPS Power Amplifier IC

Features

- *High Efficiency*
- *+32 dBm Output Power*
- *50W Matched Input*
- *SO-16 Plastic Package*
- *Monolithic Power Amp*

Applications

- *AMPS Mobile Phones*
- *CDPD Modems*
- *General ISM Band Applications*

Product Description

The TQ9147 is a high efficiency two stage GaAs MESFET power amplifier IC intended for use in AMPS (IS-19) applications that operate in the US Cellular (824 - 849 MHz) band. The TQ9147 requires minimal external RF circuitry and operates from a 4.8-Volt supply. With its flexible, off-chip, single component output matching circuit, the TQ9147 is suitable for use in other applications near the cellular band, such as 900 MHz ISM applications.

The TQ9147 utilizes a space saving SO-16 plastic package that minimizes board area and cost.

Electrical Specifications[1]

Parameter	Min	Typ	Max	Units
Output Power	+31.5	+32		dBm
Efficiency	55	60		%

Note 1: Test Conditions: V_{DD} = 4.8 V, P_{IN} = +7 dBm, Freq. = 824 & 849 MHz, T_C = 25 °C, Min/max values 100% production tested.

Electrical Characteristics

Parameter [1]	Conditions	Min	Typ/Nom	Max	Units
Frequency	tuned for cellular band	824		849	MHz
Supply Voltage (V_{DD})		2.7	4.8	6.0	V
Temperature	measured at case	-40	25	+110	°C
P_{OUT}	V_{DD} = 4.8 V	31.5	32		dBm
	V_{DD} = 4.3 V		30		dBm
Efficiency		55	60		%
Rx band Noise [2]	P_{IN} = -30 to +7 dBm		-90		dBm
Small Signal Gain	P_{IN} = -10 dBm		32		dB
Power Gain	P_{OUT} = 32 dBm (typ)		25		dB
Input Return Loss	P_{IN} = -30 to +7 dBm		10		dB
Harmonics					
2nd Harmonic				-30	dBc
3rd Harmonic				-35	dBc
4th Harmonic				-35	dBc
Spurious (Stability)	P_{IN} = -30 to +7 dBm		-70		dBc/30 kHz
RF Off Isolation			20		dBc
Ruggedness	V_{DD} at burnout		6.5		V

Note 1: Test Conditions: V_{DD} = 4.8 V, P_{IN} = +7 dBm, Freq. = 824 & 849 MHz, V_{GG} = 3.5 V, T_C = 25 °C.

Note 2: Noise power is measured in 30 kHz band width at the transmit frequency plus 45 MHz

Note 3: Load is set to 50 ohms, output power measured at nominal test conditions. Load VSWR is set to 10:1 and the angle is varied 360 degrees over 5 seconds. Load set to 50 ohms, output power remeasured and compared with the first measurement to check for no degradation from the first measurement.

Absolute Maximum Ratings

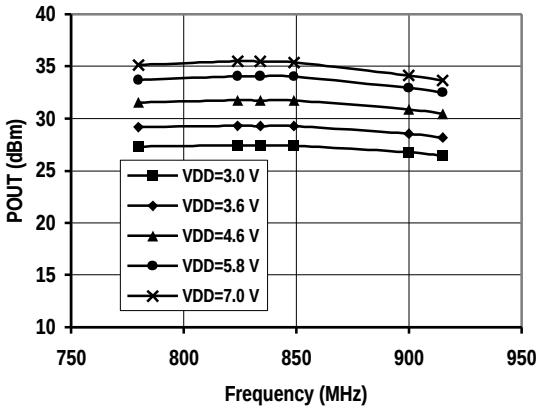
Parameter	Value	Units
DC Power Supply [1]	8.0	V
DC Gate Voltage	-5.0	V
RF Input Power	20	dBm
Storage Temperature	-55 to 150	° C
Operating Temperature (case)	-40 to 110	° C

Note 1: Into a 10:1 mismatch.

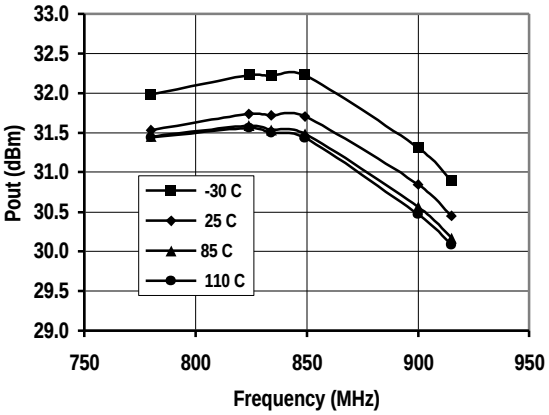
Typical Performance

Test Conditions (Unless Otherwise Specified): V_{DD} = 4.8 V, P_{IN} = +7 dBm, Freq. = 824 & 849 MHz, T_C = 25 °C, constant gate voltages: V_{G1} = -1.5 V, V_{G2} = -2.2 V.

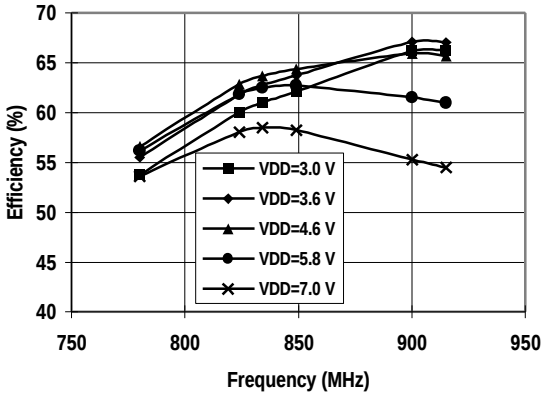
Output Power vs. Frequency and VDD



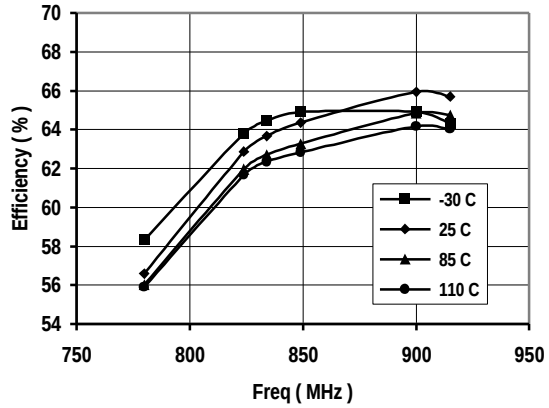
Output Power vs. Frequency vs. Temp.



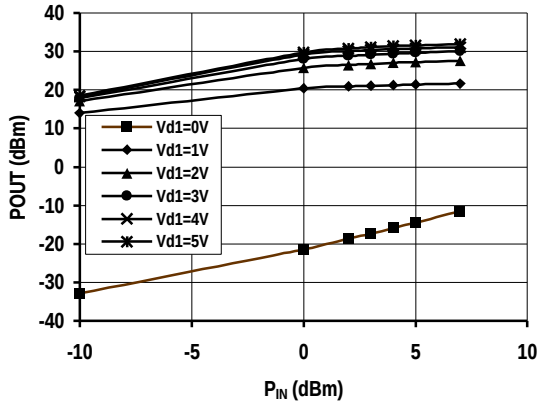
Efficiency vs. Frequency and VDD



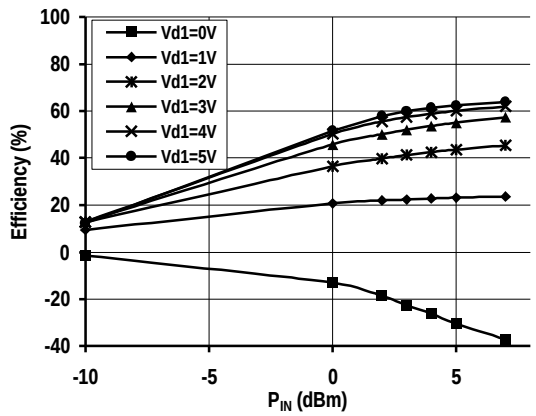
Efficiency vs. Frequency vs. Temp



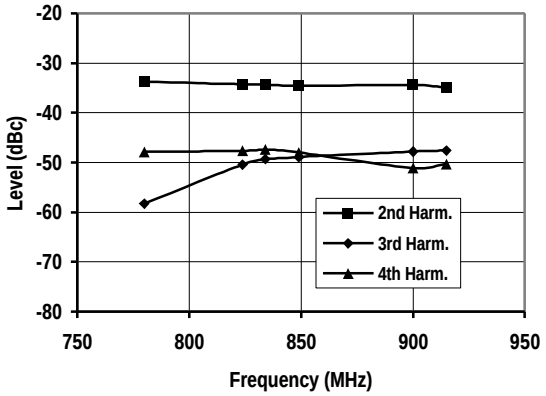
Output Power vs. Input Power vs. VD1



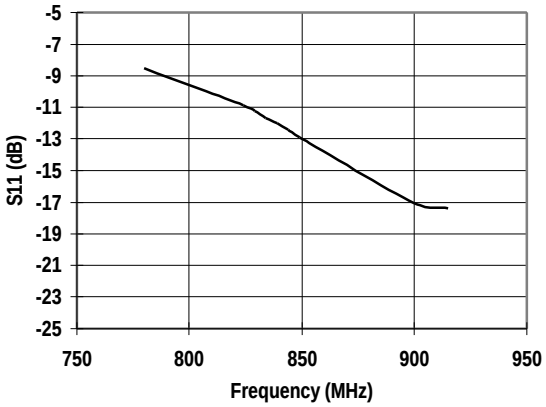
Efficiency vs. Input Power vs. Vd1



Harmonics vs. Frequency @ T = 25 C

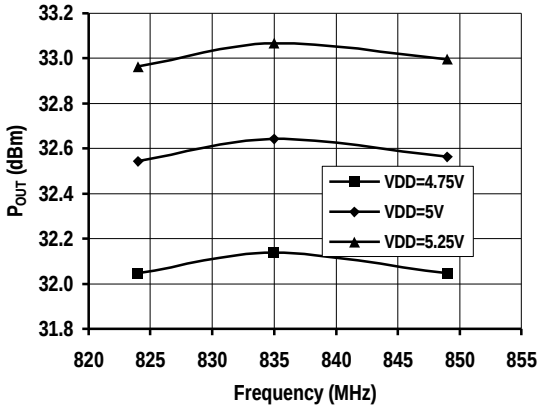


S11 vs. Frequency

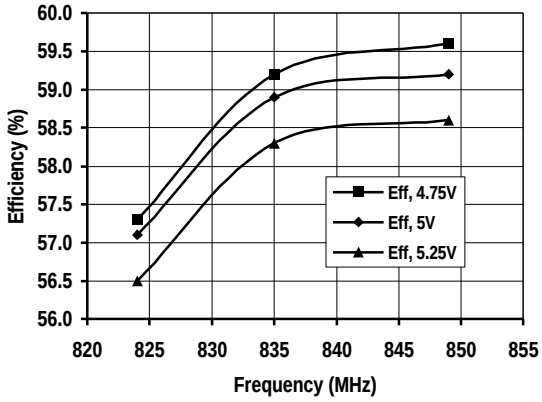


Test Conditions (Unless Otherwise Specified): V_{DD} = 5 V, P_{IN} = +7 dBm, V_{GG} = -3.5 V, Freq. = 824 & 849 MHz, T_C = 25 °C, Gate voltage determined by the recommended bias circuit

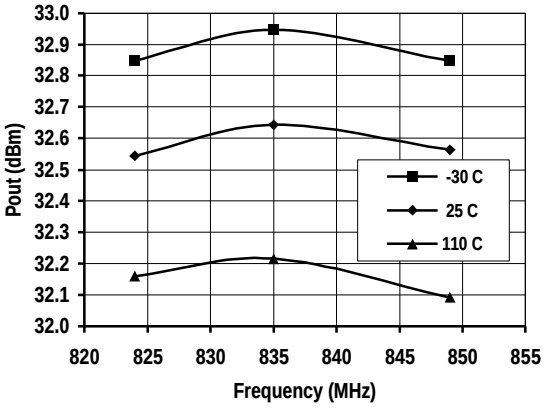
Output Power vs. Frequency vs. VDD



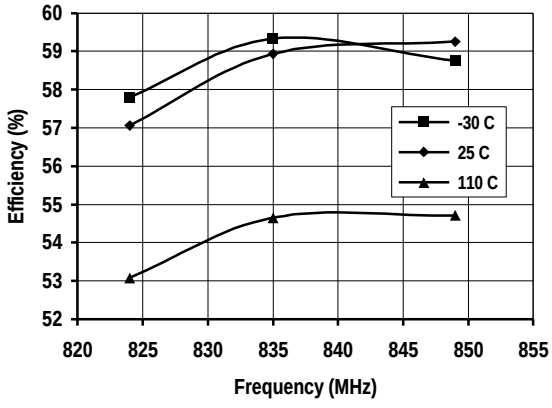
Efficiency vs. Frequency vs. VDD



Output Power vs. Frequency vs. Temperature

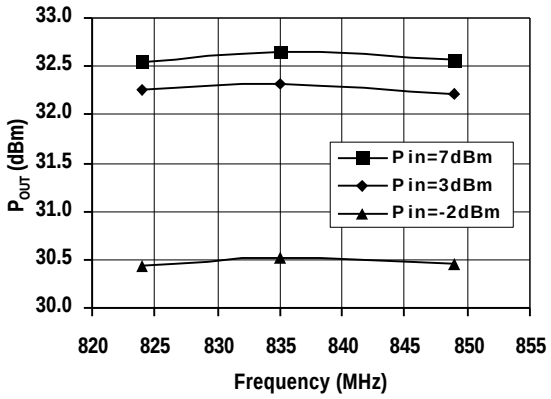


Efficiency vs. Frequency vs. Temperature

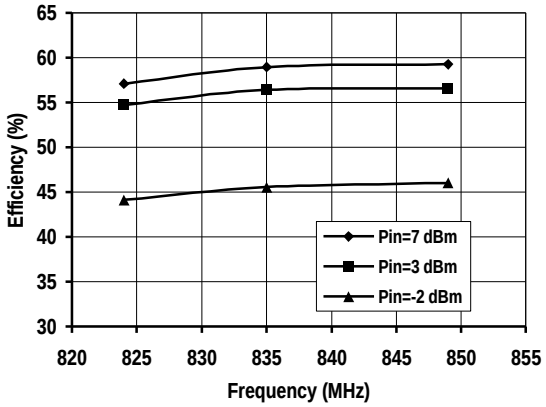


Test Conditions (Unless Otherwise Specified): V_{DD} = 5 V, P_{IN} = +7 dBm, V_{GG} = -3.5 V, Freq. = 824 & 849 MHz, T_C = 25 °C, Gate voltage determined by the recommended bias circuit

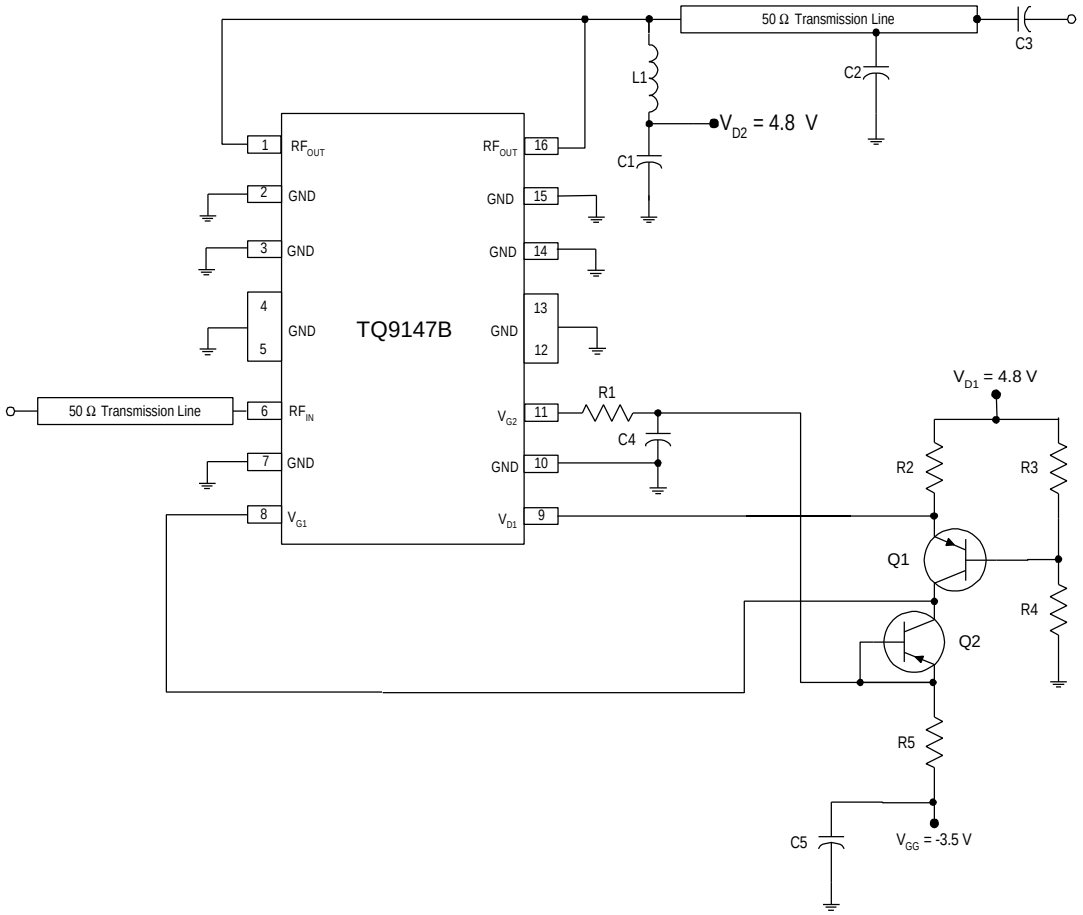
Output Power vs. Frequency vs. Input Power



Efficiency vs. Frequency vs. Input Power



Application/Test Circuit



Bill of Material for TQ9147B Power Amplifier Application/Test Circuit

Component	*Reference Designator*	*Part Number*	*Value*	*Size*	*Manufacturer*
Power Amplifier IC	U1	TQ9147B		TSSOP-20	TriQuint Semiconductor
PNP Transistor	Q1, Q2	2N3906			
Capacitor	C1, C4, C5	MCH182F104ZK	0.1 µF	0603	Rohm
Capacitor	C2,	MCH155A8R2CK	8.2 pF	0402	Rohm
Capacitor	C3	MCH155A680JK	68 pF	0402	Rohm
Resistor	R1	MCR01JW510	51 Ω	0402	Rohm
Resistor	R2	MCR01JW100	10 Ω	0402	Rohm
Resistor	R3	MCR01JW621	620 Ω	0402	Rohm
Resistor	R4	MCR01JW202	2 kΩ	0402	Rohm
Resistor	R5	MCR01JW391	390 Ω	0402	Rohm
Inductor	L1	0805CS470	47 nH		Coilcraft

Product Description

The TQ9147 is a high efficiency two stage GaAs MESFET power amplifier IC intended for use in AMPS (IS-19) applications that operate in the US Cellular (824 - 849 MHz) band. The TQ9147 requires minimal external RF circuitry and operates from a 4.8-Volt supply. With its flexible, off-chip, single component output matching circuit, the TQ9147 is suitable for use in other applications near the cellular band, such as 900 MHz ISM applications.

The TQ9147 utilizes a space saving SO-16 plastic package that minimizes board area and cost.

Operation

Please refer to the application circuit above.

Gate Biasing and Bypassing

The TQ9147 is a dual-supply power amplifier (PA). Because it utilizes depletion-mode MESFETs, a negative bias voltage must be supplied to the gate of each FET. There are several excellent choices of negative voltage bias supplies (charge pumps) on the market, such as the Maxim MAX881R, or the Harris ILC7660S. A simple resistor divider circuit is the most inexpensive way to bias the gates of each stage from the charge pump. However, due to fabrication tolerances and the large window of main supply voltages under which the device can function, the active bias method shown in the application circuit is recommended.

This bias technique accurately sets the bias point for each stage and optimizes the quiescent current and efficiency over a wide range of supply voltages and output power levels. The following table lists the nominal values of gate voltage and quiescent current when this bias method is used. It is important to remember that the negative gate voltage must be supplied first in order to protect the device from inadvertent high drain currents. If the drains are turned on before the gate bias is set, the IC can be damaged or destroyed.

Gate Bias Voltages and Drain Quiescent Current

Parameter	Value	Units
V_{DD}	4.8	V
V_{G1}	-1.5	V
V_{G2}	-2.2	V
I_{DQ1}	50	MA
I_{DQ2}	0-100	mA

The gate of each FET in the IC is RF bypassed on chip. However, additional low frequency filtering and noise suppression must be done externally. This is accomplished with a 51 Ohm resistor (R1) and 0.1 μF cap (C4) from pin 11 (Vg2). This capacitor and resistor combination also ensures device stability under all conditions.

Drain Bypassing

C1 (0.1 μF) provides RF bypassing for the high impedance side of the RF choke (L1).

Input Match

The device input is internally matched to 50 Ohms. A 50-Ohm transmission line is all that is required between the PA and the driver amp.

Output Match and High Power Bias Injection

Pins 1 and 16 are dual-purpose pins, providing for both the RF output and the high power DC input for the drain of the second stage FET. As such, these pins are connected to a 50-Ohm transmission line. Locating C2 (8.2 pF) approximately 200 mils from the device along this transmission line acts as a shorted stub tuner that transforms the low output impedance (~ 7.5 Ohms) of the power stage to 50 Ohms. Varying the position of C2 along the line can alter the output match in order to optimize either power output or efficiency. In general, the farther away C2 is from the pins the higher the efficiency at the expense of power output. The closer the cap is, the higher the output power at the expense of efficiency. By varying the value and position of C2, the device can be easily tuned for a different frequency range such as the 902 – 928 MHz ISM band. C3 (68 pF) is a DC blocking cap.

Drain current for the second stage is injected through L1 (47 nH), which acts as an RF choke on the high power DC feed line. As stated above, C1 is the bypass cap for the high impedance side of L1.

Power down Function

To fully turn off the PA when not transmitting, a PMOS FET (PFET) switch can be used to control the drain bias to the PA. There are several acceptable models available on the market, such as the IRF7604 from International Rectifier, or any device with low R_{DSon}. An added benefit of incorporating a switch of this type is that it protects the PA from inadvertently powering up the device incorrectly. Since depletion-mode FETs are used in the PA, care must be taken to insure that the gate bias is fully stabilized before drain bias is applied. If not, the full value of I_{Dss} will flow, which could damage or destroy the IC. A feature included in the Maxim charge pump allows for a separate control output to run the PFET. This control line holds the PFET off until the gate bias voltage has stabilized.

RF Power Control

There are three methods of controlling the output power from the TQ9147. All three methods can provide a minimum 25 dB of control range for the device, which exceeds the requirements of IS-19.

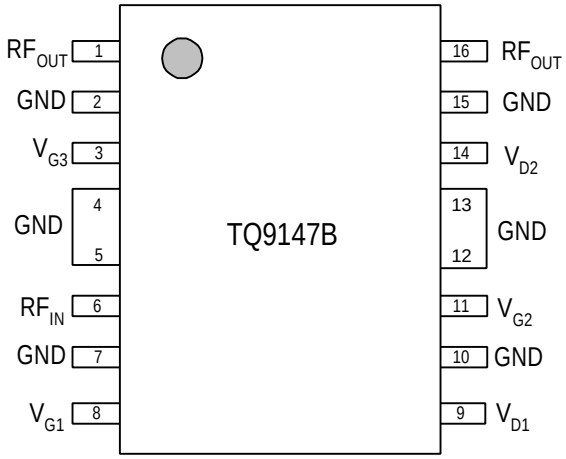
The first method is to vary the gate bias voltages. Though this approach has the advantage of increased efficiency at lower output power levels, it is hampered by two problems. First, both gate voltages must be varied. Since each stage typically requires a different bias point, the control circuit must monitor both bias points, thereby complicating the design.

The second drawback is that most charge pumps, including those recommended above, require large capacitors on the output for filtering and stability. Such large cap values may not allow full compliance with the required 20 mS transition spec between any two power levels.

The second method is to vary the input power level. Though this can be done with a simple attenuator between the driver amp and the PA, the response is very non-linear, as the PA must first come out of saturation before the output power can change. Once out of saturation, the first stage is class A biased, which means that the drain current is constant regardless of power settings. The addition of an attenuator also adds to the expense of the parts list and to the board size equation, and increases the insertion loss the driver amp must overcome.

The third, and preferred, method is to vary the drain supply voltage to the first stage. By forcing the first stage bias lower, the first stage is always heavily saturated, thus saving battery power. Since the second stage is biased class AB, drain current to that stage lowers as the drive level decreases. This method optimizes battery savings over the other approaches. The simplest implementation of this technique would be to incorporate a second PFET to control the first stage drain. This circuit can be realized buy utilizing a dual PFET such as the International Rectifier IRF7314, which has two low R_{DSon} FETs in a single SO-8 package. By cascoding the two FETs, one implements a master on/off function while the second controls only the first stage drain bias. This technique also fits very well with the active gate biasing circuit that was recommended previously.

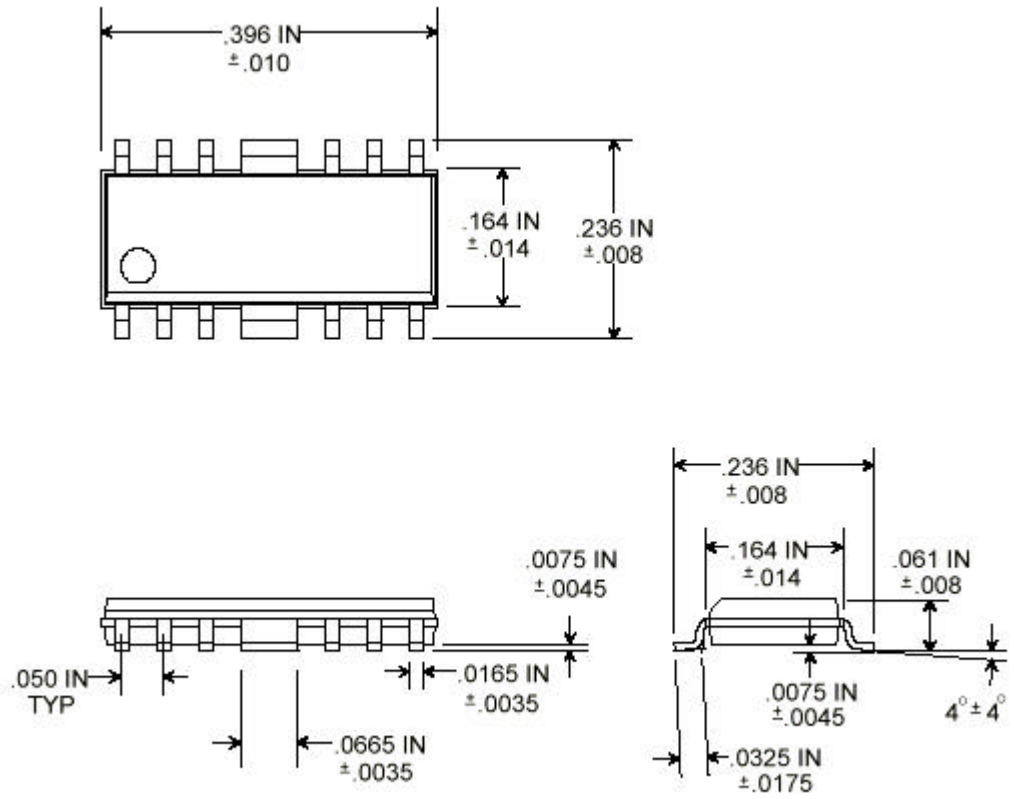
Package Pinout



Pin Descriptions

Pin Name	*Pin #*	*Description and Usage*
RF_{OUT}	1,16	Power Amplifier output and second-stage supply voltage. Critical, but simple, matching circuit required. Bias choke for V_{D2} required, local bypass cap recommend, and DC blocking capacitor required.
RF_{IN}	6	RF input to power amplifier. Matched to 50 Ω. Internal DC block.
V_{G1}	8	First stage gate voltage. Local bypass cap needed. Set V_{G1} = -1.5 V or use bias stabilization circuit.
V_{D1}	9	First stage supply voltage. Local bypass cap recommended. Use same voltage as V_{D2} or use bias stabilization circuit.
V_{G2}	11	Second stage gate voltage. Local bypass cap needed. Required 50 Ω series resistor near device for stability. Set V_{G2} = -2.2 V or use bias stabilization circuit.
GND	2, 3, 4, 5, 7, 10, 12, 13, 14, 15	Ground connections. Provide thermal path for heat dissipation and RF grounding. Very important to place multiple via holes immediately adjacent to the pins.

Package Type: SOIC-16 Plastic Package with Thermal Tabs



Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel: (503) 615-9000**
Email: info_wireless@tqs.com **Fax: (503) 615-8900**

For technical questions and additional information on specific applications:

Email: info_wireless@tqs.com

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