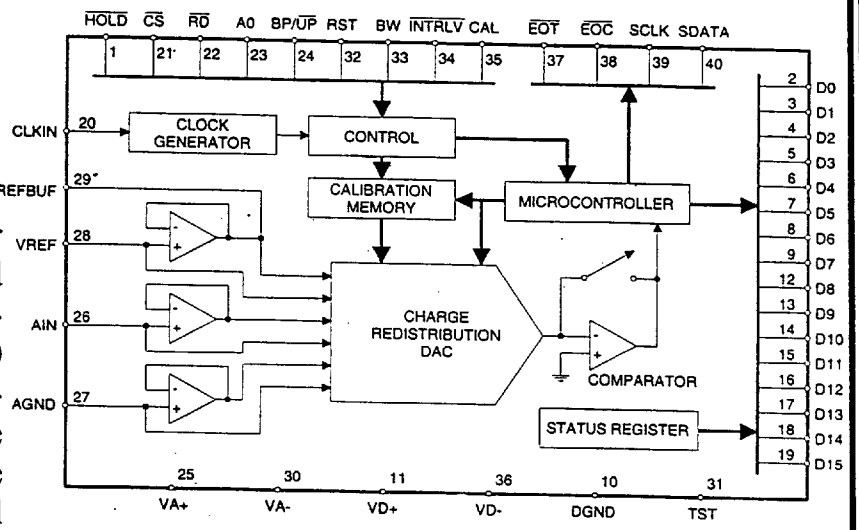
16-Bit A/D Converter - Radiation Hardened

5016RP

Self-Calibrating High Speed CMOS

For Space Applications



SEI's 5016RP (RP for RAD-PAK®)high speed CMOS microcircuit features a minimum 100 kilorad(Si) total dose tolerance. Fully equivalent to the commercial 5016, the 5016RP combines Crystal Semiconductor's advanced CMOS process and SEI's radiation hardened RAD-PAK® packaging. This device offers a unique self-calibration circuitry which insures excellent linearity and differential nonlinearity, with no missing codes. Offset and full scale errors are kept within 1 LSB, which helps eliminate the need for calibration. Unipolar and bipolar input ranges are digitally selectable. Capable of surviving space environments, the 5016RP is ideal for satellite, spacecraft, and space probe missions. The patented RAD-PAK® technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing lifetime in orbit. The 5016RP, capable of operational sample rates up to 50kHz, features the same system performance and architecture as the commercial Crystal Semiconductor's counterpart. It is available in Class S packaging and screening.

SPACE ELECTRONICS INCORPORATED

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SEI 5016RP RADHARD CMOS

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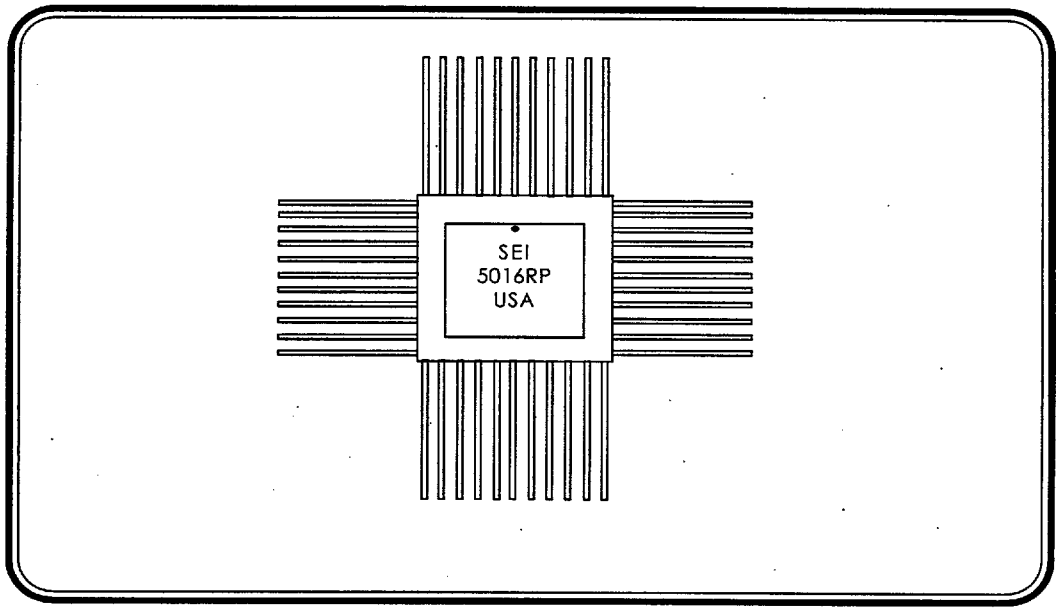
Radiation Hardened
5016RP
Self-Calibrating High Speed CMOS



Features:

- High Speed: 16.25 usec conversion time
- Pin Compatible to Crystal CS5016
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
- Package:
  - 44 Pin RAD-PAK® quad flat pack (0.655in. x 0.650 in.)
  - Weight – 8.2 grams
  - 40 Pin RAD-PAK® DIP (2.0 in. x 100 mil pitch)
  - Weight - 11.2 grams
- Low Power CMOS Technology
  - 120 mW Typical
- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - Microprocessor Interface
  - Parallel and Serial Output
  - Self Calibration Maintains Accuracy Over Time and Temperature
- True 16-Bit Precision
  - Linearity Error: +0.001% FS
  - No Missing Codes
  - S/(N+D): 92 dB
  - THD: 0.001%
- Screening per TM 5004
- QCI per TM5005

Specifications and design are subject to change without notice.

TQM
Total Quality Management

August 1995

For Further Information Contact:
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5016RP ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	SYMBOL	MIN	MAX	UNIT
DC Power Supplies:				
Positive Digital	VD+	-0.3	(VA+)+0.3	V
Negative Digital	VD-	0.3	-6.0	V
Positive Analog	VA+	-0.3	6.0	V
Negative Analog	VA-	0.3	-6.0	V
Input Current, Any Pin Except Supplies[2]	I_{in}		±10	mA
Analog Input Voltage (AIN and VREF pins)	V_{INA}	(VA-)-0.3	(VA+)+0.3	V
Digital Input Voltage	V_{IND}	-0.3	(VA+)+0.3	V
Ambient Operating Temperature	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

Notes:

1. AGND, DGND = 0V, all voltages are with respect to ground.
2. Transient currents of up to 100 mA will not causeSCR latch-up

5016RP RECOMMENDED OPERATING CONDITIONS[1]

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
DC Power Supplies:					
Positive Digital	VD+	4.5	5.0	VA+	V
Negative Digital	VD-	-4.5	-5.0	-5.5	V
Positive Analog	VA+	4.5	5.0	5.5	V
Negative Analog	VA-	-4.5	-5.0	-5.5	V
Analog Reference Voltage	VREF	2.5	4.5	(VA+)-0.5	V
Analog Input Voltage[2]:					
Unipolar	V_{AIN}	AGND		VREF	V
Bipolar	V_{AIN}	-VREF		VREF	V

Note:

1. AGND, DGND = 0V, All voltages are with respect to ground.
2. It can accept input voltages up to the analog supplies (VA+ and VA-). It will output all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

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5016RP ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Resolution No Missing Codes Guaranteed[1]	RES	16		Bits
Integral Linearity Error[1,2]	INL		±5.0	LSB
Full-scale Error[1,2]	FSE		±4.0	LSB
Full-scale Error Drift[1,2,3,4]	dFSE/d_t		±4.0	LSB
Unipolar Offset Error[1,2]	VOFF		±4.0	LSB
Unipolar Offset Error Drift[1,2,3,4]	dVOFF/d_t		±2.0	LSB
Bipolar Offset Error[1,2]	BOFF		±4.0	LSB
Bipolar Offset Error Drift[1,2,3,4]	dBOFF/d_t		±3.0	LSB
Bipolar Negative Full-scale Error[1,2]	BNFSE		±5.0	LSB
Bipolar Negative Full-scale Error Drift[1,2,3,4]	dBNFSE/d_t		±3.0	LSB
Peak Harmonic or Spurious Noise 1kHz input, full scale amp., bipolar mode[1,2] 12kHz input, full scale amp., bipolar mode[1,2]	S/PN	 92 82		 dB dB
Signal to Noise Ratio[1,2] 1kHz input, full scale amp., bipolar mode	S/(N+D)	84		dB

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5016RP ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Analog Input Capacitance in Fine Charge Mode Unipolar Mode T_A=+25°C[1,3] Bipolar Mode T_A=+25°C[1,3]	C_{IN}		 375 220	pF
Digital Input Voltage[5,6]	V_{IH} V_{IL}	2.0	 0.8	V
Digital Input Current[5,6]	I_{IN}		±10	uA
Digital Output Voltage Logic "0", I_{SINK}=-1.6mA[5,6] Logic "1", I_{SOURCE}=100uA[5,6]	V_{OL} V_{OH}	 +VD-1.0	0.4	V
High Impedance State Output Current[5,6] Pins D_0 to D_{15} only	I_{OZ}		±10	uA
Conversion Time[1,6,7]	t_C		16.25	us
Acquisition Time T_A=+25°C[1,2,3,8]	t_{ACQ}		3.75	us
Throughput[1,2,6]	t_{PUT}	50		kHz
Positive Analog Supply Current[6,9] $+V_A$, $+V_D$=5.5V $-V_A$, $-V_D$=-5.5V	I_A+		19.0	mA
Negative Analog Supply Current[6,9] $+V_A$, $+V_D$=5.5V $-V_A$, $-V_D$=-5.5V	I_A-		19.0	mA

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5016RP ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Positive Digital Supply Current[6,9] $+V_A$, $+V_D$=5.5V $-V_A$, $-V_D$=-5.5V	I_D+		6.0	mA
Negative Digital Supply Current[6,9] $+V_A$, $+V_D$=5.5V $-V_A$, $-V_D$=-5.5V	I_D-		6.0	mA
Master Clock Frequency[10] Internally Generated, CLKIN=0V dc, $+V_D$, $+V_A$=4.5V, T_A=-55°C, $-V_D$, $-V_A$=-4.5V	f_{CLK}	1.75		MHz
HOLD\ Pulse Width[5,6,11]	t_{HPW}	$1/f_{CLK}$+50	t_C	ns
Data Delay Time[5,6,11]	t_{DD}		100	ns
EOC\ Pulse Width[5,6,11]	t_{EPW}	$4/f_{CLK}$ -20		ns
CAL, INTRLV\ to CS\ Low Setup Time[5,6,11]	t_{CS}	20		ns
AO to CS\ and RD\ Low Setup Time[5,6,11]	t_{AS}	20		ns
CS\ or RD\ High to AO Invalid Hold Time[5,6,11]	t_{AH}	50		ns
CS\ High To CAL, INTRLV\ Invalid Hold Time[5,6,11]	t_{CH}	50		ns
CS\ Low to Data Valid Access Time[5,6,11] RD\=logic "0"	t_{CA}		250	ns
RD\ Low to Data Valid Access Time[5,6,11] CS\=logic "0"	t_{RA}		250	ns

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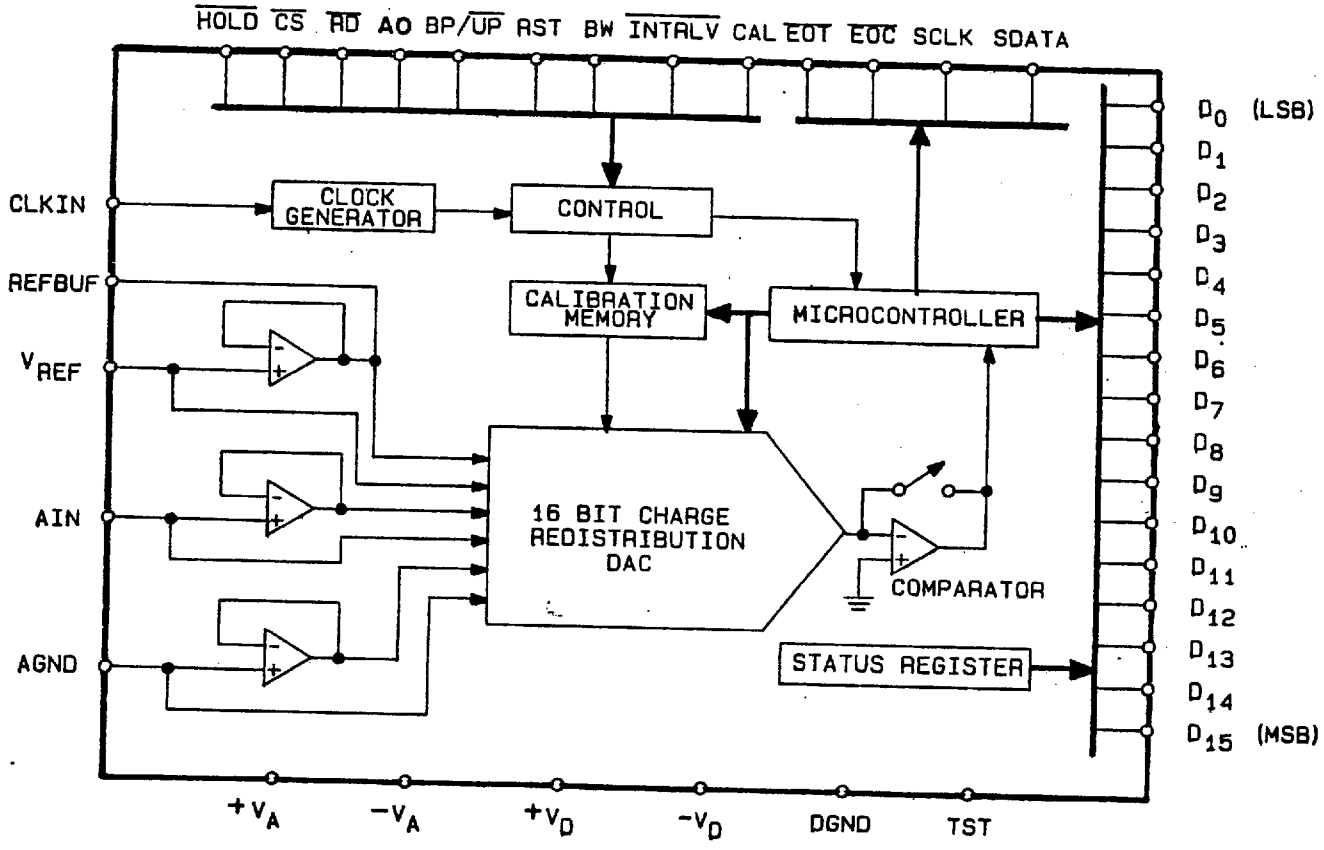
FUNCTION	HOLD	CS	CAL	INTRLV	RD	A0	RST
Hold and start convert		X	X	X	X	*	0
Initiate burst calibration	X	0	1	X	X	*	0
Stop burst cal and begin track	1	0	0	X	X	*	0
Initiate interleave cal	X	0	X	0	X	*	0
Terminate interleave cal	X	0	X	1	X	*	0
Read otput data	X	0	X	X	0	1	0
Read status register	1	0	X	X	0	0	0
High impedance data bus	X	1	X	X	X	*	X
High impedance data bus	X	X	X	X	1	*	X
Reset	X	X	X	X	X	X	1
Reset	0	0	X	X	X	0	X

* The status of A0 is not critical to the operation specified. However, A0 should not be low with CS and HOLD low, or a software reset will result.



TRUTH TABLE and FUNCTIONAL DIAGRAM

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5016RP ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Output Float Delay[5,6,11]	t_{FD}		250	ns
SDATA to SCLK Rising Setup Time[5,6,11]	t_{SS}	$2/f_{CLK}$ -50		ns
SCLK Rising to SDATA Hold Time[5,6,11]	t_{SH}	$2/f_{CLK}$ -100		ns

Notes:

1. $+V_A$, $+V_D$=+5.0V; $-V_A$, $-V_D$ =-5.0V; V_{REF} =+4.5V dc; f_{CLK} =4MHz; analog source impedance=200Ω; error tests are done after calibration at the temperature of interest.
2. Synchronous sampling mode (EOT\ connected to HOLD\), interleave disabled.
3. This parameter shall be measured only for initial characterization and after process or design changes which may affect this parameter.
4. Total drift over -55°C to +125°C since calibration at power-up at +25°C.
5. $+V_A$, $+V_D$=+5.0V dc ±10%; $-V_A$, $-V_D$=-5.0V dc ±10%.
6. This parameter is guaranteed, if not tested, at T_A=+25°C. This parameter is tested at T_A=-55°C and 125°C.
7. Measured from falling transition on HOLD\ to falling transition on EOC\.
8. Acquisition time is the time allowed by the converter for acquisition of the input voltage prior to conversion.
9. All outputs unloaded; all inputs swinging between $+V_D$ and 0V dc.
10. Externally supplied maximum clock frequency is 4MHz. Analog parametric measurements are done with the maximum external clock (See 1 above).
11. Inputs: logic "0"=0V, logic "1"=$+V_D$; C_L=50pF.

5016RP Package Ordering Guide

Package Style	Case Outline 1/	Description
D	D-40	40 Pin Dual In Line Package
Q	Q-44	44 Pin Quad Flat Package

Note:

1/ For outline information, see Appendix A (Package Information - Outline Dimension)

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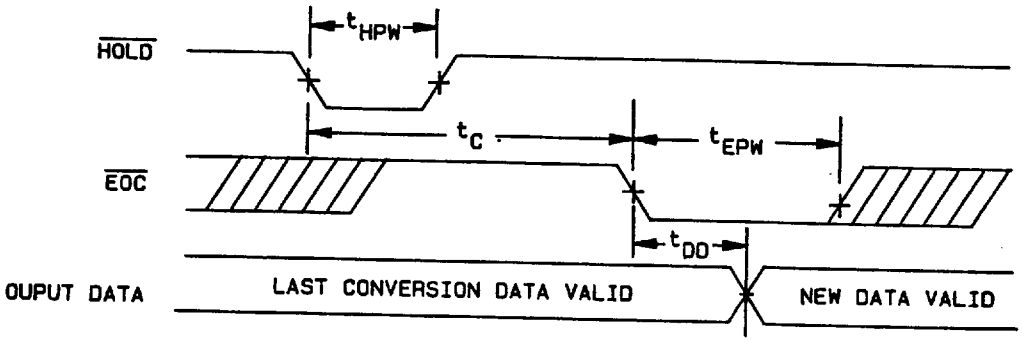

FIGURE 4. Conversion timing.

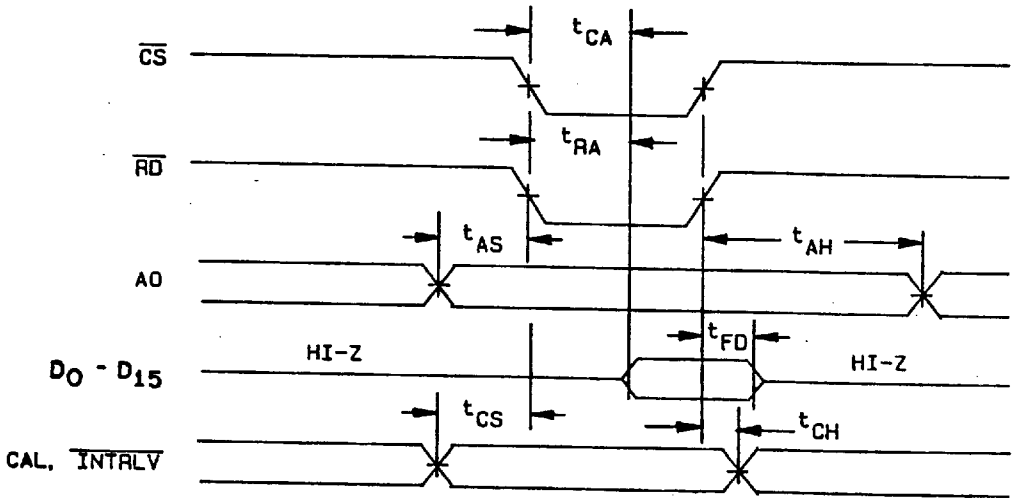

FIGURE 5. Read and calibration control timing.

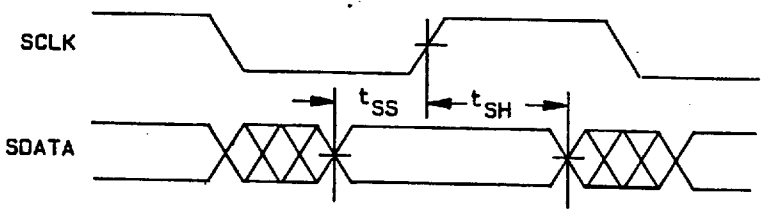

FIGURE 6. Serial output timing.

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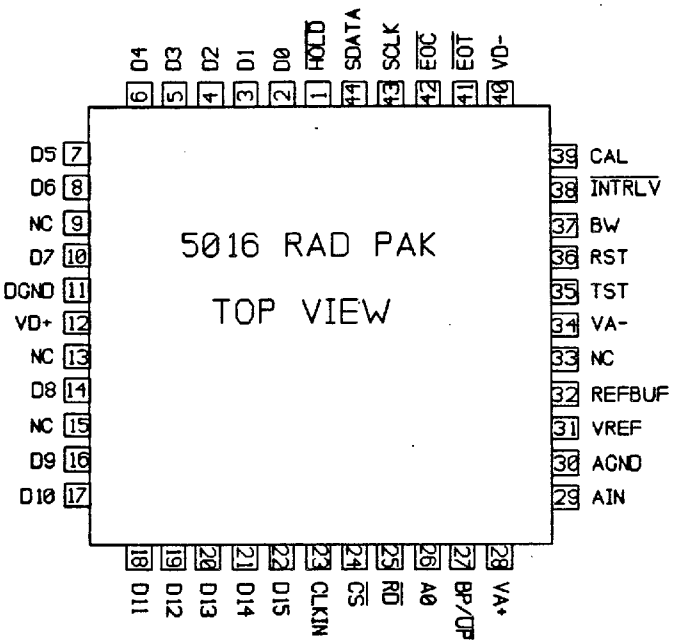

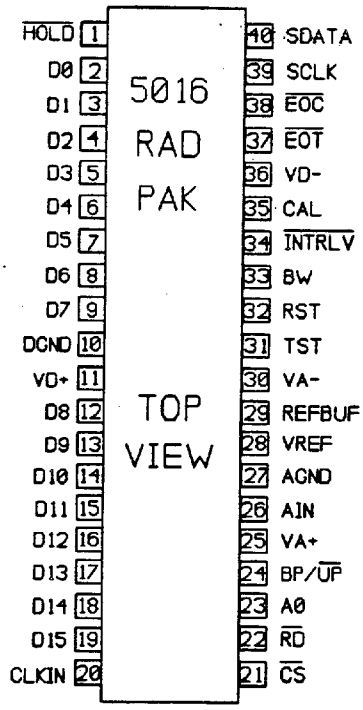

PIN CONFIGURATION

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