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DESCRIPTION

The M5M82C59AP,-2 is a programmable LSI for interrupt control. It is fabricated using silicon-gate CMOS technology and is designed to be used easily in connection with an 8085A, 8086 or 8088.

FEATURES

- Single 5V supply voltage
- TTL compatible
- Having internal anti-noise circuit on IR_0~IR_7 pins
- M5M82C59AP,-2 is compatible with M5L8259AP in pin connection.
- CALL instruction to the CPU is generated automatically
- Priority, interrupt mask and vectored address for each interrupt request input are programmable
- Up to 64 levels of interrupt requests can be controlled by cascading with M5M82C59AP,-2
- Polling functions

APPLICATION

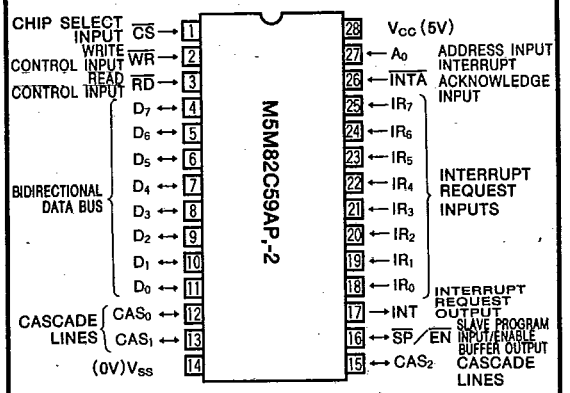
The M5M82C59AP,-2 can be used as an interrupt controller for CPUs 8085A, 8086 and 8088

FUNCTION

The M5M82C59AP,-2 is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight level requests and has built-in features for expandability to other M5M82C59AP,-2's. The priority and interrupt mask can be changed or reconfigured at any time by the main program.

When an interrupt is generated because of an interrupt request at 1 of the pins, the M5M82C59AP,-2 based on the mask and priority will output an INT to the CPU. After that, when an $\overline{INTA}$ signal is received from the CPU or the system controller, a CALL instruction and a programmed vector address is released onto the data bus.

PIN CONFIGURATION (TOP VIEW)



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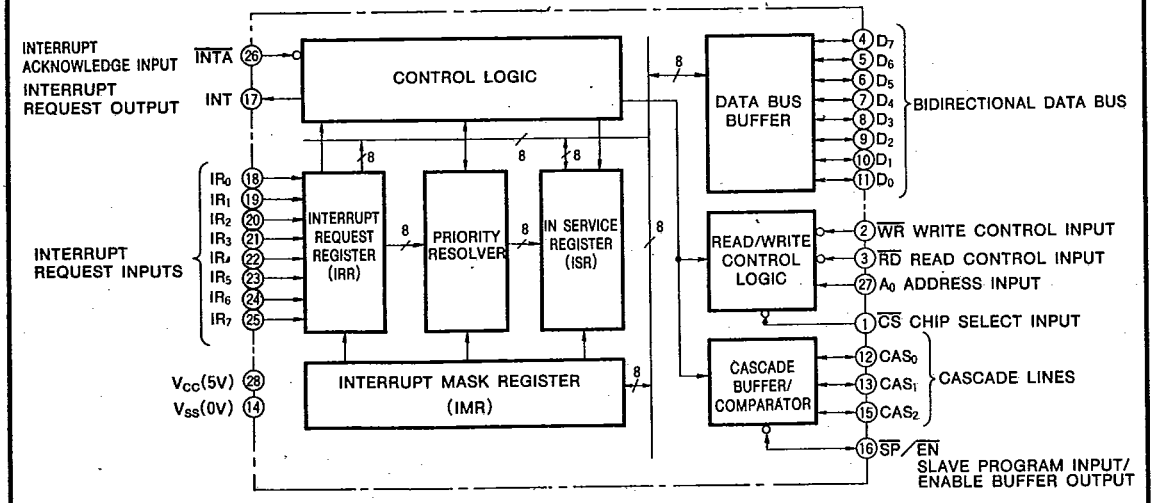
BLOCK DIAGRAM



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PIN DESCRIPTION

Symbol	Pin name	Input or output	Functional significance
$\overline{CS}$	Chip select input	Input	This input is active at low-level, but may be at high-level during interrupt request input and interrupt processing.
$\overline{WR}$	Write control input	Input	Command write control input from the CPU
$\overline{RD}$	Read control input	Input	Data read control input for the CPU
$D_7 \sim D_0$	Bidirectional data bus	Input/ output	Data and commands are transmitted through this bidirectional data bus to and from the CPU.
$CAS_2 \sim CAS_0$	Cascade lines	Input/ output	These pins are outputs for a master and inputs for a slave. And these pins of the master will be able to address each individual slave. The master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of $\overline{INTA}$.
$\overline{SP}/\overline{EN}$	Slave program input/ Enable buffer output	Input/ output	SP: In normal mode, a master is designated when $\overline{SP}/\overline{EN}$=1 and a slave is designated when $\overline{SP}/\overline{EN}$=0. EN: In the buffered mode, whenever the M5M82C59AP,-2's data bus output is enabled, its $\overline{SP}/\overline{EN}$ pin will go low.
INT	Interrupt request output	Output	This pin goes high whenever a valid interrupt is asserted.
$IR_7 \sim IR_0$	Interrupt request input	Input	The asynchronous interrupt inputs are active at high-level. The interrupt mask and priority of each interrupt input can be changed at any time. When using edge triggered mode, the rising edge (low to high) of the interrupt request and the high-level must be held until the first $\overline{INTA}$. For level triggered mode, the high-level must be held until the first $\overline{INTA}$.
$\overline{INTA}$	Interrupt acknowledge input	Input	When an interrupt acknowledge ($\overline{INTA}$) from the CPU is received, the M5M82C59AP releases a CALL instruction or vectored address onto the data bus.
A_0	A_0 address input	Input	This pin is normally connected to one of the address lines and acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ when writing commands or reading status registers.

OPERATION

The M5M82C59AP,-2 is interfaced with a standard system bus as shown in Fig. 1 and operates as an interrupt controller.

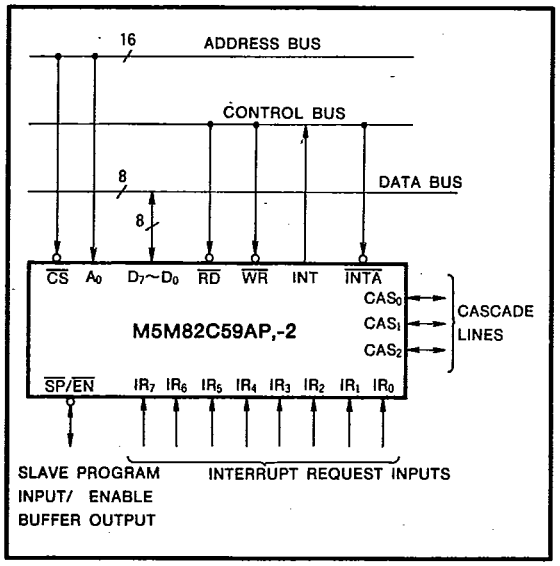

Fig. 1 The M5M82C59AP,-2 interfaces to standard system bus.

Table 1 M5M82C59AP,-2 basic operation

A_0	D_4	D_3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input operation (read)
0			0	1	0	IRR, ISR or Interrupting level→data bus
1			0	1	0	IMR→Data bus
						Output operation (write)
0	0	0	1	0	0	Data bus→OCW2
0	0	1	1	0	0	Data bus→OCW3
0	1	X	1	0	0	Data bus→ICW1
1	X	X	1	0	0	Data bus→OCW1, ICW2, ICW3, ICW4
						Disable function
X	X	X	1	1	0	Data bus→High-impedance
X	X	X	X	X	1	Data bus→High-impedance

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Interrupt Sequence

1. When the CPU is an 8085A:

(1) When one or more of the interrupt request inputs are raised high, the corresponding IRR bit(s) for the high-level inputs will be set.

(2) Mask state and priority levels are considered and, if appropriate, the M5M82C59AP,-2 sends an INT signal to the CPU.

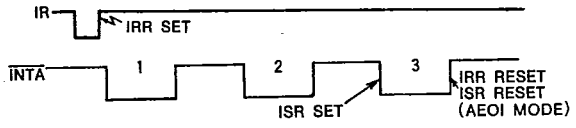
(3) The acknowledgement of the CPU to the INT signal, the CPU issues an $\overline{INTA}$ pulse to the M5M82C59AP,-2.

(4) Upon receiving the first $\overline{INTA}$ pulse from the CPU, a CALL instruction is released onto the data bus.

(5) A CALL is a 3-byte instruction, so additional two $\overline{INTA}$ pulses are issued to the M5M82C59AP,-2 from the CPU.

(6) These two $\overline{INTA}$ pulses allow the M5M82C59AP,-2 to release the program address onto the data bus. The low-order 8-bit vectored address is released at the second $\overline{INTA}$ pulse and the high-order 8-bit vectored address is released at the third $\overline{INTA}$ pulse. The ISR bit corresponding to the interrupt request input is set upon receiving the third $\overline{INTA}$ pulse from the CPU, and the corresponding IRR bit is reset.

(7) This completes the 3-byte CALL instruction and the interrupt routine will be serviced. The ISR bit is reset at the trailing edge of the third $\overline{INTA}$ pulse in the AEOI mode. In the other modes the ISR bit is not reset until an EOI command is issued.



2. When the CPU is an 8086 or 8088:

(1) When one or more of the interrupt request inputs are raised high, the corresponding IRR bit(s) for the high-level inputs will be set.

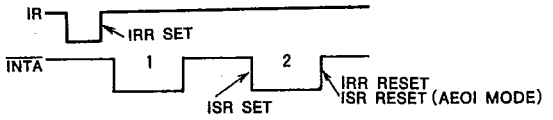
(2) Mask state and priority levels are considered and if appropriated, the M5M82C59AP,-2 sends an INT signal to the CPU.

(3) As an acknowledgement to the INT signal, the CPU issues an $\overline{INTA}$ pulse to the M5M82C59AP,-2.

(4) Upon receiving the first $\overline{INTA}$ pulse from the CPU, the M5M82C59AP,-2 does not drive the data bus, and the data bus keeps high-impedance state.

(5) When the second $\overline{INTA}$ pulse is issued from the CPU, an 8-bit pointer is released onto the data bus.

(6) This completes the interrupt cycle and the interrupt routine will be serviced. The ISR bit is reset at the trailing edge of the second $\overline{INTA}$ pulse in the AEOI mode. In the other modes the ISR bit is not reset until an EOI command is issued from the CPU.



The interrupt request input must be held at high-level until the first $\overline{INTA}$ pulse is issued. If it is allowed to return to low-level before the first $\overline{INTA}$ pulse is issued, an interrupt request in IR_7 is executed. However, in this case the ISR bit is not set.

This is a function for a noise countermeasure of interrupt request inputs. In the interrupt routine of IR_7, if ISR is checked by software either the interrupt by noise or real interrupt can be acknowledged. In the state of edge trigger mode normally the interrupt request inputs hold high-level and its input low-level pulse in the case of interrupt.

Interrupt sequence outputs

1. When the CPU is an 8085A:

A CALL instruction is released onto the data bus when the first $\overline{INTA}$ pulse is issued. The low-order 8 bits of the vectored address are released when the second $\overline{INTA}$ pulse is issued, and the high-order 8 bits are released when the third $\overline{INTA}$ pulse is issued. The format of these three outputs is shown in Table 2.

Table 2 Formats of Interrupt CALL Instruction and vectored address

First $\overline{INTA}$ pulse (CALL instruction)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	1	1	0	1

Second $\overline{INTA}$ pulse (low-order 8-bit of vectored address)

IR	Interval= 4							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_0	A_7	A_6	A_5	0	0	0	0	0
IR_1	A_7	A_6	A_5	0	0	1	0	0
IR_2	A_7	A_6	A_5	0	1	0	0	0
IR_3	A_7	A_6	A_5	0	1	1	0	0
IR_4	A_7	A_6	A_5	1	0	0	0	0
IR_5	A_7	A_6	A_5	1	0	1	0	0
IR_6	A_7	A_6	A_5	1	1	0	0	0
IR_7	A_7	A_6	A_5	1	1	1	0	0

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IR	Interval=8							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_0	A_7	A_6	0	0	0	0	0	0
IR_1	A_7	A_6	0	0	1	0	0	0
IR_2	A_7	A_6	0	1	0	0	0	0
IR_3	A_7	A_6	0	1	1	0	0	0
IR_4	A_7	A_6	1	0	0	0	0	0
IR_5	A_7	A_6	1	0	1	0	0	0
IR_6	A_7	A_6	1	1	0	0	0	0
IR_7	A_7	A_6	1	1	1	0	0	0

Third $\overline{INTA}$ pulse (high-order 8 bits of vectored address)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8

2. When the CPU is an 8086 or 8088:

The data bus keeps a high-impedance state when the first $\overline{INTA}$ pulse is issued. Then the pointer $T_7 \sim T_0$ is released when the next $\overline{INTA}$ pulse is issued. The content of the pointer $T_7 \sim T_0$ is shown in Table 3. The $T_2 \sim T_0$ are a binary code corresponding to the interrupt request level, $A_{10} \sim A_5$ are unused and ADI mode control is ignored.

Table 3 Contents of interrupt pointer
Second $\overline{INTA}$ pulse (8-bit pointer)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_0	T_7	T_6	T_5	T_4	T_3	0	0	0
IR_1	T_7	T_6	T_5	T_4	T_3	0	0	1
IR_2	T_7	T_6	T_5	T_4	T_3	0	1	0
IR_3	T_7	T_6	T_5	T_4	T_3	0	1	1
IR_4	T_7	T_6	T_5	T_4	T_3	1	0	0
IR_5	T_7	T_6	T_5	T_4	T_3	1	0	1
IR_6	T_7	T_6	T_5	T_4	T_3	1	1	0
IR_7	T_7	T_6	T_5	T_4	T_3	1	1	1

Interrupt Request Register (IRR), In-service Register (ISR)

As interrpt requests are received at inputs $IR_7 \sim IR_0$, the corresponding bits of IRR are set and as an interrupt request is serviced the corresponding bit of ISR is set. The IRR is used to store all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are being serviced. The status of these two registers can be read. These two registers are connected through the priority resolver.

An interrupt requst received by IR_n is acknowledged on the leading edge when in the edge triggered mode or it is acknowledged on the level when in the level triggered mode. After that an INT signal is released and the interrupt request signal is latched in the corresponding IRR bit if the high-level is held until the first $\overline{INTA}$ pulse is issued. It is important to remember that the interrupt request signal must be held at high-level until the first $\overline{INTA}$ pulse is issued.

The interrupt request latching in the IRR causes a signal to be sent to the priority resolver unless it is masked out. When the priority resolver receives the signals it selects the highest priority interrupt request latched in IRR. The ISR is set when the last $\overline{INTA}$ pulse is issued while the corresponding bit of IRR is reset and the other bits of IRR are unaffected.

The bit of ISR that was set is not reset during the interrupt routine, but is reset at the end of the routine by the EOI command (end of interrupt) or by the trailing edge of the last $\overline{INTA}$ pulse in AEOI mode.

Priority Resolver

The priority resolver examines all of the interrupt requests set in IRR to determine and selects the highest priority. The ISR bit corresponding to the selected (highest priority) request is set by the last $\overline{INTA}$ pulse.

Interrupt Mask Register (IMR)

The contents of the interrupt mask register are used to mask out (disable) interrupt requests of selected interrupt request pins. Each terminal is independently masked so that masking a high priority interrupt does not influence the lower or higher priority interrupts. Therefore the contents of IMR selectively enable reading.

Interrupt Request Output (INT)

The interrupt request output connects directly to the interrupt input of the CPU. The output level is compatible with the input level required for the CPUs.

The INT output is set to low after the interrupt sequence ends, irrespective of the current mode. When the power is turned on, the INT output (high output) may appear but is reset to low by executing ICW1.

Interrupt Acknowledge Input ($\overline{INTA}$)

The CALL instruction and vectored address are released onto the data bus by the $\overline{INTA}$ pulse.

Data Bus Buffer

The data bus buffer is a 3-state bidirectional data bus buffer that is used to interface with the system bus. Write commands to the M5M82C59AP,-2, CALL instructions, vectored addresses, status information, etc. are transferred through the data bus buffer.

Read/Write Control Logic

The read/write control logic is used to control functions such as receiving commands from the CPU and supplying status information to the data bus.

Chip Select ($\overline{CS}$)

The M5M82C59AP,-2 is selected (enabled) when $\overline{CS}$ is at lowlevel, but during interrupt request input or interrupt processing it may be high-level.

Write Control Input ($\overline{WR}$)

When $\overline{WR}$ goes to low-level the M5M82C59AP,-2 can be written.

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Read Control Input ($\overline{RD}$)

When $\overline{RD}$ goes low status information in the internal register of the M5M82C59AP,-2 can be read through the data bus.

Address Input (A_0)

The address input is normally connected with one of the address lines and is used along with $\overline{WR}$ and $\overline{RD}$ to control write commands and reading status information.

Cascade Buffer/Comparator

The cascade buffer/comparator stores or compares identification codes. The three cascade lines are output when the M5M82C59AP,-2 is a master or input when it is a slave. The identification code on the cascade lines select it as master or slave.

PROGRAMMING THE M5M82C59AP,-2

The M5M82C59AP,-2 is programmed through the Initialization Command Word (ICW) and the operation command word (OCW). The following explains the functions of these two commands.

Initialization Command Words (ICW_S)

The initialization command word is used for the initial setting of the M5M82C59AP,-2. There are four commands in this group and the following explains the details of these four commands.

ICW1

The meaning of the bits of ICW1 is explained in Fig. 3 along with the functions. ICW1 contains vectored address bits $A_7 \sim A_5$, a flag indicating whether interrupt input is edge triggered or level triggered, CALL address interval, whether a single M5M82C59AP,-2 or the cascade mode is used, and whether ICW4 is required or not.

Whenever a command is issued with $A_0=0$ and $D_4=1$, this is interpreted as ICW1 and the following will automatically occur.

(a) The interrupt mask register (IMR) is cleared.
(b) The interrupt request input IR_7 is assigned the lowest priority.
(c) The special mask mode is cleared and the status read is set to the interrupt request register (IRR).
(d) When IC4=0 all bits in ICW4 are set to zero.

ICW2

ICW2 contains vectored address bits $A_{15} \sim A_8$ or interrupt type $T_7 \sim T_3$, and the format is shown in Fig. 3.

ICW3

When SNGL=1 it indicates that only a single M5M82C59AP,-2 is used in the system, in which case ICW3 is not valid. When SNGL=0, ICW3 is valid and indicates cascade connections with other M5M82C59AP,-2 devices. In the master mode, a "1" is set for each slave.

When the CPU is an 8085A the CALL instruction is released from the master at the first $\overline{INTA}$ pulse and the vectored address is released onto the data bus from the slave at the second and third $\overline{INTA}$ pulses.

When the CPU is a 8086 the master and slave are in high-impedance at the first $\overline{INTA}$ pulse and the pointer is released onto the data bus from the slave at the second $\overline{INTA}$ pulse.

The master mode is specified when $\overline{SP}/\overline{EN}$ pin is highlevel or BUF=1 and M/S=1 in ICW4, and slave mode is specified when $\overline{SP}/\overline{EN}$ pin is low-level or BUF=1 and M/S=0 in ICW4. In the slave mode, three bits $ID_2 \sim ID_0$ identify the

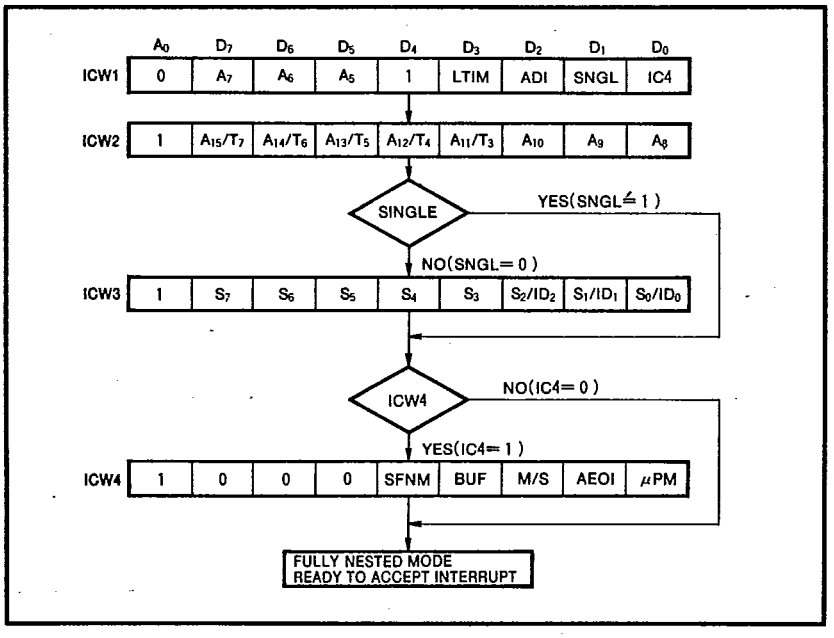


Fig. 2 Initialization sequence

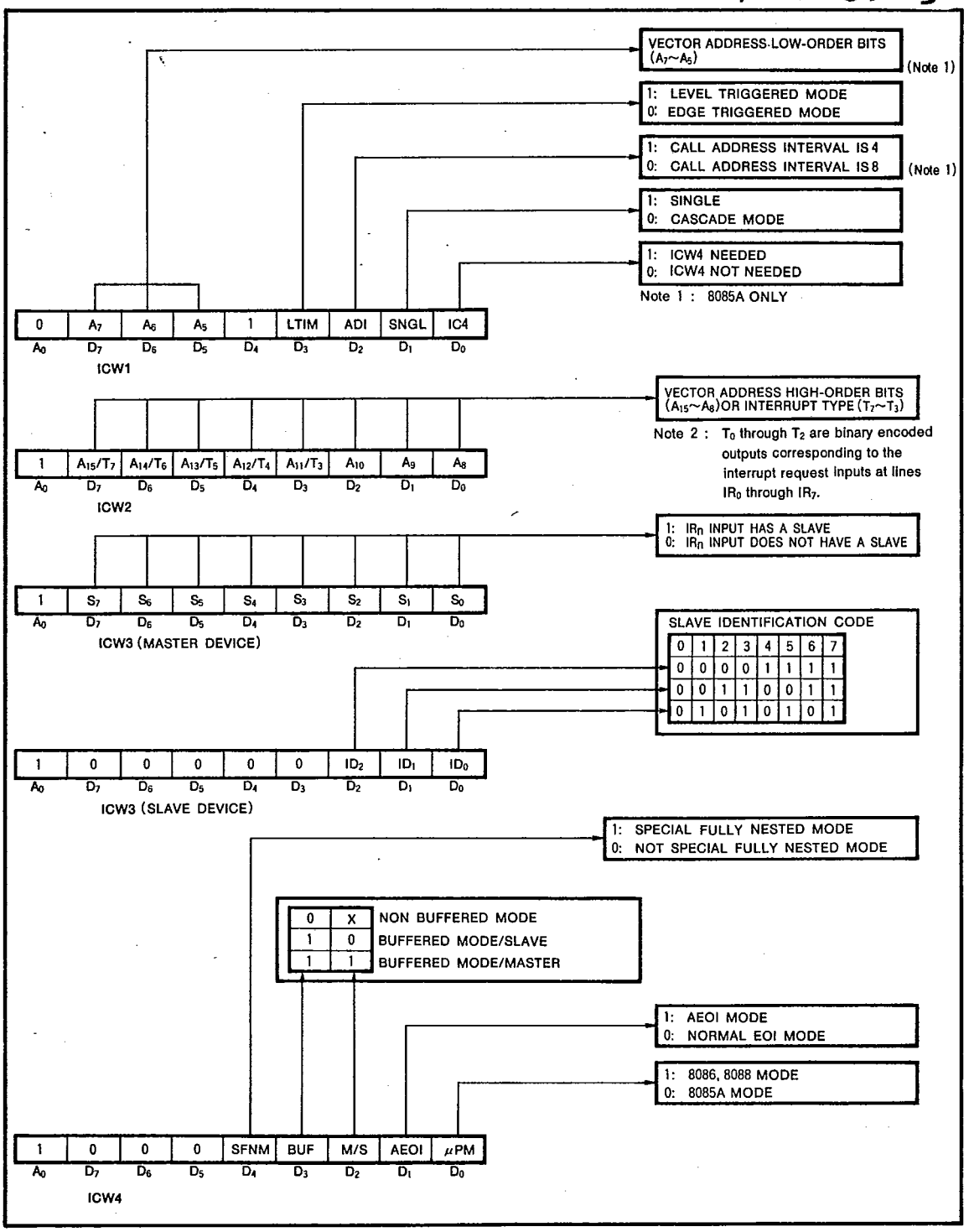


Fig. 3 Initialization command word format

slave. And then when the slave code released on the cascade lines from the master, matches the assigned ID code, the vectored address is released by it onto the data bus at the next $\overline{INTA}$ pulse.

ICW4

Only when IC4=1 in ICW1 is ICW4 valid. Otherwise all bits are set to zero. When ICW4 is valid it specifies special fully nested mode, buffer mode master/slave, automatic EOI and microprocessor mode. The format of ICW4 is shown in Fig. 3.

Operation Command Words (OCW_S)

The operation command words are used to change the contents of IMR, the priority of interrupt request inputs and the special mask. After the ICW are programmed into the M5M82C59AP,-2, the device is ready to accept interrupt requests. There are three types of OCW_S; explanation of each follows, and the format of OCW_S is shown in Fig. 4.

OCW1

The meaning of the bits of OCW1 are explained in Fig. 4 along with their functions. Each bit of IMR can be independently changed (set or reset) by OCW1.

OCW2

The OCW2 is used for issuing EOI commands to the M5M82C59AP and for changing the priority of the interrupt request inputs.

OCW3

The OCW3 is used for specifying special mask mode, poll mode and status register read.

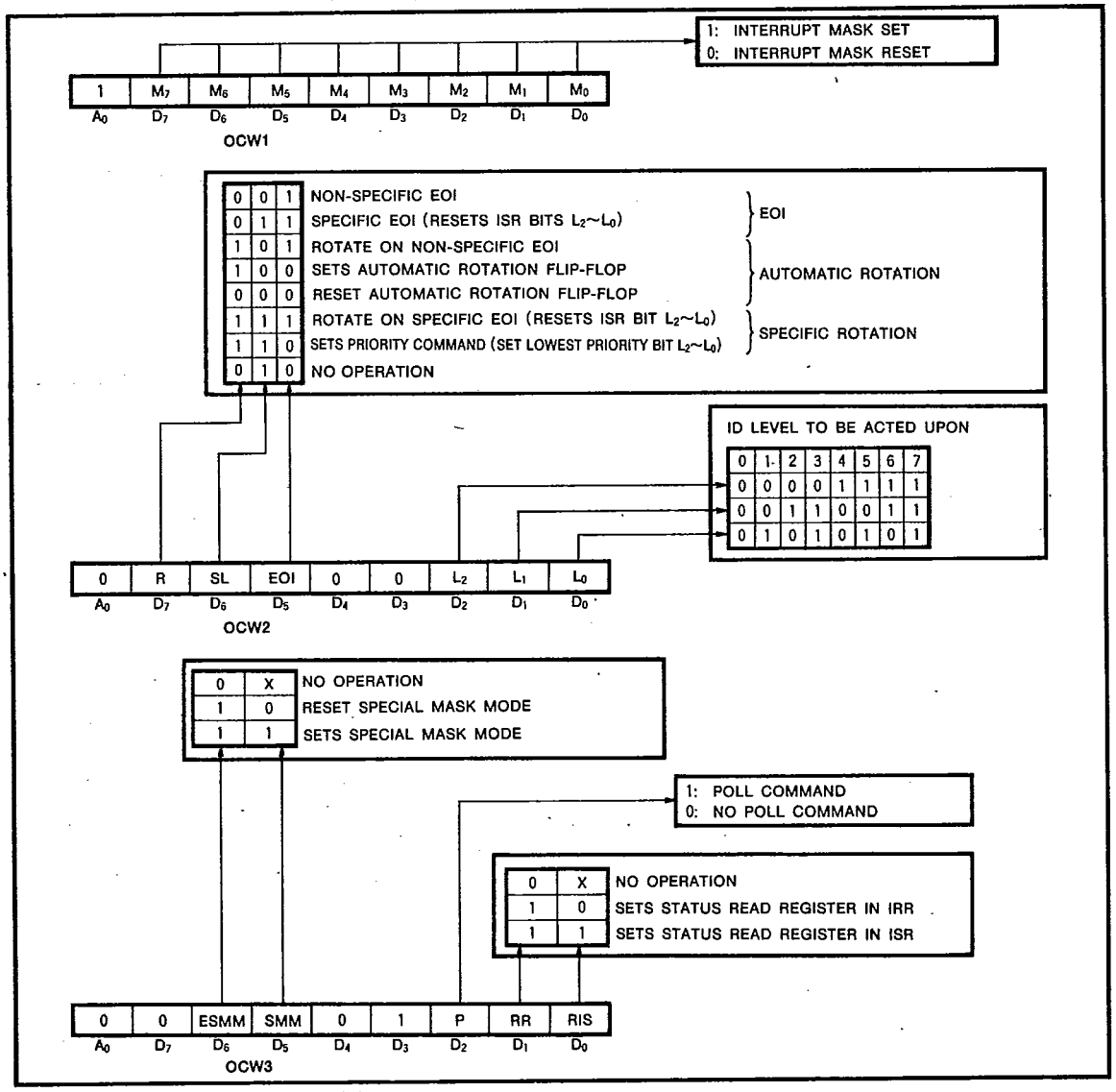


Fig. 4 Operation command word format

FUNCTION OF COMMAND

Interrupt masks

The mask register contains a mask for each individual interrupt request. These interrupt masks can be changed by programming using OCW1.

Special mask mode

When an interrupt request is acknowledged and the ISR bit corresponding to the interrupt request is not reset by EOI command (which means an interrupt service routine is executing) lower priority interrupt requests are ignored.

In special mask mode interrupt requests received at interrupt request inputs which are masked by OCW1 are disabled, but interrupts at all levels that are not masked are possible. This means that in the mask mode all level of interrupts are possible or individual inputs can be selectively programmed so all interrupts at the selected inputs are disabled. The masks are stored in IMR and special mask is set/reset by executing OCW3.

Buffered mode

The buffered mode will structure the M5M82C59AP,-2 to send an enable signal on $\overline{SP}/\overline{EN}$ to enable the data bus buffer, when the data bus requires the data bus buffer or when cascading mode is used. In this mode, when data bus output of the M5M82C59AP,-2 is enabled, the $\overline{SP}/\overline{EN}$ output becomes low-level. This allows the M5M82C59AP,-2 to be programmed whether it is a master or a slave by software. The buffered mode is set/reset by executing ICW4.

Fully nested mode

The fully nested mode is the mode when no mode is specified and is the usual operational mode. In this mode, the priority of interrupt request terminals is fixed from the lowest IR_7 to the highest IR_0. When an interrupt request is acknowledged the CALL instruction and vectored address are released onto the data bus. At the same time the ISR bit corresponding to the accepted interrupt request is set. This ISR bit remains set until it is reset by the input of an EOI command or until the trailing edge of last $\overline{INTA}$ pulse in AEOI mode. While an interrupt service routine is being executed, interrupt requests of same or lower priority are disabled while the bit of ISR remains set. The priorities can be changed by OCW2.

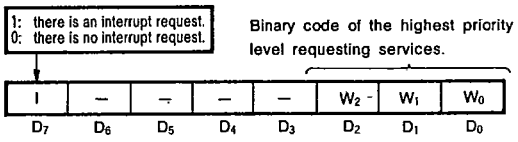
Special fully nested mode

The special fully nested mode will be used when cascading is used and this mode will be programmed to the master by ICW4. The special fully nested mode is the same as the fully nested mode with the following two exceptions.

1. When an interrupt from a certain slave is being serviced, this slave is not locked out from the master priority logic. Higher priority interrupts within the slave will be recognized by the master and the master will initiate an interrupt request to the CPU. In general in the normal fully nested mode, a serviced slave is locked out from the master's priority, and so higher priority interrupts from the same slave are not serviced.
2. When an interrupt from a certain slave is being serviced the software must check ISR to determine if there are additional interrupts requests to be serviced. If the ISR bit is 0 the EOI command may be sent to the master too. But if it is not 0 the EOI command should not be sent to the master.

Poll mode

The poll mode is useful when the internal enable flip-flop of the microprocessor is reset, and interrupt input is disabled. Service to the device is achieved by a programmer initiative using a poll command. In the poll mode the M5M82C59AP,-2 at the next $\overline{RD}$ pulse puts 8 bits on the data bus which indicates whether there is an interrupt request and reads the priority level. The format of the information on the data bus is as shown below.



When I=0 (no interrupt request), $W_2 \sim W_0$ is 111. The poll is valid from $\overline{WR}$ to $\overline{RD}$ and interrupt is frozen. This mode can be used for processing common service routines for interrupts from more than one line and does not require any $\overline{INTA}$ sequence. Poll command is issued by setting P=1 in OCW3.

End of Interrupt (EOI) and specific EOI (SEOI)

An EOI command is required by the M5M82C59AP,-2 to reset the ISR bit. So an EOI command must be issued to the M5M82C59AP,-2 before returning from an interrupt service routine.

When AEOI is selected in ICW4, the ISR bit can be reset at the trailing edge of the last $\overline{INTA}$ pulse. When AEOI is not selected the ISR bit is reset by the EOI command issued to the M5M82C59AP,-2 before returning from an interrupt service routine. When programmed in the cascade mode the EOI command must be issued to the master once and to corresponding slave once.

There are two forms of EOI command, specific EOI and non-specific EOI. When the M5M82C59AP,-2 is used in the fully nested mode, the ISR bit being serviced is reset by the EOI command. When the non-specific EOI is issued the M5M82C59AP,-2 will automatically reset the highest ISR bit of those that are set. Other ISR bits are reset by a specific EOI and the bit to be reset is specified in the EOI by the program. The SEOI is useful in modes other than fully nested mode. When the M5M82C59AP,-2 is in special mask mode ISR bits masked in IMR are not reset by EOI. EOI and SEOI are selected when OCW2 is executed.

Automatic EOI (AEOI)

In the AEOI mode the M5M82C59AP,-2 executes non-specific EOI command automatically at the trailing edge of the last $\overline{INTA}$ pulse. When AEOI = 1 in ICW4, the M5M82C59AP,-2 is put in AEOI mode continuously until reprogrammed in ICW4.

Automatic rotation

The automatic rotation mode is used in applications where many interrupt requests of the same level are expected such as multichannel communication systems. In this mode when an interrupt request is serviced, that request is assigned the lowest priority so that if there are other interrupt requests they will have higher priorities. This means that the next request on the interrupt request being serviced must wait until the other interrupt requests are serviced (worst case is waiting for all 7 of the other controllers to be serviced). The priority and serving status are rotated as shown in Fig. 5.

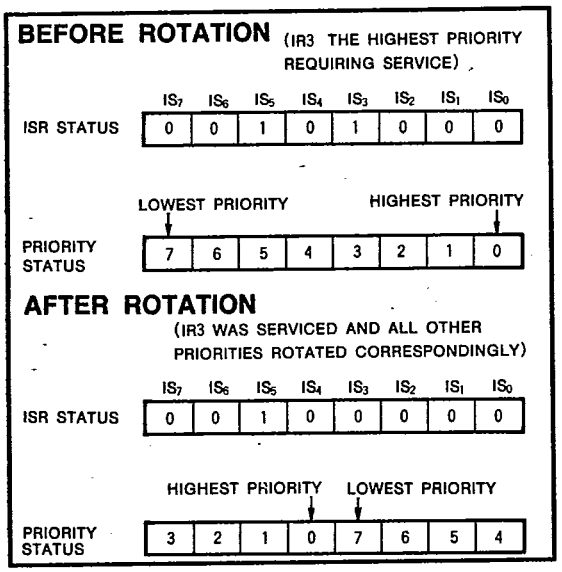


Fig. 5 An example of priority rotation

In the non-specific EOI command automatic rotation mode is selected when R=1, EOI=1, SL=0 in OCW2. The internal priority status is changed by EOI or AEOI commands. The rotation priority A flip-flop is set by R=1, EOI=0 and SL=0 which is useful when the M5M82C59AP,-2 is used in the AEOI mode.

Specific rotation

Specific rotation gives the user versatile capabilities in interrupt controlled operations. It serves in those applications in which a specific device's interrupt priority must be altered. As opposed to automatic rotation which automatically sets priorities, specific rotation is completely user controlled. That is, the user selects the interrupt level that is to receive lowest or highest priority. Priority changes can be executed during an EOI command.

Level triggered mode/Edge triggered mode

Selection of level or edge triggered mode of the M5M82C59AP,-2 is made by ICW1, When using edge triggered mode not only is a transition from low to high required, but the high-level must be held until the first $\overline{INTA}$. If the high-level is not held until the first $\overline{INTA}$, the interrupt request will be treated as if it were input on IR_7, except that the ISR bit is not set. When level triggered mode is used the functions are the same as edge triggered mode except that the transition from low to high is not required to trigger the interrupt request.

In the level triggered mode and using AEOI mode together, if the high-level is held too long the interrupt will occur immediately. To avoid this situation interrupts should be kept disabled until the end of the service routine or until the IR input returns low. In the edge triggered mode this type of mistake is not possible because the interrupt request is edge triggered.

Reading the M5M82C59AP,-2 internal status

The contents of IRR and ISR can be read by the CPU with status read. When an OCW3 is issued to the M5M82C59AP,-2 and an $\overline{RD}$ pulse issued the contents of IRR or ISR can be released onto the data bus. A special command is not required to read the contents of IMR. The contents of IMR can be released onto the data bus by issuing an $\overline{RD}$ pulse when A_0=1. There is no need to issue a read register command every time the IRR or ISR is to be read. Once a read register command is received by the M5M82C59AP,-2, it remains valid until it is changed. Remember that the programmer must issue a poll command every time to check whether there is an interrupt request and read the priority level. Polling overrides status read when P=1, RR=1 in OCW3.

CASCADING

The M5M82C59AP,-2 can be interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels. A system of three units that can be used with the 8085A is shown in Fig. 6.

The master can select a slave by outputting its identification code through the three cascade lines. The INT output of each slave is connected to the master interrupt request inputs. When an interrupt request of one of the slaves is to be serviced the master outputs the identification code of the slave through the cascade lines, so the slave will release the vectored address on the next $\overline{INTA}$ pulse.

The cascade lines of the master are nomally low, and will contain the slave identification code from the leading edge of the first $\overline{INTA}$ pulse to the trailing edge of the last $\overline{INTA}$ pulse. The master and slave can be programmed to work in different modes. ICWs must be issued for each device, and EOI commands must be issued twice: once for the master and once for the corresponding slave. Each $\overline{CS}$ of the M5M82C59AP,-2 requires an address decoder.

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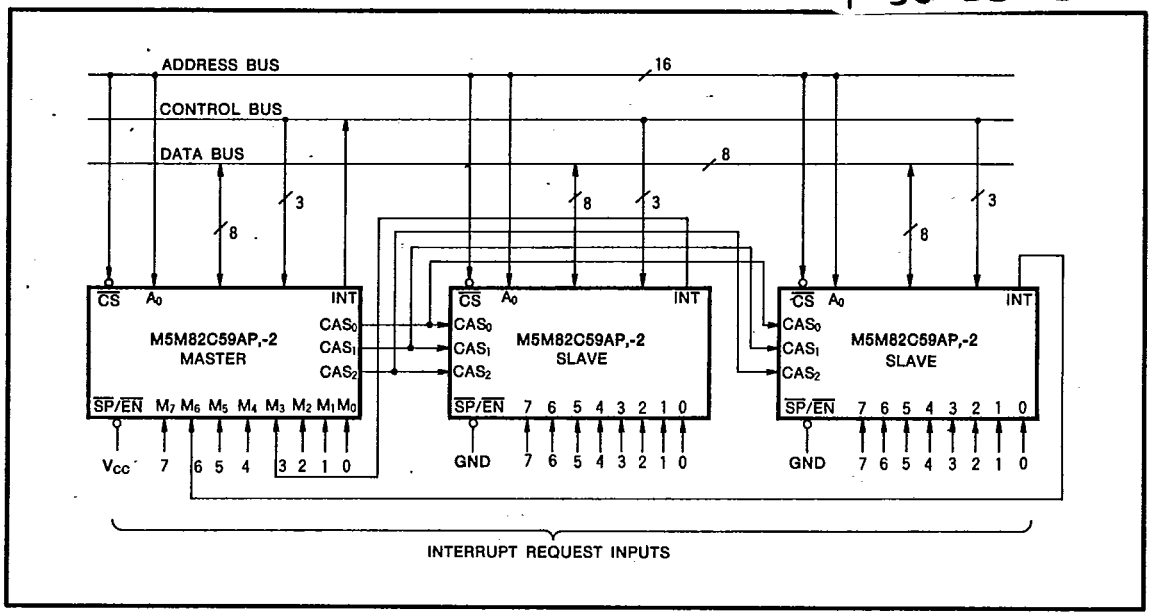
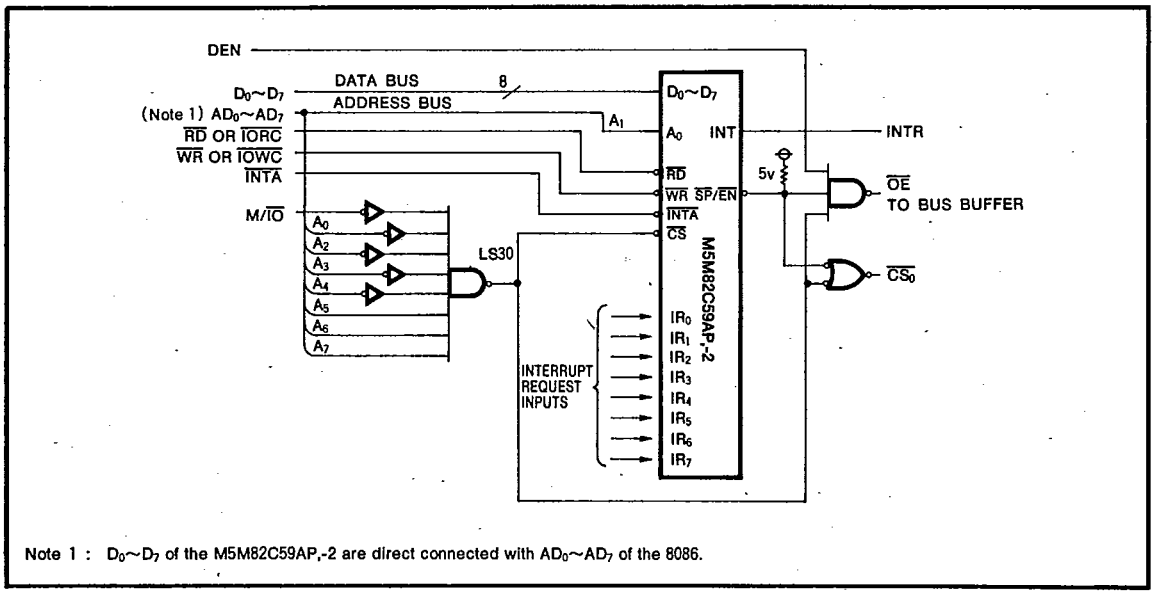


Fig. 6 Cascading the M5M82C59AP,-2



Note 1 : $D_0 \sim D_7$ of the M5M82C59AP,-2 are direct connected with $AD_0 \sim AD_7$ of the 8086.

Fig. 7 Example of interface with the 8086

MITSUBISHI ELECTRIC

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INSTRUCTION SET

Item / Number	Mnemonic	Instruction code									Function			
		A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	ICW4 required?	Intervel	Single	Trigger
1	ICW1 A	0	A_7	A_6	A_5	1	0	1	1	0	N	4	Y	E
2	ICW1 B	0	A_7	A_6	A_5	1	1	1	1	0	N	4	Y	L
3	ICW1 C	0	A_7	A_6	A_5	1	0	1	0	0	N	4	N	E
4	ICW1 D	0	A_7	A_6	A_5	1	1	1	0	0	N	4	N	L
5	ICW1 E	0	A_7	A_6	0	1	0	0	1	0	N	8	Y	E
6	ICW1 F	0	A_7	A_6	0	1	1	0	1	0	N	8	Y	L
7	ICW1 G	0	A_7	A_6	0	1	0	0	0	0	N	8	N	E
8	ICW1 H	0	A_7	A_6	0	1	1	0	0	0	N	8	N	L
9	ICW1 I	0	A_7	A_6	A_5	1	0	1	1	1	Y	4	Y	E
10	ICW1 J	0	A_7	A_6	A_5	1	1	1	1	1	Y	4	Y	L
11	ICW1 K	0	A_7	A_6	A_5	1	0	1	0	1	Y	4	N	E
12	ICW1 L	0	A_7	A_6	A_5	1	1	1	0	1	Y	4	N	L
13	ICW1 M	0	A_7	A_6	0	1	0	0	1	1	Y	8	Y	E
14	ICW1 N	0	A_7	A_6	0	1	1	0	1	1	Y	8	Y	L
15	ICW1 O	0	A_7	A_6	0	1	0	0	0	1	Y	8	N	E
16	ICW1 P	0	A_7	A_6	0	1	1	0	0	1	Y	8	N	L
17	ICW2	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	8-bit vectored address			
18	ICW3 M	1	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0	Slave connections (master mode)			
19	ICW3 S	1	0	0	0	0	0	ID_2	ID_1	ID_0	Slave identification code (slave mode)			
											SFNM	BUF	AEOI	8086
20	ICW4 A	1	0	0	0	0	0	0	0	0	N	N	N	N
21	ICW4 B	1	0	0	0	0	0	0	0	1	N	N	N	Y
22	ICW4 C	1	0	0	0	0	0	0	1	0	N	N	Y	N
23	ICW4 D	1	0	0	0	0	0	0	1	1	N	N	Y	Y
24	ICW4 E	1	0	0	0	0	0	1	0	0	N	N	N	N
25	ICW4 F	1	0	0	0	0	0	1	0	1	N	N	N	Y
26	ICW4 G	1	0	0	0	0	0	1	1	0	N	N	Y	N
27	ICW4 H	1	0	0	0	0	0	1	1	1	N	N	Y	Y
28	ICW4 I	1	0	0	0	0	1	0	0	0	N	Y S	N	N
29	ICW4 J	1	0	0	0	0	1	0	0	1	N	Y S	N	Y
30	ICW4 K	1	0	0	0	0	1	0	1	0	N	Y S	Y	N
31	ICW4 L	1	0	0	0	0	1	0	1	1	N	Y S	Y	Y
32	ICW4 M	1	0	0	0	0	1	1	0	0	N	Y M	N	N
33	ICW4 N	1	0	0	0	0	1	1	0	1	N	Y M	N	Y
34	ICW4 O	1	0	0	0	0	1	1	1	0	N	Y M	Y	N
35	ICW4 P	1	0	0	0	0	1	1	1	1	N	Y M	Y	Y
36	ICW4 NA	1	0	0	0	1	0	0	0	0	Y	N	N	N
37	ICW4 NB	1	0	0	0	1	0	0	0	1	Y	N	N	Y
38	ICW4 NC	1	0	0	0	1	0	0	1	0	Y	N	Y	N
39	ICW4 ND	1	0	0	0	1	0	0	1	1	Y	N	Y	Y
40	ICW4 NE	1	0	0	0	1	0	1	0	0	Y	N	N	N
41	ICW4 NF	1	0	0	0	1	0	1	0	1	Y	N	N	Y
42	ICW4 NG	1	0	0	0	1	0	1	1	0	Y	N	Y	N
43	ICW4 NH	1	0	0	0	1	0	1	1	1	Y	N	Y	Y
44	ICW4 NI	1	0	0	0	1	1	0	0	0	Y	Y S	N	N
45	ICW4 NJ	1	0	0	0	1	1	0	0	1	Y	Y S	N	Y
46	ICW4 NK	1	0	0	0	1	1	0	1	0	Y	Y S	Y	N
47	ICW4 NL	1	0	0	0	1	1	0	1	1	Y	Y S	Y	Y
48	ICW4 NM	1	0	0	0	1	1	1	0	0	Y	Y M	N	N
49	ICW4 NN	1	0	0	0	1	1	1	0	1	Y	Y M	N	Y
50	ICW4 NO	1	0	0	0	1	1	1	1	0	Y	Y M	Y	N
51	ICW4 NP	1	0	0	0	1	1	1	1	1	Y	Y M	Y	Y
52	OCW1	1	M_7	M_6	M_5	M_4	M_3	M_2	M_1	M_0	Interrupt mask			
53	OCW2 E	0	0	0	1	0	0	0	0	0	EOI			
54	OCW2 SE	0	0	1	1	0	0	L_2	L_1	L_0	SEOI			
55	OCW2 RE	0	1	0	1	0	0	0	0	0	Rotate on Non-Specific EOI command (Automatic rotation)			
56	OCW2 RSE	0	1	1	1	0	0	L_2	L_1	L_0	Rotate on Specific EOI command (Specific rotation)			
57	OCW2 R	0	1	0	0	0	0	0	0	0	Rotate in AEOI Mode (SET)			
58	OCW2 CR	0	0	0	0	0	0	0	0	0	Rotate in AEOI Mode (CLEAR)			
59	OCW2 RS	0	1	1	0	0	0	L_2	L_1	L_0	Set priority without EOI			
60	OCW3 P	0	0	0	0	0	1	1	0	0				
61	OCW3 RIS	0	0	0	0	0	1	0	1	1				
62	OCW3 RR	0	0	0	0	0	1	0	1	0				
63	OCW3 SM	0	0	1	1	0	1	0	0	0				
64	OCW3 RSM	0	0	1	0	0	1	0	0	0				

Note : Y: yes, N: no, E: edge, L: level, M: master, S: slave

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	−0.3~7	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		−0.3~V_{CC}+0.3	V
T_{OPr}	Operating free-air temperature range		−20~75	℃
Tstg	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
		I_{OH}=−20μA	4.4			
$V_{OH(INT)}$	High-level output voltage, interrupt request output	I_{OH}=−400μA	2.4			V
		I_{OH}=−100μA	3.5			
		I_{OH}=−20μA	4.4			
V_{OL}	Low-level output voltage	I_{OL}=2.2mA			0.45	V
I_{CC}	Standby supply current from V_{CC}	V_{CC}=5.5V, V_I=V_{CC} or GND output open			10	μA
I_{IH}	High-level input current	V_I=V_{CC}	−10		10	μA
I_{IL}	Low-level input current	V_I=0V	−10		10	μA
I_{OZ}	Off-state output current	V_{SS}=0, V_I=0~V_{CC}	−10		10	μA
I_{LIR1}	IR pin input current	V_I=0V	−300			μA
I_{LIR2}	IR pin input current	V_I=V_{CC}			10	μA
Ci	Input capacitance	V_{CC}=V_{SS}, f=1MHz, 25mVrms, T_a=25℃			10	pF
$Ci_{/O}$	Input/output capacitance	V_{CC}=V_{SS}, f=1MHz, 25mVrms, T_a=25℃			20	pF

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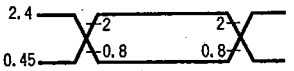
TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Alternative symbol	Limits				Unit
			M5M82C59AP		M5M82C59AP-2		
			Min	Max	Min	Max	
$t_{W(W)}$	Write pulse width	t_{WLWH}	290(200)		190(120)		ns
$t_{su(A-W)}$	Address setup time before write	t_{AHWL}	0		0		ns
$t_{h(W-A)}$	Address hold time after write	t_{WHAX}	0		0		ns
$T_{SU(DQ-W)}$	Data setup time before write	t_{DVWH}	240(100)		160(100)		ns
$t_{h(W-DQ)}$	Data hold time after write	t_{WHDX}	0		0		ns
$t_{W(R)}$	Read pulse width	t_{RLRH}	235(200)		160		ns
$t_{su(A-R)}$	Address setup time before read	t_{AHRL}	0		0		ns
$t_{h(R-A)}$	Address hold time after read	t_{RHAX}	0		0		ns
$t_{W(IR)}$	Interrupt request input width, low-level time, edge triggered mode	t_{JLJH}	100		100		ns
$t_{su(CAS-INTA)}$	Cascade setup time after $\overline{INTA}$ (slave)	t_{CVIAL}	55		40		ns
$t_{rec(W)}$	Write recovery time	t_{WHWL}	190		190		ns
$t_{rec(R)}$	Read recovery time	t_{RHRL}	160		160		ns
$t_{d(RW)}$	End of Command to next Command (Not same Command type) / End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence.	t_{CHCL}	500		400		ns

SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

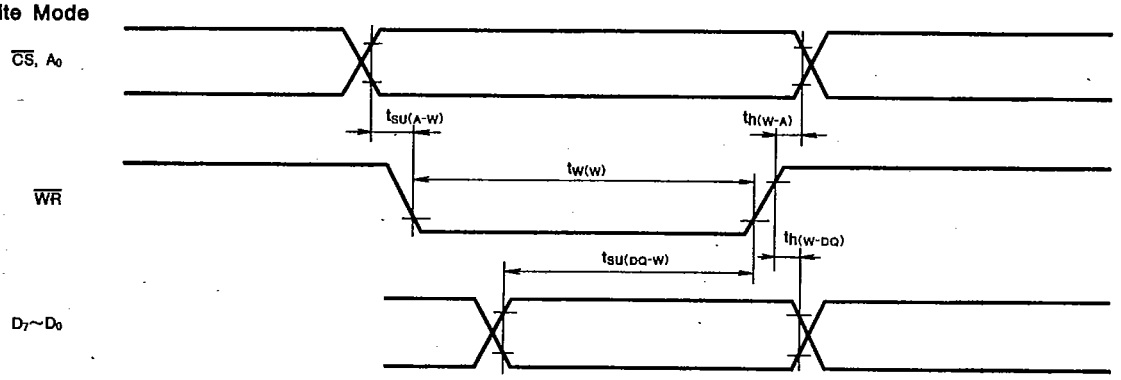
Symbol	Parameter	Alternative symbol	Limits				Unit
			M5M82C59AP		M5M82C59AP-2		
			Min	Max	Min	Max	
$t_{PZV(R-DQ)}$	Data output enable time after read	t_{RLDV}		200(170)		120	ns
$t_{PVZ(R-DQ)}$	Data output disable time after read	t_{RHDZ}	10	100	10	85	ns
$t_{PZV(A-DQ)}$	Data output enable time after address	t_{AHDV}		200(170)		200(170)	ns
$t_{PHL(R-EN)}$	Propagation time from read to enable signal output	t_{RLEL}		125		100	ns
$t_{PLH(R-EN)}$	Propagation time from read to disable signal output	t_{RHEH}		150		150	ns
$t_{PLH(IR-INT)}$	Propagation time from interrupt request input to interrupt request output	t_{JHIH}		350		300	ns
$t_{PLV(INTA-CAS)}$	Propagation time from $\overline{INTA}$ to cascade output (master)	t_{IALCV}		565		360	ns
$t_{PZV(CAS-DQ)}$	Data output enable time after cascade output (slave)	t_{CVDV}		300		200	ns

Note 1 : M5M82C59AP,-2 is also invested with the extended specification showed in the brackets.
2 : $\overline{INTA}$ signal is considered read signal
$\overline{CS}$ signal is considered address signal
Input pulse level 0.45~2.4V
Input pulse rise time 10ns
Input pulse fall time 10ns
Reference level Input V_{IH}=2V, V_{IL}=0.8V
Output V_{OH}=2V, V_{OL}=0.8V
Load capacitance C_L=100pF, where $\overline{SP/EN}$ pin is 15pF

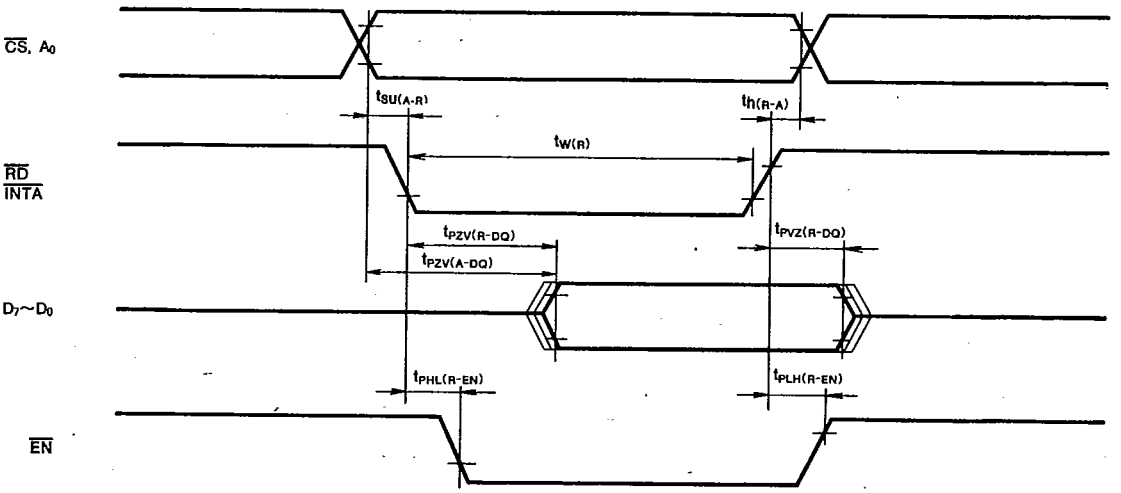


TIMING DIAGRAM

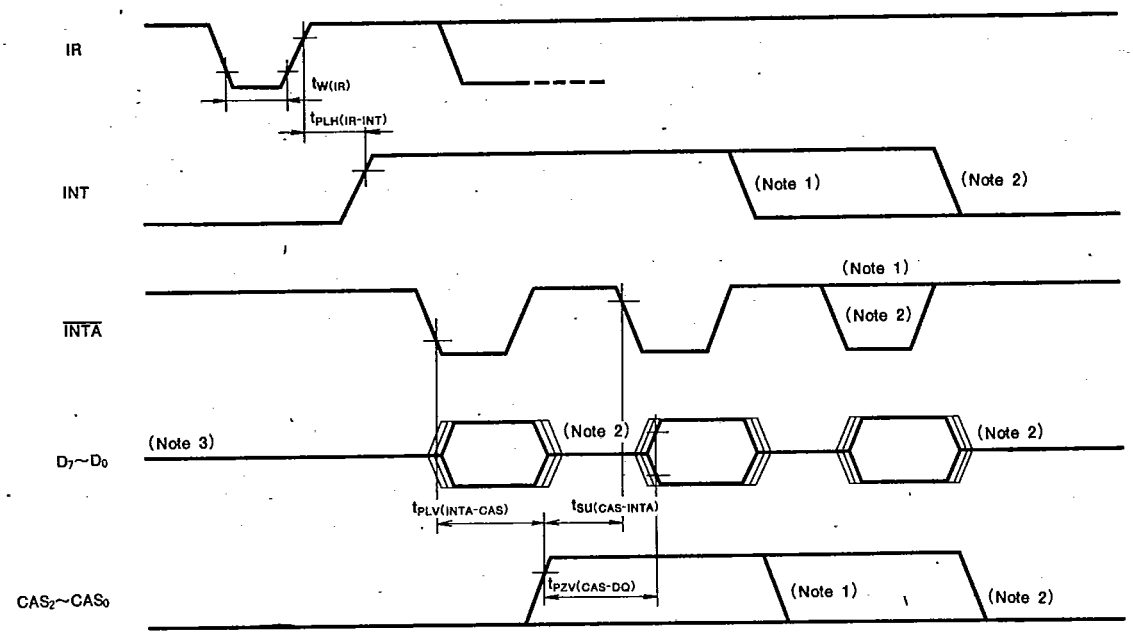
Write Mode



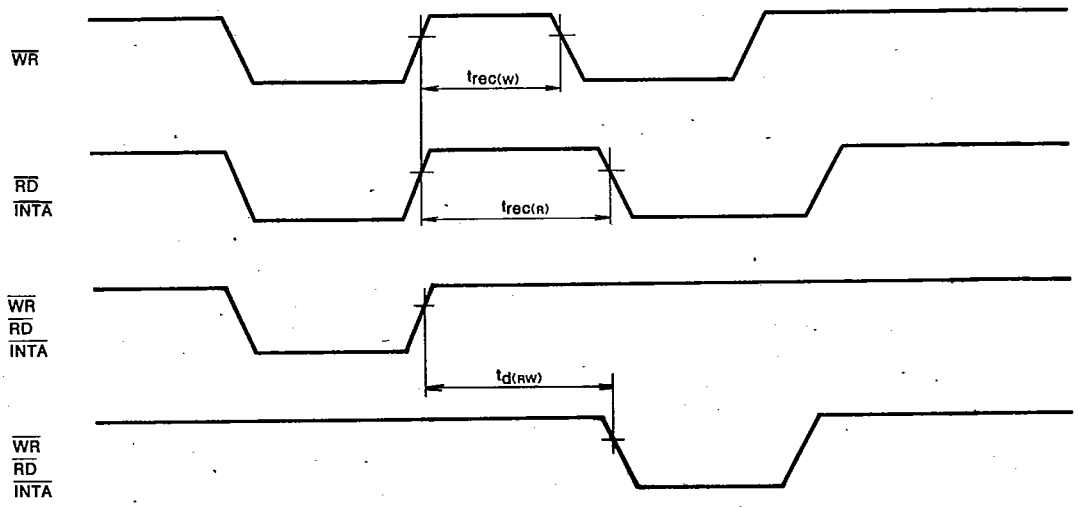
Read Mode



Interrupt Sequence



Other Timing



Note 1 : 8086, 8088 mode
2 : 8085A mode
3 : 8086, 8088 mode is in high-impedance state, pointer is released during the next $\overline{INTA}$. When in single 8085A mode, data is released by all $\overline{INTA}$s. When master, CALL instruction is released during the first $\overline{INTA}$, high impedance state during the second and third $\overline{INTA}$. When slave, high impedance state during the first $\overline{INTA}$, vectored address is released during the second and third $\overline{INTA}$.