GENERAL DESCRIPTION

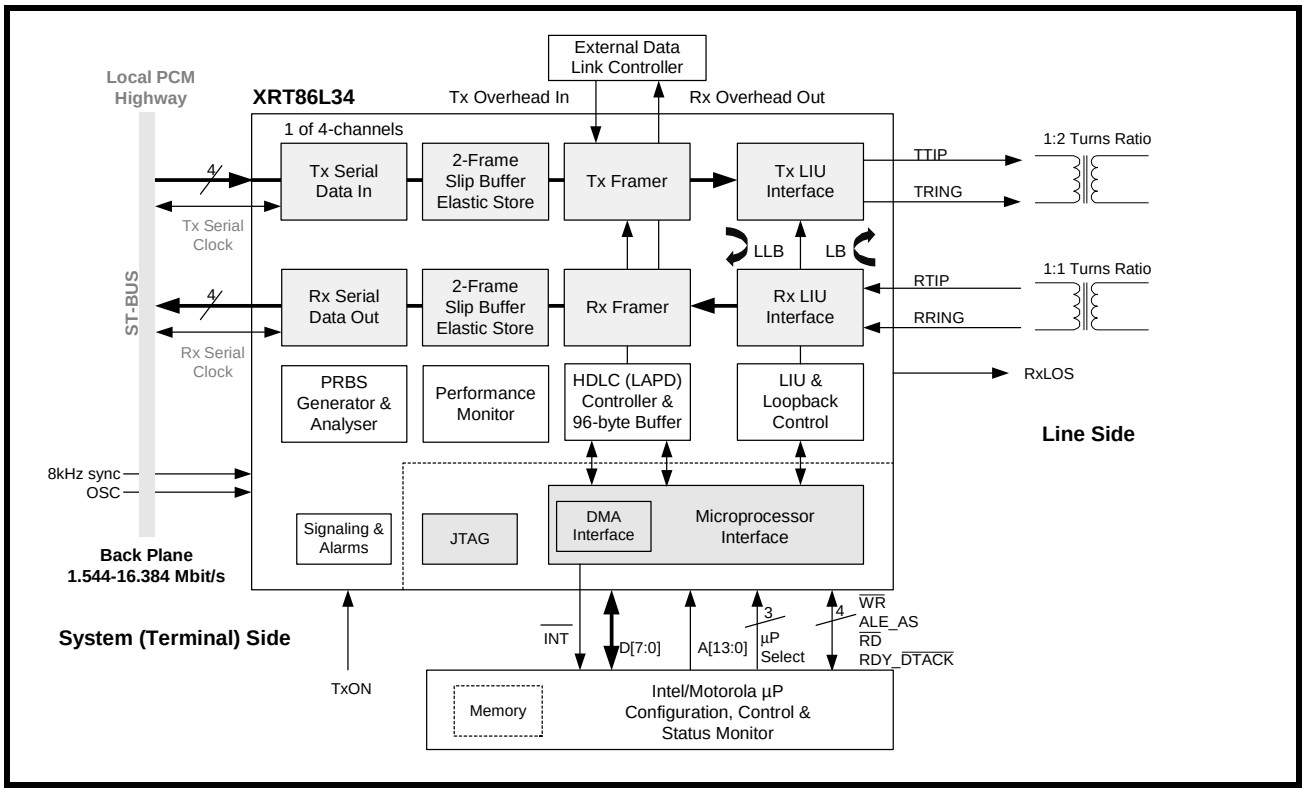
The XRT86L34 is a four-channel 1.544 Mbit/s or 2.048 Mbit/s DS1/E1/J1 framer and LIU integrated solution. The XRT86L34 contains an integrated DS1/E1/J1 framer and LIU which provide DS1/E1/J1 framing and error accumulation in accordance with ANSI/ITU_T specifications. Each framer has its own framing synchronizer and transmit-receive slip buffers. The slip buffers can be independently enabled or disabled as required and can be configured to frame to the common DS1/E1/J1 signal formats.

Each Framer block contains its own Transmit and Receive T1/E1/J1 Framing function. There are 3 Transmit HDLC controllers per channel which encapsulate contents of the Transmit HDLC buffers into LAPD Message frames. There are 3 Receive HDLC controllers per channel which extract the payload content of Receive LAPD Message frames from the incoming T1/E1/J1 data stream and write the contents into the Receive HDLC buffers. Each framer also contains a Transmit and Overhead Data Input port, which permits Data Link Terminal Equipment direct access to the outbound T1/E1/J1 frames. Likewise, a Receive Overhead output data port permits Data Link Terminal Equipment direct access to the Data Link bits of the inbound T1/E1/J1 frames.

The XRT86L34 fully meets all of the latest T1/E1/J1 specifications: ANSI T1/E1.107-1988, ANSI T1/E1.403-1995, ANSI T1/E1.231-1993, ANSI T1/E1.408-1990, AT&T TR 62411 (12-90) TR54016, and ITU G-703, G.704, G706 and G.733, AT&T Pub. 43801, and ETS 300 011, 300 233, JT G.703, JT G.704, JT G706, I.431. Extensive test and diagnostic functions include Loop-backs, Boundary scan, Pseudo Random bit sequence (PRBS) test pattern generation, Performance Monitor, Bit Error Rate (BER) meter, forced error insertion, and LAPD unchannelized data payload processing according to ITU-T standard Q.921.

Applications and Features (next page)

FIGURE 1. XRT86L34 4-CHANNEL DS1 (T1/E1/J1) FRAMER/LIU COMBO



APPLICATIONS

- High-Density T1/E1/J1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- T1/E1/J1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs): T1/E1/J1 and Fractional T1/E1/J1
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)
- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated DS1 interfaces
- Multichannel DS1 Test Equipment
- T1/E1/J1 Performance Monitoring
- Voice over packet gateways
- Routers

FEATURES

- Four independent, full duplex DS1 Tx and Rx Framer/LIUs
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx provide up to 8.192 MHz asynchronous back plane connections with jitter and wander attenuation
- Supports input PCM and signaling data at 1.544, 2.048, 4.096 and 8.192 Mbits. Also supports 4-channel multiplexed 12.352/16.384 (HMVIP/H.100) Mbit/s on the back plane bus
- Programmable output clocks for Fractional T1/E1/J1
- Supports Channel Associated Signaling (CAS)
- Supports Common Channel Signalling (CCS)
- Supports ISDN Primary Rate Interface (ISDN PRI) signaling
- Extracts and inserts robbed bit signaling (RBS)
- 3 Integrated HDLC controllers per channel for transmit and receive, each controller having two 96-byte buffers (buffer 0 / buffer 1)
- HDLC Controllers Support SS7
- Timeslot assignable HDLC
- V5.1 or V5.2 Interface
- Automatic Performance Report Generation (PMON Status) can be inserted into the transmit LAPD interface every 1 second or for a single transmission
- Alarm Indication Signal with Customer Installation signature (AIS-CI)
- Remote Alarm Indication with Customer Installation (RAI-CI)
- Gapped Clock interface mode for Transmit and Receive.
- Intel/Motorola mP and MIPS Power PC interfaces for configuration, control and status monitoring
- Parallel search algorithm for fast frame synchronization
- Wide choice of T1 framing structures: D4, ESF, SLC®96, TIDM and N-Frame (non-framing)
- Direct access to D and E channels for fast transmission of data link information
- PRBS, QRSS, and Network Loop Code generation and detection
- Programmable Interrupt output pin
- Supports programmed I/O, Burst and DMA modes of Read-Write access
- Each framer block encodes and decodes the T1/E1/J1 Frame serial data
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms
- Detects OOF, LOF, LOS errors and COFA conditions
- Loopbacks: Local (LLB) and Line remote (LB)
- Facilitates Inverse Multiplexing for ATM
- Performance monitor with one second polling
- Boundary scan (IEEE 1149.1) JTAG test port
- Accepts external 8kHz Sync reference
- 3.3V CMOS operation with 5V tolerant inputs
- 225-pin TBGA package with –40×C to +85×C operation

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86L34IB	225 Tape Ball Grid Array	-40°C to +85°C

TABLE OF CONTENTS

TABLE 1: LIST BY PIN NUMBER

PIN	PIN NAME
A1	GNDPLL
A2	AVDD
A3	E1MCLKnOUT
A4	MCLKIN
A5	VSS
A6	TRST
A7	RXSERCLK0
A8	RXCHCLK0
A9	RXOHCLK0
A10	TXMSYNC0
A11	TXOHCLK0
A12	TXSERCLK0
A13	TXCHNCLK0
A14	TXCHN0_3
A15	RXSER1
A16	RXCHCLK1
A17	RXCHN1_2
A18	RXSYNC1
B1	VDDPLL
B2	JTAG_Ring
B3	AGND
B4	T1MCLKnOUT
B5	aTEST
B6	TDI
B7	RXLOS0
B8	VDD
B9	RXCHN0_2
B10	RXCHN0_4
B11	TEST
B12	TXCHN0_0
B13	TXCHN0_2
B14	VSS
B15	RXCHN1_1
B16	RXOH1
B17	RXCASYNC1
B18	TXSYNC1
C1	GNDPLL
C2	VDDPLL
C3	JTAG_Tip
C4	DVDD
C5	DGND
C6	TMS
C7	TCLK
C8	RXCRCSYNC0
C9	RXCHN0_1
C10	RXCHN0_3
C11	RXOH0
C12	TXOH0
C13	RXCRCSYNC1
C14	TXCHN0_4
C15	TXCHNCLK1
C16	VSS
C17	TXMSYNC1
C18	RXLOS1
D1	GNDPLL
D2	VDDPLL
D3	VDDPLL
D4	GNDPLL
D5	TDO
D6	RXSER0
D7	RXCHN0_0
D8	RXSYNC0
D9	TXSYNC0
D10	RXCASYNC0
D11	TXSER0
D12	TXCHN0_1
D13	RXSERCLK1
D14	RXCHN1_0
D15	RXSERCLK2
D16	VDD
D17	RXOHCLK1
D18	RXCHN1_3
E1	RTIP0
E2	RGND0
E3	RVDD0
E4	TTIP0
E5	ANALOG
E15	TXOHCLK1
E16	TXSER1
E17	RXCHN1_4
E18	TXSERCLK1
F1	RRING0
F2	TGND0
F3	TVDD0
F4	TRING0
F15	TXOH1
F16	TXCHN1_0
F17	TXCHN1_1
F18	RXSYNC2
G1	RTIP1
G2	RGND1
G3	RVDD1
G4	TTIP1
G15	RXCHN2_1
G16	RXLOS2
G17	TXCHN1_2
G18	TXCHN1_3
H1	RRING1
H2	TGND1
H3	TVDD1
H4	TRING1
H15	RXCASYNC2
H16	RXCHN2_0
H17	RXCHCLK2
H18	TXCHN1_4
J1	RTIP2
J2	RGND2
J3	RVDD2
J4	TTIP2
J15	TXSERCLK2
J16	VDD
J17	RXCRCSYNC2
J18	RXSER2
K1	RRING2
K2	TGND2
K3	TVDD2
K4	TRING2
K15	RXOH2
K16	RXCHN2_4
K17	RXOHCLK2
K18	RXCHN2_2
L1	RTIP3
L2	RGND3
L3	RVDD3
L4	TTIP3
L15	TXSYNC2
L16	RXCHN2_3
L17	TXMSYNC2
L18	TXSER2
M1	RRING3

PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME
M2	TGND3	R11	DATA7	U8	ALE
M3	TVDD3	R12	TXMSYNC3	U9	ADDR9
M4	TRING3	R13	VDD	U10	$\overline{\text{BLAST}}$
M15	VSS	R14	TXOH3	U11	DATA6
M16	VSS	R15	VDD	U12	TXCHN3_3
M17	TXCHN2_1	R16	RXOHCLK3	U13	TXCHN3_1
M18	TXCHN2_0	R17	RXCRCSYNC3	U14	RXCHN3_4
N1	TxON	R18	RXCHN3_0	U15	TXSYNC3
N2	LOP	T1	fADDR	U16	VSS
N3	NC	T2	$\overline{\text{ACK0}}$	U17	RXSER3
N4	8KEXTOSC	T3	$\overline{\text{RDY}}$	U18	RLOS3
N15	TXCHN2_4	T4	DATA0	V1	PCLK
N16	TXCHN2_3	T5	VSS	V2	PTYPE0
N17	TXCHNCLK2	T6	ADDR3	V3	$\overline{\text{RD}}$
N18	TXOHCLK2	T7	ADDR7	V4	PTYPE1
P1	$\overline{\text{RESET}}$	T8	PTYPE2	V5	ADDR1
P2	E1OSCCLK	T9	VDD	V6	ADDR5
P3	VDD	T10	DATA4	V7	ADDR8
P4	T1OSCCLK	T11	TXCHN3_4	V8	DATA2
P15	TXOH2	T12	TXCHN3_2	V9	DATA3
P16	RXSYNC3	T13	TXCHN3_0	V10	DATA5
P17	RXCHNCLK3	T14	RXCHN3_3	V11	ADDR13
P18	RXOH3	T15	RXCHN3_2	V12	$\overline{\text{WR}}$
R1	$\overline{\text{REQ0}}$	T16	TXCHN2_2	V13	$\overline{\text{CS}}$
R2	8KSYNC	T17	RXSERCLK3	V14	TXSER3
R3	$\overline{\text{REQ1}}$	T18	RXCASYNC3	V15	TXSERCLK3
R4	VSS	U1	iADDR	V16	TXOHCLK3
R5	ADDR2	U2	$\overline{\text{ACK1}}$	V17	TXCHNCLK3
R6	ADDR6	U3	DATA1	V18	RXCHN3_1
R7	ADDR10	U4	$\overline{\text{DBEN}}$		
R8	$\overline{\text{INT}}$	U5	ADDR0		
R9	ADDR11	U6	ADDR4		
R10	ADDR12	U7	VDD		

PIN DESCRIPTIONS

TRANSMIT SERIAL DATA INPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxSER0 TxSER1 TxSER2 TxSER3	D11 E16 L18 V14	I	**Transmit Serial Data Input—Transmit Framer_n:** This input pin along with TxSerClk_n functions as the Transmit Serial input port for Framer_n. **DS1 Mode:** Any payload data applied to this pin would be inserted into a DS1 frame and output onto the T1 line. If Framer_n is configured accordingly, the framing alignment bits, the facility data link bits and the CRC-6 bits can also be inserted to input pin.The signal applied to this input pin can be latched to the Transmit Payload Data Input Interface on either the rising edge or the falling edge of TxSerClk_n according to configurations of Framer_n. **E1 Mode:** Any payload data applied to this pin would be inserted into an E1 frame and output onto the E1 line. All data intended to be transported via Time Slots 1 through 15 and Time slots 17 through 31, within each E1 frame, must be applied to this input pin. If Framer_n is configured accordingly, data intended for Time Slots 0 and 16 can also be applied to this input pin.
TxSERCLK0 TxSERCLK1 TxSERCLK2 TxSERCLK3	A12 E18 J15 V15	I or O	**Transmit Serial Clock Signal --Transmit Framer_n:** This clock signal is used by the Transmit payload data Input Interface, to latch the contents of the TxSer_n signal into the Quad T1/E1/J1 Framer IC. Data that is applied at the TxSer_n input is latched into the Transmit payload data Input Interface (for Framer_n) on either the rising edge or the falling edge of TxSerClk_n depending on configurations of Framer_n. TxSerClk_n can either be an input or an output. **DS1 Mode:** **Transmit Back-plane Interface-1.544 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 00 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 1.544 Mbit/s. If the Transmit Section of Framer_n has been configured to use the TxSerClk_n signal as the timing source, then this signal will be an **Input**. If the Transmit Section of Framer_n has been configured to use either the RxLineClk_n signal or the OSCClk signal as the timing source, then TxSerClk_n will be an **Output**. **Transmit Back-plane Interface-High Speed Clock Mode** If TxMUXEN ≠ 0 and TxIMODE[1:0] ≠ 00 in Transmit interface control register, Transmit back-plane interface of Framer_n is operating at a high-speed mode and is taking data at rates of 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s, 12.352 Mbit/s or 16.384 Mbit/s. The TxSerClk_n signal will be an Input clock signal running at 1.544 MHz. **E1 Mode:** **Transmit Back-plane Interface-2.048 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 00 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 2.048 Mbit/s. If the Transmit Section of Framer_n has been configured to use the TxSerClk_n signal as the timing source, then this signal will be an **Input**. If the Transmit Section of Framer_n has been configured to use either the RxLineClk_n signal or the OSCClk signal as the timing source, then TxSerClk_n will be an **Output**. **Transmit Back-plane Interface-High Speed Clock Mode** If TxMUXEN ≠ 0 or TxIMODE[1:0] ≠ 00 in Transmit interface control register, Transmit back-plane interface of Framer_n is operating at a high-speed mode. The TxSerClk_n signal will be an Input clock signal running at 2.048 MHz.

TRANSMIT SERIAL DATA INPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxSYNC0 TxSYNC1 TxSYNC2 TxSYNC3	D9 B18 L15 U15	I or O	**Single Frame Sync Pulse Input/Output—Transmit Framer_n:** This pin is configured to be an **input** if the TxSerClk_n input pin is configured to be the timing reference for the Transmit Portion of Framer_n. This pin is configured as an **output** if the RxLineClk_n input pin or the OSCClk input pins are configured to be the timing reference for the Transmit portion of Framer_n. **DS1 Mode:** **When pin is configured to be an Input** If this pin is configured to be an **input**, then the user must pulse this pin "High" for one period of TxSerClk_n, when the Transmit payload data Input Interface (of Framer_n) is processing the first bit (F-bit) of an outbound DS1 frame. ***NOTE:*** *It is imperative that the TxSync_n input signal be synchronized with the TxSerClk_n input signal.* **When pin is configured to be an Output** If this pin is configured to be an **output**, then it will pulse "High", for one period of TxSerClk_n, when the Transmit payload data Input Interface (of Framer_n) is processing the last payload bit within an outbound DS1 frame. **E1 Mode:** **When pin is configured to be an Input** If this pin is configured to be an **input**, then the user must pulse this pin "High" for one period of TxSerClk_n, when the Transmit payload data Input Interface (of Framer_n) is processing the International Bit (Si) of an outbound E1 frame. ***NOTE:*** *It is imperative that the TxSync_n input signal be synchronized with the TxSerClk_n input signal.* **When pin is configured to be an Output** If this pin is configured to be an **output**, then it will pulse "High", for one period of TxSerClk_n, when the Transmit payload data Input Interface (of Framer_n) is processing the last bit within a given outbound E1 frame.

TRANSMIT SERIAL DATA INPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxMSYNC0 TxMSYNC1 TxMSYNC2 TxMSYNC3	A10 C17 L17 R12	I or O	**Multiframe Sync Pulse Input/Output—Framer_n:** This signal indicates the boundary of an outbound multi-frame. **DS1 Mode:** **Transmit Back-plane Interface-1.544 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 00 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 1.544 Mbit/s. This pin is configured to be an **Input** if the TxSerClk_n input pin is configured to be the timing reference for the Transmit section of Framer_n. Conversely, this pin will be configured as an **Output** if the RxLineClk input pin or the OSCClk input pins are configured to be the timing reference for the Transmit section of Framer_n.The roles of these pins when configured as input or output, is described below. **When pin is configured to be an Input** If this pin is configured to be an **input**, this pin must be pulsed "High" for one period of TxSerClk_n, the instant that the Transmit payload data Interface (of Framer_n) is processing the first bit of a DS1 Multi-frame. ***NOTE:*** *It is imperative that the TxMSync_n input signal be synchronized with the TxSerClk_n input signal.* **When pin is configured to be an Output** If this pin is configured to be an **output**, then it will pulse "High", for one period of TxSerClk_n, when the Transmit payload data Input Interface (of Framer_n) is processing the last bit of a DS1 Multi-frame. **E1 Mode:** **Transmit Back-plane Interface-2.048 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 00 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 2.048 Mbit/s. This pin is configured to be an **Input** if the TxSerClk_n input pin is configured to be the timing reference for the Transmit section of Framer_n. Conversely, this pin will be configured as an **Output** if the RxLineClk input pin or the OSCClk input pins are configured to be the timing reference for the Transmit section of Framer_n. **When pin is configured to be an Input** If this pin is configured to be an input, this pin must be pulsed "High" for one period of TxSerClk_n, the instant that the Transmit payload data Interface (of Framer_n) is processing the first International Bit (Si) of an "outbound" CRC payload data Multiframe. ***NOTES:*** *1. This pin is ignored if CRC Multiframe Alignment has been disabled.* *2. It is imperative that the TxMSync_n input signal be synchronized with the TxSerClk_n input signal.* **When pin is configured to be an Output** If this pin is configured to be an output, then it will pulse "High", for one period of TxSerClk_n, when the Transmit payload data Input Interface (of Framer_n) is processing the last bit, within an "outbound" CRC Multi-frame. ***NOTES:*** *1. This pin is inactive if CRC Multi-frame Alignment has been disabled.* *2. The purpose of this output pin is to permit the Terminal Equipment to maintain alignment with the "outbound" CRC-Multi-frame structure.*

TRANSMIT SERIAL DATA INPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxCHCLK0 TxCHCLK1 TxCHCLK2 TxCHCLK3	A13 C15 N17 V17	I or O	**Transmit Input Clock Signal -- Transmit Framer _n** If TxMUXEN ≠ 0 or TxIMODE[1:0] ≠ 00 in Transmit interface control register, Transmit back-plane interface of Framer_n is operating at a high-speed mode. This pin will function as an input clock signal for the high-speed Transmit back-plane interface. **DS1 Mode:** **Transmit Back-plane Interface-MVIP, 2.048 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 01 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 2.048 Mbit/s. The TxInClk_n signal will be an Input clock signal running at 2.048 MHz. **Transmit Back-plane Interface-4.096 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 10 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 4.096 Mbit/s. The TxInClk_n signal will be an Input clock signal running at 4.096 MHz. **Transmit Back-plane Interface-8.192 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 11 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 8.192 Mbit/s. The TxInClk_n signal will be an Input clock signal running at 8.192 MHz. **Transmit Back-plane Interface-Multiplexed at 12.352 MHz Clock Mode** If TxMUXEN = 1 and TxIMODE[1:0] = 00 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking multiplexed data at a rate of 12.352 Mbit/s. TxInClk_0 will be an Input clock signal running at 12.352 MHz. TxInClk_1, 2, 3 signals are not required. Transmit Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_0 via TxSer_0 input pin. Inside the Quad Framer, data will be de-multiplexed into 4 channels from the serial input of Channel 0. **Transmit Back-plane Interface-Multiplexed at 16.384 MHz Clock Mode** If TxMUXEN = 1 and TxIMODE[1:0] = 01 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking multiplexed data at a rate of 16.384 Mbit/s. TxInClk_0 will be an Input clock signal running at 16.384 MHz. TxInClk_1, 2, 3 signals are not required. Transmit Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_0 via TxSer_0 input pin. Inside the Quad Framer, data will be de-multiplexed into 4 channels from the serial input of Channel 0. **Transmit Back-plane Interface-HMVIP, 16.384 MHz Clock Mode** If TxMUXEN = 1 and TxIMODE[1:0] = 10 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking multiplexed data at a rate of 16.384 Mbit/s. TxInClk_0 will be an Input clock signal running at 16.384 MHz. TxInClk_1, 2, 3 signals are not required. Transmit Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_0 via TxSer_0 input pin. Inside the Quad Framer, data will be de-multiplexed into 4 channels from the serial input of Channel 0.

TRANSMIT SERIAL DATA INPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxCHCLKn (Continued)		I	**Transmit Input Clock Signal -- Transmit Framer _n (continued)** **Transmit Back-plane Interface-H.100, 16.384 MHz Clock Mode** If TxMUXEN = 1 and TxIMODE[1:0] = 11 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking multiplexed data at a rate of 16.384 Mbit/s. TxInClk_0 will be an Input clock signal running at 16.384 MHz. TxInClk_1, 2, 3 signals are not required. Transmit Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_0 via TxSer_0 input pin. Inside the Quad Framer, data will be de-multiplexed into 4 channels from the serial input of Channel 0. **E1 Mode:** **Transmit Back-plane Interface-2.048 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 01 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 2.048 Mbit/s. The TxInClk_n signal will be an Input clock signal running at 2.048 MHz. **Transmit Back-plane Interface-4.096 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 10 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 4.096 Mbit/s. The TxInClk_n signal will be an Input clock signal running at 4.096 MHz. **Transmit Back-plane Interface-8.192 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 11 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 8.192 Mbit/s. The TxInClk_n signal will be an Input clock signal running at 8.192 MHz. **Transmit Back-plane Interface-Multiplexed at 16.384 MHz Clock Mode** If TxMUXEN = 1 and TxIMODE[1:0] = 01 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking multiplexed data at a rate of 16.384 Mbit/s. TxInClk_0 will be an Input clock signal running at 16.384 MHz. TxInClk_1, 2, 3 signals are not required. Transmit Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_0 via TxSer_0 input pin. Inside the Quad Framer, data will be de-multiplexed into 4 channels from the serial input of Channel 0. **Transmit Back-plane Interface-HMVIP, 16.384 MHz Clock Mode** If TxMUXEN = 1 and TxIMODE[1:0] = 10 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking multiplexed data at a rate of 16.384 Mbit/s. TxInClk_0 will be an Input clock signal running at 16.384 MHz. TxInClk_1, 2, 3 signals are not required. Transmit Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_0 via TxSer_0 input pin. Inside the Quad Framer, data will be de-multiplexed into 4 channels from the serial input of Channel 0.

TRANSMIT SERIAL DATA INPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxCHCLKn (Continued)		I	**Transmit Input Clock Signal -- Transmit Framer _n (continued)** **Transmit Back-plane Interface-H.100, 16.384 MHz Clock Mode** If TxMUXEN = 1 and TxIMODE[1:0] = 11 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking multiplexed data at a rate of 16.384 Mbit/s. TxInClk_0 will be an Input clock signal running at 16.384 MHz. TxInClk_1, 2, 3 signals are not required. Transmit Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_0 via TxSer_0 input pin. Inside the Quad Framer, data will be de-multiplexed into 4 channels from the serial input of Channel 0.
		O	**Transmit Channel Clock Output Signal—Framer_n:** This pin indicates the boundary of each time slot of an outbound DS1/E1 frame. **DS1 Mode:** Each of these output pins are a 192kHz clock output which pulses "High" whenever the Transmit Payload Data Input Interface block accepts the LSB of each of the 24 time slots, within the DS1 data stream, being processed via Framer _n. The Terminal Equipment should use this clock signal to sample the TxTSb0_n through TxTSb4_n output signals and identify the time-slot being processed via the "Transmit Section" of each Framer_n. If TxTSb1_n pin is configured as TxFrTD_n to input fractional DS1 payload data into Framer_n, the TxTSClk_n pin can be configured to function as one of the following: The pin will output gaped fractional DS1 clock that can be used by terminal equipment to clock out fractional DS1 payload data at rising edge of the clock. Framer_n will then input fractional DS1 payload data using falling edge of the clock.Otherwise, this pin will be a clock enable signal to Transmit fractional DS1 Input (TxFrTD_n) if Framer_n is configured accordingly. In this mode, fractional DS1 payload data is clocked into the chip using un-gaped TxSerClk_n. **E1 Mode:** Each of these output pins are a 256kHz clock output which pulses "High" whenever the Transmit Payload Data Input Interface block accepts the LSB of each of the 32 time slots, within the E1 data stream, being processed via Framer _n. The Terminal Equipment should use this clock signal to sample the TxTSb0_n through TxTSb4_n output signals, and identify the time-slot being processed via the "Transmit Section" of each Framer_n. If TxTSb1_n pin is configured as TxFrTD_n to input fractional E1 payload data into Framer_n, the TxTSClk_n pin can be configured to function as one of the following: The pin will output gaped fractional E1 clock that can be used by terminal equipment to clock out fractional E1 payload data at rising edge of the clock. Framer_n will then input fractional E1 payload data using falling edge of the clock.Otherwise, this pin will be a clock enable signal to Transmit fractional E1 Input (TxFrTD_n) if Framer_n is configured accordingly. In this mode, fractional E1 payload data is clocked into the chip using un-gaped TxSerClk_n.

TRANSMIT SERIAL DATA INPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxCHN0_0 TxCHN1_0 TxCHN2_0 TxCHN3_0	B12 F16 M18 T13	O	**Transmit Framer_n--Time Slot Octet Identifier Output-Bit [0:4]:** These output signals (TxTSb4_n through TxTSb0_n) reflects the five-bit binary value of the number of Time Slot (in the incoming DS1 frame), being accepted and processed by the Transmit Payload Data Input Interface block associated with Framer_n. Terminal Equipment should use the TxTSClk_n clock signal to sample the five output pins of each channel in order to identify the time-slot being processed by the Transmit Payload Data Input Interface block of Framer_n.
		I	**Transmit Serial Signaling Input--Transmit Framer_n** These pins can be used to input robbed-bit signaling data within an outbound DS1 frame or to input Channel Associated Signaling (CAS) bits within an outbound E1 frame, if Framer_n is configured accordingly.
TxCHN0_1 TxCHN1_1 TxCHN2_1 TxCHN3_1	D12 F17 M17 U13	O	**Transmit Framer_n--Time Slot Octet Identifier Output-Bit 1:** These output signals (TxTSb4_n through TxTSb0_n) reflects the five-bit binary value of the number of Time Slot (in the incoming DS1 frame), being accepted and processed by the Transmit Payload Data Input Interface block associated with Framer_n. Terminal Equipment should use the TxTSClk_n clock signal to sample the five output pins of each channel in order to identify the time-slot being processed by the Transmit Payload Data Input Interface block of Framer_n.
		I	**Transmit Serial Fractional T1/E1 Input--Transmit Framer_n** These pins can be used to input fractional DS1/E1 payload data within an outbound DS1/E1 frame, if Framer_n is configured accordingly. In this mode, terminal equipment will use either TxTSClk_n or TxSerClk_n output pins to clock out fractional DS1/E1 payload data. Framer_n will then use TxTSClk_n or TxSerClk_n to clock in fractional DS1/E1 payload data. Please see pin description of TxTSClk_n for details.
TxCHN0_2 TxCHN1_2 TxCHN2_2 TxCHN3_2	B13 G17 T16 T12	O	**Transmit Framer_n--Time Slot Octet Identifier Output-Bit 2:** These output signals (TxTSb4_n through TxTSb0_n) reflects the five-bit binary value of the number of Time Slot (in the incoming DS1 frame) being accepted and processed by the Transmit Payload Data Input Interface block associated with Framer_n. Terminal Equipment should use the TxTSClk_n clock signal to sample the five output pins of each channel in order to identify the time-slot being processed by the Transmit Payload Data Input Interface block of Framer_n. If TxTSb1_n pin is configured as TxFrTD_n to input fractional DS1 payload data into Framer_n, the TxTSb2_n pin will serially output the five-bit binary value of the number of the Time Slot being accepted and processed by the Transmit Payload Data Input Interface block associated with Framer_n. **Transmit 12.352MHz Clock Output-Transmit Framer_n:** These pins can be used to output 12.352MHz clock derived from OSCClk, if Framer_n is configured accordingly.

TRANSMIT SERIAL DATA INPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxCHN0_3 TxCHN1_3 TxCHN2_3 TxCHN3_3	A14 G18 N16 U12	O	**Transmit Framer_n-Time Slot Octet Identifier Output-Bit 3:** These output signals (TxTSb4_n through TxTSb0_n) reflects the five-bit binary value of the number of Time Slot (in the incoming DS1 frame) being accepted and processed by the Transmit Payload Data Input Interface block associated with Framer_n. Terminal Equipment should use the TxTSClk_n clock signal to sample the five output pins of each channel in order to identify the time-slot being processed by the Transmit Payload Data Input Interface block of Framer_n. **Transmit Overhead Synchronization Pulse--Transmit Framer_n:** These pins can be used to output Overhead Synchronization Pulse that indicate the first bit of each multi-frame, if Framer_n is configured accordingly.
TxCHN0_4 TxCHN1_4 TxCHN2_4 TxCHN3_4	C14 H18 N15 T11	O	**Transmit Framer_n--Time Slot Octet Identifier Output-Bit 4:** These output signals (TxTSb4_n through TxTSb0_n) reflects the five-bit binary value of the number of Time Slot (in the incoming DS1 frame) being accepted and processed by the Transmit Payload Data Input Interface block associated with Framer_n. Terminal Equipment should use the TxTSClk_n clock signal to sample the five output pins of each channel in order to identify the time-slot being processed by the Transmit Payload Data Input Interface block of Framer_n.

OVERHEAD INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxOH0 TxOH1 TxOH2 TxOH3	C12 F15 P15 R14	I	**Transmit Overhead Input—Framer_n:** This input pin, along with TxOHClk_n functions as the Transmit Overhead input port for Framer_n. **DS1 Mode:** This input pin will become active if the Transmit Section of Framer_n has been configured to use this input as the source of Facility Data Link bits in ESF framing mode, Fs bits in the SLC96 and N framing mode, and R bit in T1DM mode. The data that is input into this pin will be inserted into the Data Link Bits within the outbound DS1 frames at the falling edge of TxOHClk_n. ***NOTE:*** *This input pin will be disabled if Framer_n is using the Transmit HDLC Controller, or the TxSer_n input as the source for the Data Link Bits.* **E1 Mode:** This input pin will become active if the Transmit Section of Framer_n has been configured to use this input as the source of Data Link bits. The data that is input into this pin will be inserted into the Sa4 through Sa8 bits (the National Bits) within the outbound non-FAS E1 frames. ***NOTE:*** *This input pin will be disabled if Framer_n is using the Transmit HDLC Controller, or the TxSer_n input as the source for the Data Link Bits.*

OVERHEAD INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxOHCLK0 TxOHCLK1 TxOHCLK2 TxOHCLK3	A11 E15 N18 V16	O	**Transmit OH Serial Clock Output Signal—Framer_n:** This output clock signal functions as a demand clock signal for the "Transmit Overhead Data Input Interface" block associated with Framer_n. **DS1 Mode:** If the "Transmit Overhead Data Input Interface" has been configured to be the source of Facility Data Link bits in ESF framing mode, Fs bits in the SLC96 and N framing mode, and R bit in T1DM framing mode, then the Transmit Overhead data Input Interface block will provide a clock edge for each Data Link Bit. Data Link Equipment, which is interfaced to this pin, should update its data (on the TxOH_n line) on the rising edge of this clock signal. The Transmit Overhead Data Input Interface will latch the data (on the TxOH_n line) on the falling edge of this clock signal. ***NOTES:*** *1. If the "Transmit Overhead Data Input Interface" has not been configured to be the source of the Data Link information, then this output signal will be inactive.* *2. Depending on the configurations of Framer_n, the clock frequency in ESF framing mode can be 2KHz or 4KHz in ESF.* **E1 mode:** If the "Transmit Overhead data Input Interface" has been configured to be the source of Data Link information, then the Transmit Overhead data Input Interface block will provide a clock edge for each "Sa" bit that is carrying data link information. Data Link Equipment, which is interfaced to this pin, should update its data (on the TxOH_n line) on the rising edge of this clock signal. The Transmit Overhead Data Input Interface will latch the data (on the TxOH_n line) on the falling edge of this clock signal. ***NOTE:*** *If the "Transmit Overhead Data Input Interface" has not been configured to be the source of the Data Link information, then this output signal will be inactive.*
RxOH0 RxOH1 RxOH2 RxOH3	C11 B16 K15 P18	O	**Receive Overhead Output—Framer_n:** This pin, along with RxOHClk_n functions as the Receive Overhead Output Interface for Framer_n. **DS1 Mode:** This pin unconditionally outputs the contents of the Facility Data Link Bit in ESF framing mode, Fs bit in the SLC96 and N framing mode, and R bit in T1DM framing mode. ***NOTE:*** *This output pin is active even if the Receive HDLC Controller (within Framer_n) is active.* **E1 mode:** This pin unconditionally outputs the contents of the National Bits (the "Sa4" through the "Sa8" bits). If Framer_n has been configured to interpret the National bits of the incoming E1 frames as carrying "Data Link" information; then the Receive Overhead Output Interface will provide a clock pulse (via the RxOHClk_n output pin) for each "Sa" bit carrying Data Link information. ***NOTE:*** *This output pin is active even if the Receive HDLC Controller (within Framer_n) is active.*

OVERHEAD INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxOHCLK0 RxOHCLK1 RxOHCLK2 RxOHCLK3	A9 D17 K17 R16	O	**Receive OH Serial Clock Output Signal—Framer_n:** This pin, along with RxOH_n functions as the Receive Overhead Output Interface for Framer_n. **DS1 Mode:** This pin outputs a clock edge corresponding to each Facility Data Link Bit in ESF framing mode, Fs bit in the SLC96 and N framing mode, and R bit in T1DM framing mode, which carries Data Link information. ***NOTES:*** *1. Depending on the configurations of Framer_n, the clock frequency in ESF framing mode can be 2KHz or 4KHz.* *2. This output pin is inactive if the Receive HDLC Controller (within Framer_n) has been enabled.* **E1 mode:** This pin outputs a clock edge corresponding to each National Bit that is carrying "Data Link" information. ***NOTE:*** *This output pin is inactive if the Receive HDLC Controller (within Framer_n) has been enabled.*

RECEIVE SERIAL DATA OUTPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxSYNC0 RxSYNC1 RxSYNC2 RxSYNC3	D8 A18 F18 P16	I or O	**Single Frame Sync Pulse Input/Output pin—Receive Framer_n:** This pin is configured to be an **Input** if the Slip Buffer associated with Framer_n is enabled. Conversely, this pin will be configured to be an **Output** if the Slip-Buffer is by-passed. **DS1 Mode:** **When pin is configured to be an Input** If this pin is configured to be an input, then the user must pulse this pin "High" for one period of RxSerClk_n, when the Receive payload data output Interface (of Framer_n) is processing the first bit (F-bit) of an inbound DS1 frame. ***NOTE:*** *It is imperative that the RxSync_n input signal be synchronized with the RxSerClk_n input signal.* **When pin is configured to be an Output** If this pin is configured to be an output, then it will pulse "High", for one period of RxSerClk_n, when the Receive payload data output Interface (of Framer_n) is processing the first bit (F-bit) of an inbound DS1 frame. **E1 Mode:** **When pin is configured to be an Input** If this pin is configured to be an input, then this pin must be pulsed "High" for one period of RxSerClk_n, when the Receive E1 Serial (or Overhead) Output Interface, outputs the International bit (Si) of an inbound E1 frame. ***NOTE:*** *It is imperative that the RxSync_n input signal be synchronized with the RxSerClk_n input signal.* **When pin is configured to be an Output** If this pin is configured to be an output, then it will pulse "High" for one period of RxSerClk_n, when the Receive E1 Serial (or Overhead) output Interface outputs the last bit, in an inbound E1 frame.

RECEIVE SERIAL DATA OUTPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxCRCSYNC0 RxCRCSYNC1 RxCRCSYNC2 RxCRCSYNC3	C8 C13 J17 R17	O	**Multiframe Sync Pulse Output--Receive Framer_n:** This DS1-only signal will pulse "High" for one period of RxSerClk_n, the instant that the Receive payload data Interface (of Framer_n) is processing the first bit of a DS1 Multi-frame. **Receive "CRC Multiframe" Sync Output signal-Framer_n:** This E1-only signal pulses "High" for one period of RxSerClk_n whenever the Receive E1 Output Interface of Framer_n outputs the first bit, within a given "CRC Multiframe". ***NOTE:*** *This output pin is inactive if CRC Multiframe Alignment is disabled.*
RxSERCLK0 RxSERCLK1 RxSERCLK2 RxSERCLK3	A7 D13 D15 T17	I or O	**Receive Serial Clock Signal—Receive Framer_n:** This signal is used by the Receive payload data output Interface, to latch the contents of the RxSer_n signal out from the Quad T1/E1/J1 Framer IC. Framer_n can use either the rising edge or the falling edge of RxSerClk_n signal to latch the received DS1 payload data out. Depending on configurations of Framer_n. RxSerClk_n can either be an input or an output. **DS1 Mode:** **Receive Back-plane Interface-1.544 MHz Clock Mode** If RxMUXEN = 0 and RxIMODE[1:0] = 00 in Receive interface control register, Receive back-plane interface of Framer_n is presenting data at a rate of 1.544 Mbit/s. This pin is configured to be an Input if the Slip Buffer associated with Framer_n is enabled. Conversely, this pin will be configured to be an Output if the "Slip-Buffer" is "by-passed". **Receive Back-plane Interface-MVIP, 2.048 MHz Clock Mode** If RxMUXEN = 0 and RxIMODE[1:0] = 01 in Receive interface control register, Receive back-plane interface of Framer_n is presenting data at a rate of 2.048 Mbit/s. The RxSerClk_n signal will be an Input clock signal running at 2.048 MHz. **Receive Back-plane Interface-4.096 MHz Clock Mode** If RxMUXEN = 0 and RxIMODE[1:0] = 10 in Receive interface control register, Receive back-plane interface of Framer_n is presenting data at a rate of 4.096 Mbit/s. The RxSerClk_n signal will be an Input clock signal running at 4.096 MHz. **Receive Back-plane Interface-8.192 MHz Clock Mode** If RxMUXEN = 0 and RxIMODE[1:0] = 11 in Receive interface control register, Receive back-plane interface of Framer_n is presenting data at a rate of 8.192 Mbit/s. The RxSerClk_n signal will be an Input clock signal running at 8.192 MHz. **Receive Back-plane Interface-Multiplexed at 12.352 MHz Clock Mode** If RxMUXEN = 1 and RxIMODE[1:0] = 00 in Receive interface control register, Receive back-plane interface of Framer_n is presenting multiplexed data at a rate of 12.352 Mbit/s. RxSerClk_0 will be an Input clock signal running at 12.352 MHz. RxSerClk_1, 2, 3 signals are not required. Received DS1 Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_0 via RxSer_0 output pin.

RECEIVE SERIAL DATA OUTPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxSERCLKn (Continued)		I or O	**Receive Serial Clock Signal—Receive Framer_n: (Continued)** **Receive Back-plane Interface-Multiplexed at 16.384 MHz Clock Mode** If RxMUXEN = 1 and RxIMODE[1:0] = 01 in Receive interface control register, Receive back-plane interface of Framer_n is presenting multiplexed data at a rate of 16.384 Mbit/s. RxSerClk_0 will be an Input clock signal running at 16.384 MHz. RxSerClk_1, 2, 3 signals are not required. Received DS1 Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_0 via RxSer_0 output pin. **Receive Back-plane Interface-HMVIP, 16.384 MHz Clock Mode** If RxMUXEN = 1 and RxIMODE[1:0] = 10 in Receive interface control register, Receive back-plane interface of Framer_n is presenting multiplexed data at a rate of 16.384 Mbit/s. RxSerClk_0 will be an Input clock signal running at 16.384 MHz. RxSerClk_1, 2, 3 signals are not required. Received DS1 Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_0 via RxSer_0 output pin. **Receive Back-plane Interface-H.100, 16.384 MHz Clock Mode** If RxMUXEN = 1 and RxIMODE[1:0] = 11 in Receive interface control register, Receive back-plane interface of Framer_n is presenting multiplexed data at a rate of 16.384 Mbit/s. RxSerClk_0 will be an Input clock signal running at 16.384 MHz. RxSerClk_1, 2, 3 signals are not required. Received DS1 Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_0 via RxSer_0 output pin. **E1 Mode:** **Receive Back-plane Interface-2.048 MHz (XRT84V24 Compatible) Clock Mode** If RxMUXEN = 0 and RxIMODE[1:0] = 00 in Receive interface control register, Receive back-plane interface of Framer_n is presenting data at a XRT84V24 compatible rate of 2.048 Mbit/s. This pin is configured to be an Input if the Slip Buffer associated with Framer_n is enabled. Conversely, this pin will be configured to be an Output if the "Slip-Buffer" is "by-passed". **Receive Back-plane Interface-2.048 MHz Clock Mode** If RxMUXEN = 0 and RxIMODE[1:0] = 01 in Receive interface control register, Receive back-plane interface of Framer_n is presenting data at a rate of 2.048 Mbit/s. The RxSerClk_n signal will be an Input clock signal running at 2.048 MHz. **Receive Back-plane Interface-4.096 MHz Clock Mode** If RxMUXEN = 0 and RxIMODE[1:0] = 10 in Receive interface control register, Receive back-plane interface of Framer_n is presenting data at a rate of 4.096 Mbit/s. The RxSerClk_n signal will be an Input clock signal running at 4.096 MHz. **Receive Back-plane Interface-8.192 MHz Clock Mode** If RxMUXEN = 0 and RxIMODE[1:0] = 11 in Receive interface control register, Receive back-plane interface of Framer_n is presenting data at a rate of 8.192 Mbit/s. The RxSerClk_n signal will be an Input clock signal running at 8.192 MHz.

RECEIVE SERIAL DATA OUTPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxSERCLKn (Continued)		I or O	**Receive Serial Clock Signal—Receive Framer_n: (Continued)** **Receive Back-plane Interface-Multiplexed at 16.384 MHz Clock Mode** If RxMUXEN = 1 and RxIMODE[1:0] = 01 in Receive interface control register, Receive back-plane interface of Framer_n is presenting bit-multiplexed data at a rate of 16.384 Mbit/s. RxSerClk_0 will be an Input clock signal running at 16.384 MHz. RxSerClk_1, 2, 3 signals are not required. Received DS1 Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_0 via RxSer_0 output pin. **Receive Back-plane Interface-HMVIP, 16.384 MHz Clock Mode** If RxMUXEN = 1 and RxIMODE[1:0] = 10 in Receive interface control register, Receive back-plane interface of Framer_n is presenting multiplexed data at a rate of 16.384 Mbit/s. RxSerClk_0 will be an Input clock signal running at 16.384 MHz. RxSerClk_1, 2, 3 signals are not required. Received DS1 Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_0 via RxSer_0 output pin. **Receive Back-plane Interface-H.100, 16.384 MHz Clock Mode** If RxMUXEN = 1 and RxIMODE[1:0] = 11 in Receive interface control register, Receive back-plane interface of Framer_n is presenting multiplexed data at a rate of 16.384 Mbit/s. RxSerClk_0 will be an Input clock signal running at 16.384 MHz. RxSerClk_1, 2, 3 signals are not required. Received DS1 Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_0 via RxSer_0 output pin.
RxSER0 RxSER1 RxSER2 RxSER3	D6 A15 J18 U17	O	**Receive Serial Data Output—Receive Framer_n:** This output pin along with RxSerClk_n functions as the Receive Serial Output port for Framer_n. **T1 mode:** Any incoming **T1** line data that is received from the line will be decoded and output via this pin.Framer_n can use either the rising edge or the falling edge of RxSerClk_n input pin to latch the received **T1** payload data out according to configurations of Framer_n. **E1 mode:** Much of the data that is received from the line will be decoded and output via this pin, in a binary format.All data that is transported via Time Slots 1 through 15 and Time Slots 17 through 31, within each incoming **E1** frame, will be output via this pin. If Framer_n is configured accordingly, the data for Time Slots 0 and 16 will also be output via this pin. Framer_n can use either the rising edge or the falling edge of RxSerClk_n input pin to latch the received DS1/E1 payload data out according to configurations of Framer_n.
RxCHN0_0 RxCHN1_0 RxCHN2_0 RxCHN3_0	D7 D14 H16 R18	O	**Receive Framer_n--Time Slot Octet Identifier Output-Bit 0:** These output signals (RxTSb4_n through RxTSb0_n) reflect the five-bit binary value of the number of Time Slot (in the incoming DS1 frame) being received and output to the Terminal Equipment via the Receive Payload Data Output Interface block associated with Framer_n. The Terminal Equipment should use the RxTSClk_n clock to sample these five output pins in order to identify the time-slot being processed by the Receive Section of Framer_n. **Receive Serial Signaling Output--Receive Framer_n:** These pins can be used to output robbed-bit signaling data extracted from an incoming DS1 frame, if Framer_n is configured accordingly.

RECEIVE SERIAL DATA OUTPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxCHN0_1 RxCHN1_1 RxCHN2_1 RxCHN3_1	C9 B15 G15 V18	O	**Receive Framer_n--Time Slot Octet Identifier Output-Bit 1:** These output signals (RxTSb4_n through RxTSb0_n) reflect the five-bit binary value of the number of Time Slot (in the incoming DS1 frame) being received and output to the Terminal Equipment via the Receive Payload Data Output Interface block associated with Framer_n. The Terminal Equipment should use the RxTSClk_n clock to sample these five output pins in order to identify the time-slot being processed by the Receive Section of Framer_n. **Receive Serial Fractional T1/E1 Input--Receive Framer_n:** These pins can be used to output fractional DS1/E1 payload data extracted from an inbound DS1/E1 frame, if Framer_n is configured accordingly. In this mode, terminal equipment will use either rising edge of RxTSClk_n or RxSerClk_n to clock in fractional DS1/E1 payload data. Please see pin description of RxTSClk_n for details.
RxCHN0_2 RxCHN1_2 RxCHN2_2 RxCHN3_2	B9 A17 K18 T15	O	**Receive Framer_n--Time Slot Octet Identifier Output-Bit 2:** These output signals (RxTSb4_n through RxTSb0_n) reflect the five-bit binary value of the number of Time Slot (in the incoming DS1 frame) being received and output to the Terminal Equipment via the Receive Payload Data Output Interface block associated with Framer_n. The Terminal Equipment should use the RxTSClk_n clock to sample these five output pins in order to identify the time-slot being processed by the Receive Section of Framer_n. **Receive Framer_n -- Time Slot Identifier Serial Output** If RxTSb1_n pin is configured as RxFrTD_n to output fractional DS1 payload data from Framer_n, then these pins serially output the five-bit binary value of the number of the Time Slot being accepted and processed by the Transmit Payload Data Input Interface block associated with Framer_n.
RxCHN0_3 RxCHN1_3 RxCHN2_3 RxCHN3_3	C10 D18 L16 T14	O	**Receive Framer_n-Time Slot Octet Identifier Output-Bit 3:** These output signals (RxTSb4_n through RxTSb0_n) reflect the five-bit binary value of the number of Time Slot (in the incoming DS1 frame) being received and output to the Terminal Equipment via the Receive Payload Data Output Interface block associated with Framer_n. The Terminal Equipment should use the RxTSClk_n clock to sample these five output pins in order to identify the time-slot being processed by the Receive Section of Framer_n. **Receive 8KHz Clock-Receive Framer_n:** These pins output a reference 8KHz signal clock as if Framer_n is configured accordingly.
RxCHN0_4 RxCHN1_4 RxCHN2_4 RxCHN3_4	B10 E17 K16 U14	O	**Receive Framer_n--Time Slot Octet Identifier Output-Bit 4:** These output signals (RxTSb4_n through RxTSb0_n) reflect the five-bit binary value of the number of Time Slot (in the incoming DS1 frame) being received and output to the Terminal Equipment via the Receive Payload Data Output Interface block associated with Framer_n. The Terminal Equipment should use the RxTSClk_n clock to sample these five output pins in order to identify the time-slot being processed by the Receive Section of Framer_n.

RECEIVE SERIAL DATA OUTPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxCHCLK0 RxCHCLK1 RxCHCLK2 RxCHCLK3	A8 A16 H17 P17	O	**Receive Channel Clock Output Signal—Framer_n:** This pin indicates the boundary of each time slot of an inbound DS1/E1 frame. **DS1 Mode:** Each of these output pins are a 192kHz clock output which pulses "High" whenever the Receive Payload Data Output Interface block outputs the LSB of each of the 24 time slots (within the inbound DS1 data stream) on the RxSer_n pin. The Terminal Equipment should use this clock signal to sample the RxTSb0_n through RxTSb4_n output signals, and identify the time-slot being processed via the "Receive Section" of each Framer_n. If RxTSb1_n pin is configured as RxFrTD_n to output fractional DS1 payload data from Framer_n, the RxTSClk_n pin can be configured to function as one of the following: The pin will output gaped fractional DS1 clock that can be used by terminal equipment to clock out fractional DS1 payload data at rising edge of the clock. Otherwise, this pin will be a clock enable signal to Receive fractional DS1 Output (RxFrTD_n) if Framer_n is configured accordingly. In this mode, fractional DS1 payload data is clocked into the terminal equipment using un-gapped RxSerClk_n. **E1 Mode:** Each of these output pins are a 256kHz clock output which pulses "High" whenever the Receive Payload Data Output Interface block outputs the LSB of each of the 32 time slots (within the inbound E1 data stream) on the RxSer_n pin. The Terminal Equipment should use this clock signal to sample the RxTSb0_n through RxTSb4_n output signals, and identify the time-slot being processed via the "Receive Section" of each Framer_n. If RxTSb1_n pin is configured as RxFrTD_n to output fractional E1 payload data from Framer_n, the RxTSClk_n pin can be configured to function as one of the following: The pin will output gaped fractional E1 clock that can be used by terminal equipment to clock out fractional E1 payload data at rising edge of the clock. Otherwise, this pin will be a clock enable signal to Receive fractional E1 Output (RxFrTD_n) if Framer_n is configured accordingly. In this mode, fractional E1 payload data is clocked into the terminal equipment using un-gaped RxSerClk_n.
RxCASYNC0 RxCASYNC1 RxCASYNC2 RxCASYNC3	D10 B17 H15 T18	O	**Receive "CAS Multiframe" Sync Output Signal--Framer_n:** This E1-only signal pulses "High" for one period of RxSerClk_n whenever the Receive E1 Output Interface of Framer_n outputs the first bit, within a given "CAS Multiframe". ***NOTE:*** *This output pin is inactive if Common Channel Signaling is enabled.*

RECEIVE LINE INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RTIP0 RTIP1 RTIP2 RTIP3	E1 G1 J1 L1	I	**Receive Positive Analog Input** RTIP is the positive differential input from the line interface. Along with the RRING signal, these pins should be coupled to a 1:1 transformer for proper operation.

RECEIVE LINE INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RRING0 RRING1 RRING2 RRING3	F1 H1 K1 M1	I	**Receive Negative Analog Input** RRING is the negative differential input from the line interface. Along with the RTIP signal, these pins should be coupled to a 1:1 transformer for proper operation.
RxLOS_0 RxLOS_1 RxLOS_2 RxLOS_3	B7 C18 G16 U18	O	**Receive Loss of Signal Output Indicator** This output pin will toggle "High" (declare LOS) if the Receive block associated with Channel N determines that an RLOS condition occurs according to G.775.

TRANSMIT LINE INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TTIP0 TTIP1 TTIP2 TTIP3	E4 G4 J4 L4	O	**Transmit Positive Analog Output** TTIP is the positive differential output to the line interface. Along with the TRING signal, these pins should be coupled to a 1:2 step up transformer for proper operation.
TRING0 TRING1 TRING2 TRING3	F4 H4 K4 M4	O	**Transmit Negative Analog Output** TRING is is the negative differential output to the line interface. Along with the TTIP signal, these pins should be coupled to a 1:2 step up transformer for proper operation.
TxON	N1	I	**Transmitter On** Upon power up, the transmit outputs (TTIP/TRING) are tri-stated. Turning the transmitters On or Off is selected by programming the appropriate channel register if this pin is pulled "High". If the TxON pin is pulled "Low", all 4 Channels are tri-stated. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

TIMING INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
MCLKIN	A4	I	**Oscillator Clock:** This is a programmable operation clock input. This clock input can be selected by programming the appropriate global register.
E1MCLKnOUT	A3	O	**2.048MHz Output Clock Reference**
T1MCLKnOUT	B4	O	**1.544MHz Output Clock Reference**
E1OSCCLK	P2	I/O	**E1 Master Clock** This pin is used to apply a 65.536MHz, 32.768MHz, or a 16.384MHz input clock to be used as the internal clock reference if 8KEXTOSC is pulled "High". If 8KEXTOSC is pulled "Low", this pin becomes an E1 output clock.
T1OSCCLK	P4	I/O	**T1 Master Clock** This pin is used to apply a 49.408MHz, 24.704MHz, or a 12.352MHz input clock to be used as the internal clock reference if 8KEXTOSC is pulled "High". If 8KEXTOSC is pulled "Low", this pin becomes a T1 output clock.

TIMING INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
8KSYNC	R2	I/O	**8kHz Clock Reference** This pin accepts an 8kHz clock reference when 8KEXTOSC is pulled "High". When 8KEXTOSC is pulled "Low", this pin becomes an output reference of 8kHz based on the MCLKIN input. Therefore, the duty cycle of this output is determined by the time period of the input clock reference.
8KEXTOSC	N4	I	**External Oscillator Select** This pin is used to select between an external or internal clock reference for T1 and E1 operation. If this pin is pulled "High", pins E1OSCCLK and T1OSCCLK are used to provide the timing reference for this device. If this pin is pulled "Low", the device uses an external 8kHz clock (applied directly to pin 8KSYNC, AB3) and the recovered clock from the line interface CDR. ***NOTE:*** *This pin is pulled "Low" with a 50kΩ resistor.*
ANALOG	E5	O	**Factory Test Mode Pin** ***Note:*** *For Internal Use Only*
LOP	N2	I	**Loss of Power for E1 Only / Input Pin for Messaging**

JTAG

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TCK	C7	I	**Test clock:** Boundary Scan clock input. ***Note****: This input pin should be pulled "Low" for normal operation*
TMS	C6	I	**Test Mode Select:** Boundary Scan Mode Select input. ***Note****: This input pin should be pulled "Low" for normal operation*
TDI	B6	I	**Test Data In:** Boundary Scan Test data input ***Note****: This input pin should be pulled "Low" for normal operation*
TDO	D5	O	**Test Data Out:** Boundary Scan Test data output
TRST	A6	I	**JTAG Test Reset Input**
TEST	B11	I	**Factory Test Mode Pin** ***Note:*** *User should tie this pin to ground*
aTEST	B5	I	**Factory Test Mode Pin** ***Note:*** *User should tie this pin to ground*
JTAG_Ring	B2	I	**JTAG_Ring Test Pin**
JTAG_Tip	C3	I	**JTAG_Tip Test Pin**

MICROPROCESSOR INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7	T4 U3 V8 V9 T10 V10 U11 R11	I/O	**Bidirectional Microprocessor Data Bus** Data[7:0] is a bi-directional data bus used for read and write operations. ***NOTE:*** *The bi-directional data bus is used for storing and retrieving information through the DMA interface if enabled.*
$\overline{REQ0}$ $\overline{REQ1}$	R1 R3	O	**DMA Cycle Request Output—DMA Controller 0 (Write)**: The Framer asserts this output pin (toggles it "Low") when at least one of the Transmit HDLC buffers are empty and can receive one more HDLC message. The Framer negates this output pin (toggles it “High”) when the HDLC buffer can no longer receive another HDLC message. **DMA Cycle Request Output—DMA Controller 1 (Read):** The Framer asserts this output pin (toggles it "Low") when one of the Receive HDLC buffer contains a complete HDLC message that needs to be read by the µC/µP. The Framer negates this output pin (toggles it High) when the Receive HDLC buffers are depleted.
$\overline{INT}$	R8	O	**Interrupt Request Output:** The Framer will assert this active "Low" output (toggles it "Low"), to the local µP, anytime it requires interrupt service.
PCLK	V1	I	**Microprocessor Clock Input:** This clock signal is the Microprocessor Interface System clock. This clock signal is used for synchronous/burst/DMA data transfer. The maximum frequency of this clock signal is 33MHz.
iADDR	U1	I	**This Pin Must be Tied “Low” for Normal Operation.**
fADDR	T1	I	**This Pin Must be Tied “High” for Normal Operation.**
PTYPE0 PTYPE1 PTYPE2	V2 V4 T8	I	**Microprocessor Type Input: Bit 0 (LSB):** This input pin, along with µPTYPE1 and µPTYPE2 permit the user to specify which type of Microprocessor/Microcontroller to be interfaced the Framer. **Microprocessor Type Input: Bit 1** **Microprocessor Type Input: Bit 2**

µPType2	µPType1	µPType0	MICROPROCESSOR TYPE
0	0	0	68HC11, 8051, 80C188
0	0	1	MOTOROLA 68K
1	0	1	IBM POWER PC 403

MICROPROCESSOR INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
$\overline{RDY}$	T3	O	**Ready/Data Transfer Acknowledge Output:** The exact behavior of this pin depends upon which Microprocessor the Framer is configured to interface to: **Intel Type Microprocessors** This output pin toggles "Low" when the Framer is ready to respond to the current PIO (Programmed I/O) or Burst Transaction. **Motorola Type Microprocessors** This output pin toggles "Low" when the Framer has completed the current bus cycle.
ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 ADDR5 ADDR6 ADDR7 ADDR8 ADDR9 ADDR10 ADDR11 ADDR12 ADDR13	U5 V5 R5 T6 U6 V6 R6 T7 V7 U9 R7 R9 R10 V11	I	**Microprocessor Interface Address Bus Input Bit 0 -- (LSB)** A[13:0] is a direct address bus for permitting access to internal registers for read and write operations.
$\overline{DBEN}$	U4	I	**Data Bus Enable Input pin**.
ALE	U8	I	**Address Latch Enable Input_Address Strobe**
$\overline{CS}$	V13	I	**Microprocessor Interface—Chip Select Input:** The Microprocessor/Microcontroller must assert this input pin (toggle it "Low") in order to exchange data with the Framer. ***Note:*** *For the 68K MPU, this signal is generated by address decode and address strobe.*
$\overline{RD}$	V3	I	**Microprocessor Interface—Read Strobe Input:** The exact behavior of this pin depends upon the type of Microprocessor/Micro-controller the Framer has been configured to interface to, as defined by the µPTYPE[2:0] pins. ***Note:*** *See pin T25 (µPType0) for the µP selection table.*
$\overline{WR}$	V12	I	**Microprocessor Interface—Write Strobe Input** **"Low" :** Indicates current bus cycle is a write cycle: Intel 51, 188, MIPS350x **"High" :** Indicates present bus cycle is a write cycle: Intel x86, i960 **"Low" :** Indicates current bus cycle is a read cycle: Intel x86, i960 **"High" :** Indicates present bus cycle is a read cycle: Motorola, Power PC 403 **"Low" :** Also used as write strobe in DMA transfer

MICROPROCESSOR INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
$\overline{ACK0}$	T2	I	**DMA Cycle Acknowledge Input—DMA Controller 0 (Write):** The external DMA Controller will assert this input pin "Low" when the following two conditions are met: a. After the DMA Controller, within the Framer has asserted (toggled "Low"), the Req_0 output signal. b. When the external DMA Controller is ready to transfer data from external memory to the selected Transmit HDLC buffer. At this point, the DMA transfer between the external memory and the selected Transmit HDLC buffer may begin. After completion of the DMA cycle, the external DMA Controller will negate this input pin after the DMA Controller within the Framer has negated the $\overline{Req\_0}$ output pin. The external DMA Controller must do this in order to acknowledge the end of the DMA cycle.
$\overline{ACK1}$	U2		**DMA Cycle Acknowledge Input—DMA Controller 1 (Read):** The external DMA Controller asserts this input pin "Low" when the following two conditions are met: a. After the DMA Controller, within the Framer has asserted (toggled "Low"), the Req_1 output signal. b. When the external DMA Controller is ready to transfer data from the selected Receive HDLC buffer to external memory. At this point, the DMA transfer between the selected Receive HDLC buffer and the external memory may begin. After completion of the DMA cycle, the external DMA Controller will negate this input pin after the DMA Controller within the Framer has negated the $\overline{Req\_1}$ output pin. The external DMA Controller will do this in order to acknowledge the end of the DMA cycle.
$\overline{BLAST}$	U10	I	**Last Cycle of Burst Indicator Input:** The Microprocessor asserts this pin "Low"when it is performing its last read or write cycle, within a burst operation.
$\overline{RESET}$	P1	I	**Hardware Reset Input** $\overline{Reset}$ is an active low input. If this pin is pulled "Low" for more than 10µS, the device will be reset.

POWER SUPPLY PINS

SIGNAL NAME	TYPE	DESCRIPTION
VDD	PWR	**Framer Block Power Supply** B8, D16, J16, P3, R13, R15, T9, U7
DVDD	PWR	**Digital Power Supply for LIU Section** C4
AVDD	PWR	**Analog Power Supply for LIU Section** A2
RVDD	PWR	**Receiver Analog Power Supply for LIU Section** E3, G3, J3, L3
TVDD	PWR	**Transmitter Analog Power Supply for LIU Section** F3, H3, K3, M3
VDDPLL	PWR	**Analog Power Supply for PLL** B1, C2, D2, D3

GROUND PINS

SIGNAL NAME	TYPE	DESCRIPTION
VSS	GND	**Framer Block Ground** A5, B14, C16, M15, M16, R4, T5, U16
DGND	GND	**Digital Ground for LIU Section** C5
AGND	GND	**Analog Ground for LIU Section** B3
RGND	GND	**Receiver Analog Ground for LIU Section** E2, G2, J2, L2
TGND	GND	**Transmitter Analog Ground for LIU Section** F2, H2, K2, M2
PLLGND	GND	**Analog Ground for PLL** A1, C1, D1, D4

1.0 MICROPROCESSOR INTERFACE BLOCK

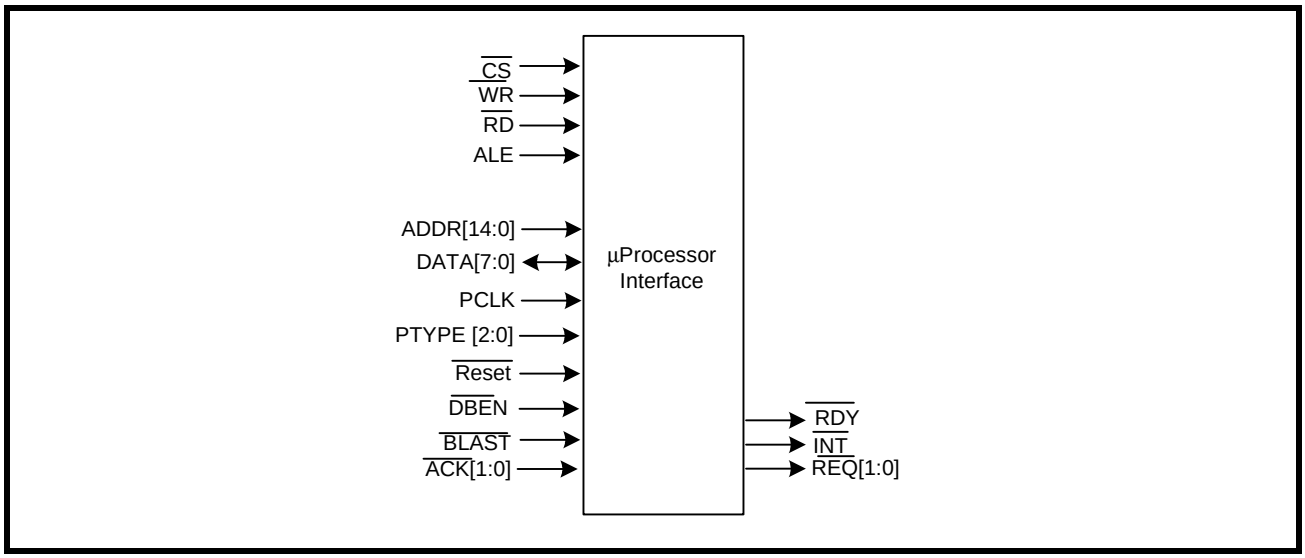
The Microprocessor Interface section supports communication between the local microprocessor (µP) and the Framer/LIU combo. The XRT86L34 supports an Intel asynchronous interface, Motorola 68K asynchronous, and a Motorola Power PC interface. The microprocessor interface is selected by the state of the PTYPE[2:0] input pins. Selecting the microprocessor interface is shown in Table 2.

TABLE 2: SELECTING THE MICROPROCESSOR INTERFACE MODE

PTYPE[2:0]	MICROPROCESSOR MODE
0h (000)	Intel 68HC11, 8051, 80C188 (Asynchronous)
1h (001)	Motorola 68K (Asynchronous)
7h (111)	Motorola MPC8260, MPC860 Power PC (Synchronous)

The XRT86L34 uses multipurpose pins to configure the device appropriately. The local µP configures the Framer/LIU by writing data into specific addressable, on-chip Read/Write registers. The microprocessor interface provides the signals which are required for a general purpose microprocessor to read or write data into these registers. The microprocessor interface also supports polled and interrupt driven environments. A simplified block diagram of the microprocessor is shown in Figure 2.

FIGURE 2. SIMPLIFIED BLOCK DIAGRAM OF THE MICROPROCESSOR INTERFACE BLOCK



1.0.1 The Microprocessor Interface Block Signals

The XRT86L34 may be configured into different operating modes and have its performance monitored by software through a standard microprocessor using data, address and control signals. These interface signals are described below in Table 3, Table 4, and Table 5. The microprocessor interface can be configured to operate in Intel mode or Motorola mode. When the microprocessor interface is operating in Intel mode, some of the control signals function in a manner required by the Intel 80xx family of microprocessors. Likewise, when the microprocessor interface is operating in Motorola mode, then these control signals function in a manner as required by the Motorola Power PC family of microprocessors. (For using a Motorola 68K asynchronous processor, see Figure 5 and Table 8) Table 3 lists and describes those microprocessor interface signals whose role is constant across the two modes. Table 4 describes the role of some of these signals when the microprocessor interface is operating in the Intel mode. Likewise, Table 5 describes the role of these signals when the microprocessor interface is operating in the Motorola mode.

TABLE 3: XRT86L34 MICROPROCESSOR INTERFACE SIGNALS THAT EXHIBIT CONSTANT ROLES IN BOTH INTEL AND MOTOROLA MODES

PIN NAME	TYPE	DESCRIPTION
PTYPE[2:0]	I	**Microprocessor Interface Mode Select Input pins** These three pins are used to specify the microprocessor interface mode. The relationship between the state of these three input pins, and the corresponding microprocessor mode is presented in Table 2.
DATA[7:0]	I/O	**Bi-Directional Data Bus for register "Read" or "Write" Operations.**
ADDR[14:0]	I	**15-Bit Address Bus Inputs** The XRT86L34 microprocessor interface uses a direct address bus. This address bus is provided to permit the user to select an on-chip register for Read/Write access.
$\overline{CS}$	I	**Chip Select Input** This active low signal selects the microprocessor interface of the XRT86L34 and enables Read/Write operations with the on-chip register locations.

TABLE 4: INTEL MODE: MICROPROCESSOR INTERFACE SIGNALS

XRT86L34 PIN NAME	INTEL EQUIVALENT PIN	TYPE	DESCRIPTION
ALE	ALE	I	**Address-Latch Enable:** This active high signal is used to latch the contents on the address bus ADDR[14:0]. The contents of the address bus are latched into the ADDR[14:0] inputs on the falling edge of ALE.
$\overline{RD}$	$\overline{RD}$	I	**Read Signal:** This active low input functions as the read signal from the local µP. When this pin is pulled "Low" (if $\overline{CS}$ is "Low") the XRT86L34 is informed that a read operation has been requested and begins the process of the read cycle.
$\overline{WR}$	$\overline{WR}$	I	**Write Signal:** This active low input functions as the write signal from the local µP. When this pin is pulled "Low" (if $\overline{CS}$ is "Low") the XRT86L34 is informed that a write operation has been requested and begins the process of the write cycle.
$\overline{RDY}$	$\overline{RDY}$	O	**Ready Output:** This active low signal is provided by the XRT86L34 device. It indicates that the current read or write cycle is complete, and the XRT86L34 is waiting for the next command.

TABLE 5: MOTOROLA MODE: MICROPROCESSOR INTERFACE SIGNALS

XRT86L34 PIN NAME	MOTOROLA EQUIVALENT PIN	TYPE	DESCRIPTION
ALE	TS	I	**Transfer Start:** This active high signal is used to latch the contents on the address bus ADDR[14:0]. The contents of the address bus are latched into the ADDR[14:0] inputs on the falling edge of TS.
$\overline{WR}$	R/$\overline{W}$	I	**Read/Write:** This input pin from the local µP is used to inform the XRT86L34 whether a Read or Write operation has been requested. When this pin is pulled "High", $\overline{WE}$ will initiate a read operation. When this pin is pulled "Low", $\overline{WE}$ will initiate a write operation.
$\overline{RD}$	$\overline{WE}$	I	**Write Enable:** This active low input functions as the read or write signal from the local µP dependent on the state of R/W. When $\overline{WE}$ is pulled "Low" (If $\overline{CS}$ is "Low") the XRT86L34 begins the read or write operation.
No Pin	$\overline{OE}$	I	**Output Enable:** This signal is not necessary for the XRT86L34 to interface to the MPC8260 or MPC860 Power PCs.
PCLK	CLKOUT	I	**Synchronous Processor Clock:** This signal is used as the timing reference for the Power PC synchronous mode.
$\overline{RDY}$	$\overline{TA}$	O	**Transfer Acknowledge:** This active low signal is provided by the XRT86L34 device. It indicates that the current read or write cycle is complete, and the XRT86L34 is waiting for the next command.

1.1 INTEL MODE PROGRAMMED I/O ACCESS (ASYNCHRONOUS)

If the XRT86L34 is interfaced to an Intel type µP, then it should be configured to operate in the Intel mode. Intel type Read and Write operations are described below.

Intel Mode Read Cycle

Whenever an Intel-type µP wishes to read the contents of a register, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[14:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the XRT86L34, by toggling it "Low". This action enables further communication between the µP and the XRT86L34 microprocessor interface block.
3. Toggle the ALE input pin "High". This step enables the address bus input drivers, within the microprocessor interface block of the XRT86L34.
4. The µP should then toggle the ALE pin "Low". This step causes the XRT86L34 to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
5. Next, the µP should indicate that this current bus cycle is a Read operation by toggling the $\overline{RD}$ input pin "Low". This action also enables the bi-directional data bus output drivers of the XRT86L34.
6. After the µP toggles the Read signal "Low", the XRT86L34 will toggle the $\overline{RDY}$ output pin "Low". The XRT86L34 does this in order to inform the µP that the data is available to be read by the µP, and that it is ready for the next command.
7. After the µP detects the $\overline{RDY}$ signal and has read the data, it can terminate the Read Cycle by toggling the $\overline{RD}$ input pin "High".

NOTE: *ALE can be tied "High" if this signal is not available.*

The Intel Mode Write Cycle

Whenever an Intel type µP wishes to write a byte or word of data into a register within the XRT86L34, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[14:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the XRT86L34, by toggling it "Low". This action enables further communication between the µP and the XRT86L34 microprocessor interface block.
3. Toggle the ALE input pin "High". This step enables the address bus input drivers, within the microprocessor interface block of the XRT86L34.
4. The µP should then toggle the ALE pin "Low". This step causes the XRT86L34 to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
5. The µP should then place the byte or word that it intends to write into the target register, on the bi-directional data bus DATA[7:0].
6. Next, the µP should indicate that this current bus cycle is a Write operation by toggling the $\overline{WR}$ input pin "Low". This action also enables the bi-directional data bus input drivers of the XRT86L34.
7. After the µP toggles the Write signal "Low", the XRT86L34 will toggle the $\overline{RDY}$ output pin "Low". The XRT86L34 does this in order to inform the µP that the data has been written into the internal register location, and that it is ready for the next command.

NOTE: ALE *can be tied "High" if this signal is not available.*

The Intel Read and Write timing diagram is shown in Figure 3. The timing specifications are shown in Table 6.

FIGURE 3. INTEL µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

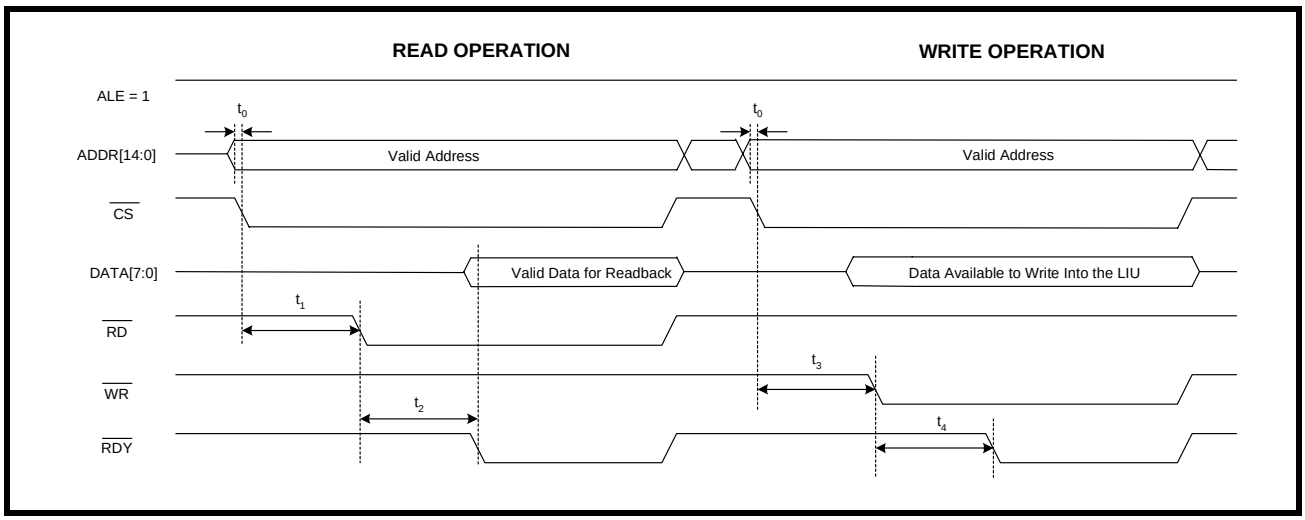


TABLE 6: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{RD}$ Assert	65	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	90	ns
NA	$\overline{RD}$ Pulse Width (t_2)	90	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{WR}$ Assert	65	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	90	ns
NA	$\overline{WR}$ Pulse Width (t_4)	90	-	ns

1.2 MOTOROLA MODE PROGRAMMED I/O ACCESS (SYNCHRONOUS)

If the XRT86L34 is interfaced to a Motorola type µP, it should be configured to operate in the Motorola mode. Motorola type programmed I/O Read and Write operations are described below.

Motorola Mode Read Cycle

Whenever a Motorola type µP wishes to read the contents of a register, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[14:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the XRT86L34, by toggling it "Low". This action enables further communication between the µP and the XRT86L34 microprocessor interface block.
3. The µP should then toggle the TS pin "Low". This step causes the XRT86L34 to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
4. Next, the µP should indicate that this current bus cycle is a Read operation by pulling the R/$\overline{W}$ input pin "High".
5. Toggle the $\overline{WE}$ input pin "Low". This action enables the bi-directional data bus output drivers of the XRT86L34.
6. After the µP toggles the $\overline{WE}$ signal "Low", the XRT86L34 will toggle the $\overline{TA}$ output pin "Low". The XRT86L34 does this in order to inform the µP that the data is available to be read by the µP, and that it is ready for the next command.
7. After the µP detects the $\overline{TA}$ signal and has read the data, it can terminate the Read Cycle by toggling the $\overline{WE}$ input pin "High".

Motorola Mode Write Cycle

Whenever a motorola type µP wishes to write a byte or word of data into a register within the XRT86L34, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[14:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the XRT86L34, by toggling it "Low". This action enables further communication between the µP and the XRT86L34 microprocessor interface block.
3. The µP should then toggle the TS pin "Low". This step causes the XRT86L34 to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
4. Next, the µP should indicate that this current bus cycle is a Write operation by pulling the R/$\overline{W}$ input pin "Low".
5. Toggle the $\overline{WE}$ input pin "Low". This action enables the bi-directional data bus output drivers of the XRT86L34.
6. After the µP toggles the $\overline{WE}$ signal "Low", the XRT86L34 will toggle the $\overline{TA}$ output pin "Low". The XRT86L34 does this in order to inform the µP that the data has been written into the internal register location, and that it is ready for the next command.
7. After the µP detects the $\overline{TA}$ signal and has read the data, it can terminate the Read Cycle by toggling the $\overline{WE}$ input pin "High".

The Motorola Read and Write timing diagram is shown in Figure 4. The timing specifications are shown in Table 7.

FIGURE 4. MOTOROLA µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

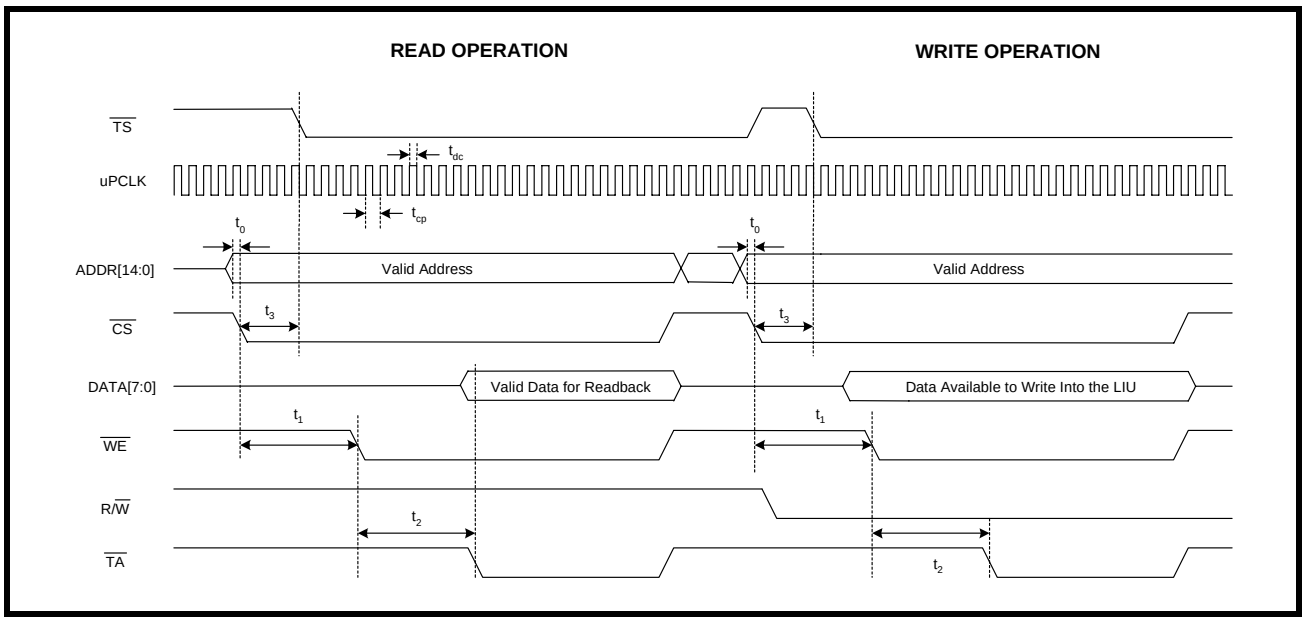


TABLE 7: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{WE}$ Assert	0	-	ns
t_2	$\overline{WE}$ Assert to $\overline{TA}$ Assert	-	90	ns
NA	$\overline{WE}$ Pulse Width (t_2)	90	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{TS}$ Falling Edge	0	-	
t_{dc}	µPCLK Duty Cycle	40	60	%
t_{cp}	µPCLK Clock Period	20	-	ns

FIGURE 5. MOTOROLA 68K µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

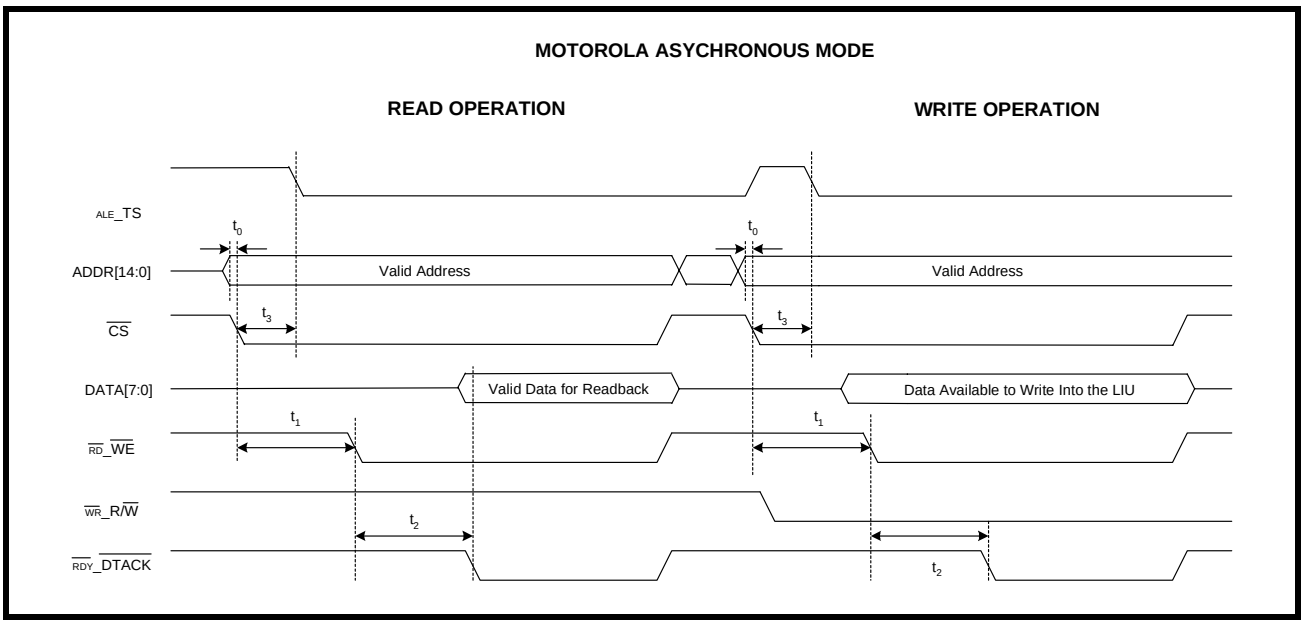


TABLE 8: MOTOROLA 68K MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{DS}$ (Pin $\overline{RD}$_$\overline{WE}$) Assert	65	-	ns
t_2	$\overline{DS}$ Assert to $\overline{DTACK}$ Assert	-	90	ns
NA	$\overline{DS}$ Pulse Width (t_2)	90	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{AS}$ (Pin ALE_TS) Falling Edge	0	-	ns

1.2.1 DMA Read/Write Operations

The XRT86L34 Framer contains two DMA Controller Interfaces which provide support for all eight framers within the chip. The purpose of the two DMA Controllers is to facilitate the rapid block transfer of data between an external memory location and the on-chip HDLC buffers via the Microprocessor Interface.

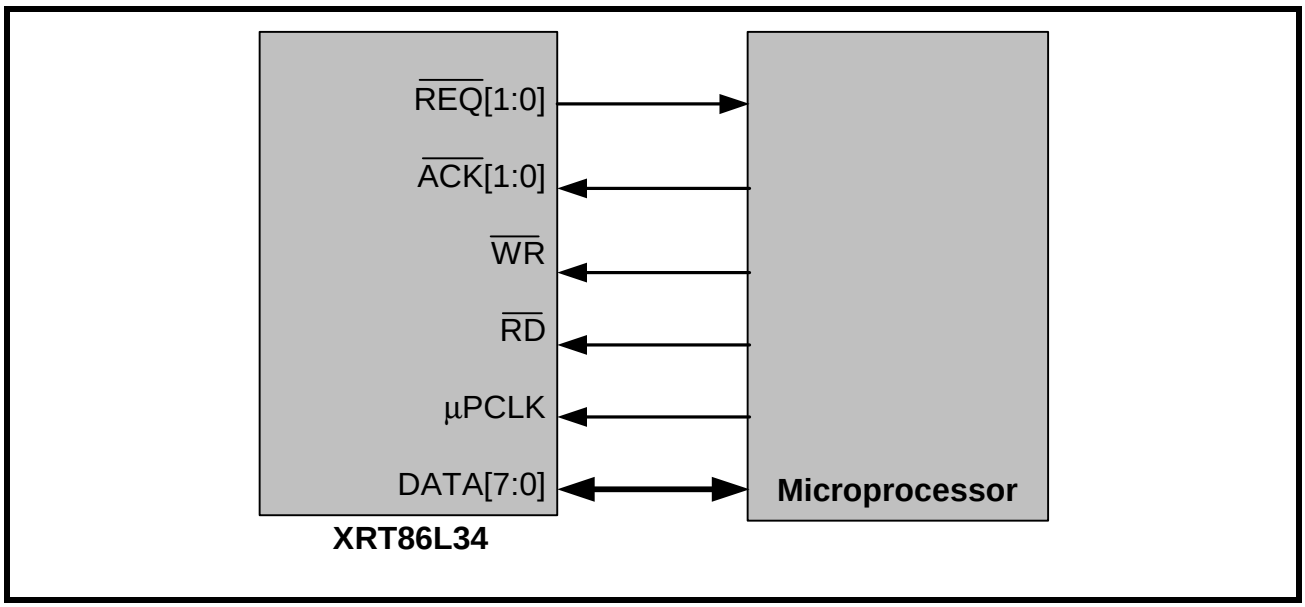
DMA-0 Write DMA Interface

DMA 0 Controller Interface handles data transfer between external memory and the selected Transmit HDLC Buffer.

The DMA cycle starts when the XRT86L34 asserts the $\overline{REQ0}$ output pin. The external DMA Controller then responds by asserting the $\overline{ACK0}$ input pin. The contents of the Microprocessor Interface bi-directional data bus are latched into the XRT86L34 each time the $\overline{WR}$ (Write Strobe) input pin is strobed "Low".

The XRT86L34 ends the DMA cycle by negating the DMA request input ($\overline{REQ0}$) while $\overline{WR}$ is still active. The external DMA Controller acknowledges the end of DMA Transfer by driving the $\overline{ACK0}$ input pin "High".

FIGURE 6. DMA MODE FOR THE XRT86L34 AND A MICROPROCESSOR



1.3 MEMORY MAPPED I/O ADDRESSING

TABLE 9: XRT86L34 FRAMER/LIU REGISTER MAP

ADDRESS [14:0]	CONTENTS
n100h - n1FFh	Channel n - Control Register (Framer Block)
n300h - n3FFh	Channel n - Time Slot (Payload) Control (Framer Block)
n500h - n5FFh	Channel n - Receive Signaling Array (Framer Block)
n600h - n6FFh	Channel n - LAPDn Buffer 0 (Framer Block)
n700h - n7FFh	Channel n - LAPDn Buffer 1 (Framer Block)
n900h - n9FFh	Channel n - Performance Monitor (Framer Block)
nB00h - nBFFh	Channel n - Interrupt Generation/Enable (Framer Block)
nC00h - nDFFh	Reserved
0F00h - 0FFFh	Line Interface Control (LIU Block)

1.4 DESCRIPTION OF THE CONTROL REGISTERS

TABLE 10: REGISTER SUMMARY

REG #	FUNCTION	SYMBOL	HEX	MODE
Control Registers (0xn100 - 0xn1FF)				
0	Clock and E1 Select Register (bit-6 selects E1 mode)	CSR	0xn100	E1
	Clock and T1 Select Register (bit-6 selects T1 mode)			T1
1	Line Interface Control Register	LICR	0xn101	E1
	Line Interface Control Register			T1
2	Reserved	-	0xn102	-
3	Reserved	-	0xn103	-
4	Reserved	-	0xn104	-
5	Reserved	-	0xn105	-
6	Reserved	-	0xn106	-
7	Framing Select Register	FSR	0xn107	E1
	Framing Select Register	FSR	0xn107	T1, J1
8	Alarm Generation Register	AGR	0xn108	E1
	Alarm Generation Register			T1
9	Synchronization MUX Register	SMR	0xn109	E1
	Synchronization MUX Register			T1
10	Transmit Signaling and Data Link Select Register	TSDLSR	0xn10A	E1
	Transmit Signaling and Data Link Select Register	TSDLSR	0xn10A	T1
11	Framing Control Register	FCR	0xn10B	E1
	Framing Control Register	FCR	0xn10B	T1
12	Receive Signaling & Data Link Select Register	RS&DLSR	0xn10C	E1
	Receive Signaling & Data Link Select Register	RS&DLSR	0xn10C	T1
13	Signaling Change Register 0	SCR0	0xn10D	T1/E1
14	Signaling Change Register 1	SCR1	0xn10E	T1/E1
15	Signaling Change Register 2	SCR2	0xn10F	T1/E1
16	Signaling Change Register 3	SCR3	0xn110	T1/E1
17	Receive National Bits Register	RNBR	0xn111	E1
18	Receive Extra Bits Register	REBR	0xn112	T1/E1
19	Data Link Control Register 1	DLCR1	0xn113	T1/E1
20	Transmit Data Link Byte Count Register 1	TDLBCR1	0xn114	T1/E1

TABLE 10: REGISTER SUMMARY

REG #	FUNCTION	SYMBOL	HEX	MODE
21	Receive Data Link Byte Count Register 1	RDLBCR1	0xn115	T1/E1
22	Slip Buffer Control Register	SBCR	0xn116	T1/E1
23	FIFO Latency Register	FIFOLR	0xn117	T1/E1
24	DMA 0 (Write) Configuration Register	D0WCR	0xn118	T1/E1
25	DMA 1 (Read) Configuration Register	D1CR	0xn119	T1/E1
26	Interrupt Control Register	ICR	0xn11A	T1/E1
27	LAPD Select Register	LAPDSR	0xn11B	T1/E1
28	Customer Installation Alarm Generation Register	CIAGR	0xn11C	T1
29	Performance Report Control Register	PRCR	0xn11D	T1
30	Gapped Clock Control Register	GCCR	0xn11E	T1
31	Transmit Interface Control Register	TICR	0xn120	E1
	Transmit Interface Control Register			T1
32	Receive Interface Control Register	RICR	0xn122	E1
	Receive Interface Control Register			T1
33	DS1 Test Register: PRBS Control & Status	DS1TR	0xn123	T1
34	Loopback Code Control Register	LCCR	0xn124	T1/E1
35	Transmit Loopback Code Register	TLCR	0xn125	T1/E1
36	Receive Loopback Activation Code Register	RLACR	0xn126	T1/E1
37	Receive Loopback Deactivation Code Register	RLDCR	0xn127	T1/E1
38	Transmit Sa Select Register	TSASR	0xn130	T1/E1
39	Transmit Sa Auto Control Register 1	TSACR1	0xn131	T1/E1
40	Transmit Sa Auto Control Register 2	TSACR2	0xn132	T1/E1
41	Transmit Sa4 Register	TSA4R	0xn133	T1/E1
42	Transmit Sa5 Register	TSA5R	0xn134	T1/E1
43	Transmit Sa6 Register	TSA6R	0xn135	T1/E1
44	Transmit Sa7 Register	TSA7R	0xn136	T1/E1
45	Transmit Sa8 Register	TSA8R	0xn137	T1/E1
46	Receive Sa4 Register	RSA4R	0xn13B	T1/E1
47	Receive Sa5 Register	RSA5R	0xn13C	T1/E1
48	Receive Sa6 Register	RSA6R	0xn13D	T1/E1
49	Receive Sa7 Register	RSA7R	0xn13E	T1/E1
50	Receive Sa8 Register	RSA8R	0xn13F	T1/E1

TABLE 10: REGISTER SUMMARY

REG #	FUNCTION	SYMBOL	HEX	MODE
51	Data Link Control Register 2	DLCR2	0xn113	T1/E1
52	Transmit Data Link Byte Count Register 2	TDLBCR2	0xn114	T1/E1
53	Receive Data Link Byte Count Register 2	RDLBCR2	0xn115	T1/E1
54	Data Link Control Register 3	DLCR3	0xn113	T1/E1
55	Transmit Data Link Byte Count Register 3	TDLBCR3	0xn114	T1/E1
56	Receive Data Link Byte Count Register 3	RDLBCR3	0xn115	T1/E1
57	Device ID Register	DEVID	0xn1FE	T1/E1
58	Version Number Register	REVID	0xn1FF	T1/E1
Time Slot (payload) Control (0xn300 - 0xn3FF)				
59-90	Transmit Channel Control Register 0-31	TCCr 0-31	0xn300 to 0xn31F	E1
	Transmit Channel Control Register 0-31			T1
91-122	User Code Register 0-31	UCR0-31	0xn320 to 0xn33F	T1/E1
123-154	Transmit Signaling Control Register 0 -31	TSCR0-31	0xn340 to 0xn35F	E1
	Transmit Signaling Control Register 0-31			T1
155-186	Receive Channel Control Register 0-31	RCCR0-31	0xn360 to 0xn37F	E1
	Receive Channel Control Register 0-31			T1
187-218	Receive User Code Register 0-31	RUCR0-31	0xn380 to 0xn39F	E1
	Receive User Code Register 0-31			T1
219-250	Receive Signaling Control Register 0-31	RSCR0-31	0xn3A0 to 0xn3BF	T1/E1
251-282	Receive Substitution Signaling Register 0-31	RSSR0-31	0xn3C0 to 0xn3DF	E1
	Receive Substitution Signaling Register 0-24	RSSR0-24		T1
Receive Signaling Array (0xn500 - 0xn51F)				
283-314	Receive Signaling Array Register 0	RSAR0-31	0xn500 to 0xn51F	T1/E1

TABLE 10: REGISTER SUMMARY

REG #	FUNCTION	SYMBOL	HEX	MODE
LAPDn Buffer 0 (0xn600 - 0xn660)				
315-410	LAPD Buffer 0 Control Register	LAPDBCR0	0xn600 to 0xn660	T1/E1
LAPDn Buffer 1 (0xn700 - 0xn760)				
411-506	LAPD Buffer 1 Control Register	LAPDBCR1	0xn700 to 0xn760	T1/E1
Performance Monitor				
507	T1/E1 Receive Line Code Violation Counter: MSB	T1/E1 RLCVCL	0xn900	T1/E1
508	T1/E1 Receive Line Code Violation Counter: LSB	T1/E1 RLCVCU	0xn901	T1/E1
509	T1/E1 Receive Frame Alignment Error Counter: LSB	T1/E1 RFBECU	0xn902	T1/E1
510	T1/E1 Receive Frame Alignment Error Counter: LSB	T1/E1 RFAECL	0xn903	T1/E1
511	T1/E1 Receive Severely Errored Frame Counter: MSB	T1/E1RSEFC	0xn904	T1/E1
512	T1/E1 Receive Synchronization Bit (CRC-6 (T1) CRC-4 (E1) Block) Error Counter: MSB	T1/E1 RSBEC	0xn905	T1/E1
513	T1/E1 Receive Far-End Block Error Counter: MSB	T1/E1 RFEBECU	0xn907	T1/E1
514	PMON E1 Receive Far-End Block Error Counter -MSB	PE1RFEBEC	0xn908	E1
515	T1/E1 Receive Far-End Block Error Counter: LSB P	T1/E1 RFEBECL	0xn908	T1/E1
516	T1/E1 Receive Slip Counter	T1/E1RSR	0xn909	T1/E1
517	T1/E1 Receive Loss of Frame Counter	T1/E1 RLOVC	0xn90A	T1/E1
518	T1/E1 Receive Change of Frame Alignment Counter	T1/E1 RCOAC	0xn90B	T1/E1
519	LAPD Frame Check Sequence Error counter	LFCSEC	0xn90C	T1/E1
520	T1/E1 PRBS bit Error Counter: MSB P	T1/E1 PBECU	0xn90D	T1/E1
521	T1/E1 PRBS bit Error Counter: LSB P	T1/E1 PBECL	0xn90E	T1/E1
522	T1/E1 Transmit Slip Counter	T1/E1RSR	0xn90F	T1/E1
Interrupt Generation/Enable Register Address Map (0xnB00 - 0xnB41)				
523	Block Interrupt Status Register	BISR	0xnB00	T1/E1
524	Block Interrupt Enable Register	BIER	0xnB01	T1/E1
525	Alarm & Error Interrupt Status Register	AESR	0xnB02	T1/E1
526	Alarm & Error Interrupt Enable Register	AEIER	0xnB03	E1
	Alarm & Error Interrupt Enable Register			T1
527	Framer Interrupt Status Register	FISR	0xnB04	E1
	Framer Interrupt Status Register			T1

TABLE 10: REGISTER SUMMARY

REG #	FUNCTION	SYMBOL	HEX	MODE
528	Framer Interrupt Enable Register	FIER	0xnB05	E1
	Framer Interrupt Enable Register			T1
529	Data Link Status Register 1	DLSR1	0xnB06	T1/E1
530	Data Link Interrupt Enable Register 1	DLIER1	0xnB07	T1/E1
531	Slip Buffer Interrupt Enable Register	SBIER	0xnB08	T1/E1
532	Slip Buffer Interrupt Status Register	SBISR	0xnB09	T1/E1
533	Receive Loopback code Interrupt and Status Register	RLCISR	0xnB0A	T1/E1
534	Receive Loopback code Interrupt Enable Register	RLCIER	0xnB0B	T1/E1
535	Receive SA (Sa6) Interrupt Register	RSAIR	0xnB0C	T1/E1
536	Receive SA (Sa6) Interrupt Enable Register	RSAIER	0xnB0D	T1/E1
537	Excessive Zero Status Register	EXZSR	0xnB0E	T1/E1
538	Excessive Zero Enable Register	EXZER	0xnB0F	T1/E1
539	SS7 Status Register for LAPD 1	SS7SR1	0xnB10	T1
540	SS7 Enable Register for LAPD 1	SS7ER1	0xnB11	T1
541	Data Link Status Register 2	DLSR2	0xnB16	T1/E1
542	Data Link Interrupt Enable Register 2	DLIER2	0xnB17	T1/E1
543	SS7 Status Register for LAPD 2	SS7SR2	0xnB18	T1
544	SS7 Enable Register for LAPD 2	SS7ER2	0xnB19	T1
545	Data Link Status Register 3	DLSR3	0xnB26	T1/E1
546	Data Link Interrupt Enable Register 3	DLIER3	0xnB27	T1/E1
547	SS7 Status Register for LAPD 3	SS7SR3	0xnB28	T1
548	SS7 Enable Register for LAPD 3	SS7ER3	0xnB29	T1
549	Customer Installation Alarm Status Register	CIASR	0xnB40	T1
550	Customer Installation Alarm Interrupt Enable Register	CIAIER	0xnB41	T1
LIU Register Summary				
551 to 566	Channel 0 LIU Control Register	-	0x0F00 to 0x0F0F	-

TABLE 10: REGISTER SUMMARY

REG #	FUNCTION	SYMBOL	HEX	MODE
567 to 582	Channel 1 LIU Control Register	-	0x0F10 to 0x0F1F	-
583 to 598	Channel 2 LIU Control Register	-	0x0F20 to 0x0F2F	-
599 to 614	Channel 3 LIU Control Register	-	0x0F30 to 0x0F3F	-
615 to 630	Reserved	-	0x0F40 to 0x0F4F	-
631 to 646	Reserved	-	0x0F50 to 0x0F5F	-
647 to 662	Reserved	-	0x0F60 to 0x0F6F	-
663 to 678	Reserved	-	0x0F70 to 0x0F7F	-
679 to 694	Reserved	-	0x0F80 to 0x0FDF	-
695 to 710	LIU Command Control Registers	-	0x0FE0 to 0x0FE9	-
711 to 726	Reserved	-	0x0FEA to 0x0FFF	-

1.4.1 Register Descriptions

TABLE 11: CLOCK SELECT REGISTER E1 MODE

REGISTER 0 - E1 MODE **CLOCK SELECT REGISTER (CSR)** **HEX ADDRESS: 0XN100**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	BPVI	R/W	0	**Bipolar Violation Insertion** This bit forces the BPV on transmit. 0 = No BPV is inserted on transmit encoder. 1 = BPV is inserted on transmit encoder once. A 0 to 1 transition will cause a BPV inserted in the non-BPV data
6	IST1	R/W	1	**T1/E1 Mode select** This bit is used to program the chip to either T1 or E1 mode. 1 =T1 mode 0 =E1 mode.
5	8kHz	R/W	0	**8kHZ Sync Enable** This Read/Write Bit-Field allows the user to configure the transmit sections of all eight framer blocks to synchronize their frame alignment with the signal applied to the 8kREF input pin. Setting this bit-field to a “1” enables this feature for all eight channels. ***NOTE:*** *This bit-field is ignored if TxSerClk_n or RxLineClk_n is configured to be the timing reference for the transmit section.*
4	CLDET	R/W	0	**Clock Loss Detect Enable/Disable Select** Enables a protection feature for the Framer whenever the Recovered Received Line Clock (RxLineClk) is used as the timing source for the transmit section of the framer. If the Clock Loss Detection protection feature is enabled and the Recovered Received Line Clock is used as the timing source, then if the LIU somehow loses clock recovery the Clock Distribution Block will detect this occurrence and automatically begin to use the OSCClk Driven Divided clock as the Transmitter source, until the LIU is able to regain clock recovery.
3	CFS(1)	R/W	0	**Frequency Select** Specifies the frequency of the oscillator clock. 00 = The OSCClk input is 16.384 MHz (internally divided by 1) 01 = The OSCClk input is 32.768 MHz (internally divided by 2) 10 = The OSCClk input is 65.536 MHz (internally divided by 4) 11 = Reserved ***NOTE:*** *This bit-field is ignored if TxSerClk_n or RxLineClk_n is configured to be the timing reference for the transmit section.*
2	CFS(0)	R/W	0	
1	CSS(1)	R/W	0	**Clock Source Select** Specifies the timing source for the Transmit E1 Framer block (associated with this register). 00 = RxLineClk - the Recovered Received Channel Input Clock is chosen as the timing reference for the transmit section of Framer N (Loop Timing) 01 = TxSerClk - The Transmit Serial Data Input Clock is chosen as the timing reference for the timing source for the transmit section of Framer n. 10 = OSCClk - the OSCClk-driven divided clock is chosen as the timing reference for the transmit section of Framer n. 11 = RxLineClk - The Recovered Received Channel Input Clock is chosen as the timing reference for the transmit section of Framer n.
0	CSS(0)	R/W	1	

TABLE 12: CLOCK SELECT REGISTER - T1 MODE

REGISTER 0 -T1 MODE **CLOCK SELECT REGISTER (CSR)** **HEX ADDRESS: 0XN100**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	BPVI	R/W	0	**Bipolar Violation Insertion** This bit forces the BPV on transmit. 0 = No BPV is inserted on transmit encoder. 1 = BPV is inserted on transmit encoder once. A 0 to 1 transition will cause a BPV inserted in the non-BPV data
6	IST1	R/W	1	**T1/E1 Mode select** This bit is used to program the chip to either T1 or E1 mode. 1 =T1 mode 0 =E1 mode.
5	8kHz	R/W	0	**8KhZ Sync Enable** This Read/Write Bit-Field allows the user to configure the transmit sections of all eight framer blocks to synchronize their frame alignment with the signal applied to the 8kREF input pin. Setting this bit-field to a "1" enables this feature for all eight channels. ***NOTE:*** *This bit-field is ignored if TxSerClk_n or RxLineClk_n is configured to be the timing reference for the transmit section.*
4	CLDET	R/W	0	**Clock Loss Detect Enable/Disable Select** 1 = Enables a protection feature for the Framer whenever the Recovered Received Line Clock (RxLineClk) is used as the timing source for the transmit section of the framer. If the Clock Loss Detection protection feature is enabled and the Recovered Received Line Clock is used as the timing source, then if the LIU somehow loses clock recovery the Clock Distribution Block will detect this occurrence and automatically begin to use the OSCClk Driven Divided clock as the Transmitter source, until the LIU is able to regain clock recovery. 0 = Disables protection feature.
3	CFS(1)	R/W	0	**Frequency Select T1 Mode** Specifies the frequency of the oscillator clock. 00 = The OSCClk input is 12.352 MHz (internally divided by 1) 01 = The OSCClk input is 24.704 MHz (internally divided by 2) 10 = The OSCClk input is 49.408 MHz (internally divided by 4) 11 = Reserved ***NOTE:*** *This bit-field is ignored if TxSerClk_n or RxLineClk_n is configured to be the timing reference for the transmit section.*
2	CFS(0)	R/W	0	
1	CSS(1)	R/W	0	**Clock Source Select** Specifies the timing source for the Transmit E1 Framer block (associated with this register). 00 = RxLineClk - the Recovered Received Channel Input Clock is chosen as the timing reference for the transmit section of Framer N (Loop Timing) 01 = TxSerClk - The Transmit Serial Data Input Clock is chosen as the timing reference for the timing source for the transmit section of Framer n. 10 = OSCClk - the OSCClk-driven divided clock is chosen as the timing reference for the transmit section of Framer n. 11 = RxLineClk - The Recovered Received Channel Input Clock is chosen as the timing reference for the transmit section of Framer n.
0	CSS(0)	R/W	1	

TABLE 13: LINE INTERFACE CONTROL REGISTER E1 MODE

REGISTER 1 - E1 MODE **LINE INTERFACE CONTROL REGISTER (LICR)** **HEX ADDRESS: 0XN101**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	FORCE_LOS	R/W	0	**Force Transmit LOS** This bit forces transmitter to emulate LOS outputs. 0 = No LOS is generated. 1 = LOS is transmitted on the line outputs.
6	Reserved	R/W	0	**Reserved**
5	LB(1)	R/W	0	**Loopback Selection** These two Read/Write bit-fields are used to configure a given channel to operate in any of the following loop-back modes 00 = No local loopback 01 = Local loopback 10 = Remote Line Loopback 11 = Reserved
4	LB(0)	R/W	0	
3	Reserved	R/W	0	**Reserved**
2	Reserved	R/W	0	**Reserved**
1	Encode AMI/$\overline{\text{HDB3}}$	R/W	0	**Encode AMI/$\overline{\text{HDB3}}$ Line Code Select** Configures the Transmit LIU Interface block to transmit data via the AMI or HDB3 line codes. 0 = Transmit LIU interface block transmits the E1 frame data in the HDB3 line code. 1 = Transmit LIU interface block transmits the E1 frame data in the AMI line code.
0	Decode AMI/$\overline{\text{HDB3}}$	R/W	0	**Decode AMI/$\overline{\text{HDB3}}$ Line Code Select** Enables or disables the HDB3 decoder with in the Receive LIU interface block. 0 = Enables the HDB3 decoder 1 = Disables the HDB3 decoder

TABLE 14: LINE INTERFACE CONTROL REGISTER T1 MODE

REGISTER 1 - T1 MODE **LINE INTERFACE CONTROL REGISTER (LICR)** **HEX ADDRESS: 0XN101**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	FORCE_LOS	R/W	0	**Force Transmit LOS** This bit forces transmitter to emulate LOS outputs. 0 = No LOS is generated. 1 = LOS is transmitted on the line outputs.
6	Reserved	-	-	**Reserved**
5	LB(1)	R/W	0	**Loopback Selection** These two Read/Write bit-fields are used to configure a given channel to operate in any of the following loop-back modes 00 = No local loopback 01 = Local loopback 10 = Remote Line Loopback 11 = Reserved
4	LB(0)	R/W	0	
3	Reserved	R/W	0	**Reserved**
2	Reserved	R/W	0	**Reserved**
1	Encode AMI/B8ZS	R/W	0	**Encode AMI/B8ZS Line Code Select** Configures the Transmit LIU Interface block to transmit data via the AMI or B8ZS line codes. 0 = Transmit LIU interface block transmits the T1 frame data in the B8ZS line code. 1 = Transmit LIU interface block transmits the T1 frame data in the AMI line code.
0	Decode AMI/B8ZS	R/W	0	**Decode AMI/B8ZS Line Code Select** Enables or disables the HDB3 decoder with in the Receive LIU interface block. 0 = Enables the B8ZS decoder 1 = Disables the B8ZS decoder

TABLE 15: FRAMING SELECT REGISTER-E1 MODE

REGISTER 7- E1 MODE **FRAMING SELECT REGISTER (FSR)** **HEX ADDRESS: 0XN107**

BIT		FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	E1	MODENB	R/W	0	**Annex B Enable** This bit forces framing synchronizer to to be compliant with ITU-T G.706 Annex B for CRC-to-non-CRC interworking detection. 0 = Normal operation. 1 = Annex B is enabled.
6	E1	CRCDIAG	R/W	0	**CRC Diagnostics Select Enable/Disable** This Read/Write bit-field is used to force an errored CRC pattern in the outbound CRC multiframe to be sent on the transmission line. The transmit section will implement this error by inverting the value of CRC bit (C1) 0 = Transmit E1 Framer functions normally (no errors) 1 = Transmits errored CRC bit ***NOTE:*** *This bit-field is ignored if CRC multi-Framing is disabled.*
5	E1	CASSEL(1)	R/W	0	**CAS Multiframe Alignment Algorithm Select** Allows the user to select which CAS Multiframe Alignment algorithm to employ. 00 = CAS Multiframe Alignment disabled 01 = CAS Multiframe Alignment Algorithm 1 enabled 10 = CAS Multiframe Alignment Algorithm 2 (G.732) enabled 11 = CAS Multiframe Alignment disabled
4	E1	CASSEL(0)	R/W	0	
3	E1	CRCSEL(1)	R/W	0	**CRC Multiframe Alignment Criteria Select** Allows the user to select which CRC-Multiframe Alignment to employ. 00 = CRC Multiframe Alignment disabled 01 = CRC Multiframe Alignment enabled. Alignment is declared if at least one valid CRC multiframe alignment signal (0,0,1,0,1,1,E1,E2) is observed within 8ms. 10 = CRC Multiframe Alignment enabled. Alignment is declared if at least two valid CRC multiframe alignment signals (0,0,1,0,1,1,E1,E2) are observed within 8ms with the time separating the two alignment signals being multiples of 2ms. 11:CRC Multiframe Alignment enabled. Alignment is declared if at least 3 valid CRC multiframe alignment signals (0,0,1,0,1,1,E1,E2) are observed within 8ms with the time separating the two alignment signals being multiples of 2ms.
2	E1	CRCSEL(0)	R/W	0	
1	E1	CKSEQ_ENB	R/W	0	**Check Sequence Enable-FAS Alignment** Enable/Disable frame check sequence in FAS alignment process. 0 = Disables Frame Check Sequence 1 = Enables Frame Check Sequence‘
0	E1	FASSEL	R/W	0	**FAS Alignment Algorithm Select** Specifies which algorithm the Receive E1 Framer block uses in its search for FAS Alignment. 0 = Algorithm 1 1 = Algorithm 2

TABLE 16: FRAMING SELECT REGISTER-T1 MODE

REGISTER 7- T1 MODE **FRAMING SELECT REGISTER (FSR)** **HEX ADDRESS: 0xn107**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SIGFRAME	R/W	0	**Enable Signaling Update** Setting this bit to 1 will enable signaling update (transmit and receive) on the superframe boundary. Otherwise, signaling data will be updated once it is received.
6	CRCDIAG	R/W	0	**Force CRC Errors** Setting this bit to 1 will force CRC error on transmit stream.
5	J1_CRC	R/W	0	**CRC Calculation in J1 Mode** Setting this bit to 1 will force CRC calcualtion for J1 format. The J1 CRC6 calculation is based on the actual values of all 4632 bits in a DS1 multiframe including Fe bits instead of assuming all Fe bits to be a one in T1 format.
4	ONEONLY	R/W	0	**Allow Only One Sync Candidate** Setting this bit to 1 will enable framing search engine to declare sync while there is one and only one candidate left.
3	FASTSYNC	R/W	1	**Faster Sync Algorithm** Setting this bit to 1 will enable framing search engine to declare SYNC condition earlier.
2 1 0	FS[2] FS[1] FS[0]	R/W R/W R/W	0 0 0	**Framing Select bit 2** **Framing Select bit 1** **Framing Select bit 0** These three bits select the DS1 framing mode. Bit 2 is MSB and Bit 0 is LSB. ***NOTE:*** *Changing framing format will cause a RESYNC to be generated automatically.*

Framing	FS[2]	FS[1]	FS[0]
ESF	0	X	X
SF	1	0	1
N	1	1	0
T1DM	1	1	1
SLC®96	1	0	0

TABLE 17: ALARM GENERATION REGISTER - E1 MODE

REGISTER 8 -E1 MODE **ALARM GENERATION REGISTER (AGR)** **HEX ADDRESS: 0XN108**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	AUXPG	RO	0	**AUXP Generation** Enables the generation of AUXP pattern which is an unframed 1010…. pattern. 0 = AUXP is disabled. 1 = AUXP is enabled.
6	LOF	R/W	0	**Loss of Frame Declaration Criteria** This Read/Write bit-field is used to select the LOF or Red Alarm generation criteria the Receive E1 Framer block will employ. 0 = Receive E1 Framer declares Red Alarm unless both FAS and multi-frame alignment are achieved. 1 = Prevents Receive E1 Framer from declaring Red Alarm condition; FAS Alignment is maintained.
5	YEL(1)	R/W	0	**Yellow Alarm and Multiframe Yellow Alarm Generation** These bits activate and deactivate the transmission of a yellow alarm. The Yellow alarm and multiframe Yellow alarm data pattern can be injected either automatically upon detection of the loss of alignment or controlled by YEL bits. Setting thess bits to b01 will enable automatic yellow alarm transmission in response to a loss of frame alignment (FAS red alarm) and multiframe yellow alarm is transmitted in response to a loss of multiframe alignment (CAS red alarm). The decoding of these bits are explained as follows: 00 = Disable the transmission of yellow alarm. 01 = Enable automatical yellow alarm generation. 1. The yellow alarm bits (bit 3 of non-FAS frames in TS0) is transmitted by echoing the receive FAS alignment status. Logic one is transmitted if loss of FAS alignment occured. 2. The multiframe yellow alarm bits (bit 6 of frame 0 in TS16) is transmitted by echoing the receive CAS multiframe alignment status. Logic one is transmitted if loss of CAS multiframe alignment occured. 10 = Yellow and multiframe yellow alarms are transmitted as 0. 11 = Yellow and multiframe yellow alarms are transmitted as 1.
4	YEL(0)	R/W	0	
3	AISG(1)	R/W	0	**AIS Generation Select** These Read/Write bit-fields are used to configure the channel to generate and transmit an AIS pattern, as described below. 00 = No AIS Alarm generated 01 = Enable unframed AIS alarm generation 10 = Enable AIS16 generation 11 = Enable framed AIS alarm generation
2	AISG(0)	R/W	0	
1	AISD(1)	R/W	0	**AIS Pattern Detection Select** These Read/Write bit-fields are used to specify the type of AIS pattern that the receive E1 framer block will detect as described below. 00 = AIS alarm detection is disabled. 01 = Enable unframed AIS alarm detection. 10 = Enable AIS 16 detection. 11 = Enable framed AIS alarm detection.
0	AISD(0)	R/W	0	

TABLE 18: ALARM GENERATION REGISTER -T1 MODE

REGISTER 8 - T1 MODE **ALARM GENERATION REGISTER (AGR)** **HEX ADDRESS: 0XN108**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	**Reserved**
6	LOF	R/W	0	**Loss of Frame Declaration Criteria** A Red Alarm is generated by the receiver to indicate the loss of frame (LOF) alignment. A Yellow Alarm is then returned to the remote transmitter to report that the receiver detects LOF. Setting this bit will set the criteria for preventing red alarm from generation as long as the frame is aligned. Otherwise, the frame and multiframe must be both aligned in order to keep red alarm from happening.
5	YEL(1)	R/W	0	**Yellow Alarm and Multiframe Yellow Alarm Generation** These bits activate and deactivate the transmission of a yellow alarm. The decoding of these bits are explained as follows: 00, = Disable the transmission of yellow alarm. 01 = In SF mode (or N mode), yellow alarm is transmitted as bit 2 = 0 (second MSB) in all DS0 data channel. In T1DM mode, yellow is transmitted to the remote terminal by setting the outgoing Y-bit to zero. In ESF mode, follow the following scenario: 1. If YEL[0] forms a pulse width shorter or equal to the time required to transmit 255 pattern of 1111_1111_0000_0000 (eight ones followed by eight zeros) on the 4-kbit/s data link (M1-M12), the alarm is transmitted for 255 patterns. 2. If YEL[0] is a pulse width longer than the time required to transmit 255 patterns, the alarm continues until TYEL[0] goes low. 3. A second YEL[0] pulse during an alarm transmission resets the pattern counter and extends the alarm duration for another 255 patterns. 10 = In SF mode, yellow alarm is transmitted as a "1" for the Fs bit of frame 12, this is yellow alarm for J1 standard. In T1DM mode, yellow is transmitted to the remote terminal by setting the outgoing Y-bit to zero. In ESF mode, yellow alarm is controlled by the duration of YEL[1]. This allows continuous alarms of any length. 11 = Disable the transmission of yellow alarm.
4	YEL(0)	R/W	0	
3	AISG(1)	R/W	0	**AIS Generation Select** These Read/Write bit-fields are used to configure the channel to generate and transmit an AIS pattern, as described below. 00 = No AIS Alarm generated 01 = Enable unframed AIS alarm generation 10 = No AIS Alarm generated 11 = Enable framed AIS alarm generation
2	AISG(0)	R/W	0	
1	AISD(1)	R/W	0	**AIS Pattern Detection Select** These Read/Write bit-fields are used to specify the type of AIS pattern that the receive E1 framer block will detect as described below. 00 = Disabled 01 = Unframed AIS alarm detection 10 = AIS16 detection 11 = Unframed AIS alarm detection
0	AISD(0)	R/W	0	

TABLE 19: SYNCHRONIZATION MUX REGISTER - E1 MODE

REGISTER 9 - E1 MODE **SYNCHRONIZATION MUX REGISTER (SMR)** **HEX ADDRESS: 0XN109**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	ESRC[1:0]	R/W	0	**Source for E bits** These bits determine where the E bits should be inserted from. 00 = Transparent, inserted from the status of receiver. 01 = 0. 10 = 1. 11 = Data link.
5	Reserved	-	-	**Reserved**
4	SYNC INV	R/W	0	**Sync Inversion Select** Selects the direction of the transmit sync and multisync signals. 0 = Syncs are input if the CSS(1:0) bits of CSR equal 01 (TxSerClk input is selected as the timing reference for the Transmit section of the framer); otherwise syncs are outputs 1 = Syncs are output if CSS(1:0) bits of CSR equal 01 (TxSerClk input is selected as the timing reference for the Transmit section of the framer); otherwise syncs are inputs
3	DLSRC(1)	R/W	0	**Data Link Source Select** Specifies the source of the Data Link bits that will be inserted in the outbound E1 frames. 00 = TxSer_n Input: Transmit Payload data Input port will be source of Data Link bits. 01 = TX HDLC Controller: Transmit HDLC Controller will generate either BOS (Bit Oriented Signaling) or MOS (Message Oriented Signaling) messages which will be inserted into the Data Link bit-fields in the outbound E1 frames. 10 = TxOH_n Input: Transmit Overhead data Input Port will be the source of the Data Link bits. 11 = TxSer_n Input: Transmit Payload data Input port will be the source of the Data Link Bits.
2	DLSRC(0)	R/W	0	
1	CRCSRC	R/W	0	**CRC-4 Bits Source Select** This Read/Write bit-field is used to configure the transmit section of the channel to use either internal generation or the TxSER_n input pin as the source of the CRC-4 bits inserted into the outbound frames. 0 = Internally Generated and inserted into E1 data stream internally. 1 = Tx_Ser_n Input: Transmit Payload data Input port will be source of CRC-4 bits. ***NOTE:*** *This bit-field is ignored if CRC Multiframe Alignment is disabled*
0	FSRC	R/W	0	**Framing Alignment Bits Source Select** Specifies source of the Framing Alignment bits, which include FAS alignment bits, multiframe alignment bits, E and A bits. 0 = Internally generated and inserted into the outbound E1 frames. 1 = TxSer_n Input: Transmit Serial Input port will be source of the FAS bits, CRC Multiframe Alignments and the E and A bits.

TABLE 20: SYNCHRONIZATION MUX REGISTER - T1 MODE

REGISTER 9 - T1 MODE **SYNCHRONIZATION MUX REGISTER (SMR)** **HEX ADDRESS: 0XN109**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	**Reserved**
6	MFRAMEALIGN	R/W	0	**Multirame Alignment** This bit forces transmit frame counter aligns with the backplance multiframe sync. 0 = The multiframe alignment is not enforced from backplance interface. 1 = The transmit multiframe is aligned with the incoming backplance multiframe timing.
5	MSYNC	R/W	O	**Tx Super Frame Sync** This bit selects the transmit input sync signal from either the frame sync or superframe sync signals. 0 = Sync input (TxSync) is a frame sync. In 1.544MHz clock mode, TxMSync is used, in other clock mode, TxMsync is an input transmit clock. 1 = Sync input is a superframe sync.
4	SYNC INV	R/W	0	**Sync Inversion Select** This bit changes the direction of transmit sync and multi-sync signals. 0 = The syncs are inputs if CSS bits of CSR equal to 1, otherwise, syncs are outputs. 1 = The syncs are outputs if CSS bits of CSR equal to 1, otherwise, syncs are inputs.
3 - 2	Reserved	-	-	**Reserved**
1	CRCSRC	R/W	0	**CRC-6 Bits Source Select** This bit determines where the CRC-6 bits should be inserted from. 0 = The CRC-6 bits are generated and inserted internally. 1 = The CRC-6 bits are passed through from the input serial data only when IOMUX=0 and CSS < 3. ***NOTE:*** *This bit-field is ignored if CRC Multiframe Alignment is disabled*
0	FSRC	R/W	0	**Framing Alignment Bits Source Select** Determines where the framing alignment bits should be inserted from. 0 = The framing alignment bits are inserted internally. 1 = The framing alignment bits are passed through from the input serial data only when IOMUX=0 and CSS < 3.

TABLE 21: TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER - E1 MODE

REGISTER 10 - E1 MODE TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) HEX ADDRESS:0XN10A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSa8ENB	R/W	0	Specifies if the Sa8 bit-field (bit 7 within timeslot 0 of non-FAS frames) will be involved in the transport of Data Link Information 0 = Data Link Interface does not use Sa8 bit-field. Sa8 bit-field within each outbound non-FAS frame will be set to 1. 1 = Data Link Interface uses Sa8 bit-field. ***NOTE:*** *This bit-field is only active when the TxSIGDL[2:0] bits within this register are set to 00x. This bit-field is ignored in all other case.*
6	TxSa7ENB	R/W	0	Specifies if the Sa7 bit-field (bit 6 within timeslot 0 of non-FAS frames) will be involved in the transport of Data Link Information 0 = Data Link Interface does not use Sa7 bit-field. Sa7 bit-field within each outbound non-FAS frame will be set to 1. 1 = Data Link Interface uses Sa7 bit-field. ***NOTE:*** *This bit-field is only active when the TxSIGDL[2:0] bits within this register are set to 00x. This bit-field is ignored in all other cases.*
5	TxSa6ENB	R/W	0	Specifies if the Sa6 bit-field (bit 5 within timeslot 0 of non-FAS frames) will be involved in the transport of Data Link Information 0 = Data Link Interface does not use Sa6 bit-field. Sa6 bit-field within each outbound non-FAS frame will be set to 1. 1 = Data Link Interface uses Sa6 bit-field. ***NOTE:*** *This bit-field is only active when the TxSIGDL[2:0] bits within this register are set to 00x. This bit-field is ignored in all other case.*
4	TxSa5ENB	R/W	0	Specifies if the Sa5 bit-field (bit 4 within timeslot 0 of non-FAS frames) will be involved in the transport of Data Link Information 0 = Data Link Interface does not use Sa5 bit-field. Sa5 bit-field within each outbound non-FAS frame will be set to 1. 1 = Data Link Interface uses Sa5 bit-field. ***NOTE:*** *This bit-field is only active when the TxSIGDL[2:0] bits within this register are set to 00x. This bit-field is ignored in all other case.*
3	TxSa4ENB	R/W	0	Specifies if the Sa4 bit-field (bit 3 within timeslot 0 of non-FAS frames) will be involved in the transport of Data Link Information 0 = Data Link Interface does not use Sa4 bit-field. Sa4 bit-field within each outbound non-FAS frame will be set to 1. 1 = Data Link Interface uses Sa4 bit-field. ***NOTE:*** *This bit-field is only active when the TxSIGDL[2:0] bits within this register are set to 00x. This bit-field is ignored in all other case.*

TABLE 21: TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER - E1 MODE

REGISTER 10 - E1 MODE TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) HEX ADDRESS:0XN10A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	TxSIGDL(2)	R/W	0	These three Read/Write bits are used to specify the type of data that is to be transported via National Bits in timeslot 0 of the non-FAS frames and in Timeslot 16 in the outbound frames. The relationship between these bit fields and the role/function of the National and Timeslot 16 bits are presented below. *National Bits (Sa4-8)* 000 = Data Link Data inserted into National bits 001 = Data Link Data inserted into National bits 010 = National bits forced to 1, not used to carry data link data 011 = None (forced to 1) 1xx = None (forced to 1) *Timeslot 16* 000:PCM Data. Timeslot 16 data taken directly from PCM data input, could include signaling 001 = CAS Signaling bits A,B,C,D 010 = PCM Data. Timeslot 16 data taken directly from PCM data input, could include signaling 011 = CAS Signaling bits A,B,C,D 1xx = HDLC Data Link. Common Channel Signaling enabled and timeslot 16 is taken from the Transmit HDLC Controller.
1	TxSIGDL(1)	R/W	0	
0	TxSIGDL(0)	R/W	0	

TABLE 22: TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER - T1 MODE

REGISTER 10 - T1 MODE TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) HEX ADDRESS:0XN10A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	**Reserved**
6	Reserved	-	-	**Reserved**
5	TxDLBW[1]	R/W R/W	0 0	**Data Link Bandwidth** 00 = FDL is a 4kHz data link channel 01 = FDL is a 2kHz data link channel caarried by odd framing bits (1,5,9....) 10 = FDL is a 2kHz data link channel carried by even framing bits(3,7,11...)
4	TxDLBW[0]	R/W	0	
3	TxDE[1]	R/W	0	**DE Select** 00 = Data (Serial Input). The D/E time slots are inserted from the serial data input. 01 = LAPD Controller. The D/E time slots are inserted from the LAPD controller. 10 = Data (Serial Input). The D/E time slots are inserted from the serial data input. 11 = Fractional Input. The D/E time slots are inserted from the fractional input.
2	TxDE[0]	R/W	0	
1	TxDL[1]	R/W	0	**DL Select** 00 = LAPD Controlller/SLC96 Buffer. The data link bits are inserted from the LAPD controller. (LAPD1 is the only controller that can be used to transport LAPD messages through the data link bits) 01 = Serial Input. The data link bits are inserted from serial data input. 10 = Overhead Input. The data link bits are inserted from overhead input. 11 = None (forced to 1). The data link bits are forced to 1.
0	TxDL01]	R/W	0	

TABLE 23: FRAMING CONTROL REGISTER E1 MODE

REGISTER 11 -- E1 MODE **FRAMING CONTROL REGISTER (FCR)** **HEX ADDRESS: 0XN10B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSYNC	R/W	0	**Force Re-Synchronization** A 0 to 1 transition in this bit-field forces the Receive E1 Framer to restart the synchronization process. This bit field is automatically cleared (set to 0) after frame synchronization is reached.
6	CASC(1)	R/W	0	**Loss of CAS Multiframe Alignment Criteria Select** These two Read/Write bits are used to select the Loss of CAS Multi-frame Alignment Declaration criteria. The relationship between the state of these two bit fields and the corresponding Loss of CAS Multi-Frame is presented below. 00 = Two consecutive CAS Multi-Frames with Multiframe Alignment Signal (MAS) errors 01 = Three consecutive CAS Multi-Frames with MAS errors 10 = Four consecutive CAS Multi-Frames with MAS errors 11 = Eight consecutive CAS Multi-Frames with MAS errors ***NOTE:*** *These bits are only active if Channel Associated Signaling is used.*
5	CASC(0)	R/W	0	
4	CRCC(1)	R/W	0	**Loss of CRC-4 Multiframe Alignment Criteria Select** Selects criteria for Loss of CRC-4 Multiframe Alignment. 00 = Four consecutive CRC Multiframe Alignment signals have been received in error 01 = Two consecutive CRC Multiframe Alignment signals have been received in error 10 = Eight consecutive CRC Multiframe Alignment signals have been received in error 11 = 915 or more CRC-4 errors have been detected in one second. ***NOTE:*** *These bit-fields are ignored if CRC Multiframe Alignment has been disabled.*
3	CRCC(0)	R/W	0	
2	FASC(2)	R/W	0	**Loss of FAS Alignment Criteria Select** These three Read/Write bits are used to select Loss of FAS Frame Declaration criteria. The relationship between the state of these bits and the corresponding Loss of FAS Frame declaration is presented below. 000 = Illegal - do not use 001 = 1 errored FAS pattern 010 = 2 consecutive errored FAS patterns 011 = 3 consecutive errored FAS patterns 100 = 4 consecutive errored FAS patterns 101 = 5 consecutive errored FAS patterns 110 = 6 consecutive errored FAS patterns 111 = 7 consecutive errored FAS patterns
1	FASC(1)	R/W	1	
0	FASC(0)	R/W	1	

TABLE 24: FRAMING CONTROL REGISTER T1 MODE

REGISTER 11 -- T1 MODE **FRAMING CONTROL REGISTER (FCR)** **HEX ADDRESS: 0XN10B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSYNC	R/W	0	**Force Re-Synchronization** A 0 to 1 transition in this bit-field forces the Receive DS1 Framer to restart the synchronization process. This bit field is automatically cleared (set to 0) after frame synchronization is reached.
6	CRCENB/ ONEONLY	R/W	0	**Sync with CRC verification in ESF.** (Assuming only one Ft sync candidate exists.) 0 = No CRC match test 1 = Include CRC match test as part of Synchronization criteria.
5	TOLR[2]	R/W	0	**Tolerance Bits [2:0]** The Tolerance (TOLR) and Range (RANG) form the criteria for loss of frame alignment. A loss of frame is declared if there is "TOLR out of RANG" errors in the framing pattern. The recommended TOLR value is 2. ***NOTE:*** *A "0" value for TOLR is internally blocked. A TOLR value must be specified.*
4	TOLR[1]	R/W	1	
3	TOLR[0]	R/W	0	
2	RANG[2]	R/W	1	**Range Bits [2:0]** The Tolerance (TOLR) and Range (RANG) form the criteria for loss of frame alignment. A loss of frame is declared if there is "TOLR out of RANG" errors in the framing pattern. The recommended RANG value is 5. ***NOTE:*** *A "0" value for RANG is internally blocked. A RANG value must be specified.*
1	RANG[1]	R/W	0	
0	RANG[0]	R/W	1	

TABLE 25: RECEIVE SIGNALING & DATA LINK SELECT REGISTER - E1 MODE

REGISTER 12 - E1 MODE RECEIVE SIGNALING & DATA LINK SELECT REGISTER (RS&DLSR) HEX ADDRESS: 0XN10C

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RxSa8ENB	R/W	0	This Read/Write bit is used to specify whether or not data link information will be transported via National Bit Sa8 (bit 7 within timeslot 0 of non-FAS frames) 0 = Sa8 does not carry data link information 1 = Sa8 carries data link information ***NOTE:*** *This bit-field is valid only if the RxSIGDL[2:0] = "000" or "001". (The National bits have been configured to carry data link bits).*
6	RxSa7ENB	R/w	0	This Read/Write bit is used to specify whether or not data link information will be transported via National Bit Sa7 (bit 6 within timeslot 0 of non-FAS frames) 0 = Sa7 does not carry data link information 1 = Sa7 carries data link information ***NOTE:*** *This bit-field is valid only if the RxSIGDL[2:0] = "000" or "001". (The National bits have been configured to carry data link bits).*
5	RxSa6ENB	R/W	0	This Read/Write bit is used to specify whether or not data link information will be transported via National Bit Sa6 (bit 5 within timeslot 0 of non-FAS frames) 0 = Sa6 does not carry data Link information 1 = Sa6 carries data link information ***NOTE:*** *This bit-field is valid only if the RxSIGDL[2:0] = "000" or "001". (The National bits have been configured to carry data link bits).*
4	RxSa5ENB	R/W	0	This Read/Write bit is used to specify whether or not data link information will be transported via National Bit Sa5 (bit 4 within timeslot 0 of non-FAS frames) 0 = Sa5 does not carry data link information 1 = Sa5 carries data link information ***NOTE:*** *This bit-field is valid only if the RxSIGDL[2:0] = "000" or "001". (The National bits have been configured to carry data link bits).*
3	RxSa4ENB	R/W	0	This Read/Write bit is used to specify whether or not data link information will be transported via National Bit Sa4 (bit 3 within timeslot 0 of non-FAS frames) 0 = Sa4 does not carry data link information 1 = Sa4 carries data link information ***NOTE:*** *This bit-field is valid only if the RxSIGDL[2:0] = "000" or "001". (If the National bits have been configured to carry data link bits).*
2	RxSIGDL(2)	R/W	0	These three Read/Write bits are used to configure the receive section of the channels on how to interpret the National and Timeslot 16 Bits. Specifies how signaling and data link information is received via the E1 Frames. *National Bits (Sa4-8)* 000 = Data link data extracted from National bits 001 = Data link data extracted from National bits 010 = Data link data is not extracted from National bits 011 = Data link data is not extracted from National bits 1xx = Data link data is not extracted from National bits *Timeslot 16 Bits* 000 = PCM Data. 001 = CAS Signal A,B,C,D 010 = PCM Data. 011 = CAS Signal A,B,C,D 1xx = Data Link (CCS). Timeslot 16 data is extracted by the Receive HDLC controller
1	RxSIGDL(1)	R/W	0	
0	RxSIGDL(0)	R/W	0	

TABLE 26: RECEIVE SIGNALING & DATA LINK SELECT REGISTER (RS&DLSR) T1 MODE

REGISTER 12 - T1 MODE RECEIVE SIGNALING & DATA LINK SELECT REGISTER (RS&DLSR) HEX ADDRESS: 0XN10C

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	**Reserved**
6	Reserved	-	-	**Reserved**
5	RxDLBW[1]	R/W	0	**Data Link Bandwidth** 00 = FDL is a 4kHz data link channel. 01 = FDL is a 2kHz data link channel carried by old framing bits(1,5,9,....). 10 = FDL is a 2kHz data link channel carried by even framing bits(3,7,11,....).
4	RxDLBW[0]	R/w	0	
3	RxDE[1]	R/W	0	**DE Select** 00 = Serial output only. The D/E time slots are sent to serial data output. 01 = LAPD controller. The D/E time slots are fed into LAPD controller. 10 = Data (fractional output). The D/E time slots are sent to serial fractional data output. 11 = Overhead output. The D/E time slots are sent to overhead output.
2	RxDE[0]	R/W	0	
1	RxDL[1]	R/W	0	**DL Select (ESF,T1DM,SLC96, N Fs bits)** 00 =LAPD controller and Serial output. The data link bits are fed into the LAPD controller and also serial data output. (LAPD1 is the only controller that can be used to receive LAPD messages through the data link bits) 01 = Serial output only. The data link bits are sent to serial data output. 10 = Overhead output and Serial output. The data link bits are sent to overhead output and also serial data output. 11 = None (forced to 1). The data link bits are forced to 1.
0	RxDL[0]	R/W	0	

TABLE 27: SIGNALING CHANGE REGISTER 0 - T1 MODE

REGISTER 13 - T1 MODE SIGNALING CHANGE REGISTER 0 (SCR 0) HEX ADDRESS: 0XN10D

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch. 0	RUR	0	These Reset Upon Read bits indicate whether the signaling data associated with Channels 0-7 has changed since the last read of this register. 0 = Signaling data has not changed since last read of register 1 = Signaling data has changed since last read of register ***NOTE:*** *This register is only relevant if the Framing Channel is using Channel Associated Signaling*
6	Ch. 1	RUR	0	
5	Ch.2	RUR	0	
4	Ch.3	RUR	0	
3	Ch.4	RUR	0	
2	Ch.5	RUR	0	
1	Ch.6	RUR	0	
0	Ch.7	RUR	0	

TABLE 28: SIGNALING CHANGE REGISTER 0 - E1 MODE

REGISTER 13 - E1 MODE **SIGNALING CHANGE REGISTER 0 (SCR 0)** **HEX ADDRESS: 0XN10D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	N/A	RO	0	These Reset Upon Read bits indicate whether the signaling data associated with Channels 1-7 has changed since the last read of this register. 0 = Signaling data has not changed since last read of register 1 = Signaling data has changed since last read of register ***NOTE:*** *This register is only relevant if the Framing Channel is using Channel Associated Signaling*
6	Ch. 1	RUR	0	
5	Ch.2	RUR	0	
4	Ch.3	RUR	0	
3	Ch.4	RUR	0	
2	Ch.5	RUR	0	
1	Ch.6	RUR	0	
0	Ch.7	RUR	0	

TABLE 29: SIGNALING CHANGE REGISTER 1

REGISTER 14 **SIGNALING CHANGE REGISTER 1 (SCR 1)** **HEX ADDRESS: 0XN10E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch.8	RUR	0	These Reset Upon Read bits indicate whether the signaling data associated with Channels 8-15 has changed since the last read of this register. 0 = Signaling data has not changed since last read of register 1 = Signaling data has changed since last read of register ***NOTE:*** *This register is only relevant if the Framing Channel is using Channel Associated Signaling*
6	Ch.9	RUR	0	
5	Ch.10	RUR	0	
4	Ch.11	RUR	0	
3	Ch.12	RUR	0	
2	Ch.13	RUR	0	
1	Ch.14	RUR	0	
0	Ch.15	RUR	0	

TABLE 30: SIGNALING CHANGE REGISTER 2

REGISTER 15 **SIGNALING CHANGE REGISTER 2 (SCR 2)** **HEX ADDRESS: 0XN10F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch.16	RUR	0	These Reset Upon Read bits indicate whether the signaling data associated with Channels 16-23 has changed since the last read of this register. 0 = Signaling data has not changed since last read of register 1 = Signaling data has changed since last read of register ***NOTE:*** *This register is only relevant if the Framing Channel is using Channel Associated Signaling*
6	Ch.17	RUR	0	
5	Ch.18	RUR	0	
4	Ch.19	RUR	0	
3	Ch.20	RUR	0	
2	Ch.21	RUR	0	
1	Ch.22	RUR	0	
0	Ch.23	RUR	0	

TABLE 31: SIGNALING CHANGE REGISTER 3

REGISTER 16 - E1 ONLY **SIGNALING CHANGE REGISTER 3 (SCR 3)** **HEX ADDRESS: 0XN110**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch.24	RUR	0	These Reset Upon Read bits indicate whether the signaling data associated with Channels 24-31 has changed since the last read of this register. 0 = Signaling data has not changed since last read of register 1 = Signaling data has changed since last read of register ***NOTE:*** *This register is only relevant if the Framing Channel is using Channel Associated Signaling*
6	Ch.25	RUR	0	
5	Ch.26	RUR	0	
4	Ch.27	RUR	0	
3	Ch.28	RUR	0	
2	Ch.29	RUR	0	
1	Ch.30	RUR	0	
0	Ch.31	RUR	0	

TABLE 32: RECEIVE NATIONAL BITS REGISTER

REGISTER 17 **RECEIVE NATIONAL BITS REGISTER (RNBR)** **HEX ADDRESS: 0XN111**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Si_FAS	RO	x	**Received International Bit - FAS Frame** This Read Only bit-field contains the value of the International Bit in the most recently received FAS frame
6	Si_nonFAS	RO	x	**Received International Bit - Non FAS Frame** This Read Only bit-field contains the value of the International Bit in the most recently received non-FAS frame
5	R_ALARM	RO	x	**Received FAS Yellow Alarm** This Read Only bit-field contains the value in the Remote Alarm bit-field (frame Yellow Alarm) within the non-FAS frame.
4	Sa4	RO	x	**Received National Bits** These Read Only bit-fields contain the values of the National bits within the most recently received non-FAS frame.
3	Sa5	RO	x	
2	Sa6	RO	x	
1	Sa7	RO	x	
0	Sa8	RO	x	

TABLE 33: RECEIVE EXTRA BITS REGISTER

REGISTER 18 **RECEIVE EXTRA BITS REGISTER (REBR)** **HEX ADDRESS: 0XN112**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Reserved	-	-	**Reserved**
3	EX1	RO	x	**Extra Bit 1** Corresponds to value in bit 5 within timeslot 16 of frame 0 of the signaling multi-frame
2	ALARMFE	RO	x	**CAS Multi-Frame Yellow Alarm** Corresponds to value in bit 6(CAS Multiframe Yellow Alarm) within timeslot 16 of frame 0 of the signaling multiframe. 0 = Remote E1 transmitting terminal is not sending CAS Multiframe Yellow Alarm 1 = Remote E1 transmitting terminal is sending CAS Multiframe Yellow Alarm
1	EX2	RO	x	**Extra Bit 2** Corresponds to value in Bit 7 within timeslot 16 of frame 0 of the signaling multi-frame
0	EX3	RO	x	**Extra Bit 3** Corresponds to value in Bit 8 within timeslot 16 of frame 0 of the signaling multi-frame

NOTE: *The value of the bit-fields within this register only have meaning if the framer is using Channel Associated Signaling.*

TABLE 34: DATA LINK CONTROL REGISTER

REGISTER 19 **DATA LINK CONTROL REGISTER 1 (DLCR1)** **HEX ADDRESS: 0XN113**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SLC-96	R/W	0	**SLC®96 Enable, 6 bit for ESF** If SLC®96 framing is selected, setting this bit high will enable SLC®96 data link transmission; Otherwise, the regular SF framing bits are transmitted. In ESF framing mode, setting this bit high will cause facility data link to transmit/receive SLC®96-like message.
6	MOSA	R/W	0	**MOS Abort Enable/Disable Select** This Read/Write bit-field is used to configure the transmit HDLC1 controller to automatically transmit an abort sequence anytime it transitions from the MOS mode to the BOS mode. 0 = Transmit HDLC1 Controller inserts an MOS abort sequence if the MOS message is interrupted 1 = Prevents Transmit HDLC1 Controller from inserting an MOS abort sequence.
5	Rx_FCS_DIS	R/W	0	**Receive FCS Verification Disable** Enables/Disables Receive HDLC1 Controller's computation and verification of the FCS value in the incoming LAPD message frame 0 = Verifies FCS value of each MOS frame. 1 = Does not verify FCS value of each MOS frame.
4	AutoRx	R/W	0	**Auto Receive LAPD Message** Configures the Rx HDLC1 Controller to discard any incoming LAPD Message frame that exactly match which is currently stored in the Rx HDLC1 buffer. 0 = Disabled 1 = Enables this feature.
3	Tx_ABORT	R/W	0	**Transmit ABORT** Configures the Tx HDLC1 Controller to transmit an ABORT sequence (string of 7 or more consecutive 1's) to the Remote terminal. 0 = Tx HDLC1 Controller operates normally 1 = Tx HDLC1 Controller inserts an ABORT sequence into the data link channel.
2	Tx_IDLE	R/W	0	**Transmit Idle (Flag Sequence Byte)** Configures the Tx HDLC1 controller to transmit a string of Flag Sequence octets (0X7E) in the data link channel to the Remote terminal. 0 = Tx HDLC1 Controller resumes transmitting data to the Remote terminal 1 = Tx HDLC1 Controller transmits a string of Flag Sequence bytes. ***NOTE:*** *This bit-field is ignored if the Tx HDLC1 controller is operating in the BOS Mode - bit-field 0(MOS/BOS) within this register is set to 0.*
1	Tx_FCS_EN	R/W	0	**Transmit LAPD Message with FCS** Configure HDLC1 Controller to include/not include FCS octets in the outbound LAPD message frames. 0 = Does not include FCS octets into the outbound LAPD message frame. 1 = Inserts FCS octets into the outbound LAPD message frame. ***NOTE:*** *This bit-field is ignored if the transmit HDLC1 controller has been configured to operate in the BOS mode.*
0	MOS/$\overline{\text{BOS}}$	R/W	0	**Message Oriented Signaling/Bit Oriented Signaling Select** Specifies whether the TxRx HDLC1 Controller will be transmitting and receiving LAPD message frames (MOS) or Bit Oriented Signal (BOS) messages. 0 = Tx/Rx HDLC1 Controller transmits and receives BOS messages. 1 = Tx/Rx HDLC1 Controller transmits and receives MOS messages.

TABLE 35: TRANSMIT DATA LINK BYTE COUNT REGISTER

REGISTER 20 **TRANSMIT DATA LINK BYTE COUNT REGISTER 1 (TDLBCR1)** **HEX ADDRESS: 0XN114**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	BUFAVAL//BUFSEL	R/W	0	**Transmit HDLC1 Buffer Available/Buffer Select** Specifies which of the two Tx HDLC1 Buffers that the Tx HDLC1 controller should read from to generate the next outbound HDLC1 message. 0 = transmits message data residing in Tx HDLC1 Buffer 0. 1 = transmits message data residing in Tx HDLC1 buffer 1. ***NOTE:*** *If one of these Tx HDLC1 buffers contain a message which has yet to be completely read-in and processed for transmission by the Tx HDLC1 controller, then this bit-field will automatically reflect the value corresponding to the available buffer. Changing this bit-field to the in-use buffer is not permitted.*
6	TDLBC6	R/W	0	**Transmit HDLC1 Message - Byte Count** Depends on whether an MOS or BOS message is being transmitted to the Remote Terminal Equipment ***If BOS message is being transmitted*:** These bit fields contain the number of repetitions the BOS message must be transmitted before the Tx HDLC1 controller generates the TxEOT interrupt and halts transmission. If these fields are set to 00000000, then the BOS message will be transmitted for an indefinite number of times. ***If MOS message is being transmitted:*** These bit fields contain the length, in number of octets, of the message to be transmitted.
5	TDLBC5	R/W	0	
4	TDLBC4	R/W	0	
3	TDLBC3	R/W	0	
2	TDLBC2	R/W	0	
1	TDLBC1	R/W	0	
0	TDLBC0	R/W	0	

TABLE 36: RECEIVE DATA LINK BYTE COUNT REGISTER

REGISTER 21 **RECEIVE DATA LINK BYTE COUNT REGISTER 1 (RDLBCR1)** **HEX ADDRESS: 0XN115**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RBUFPTR	R/W	0	**Receive HDLC1 Buffer-Pointer** Identifies which RxHDLC1 buffer contains the newly received HDLC1 message. 0 = HDLC1 message is stored in Rx HDLC1 Buffer 0. 1 = HDLC1 message is stored in Rx HDLC1 Buffer 1.
6	RDLBC6	R/W	0	**Receive HDLC Message - byte count** **In MOS Mode** These seven bit-fields contain the size in bytes of the HDLC1 message that has been extracted and written into the Rx HDLC1 buffer. In BOS Mode These bits should be set to the value of the message repetitions before each receive interrupt. If ithey are set to “0”, no RxEOT interrupt will be generated.
5	RDLBC5	R/W	0	
4	RDLBC4	R/W	0	
3	RDLBC3	R/W	0	
2	RDLBC2	R/W	0	
1	RDLBC1	R/W	0	
0	RDLBC0	R/W	0	

TABLE 37: SLIP BUFFER CONTROL REGISTER

REGISTER 22 **SLIP BUFFER CONTROL REGISTER (SBCR)** **HEX ADDRESS: 0XN116**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSB_ISFIFO	R/W	0	Selects slip buffer as a FIFO for all clock modes while TxClk and TxSerClk are synced. 0 = Buffer acts as slip buffer if enabled. 1 = Buffer acts as a FIFO. The data latency is dictated by FIFO Latency.
6-5	Reserved	-	-	**Reserved**
4	SB_FORCESF	R/W	0	**Force Signaling Freeze** Setting this bit "High" stops further signal updating until this bit is cleared. 1 = Signaling array is not updated. 0 = Signaling array is updated only if SB_ENB[1:0] = 01 or 10
3	SB_SFENB	R/W	0	**Signal Freeze Enable** This bit enables signaling freeze for one multiframe after buffer slipping. 1 = Signaling freeze is enabled. 0 = Signaling freeze is disabled.
2	SB_SDIR	R/W	1	**Slip Buffer (RxSync) Direction Selec**t Allows RxSync output pin to be an input or an output. 0 = RxSync is an output pin 1 = RxSync is an input pin
1	SB_ENB(1)	R/w	0	**Slip Buffer Mode Select** Selects mode of operation of slip buffer. 00 = Buffer is bypassed and RxSync and RxSERClk are outputs. 01 = Elastic store slip buffer enabled. RxSERClk is an input. 10 = Buffer acts as FIFO Data latency dictated by the setting within the FIFO Latency Register. RxSERClk is an input. 11 = Buffer is bypassed. RxSync and RxSERClk are outputs.
0	SB_ENB(0)	R/W	0	

TABLE 38: FIFO LATENCY REGISTER

REGISTER 23 **FIFO LATENCY REGISTER (FFOLR)** **HEX ADDRESS: 0XN117**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-5	Reserved	-	-	**Reserved**
4-0	Latency	R/W	0	Sets the distance between slip buffer read and slip buffer write pointers in FIFO mode.

TABLE 39: DMA 0 (WRITE) CONFIGURATION REGISTER

REGISTER 24 **DMA 0 WRITE CONFIGURATION REGISTER (D 0 WCR)** **HEX ADDRESS: 0XN118**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	DMA0 RST	R/W	0	**DMA_0 Reset** Resets transmit DMA 0 channel. 0 = Normal operation. 1 = A zero to one transition resets DMA channel_0.
6	DMA0 ENB	R/W	0	**DMA_0 Enable** Enables DMA_0 interface. 0 = Disables DMA_0 interface 1 = Enables DMA_0 interface
5	WR TYPE	R/W	0	**Write Type Select** $\overline{\text{\_\_\_}}$ Selects function of $\overline{\text{WR}}$ signal. 0 = $\overline{\text{WR}}$ functions as direction signal (indicates whether the current bus cycle is a read or write operation) and $\overline{\text{RD}}$ functions as a data strobe signal. 1 = $\overline{\text{WR}}$ functions as a write strobe signal and $\overline{\text{RD}}$ functions as configured in the DMA 1 configuration register.
4 - 3	Reserved	-	-	**Reserved**
2	DMA0_CHAN(2)	R/W	0	**Channel Select** Selects which channel, within the chip, is to use the DMA_0 (Write) interface. 000 = Channel 0 001 = Channel 1 001 = Channel 2 011 = Channel 3 100 = Channel 4 101 = Channel 5 110 = Channel 6 111 = Channel 7
1	DMA0_CHAN(1)	R/W	0	
0	DMA0_CHAN(0)	R/W	0	

TABLE 40: DMA 1 (READ) CONFIGURATION REGISTER

REGISTER 25 **DMA 1 (READ) CONFIGURATION REGISTER (D1CR)** **HEX ADDRESS: 0XN119**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	Reserved	-	-	**Reserved**
7	DMA1 RST	R/W	0	**DMA_1 Reset** Resets the DMA 1 Channel 0 = Normal operation. 1 = A zero to one transition resets DMA channel.
6	DMA1 ENB	R/W	0	DMA1_ENB Enables DMA_1 interface 0 = Disables DMA_1 interface 1 = Enables DMA_1 interface
5	RD TYPE	R/W	0	Selects the function of pRD_L signal. 0 = $\overline{RD}$ functions as a Read Strobe signal 11 = $\overline{RD}$ acts as a direction signal, $\overline{WR}$ works as a data strobe.
4 - 3	Reserved	-	-	**Reserved**
2	DMA1_CHAN(2)	R/W	0	**Channel Select** Selects which channel, within the chip, is to use the DMA_1 interface. 000 = Channel 0 001 = Channel 1 001 = Channel 2 011 = Channel 3 100 = Channel 4 101 = Channel 5 110 = Channel 6 111 = Channel 7
1	DMA1_CHAN(1)	R/W	0	
0	DMA1_CHAN(0)	R/W	0	

TABLE 41: INTERRUPT CONTROL REGISTER

REGISTER 26 **INTERRUPT CONTROL REGISTER (ICR)** **HEX ADDRESS: 0XN11A**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-3	Reserved	-	-	**Reserved**
2	INT_WC_RUR	R/W	0	**Interrupt Write-to-Clear or Reset-upon-Read Select** Configures Interrupt Status bits to either Reset Upon Read or Write-to-Clear 0=Interrupt Status bit RUR 1=Interrupt Status bit Write-to-Clear
1	ENBCLR	R/W	0	**Interrupt Enable Auto Clear** 0=Interrupt Enable bits are not cleared after status reading 1=Interrupt Enable bits are cleared after status reading
0	INTRUP_ENB	R/W	0	**Interrupt Enable for Framer_n** Enables Framer n for Interrupt Generation. 0 = Disables corresponding framer block for Interrupt Generation 1 = Enables corresponding framer block for Interrupt Generation

TABLE 42: LAPD SELECT REGISTER

REGISTER 20 LAPD SELECT REGISTER (LAPDSR) HEX ADDRESS: 0XN11B

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
[7:2]	Reserved	-	-	These bits are reserved
[1:0]	LAPDsel	R/W	0	**LAPD Select** Bits [1:0] determine which HDLC controller has access to the Read/ Write registers 0xn600 and 0xn700 for storing or extracting LAPD messages. 00 = HDLC Controller 1 01 = HDLC Controller 2 10 = HDLC Controller 3 11 = HDLC Controller 1

TABLE 43: CUSTOMER INSTALLATION ALARM GENERATION REGISTER

REGISTER 20 - T1 CUSTOMER INSTALLATION ALARM GENERATION REGISTER (CIAGR) HEX ADDRESS: 0XN11C

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
[7:4]	Reserved	-	-	These bits are reserved
[3:2]	CIAG	R/W	0	**CI Alarm Transmit (Only in ESF)** Alarm Indication Signal-Customer Installation (AIS-CI) and Remote Alarm Indication-Customer Installation (RAI-CI) are intendedfor use in a network to differentiate between an issue within the network or the CI. AIS-CI is an all ones signal with an embedded signature of 01111100 11111111 right-to left which recurs at 386 bit intervals in-the DS-1 signal. 00 = No CI alarm generation 01 = Enable unframed AIS-CI alarm generation 10 = Enable RAI-CI generation 11 = No CI alarm generation
[1:0]	CIAD	R/W	0	**CI Alarm Detect (Only in ESF)** 00 = CI alarm detection is disabled 01 = Enable unframed AIS-CI alarm detection 10 = Enable RAI-CI detection 11 = CI alarm detection is disabled

TABLE 44: PERFORMANCE REPORT CONTROL REGISTER

REGISTER 20 - T1 **PERFORMANCE REPORT CONTROL (PRCR)** **HEX ADDRESS: 0XN11D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
[7:2]	Reserved	-	-	These bits are reserved
[1:0]	APCR	R/W	0	**Automatic Performance Control/Response Report** These bits automatically generates a summary report of the PMON status so that it can be inserted into an out going LAPD message. 00 = No performance report issued 01 = Single performance report issued when a write of 00 follows by a write of 01 10 = Automatically issues a performance report every one second 11 = No performance report issued

TABLE 45: GAPPED CLOCK CONTROL REGISTER

REGISTER 20 - T1 **GAPPED CLOCK CONTROL REGISTER (GCCR)** **HEX ADDRESS: 0XN11E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
[7:2]	Reserved	-	-	These bits are reserved
1	TxGCCR	R/W	0	**Transmit Gapped Clock Interface** This bit is used to select a gapped clock interface operating at 2.048Mbit/s in DS-1 mode. In this application, 63 gaps (missing data) are inserted so that the overall bit rate is reduced to 1.544Mbit/s. (In this mode, TxMSYNC is used as the 2.048MHz Gapped Clock Input. TxSER is used as the 2.048MHz Gapped Data Input. TxSERCLK must be 1.544MHz.) 0 = Disabled 1 = Transmit gapped clock for the Transmit Path
0	RxGCCR	R/W	0	**Receive Gapped Clock Interface** This bit is used to select a gapped clock interface operating at 2.048Mbit/s in DS-1 mode. In this application, 63 gaps (missing data) are inserted so that the overall bit rate is reduced to 1.544Mbit/s. (In this mode, RxSERCLK should be configured as an input so that a 2.048MHz Gapped Clock can be applied to the Framer block. RxSER is used as the 2.048MHz Gapped Data Output. The position of the gaps will be determined by the gaps placed in RxSERCLK by the user.) 0 = Disabled 1 = Receive gapped clock for the Receive Path

Registers 0x1B thru 0x1F unused.

TABLE 46: TRANSMIT INTERFACE CONTROL REGISTER - E1 MODE

REGISTER 27 - E1 MODE **TRANSMIT INTERFACE CONTROL REGISTER (TICR)** **HEX ADDRESS:0Xn120**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSyncFrD	R/W	0	**Tx Synchronous fraction data interface** 0 = Fractionl data Is clocked into the chip using TxChCLK 1 = Fractional data is clocked in to the chip using TxSerClk (ungaped). TxChn[4:0] still indicates the time slot number if TxFr2048 is not 1, TxIMODE[1:0] = 00, and TxMUXEN = 0. TxChClk is used as fractional data enable.
6	Reserved	-	-	**Reserved**
5	TxPLClkEnb	R/W	0	**Tx payload clock enable** 1 = TxSerClk will output Tx clock with OH bit period blocked in 2.048Hz clock output mode.
	TxSync is Low	R/W	0	**TxSync is Low** In H.100 and HMVIP Mode 0 = TxSync is active “Low” 1 = TxSync is active “High”
4	TxFr2048	R/W	0	If TxMUXEN = 0 and TxIMODE[1:0] = 00 0 = TxChn[4:0] outputs the channel number as ususal. 1 = TxChn[0]/TxSig inputs signaling information and TxChn[1]/TxFrTD will input fractional channel data in 2.048 Mbit mode. *Note; This bit has no effect while either TxMUXEN = 1 or TxIMODE[1:0] = 00, TxChn[4:0] signals input TxSig and fractional data.*
3	TxICLKINV	R/W	0	**Clock Inversion** 0 = Data transition happens on rising edge of the transmit clocks. 1 = Data transition happens on falling edge of the transmit clocks.
2	TxMUXEN	R/W	0	**Mux Enable** 0 = No channel multiplexing. 1 = Four channels are multiplexed in single serial stream.
1	TxIMODE[1]	R/W	0	**Tx Interface Mode selection** This mode selection determines the interface speed. **When TxMUXEN = 0,** 00 = Transmit interface is taking data at a rate of 2.048Mbit/s. 01 = Transmit interface is taking data at a rate of 2.048Mbit/s. 10 = Transmit interface is taking data at a rate of 4.096Mbit/s. 11 = Transmit interface is taking data at a rate of 8.192Mbit/s. **When TxMUXEN = 1,** 00 = Rserved 01 = Transmit interface is taking data at a rate of 16.384Mbit/s from channel 0 and bit-demultiplexing into 4 channels from to the LIU outputs on channels 0 through 3. The TxSYNC pulse remains “High” during the framing bit of each E1 frame. 10 = Transmit interface is taking data at a rate of 16.384Mbit/s from channel 0 and byte-demultiplexing into 4 channels from to the LIU outputs on channels 0 through 3 (HMVIP Mode). The TxSYNC pulse remains “High” during the last two bits of the previous E1 frame and the first two bits of the current E1 frame. 11 = Transmit interface is taking data at a rate of 16.384Mbit/s from channel 0 and byte-demultiplexing into 4 channels from to the LIU outputs on channels 0 through 3 (H.100 Mode). The TxSYNC pulse remains “High” during the last bit of the previous E1 frame and the first bit of the current E1 frame. ***NOTE:*** *Channel 4 is de-multiplexed into the LIU outputs at channel 4 through 7.*
0	TxIMODE[0]	R/W	0	

TABLE 47: TRANSMIT INTERFACE CONTROL REGISTER - T1 MODE

REGISTER 27 - T1 MODE **TRANSMIT INTERFACE CONTROL REGISTER (TICR)** **HEX ADDRESS:0xn120**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSyncFrD	R/W	0	**Transmit Synchronous Fractional Data Interface** 0 = Fractional data is clocked into the chip using TxChCLK 1 = Fractional data is clocked in to the chip using TxSerClk (ungapped). TxChn[4:0] still indicates the time slot number if TxFr1544 is not 1, TxIMODE[1:0] = 00, and TxMUXEN = 0. TxChClk is used as fractional data enable.
6	Reserved	-	-	**Reserved**
5	TxPLClkEnb	R/W	0	**Transmit Payload Clock Enable** 1 = TxSerClk will output Tx clock with OH bit period blocked in 1.544MHz clock output mode.
	TxSync Is Low		0	**TxSync is Low** In H.100 and HMVIP Mode 0 = TxSync is active “Low” 1 = TxSync is active “High”
4	TxFr1544	R/W	0	**If TxMUXEN = 0 and TxIMODE[1:0] = 00** 0 = TxChn[4:0] will output the channel number as usual. 1 = TxChn[0]/TxSig will input signaling information and TxChn[1]/TxFrTD will input fractional channel data in 1.544 Mbit mode. ***NOTE:*** *This bit has no effect while either TxMUXEN = 1 or TxIMODE[1:0] = 00, TxChn[4:0] signals input TxSig and fractional data.*
3	TxICLKINV	R/W	0	**Clock Inversion** 0 = Data transition occurs on rising edge of the transmit clock. 1 = Data transition occurs on falling edge of the transmit clock.
2	TxMUXEN	R/W	0	**Mux Enable** 0 = No channel multiplexing. 1 = Four channels are multiplexed in single serial stream.
1	TxIMODE[1]	R/W	0	**Tx Intf Mode selection** This mode selection determines the interface speed. **When TxMUXEN = 0** 00 = Transmit interface is taking data at a rate of 1.544Mbit/s. 01 = Transmit interface is taking data at a rate of 2.048Mbit/s. 10 = Transmit interface is taking data at a rate of 4.096Mbit/s. 11 = Transmit interface is taking data at a rate of 8.192Mbit/s. **When TxMUXEN = 1,** 00 = Transmit interface is taking data at a rate of 12.352Mbit/s from channel 0 and bit-demultiplexing into 4 channels from to the LIU outputs on channels 0 through 3. The TxSYNC pulse remains “High” during the framing bit of each DS-1 frame. 01 = Transmit interface is taking data at a rate of 16.384Mbit/s from channel 0 and bit-demultiplexing into 4 channels from to the LIU outputs on channels 0 through 3. The TxSYNC pulse remains “High” during the framing bit of each DS-1 frame. 10 = Transmit interface is taking data at a rate of 16.384Mbit/s from channel 0 and byte-demultiplexing into 4 channels from to the LIU outputs on channels 0 through 3 (HMVIP Mode). The TxSYNC pulse remains “High” during the last two bits of the previous DS-1 frame and the first two bits of the current DS-1 frame. 11 = Transmit interface is taking data at a rate of 16.384Mbit/s from channel 0 and byte-demultiplexing into 4 channels from to the LIU outputs on channels 0 through 3 (H.100 Mode). The TxSYNC pulse remains “High” during the last bit of the previous DS-1 frame and the first bit of the current DS-1 frame. ***NOTE:*** *Channel 4 is de-multiplexed into the LIU outputs at channel 4 through 7.*
0	TxIMODE[0]	R/W	0	

TABLE 48: RECEIVE INTERFACE CONTROL REGISTER (RICR) - E1 MODE

Register 28 - E1 Mode **RECEIVE INTERFACE CONTROL REGISTER (RICR)** **0Xn122**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RxSyncFrD	R/W	0	**Rx synchronous fractional data interface** 0 = Fractional data is clocked out from the chip using RxChCLK 1 = RxChClk is used to output fractional data enable instead of being fraction data clock. In this mode, fractional data is clocked out of the chip using RxSerClk (ungapped). RxChn still indicates the time slot number if RxFr2048 is not 1, RxIMODE[1:0] = 0, and RxMUXEN = 0.
6	Reserved	-	-	**Reserved**
5	RxPLClkEnb/	R/W	0	**Rx Payload Clock Enable** 1 = RxSerClk outputs Rx clock with OH bit period blocked while in 2.048MHz clock output mode.
	RxSyncislow			**RxSync is low** In H.100 and HMVIP Mode 1 = RxSync active low. 0 = RxSync active high.
4	RxFr2048	R/W	0	**Clock Inversion** 1 = RxChn[0]/RxSig outputs signaling information, RxChn[1]/RxFrTD will output fractional channel data in 2.048 MHz mode and RxChn[2] will output the serial channel number of each time slot. 0 = RxChn[4:0] outputs the parallel channel number as usual.
3	RxICLKINV	N/A	0	**Clock Inversion** 0 = Data transition happens on the rising edge of the transmit clocks. 1 = Data transition happens on the falling edge of the transmit clocks.
2	RxMUXEN	R/W	0	Mux Enable 0 = No channel Multiplexing. 1 = Four channels are multiplexed in single serial stream.
1	RxIMODE[1]	R/W	0	**Rx Intf Mode Selection** This mode selection determines the interface speed. **When RxMUXEN = 0** 00 = Receive interface is presenting data at a rate of 2.048Mbit/s. 01 = Receive interface is presenting data at a rate of 2.048Mbit/s. 10 = Receive interface is presenting data at a rate of 4.096Mbit/s. 11 = Receive interface is presenting data at a rate of 8.192Mbit/s. **When RxMUXEN = 1** 00 = Rserved 01 = Receive interface is taking data from the four LIU input channels 0 through 3 and byte-multiplexing into the serial output channel 0. The TxSYNC pulse remains "High" during the framing bit of each E1 frame. 10 = Receive interface is taking data from the four LIU input channels 0 through 3 and byte-multiplexing into the serial output channel 0 (HMVIP Mode). The TxSYNC pulse remains "High" during the last two bits of the previous E1 frame and the first two bits of the current E1 frame. 11 = Receive interface is taking data from the four LIU input channels 0 through 3 and byte-multiplexing into the serial output channel 0 (H.100 Mode). The TxSYNC pulse remains "High" during the last bit of the previous E1 frame and the first bit of the current E1 frame. ***NOTE:*** *Channels 4 through 7 are multiplexed into the serial output at channel 4.*
0	RxIMODE[0]	R/W	0	

TABLE 49: RECEIVE INTERFACE CONTROL REGISTER (RICR) - T1 MODE

Register 28 - T1 Mode **RECEIVE INTERFACE CONTROL REGISTER (RICR)** **0Xn122**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RxSyncFrD	R/W	0	**Rx synchronous fractional data interface** 1 = RxChClk is used to output fractional data instead of being fraction data clock. In this mode, fractional data is clocked out of the chip using RxSerClk (ungapped). RxChn still indicates the time slot number if RxFr1544 is not 1, RxIMODE[1:0] = 00, and RxMUXEN = 0. RxCClk will be a valid signal for fractional data output (RxFrTD) if RxFr1544 is 1 or RxIMODE[1:0] = 00 or RxMUXEN = 0
6	Reserved	-	-	**Reserved**
5	RxPLClkEnb/	R/W	0	**Rx Payload Clock Enable** 1 = RxSerClk will output Rx clock with OH bit period blocked while in 1.544MHz clock output mode.
	RxSyncislow			**RxSync is low** In H.100 and HMVIP Mode 1 =Rx Sync active low. 0 = RxSync active high.
4	RxFr1544	R/W	0	**Clock Inversion/RxSig** 1 = RxChn[0]/RxSig outputs signaling information, RxChn[1]/RxFrTD will output fractional channel data in 1.544 MHz mode and RxChn[2] will output the serial channel number of each time slot. 0 = RxChn[4:0] outputs the parallel channel number as usual.
3	RxICLKINV	N/A	0	**Clock inversion** 0 = Data transition happens on the rising edge of the transmit clocks. 1 = Data transition happens on the falling edge of the transmit clocks.
2	RxMUXEN	R/W	0	**Mux Enable** 0 = No channel Multiplexing. 1 = Four channels are multiplexed in single serial stream.
1	RxIMODE[1]	R/W	0	**Rx Interface Mode selection** This mode selection determines the interface speed. **When RxMUXEN = 0,** 00 = Receive interface is presenting data at a rate of 1.544Mbit/s. 01 = Receive interface is presenting data at a rate of 2.048Mbit/s. 10 = Receive interface is presenting data at a rate of 4.096Mbit/s. 11 = Receive interface is presenting data at a rate of 8.192Mbit/s. **When RxMUXEN = 1,** 00 = Receive interface is taking data from the four LIU input channels 0 through 3 and byte-multiplexing into a 12.352MHz serial output on channel 0. The TxSYNC pulse remains “High” during the framing bit of each DS-1 frame. 01 = Receive interface is taking data from the four LIU input channels 0 through 3 and byte-multiplexing into a 16.384MHz serial output on channel 0. The TxSYNC pulse remains “High” during the framing bit of each DS-1 frame. 10 = Receive interface is taking data from the four LIU input channels 0 through 3 and byte-multiplexing into a 16.384MHz serial output on channel 0 (HMVIP Mode). The TxSYNC pulse remains “High” during the last two bits of the previous DS-1 frame and the first two bits of the current DS-1 frame. 11 = Receive interface is taking data from the four LIU input channels 0 through 3 and byte-multiplexing into a 16.384MHz serial output on channel 0 (H.100 Mode). The TxSYNC pulse remains “High” during the last bit of the previous DS-1 frame and the first bit of the current DS-1 frame. ***NOTE:*** *Channels 4 through 7 are multiplexed into the serial output at channel 4.*
0	RxIMODE[0]	R/W	0	

TABLE 50: DS1 TEST REGISTER

Register 29 DS1 Test Register (DS1TR) 0xn123

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	PRBSTyp	R/W	0	**PRBS Pattern Type** 0 = The (X^{15} + X^{14} +1) PBRS Polynomial is generated. 1 = QRTS (Quasi-Random Test Signal) Pattern is generated.
6	ERRORIns	R/W	0	**Error Insertion** 0 to 1 transition will cause one output bit inverted
5	Reserved	-	-	**Reserved**
4	RxPRBSLock	R	0	**Lock Status** 0 = Rx PRBS has not Locked. 1 = Rx PRBS has locked to the input patterns.
3	RxPRBSEnb	R/W	0	**Rx PRBS Generation Enable** 0 = Receive PRBS checker is not enabled. 1 = Receive PRBS checker is enabled.
2	TxPRBSEnb	R/W	0	**Tx PRBS Generation Enable** 0 = Tx PRBS generator is not enabled. 1 = Tx PRBS generator is enabled.
1	RxDS1Bypass	R/W	0	**Rx DS1 Framer Bypass** Reserved
0	TxDS1Bypass	R/W	0	**Tx DS1 Framer Bypass** 0 = Tx frame pulse bypassed. 1 = Tx frame pulse and data are from TxSer and TxSync inputs.

TABLE 51: LOOPBACK CODE CONTROL REGISTER

Register 30 LOOPBACK CODE CONTROL REGISTER (LCCR) 0xn124

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	RXLBCDLEN[1:0]	R/W	0	**Receive Loopback Code Activation Length** Determines the receive loopback code activation length. 00 = 4-bit sequence 01 = 5-bit sequence 10 = 6-bit sequence 11 = 7-bit sequence
5-4	RXLBCDLEN[1:0]	R/W	0	**Receive Loopback Code Deactivation Length** Determines the receive loopback code deactivation length 00 = 4-bit sequence 01 = 5-bit sequence 10 = 6-bit sequence 11 = 7-bit sequence
3-2	TXLBCDLEN[1:0]	R/W	0	**Transmit Loopback Code Length** Determines transmit loopback code length. 00 = 4-bit sequence 01 = 5-bit sequence 10 = 6-bit sequence 11 = 7-bit sequence
1	FRAMED	R	0	**Framed Loopback Code** Selects either framed or unframed loopback code operation. 0 = Unframed 1 = Framed
0	AUTOENB	R/W	0	**Loopback Automatically** Enables loopback automatically. 0 = Automatic loopback is disabled 1 = Automatic loopback is enabled

TABLE 52: TRANSMIT LOOPBACK CODER REGISTER

Register 31 Transmit Loopback Coder Register (TLCR) 0xn125

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-1	TXLBC[6:0]	R/W	1010101	**Transmit Loopback Code** Determines the transmit loopback coding sequence.
0	TXLBCENB	R/W	0	**Transmit Loopback Code Enable** Enables loopback code generation. 0 = Transmit loopback code is disabled. 1 = Transmit loopback code is enabled

TABLE 53: TRANSMIT LOOPBACK ACTIVATION CODE REGISTER

Register 32 Receive Loopback Activation Code Register (RLACR) 0xn126

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-1	RXLBAC[6:0]	R/W	1010101	**Receive activation loopback code** Determines the receive activation loopback coding sequence.
0	RXLBACENB	R/W	0	**Receive activation loopback code enable** Enables receive loopback code activation detection. 0 = Receive loopback code activation detection is disabled. 1 = Receive loopback code activation detection is enabled

TABLE 54: TRANSMIT LOOPBACK DEACTIVATION CODE REGISTER

Register 33 Receive Loopback Deactivation Code Register (RLDCR) 0xn127

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-1	RXLBDC[6:0]	R/W	1010101	**Receive deactivation loopback code** Determines the receive deactivation loopback coding sequence.
0	RXLBDCENB	R/W	0	**Receive deactivation loopback code enable** Enables receive loopback code deactivation detection. 0 = Receive loopback code deactivation detection is disabled. 1 = Receive loopback code deactivation detection is enabled

TABLE 55: TRANSMIT Sa SELECT REGISTER

Register 34 **TRANSMIT Sa SELECT REGISTER (TSASR)** **0xn130**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSa8SEL	R/W	0	**Sa8 bit** Determines whether Sa8 is from serial input or register. 0 = Serial input. 1 = Sa8 register.
6	TxSa7SEL	R/W	0	**Sa7 bit select** Determines whether Sa7 is from serial input or register. 0 = Serial input. 1 = Sa7 register
5	TxSa6SEL	R/W	0	**Sa6 bit select** Determines whether Sa6 is from serial input or register. 0 = Serial input. 1 = Sa6 register
4	TxSa5SEL	R/W	0	**Sa5 bit select** Determines whether Sa5 is from serial input or register. 0 = Serial input. 1 = Sa5 register
3	TxSa4SEL	R/W	0	**Sa4 bit select** Determines whether Sa4 is from serial input or register. 0 = Serial input. 1 = Sa4 register
2	LB1ENB	R/W	0	**Loopback 1 auto enable** Local loopback is activated while the followings happened from the transmit serial input. Sa5 = 0 and Sa6 = 1111 occur for 8 consecutive times. A = 1
1	LB2ENB	R/W	0	**Loopback 2 auto enable** Local loopback is activated while the followings happened from the transmit serial input. Sa5 = 0 and Sa6 = 1010 occur for 8 consecutive times. A = 1
0	LBRENB	R/W	0	**Loopback release enable** Local loopback is released while the followings happened from the transmit serial input. Sa5 = 0 and Sa6 = 0000 occur for 8 consecutive times.

TABLE 56: TRANSMIT Sa AUTO CONTROL REGISTER 1

Register 35 TRANSMIT Sa AUTO CONTROL REGISTER 1 (TSACR1) 0xn131

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	LOSLFA_1_ENB	R/W	0	**LOS/LFA 1 auto transmit**
6	LOS_1_ENB	R/W	0	**LOS 1 auto transmit**
5	LOSLFA_2_ENB	R/W	0	**LOS/LFA 2 auto transmit**
4	LOSLFA_3_ENB	R/W	0	**LOS/LFA 3 auto transmit**
3	LOSLFA_4_ENB	R/W	0	**LOS/LFA 4 auto transmit**
2	NOP_ENB	R/W	0	**No power auto transmit**
1	NOP_LOSLFA_ENB	R/W	0	**No power and LOS/LFA auto transmit**
0	LOS_2_ENB	R/W	0	**LOS 3 auto transmit**

The following table demonstrates the conditions on the receive side which trigger the actions while these bits are enabled.

NOTE: *A will be and 'with the value generated from yellow alarm control.*

TABLE 57: CONDITIONS ON RECEIVE SIDE WHEN TSACR1 BITS ARE ENABLED

CONDITIONS	ACTIONS - SENDING PATTERN			COMMENTS
	A	Sa5	Sa6	
LOSLFA_1_ENB: Loss of signal or Loss of frame alignment	X	1	0000	LOS/LFA at TE (FC2)
LOS_1_ENB: Loss of signal	1	1	1110	LOS (FC3)
LOSLFA_2_ENB: LOS or LFA	1	0	0000	LOS/LFA (FCL)
LOSLFA_3_ENB: LOS or LFA	0	1	1100	LOS/LFA (FC4)
LOSLFA_4_ENB: LOS or LFA	0	1	1110	LOS/LFA (FC3&FC4)
NOP_ENB: Loss of power	0	1	1000	Loss of power at NT1
NOP_LOSLFA_ENB: Loss of power and LOS or LFA	1	1	1000	Loss of power and LOS/LFA
LOS_2_ENB: LOS	AUXP pattern			LOS (FC1). Transmit AUXP pattern

TABLE 58: TRANSMIT Sa AUTO CONTROL REGISTER 2

Register 36 TRANSMIT Sa SELECT REGISTER (TSACR2) 0xn132

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	AIS_1_ENB	R/W	0	**AIS reception**
6	AIS_2_ENB	R/W	0	**AIS reception**
5	Reserved	-	-	**Reserved**
4	Reserved	-	-	**Reserved**
3-2	CRCREP_ENB	R/W	0	**CRC report**
1	CRCDET_ENB	R/W	0	**CRC detection**
0	CRCREC/DET_ENB	R/W	0	**CRC report and detect**

The following table demonstrates the conditions on receive side which trigger the actions while these bit are enabled.

TABLE 59: CONDITIONS ON RECEIVE SIDE WHEN TSACR1 BITS ENABLED

CONDITIONS	ACTIONS - SENDING PATTERN FOR			
	A	Sa5	Sa6	E
AIS_1_ENB	1	1	1111	X
AIS_2_ENB	0	1	1111	x
CRCREP_ENB = 01, CRC reported (E = 0)	0	1	0000	0
CRCREP_ENB = 10, CRC reported	0	0	0000	0
CRCREP_ENB = 11, CRC reported	0	1	0001	1
CRCDET_ENB	0	1	0010	1
CRCDET/REP_ENB	0	1	0011	1

TABLE 60: TRANSMIT Sa4 REGISTER

Register 37 TRANSMIT Sa4 REGISTER (TSA4R) 0xn133

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TxSa4[7:0]	R/W	11111111	**Sa4** The content of this register sources the transmit Sa4 bits while TxSa4ENB (register 0xn10Ah) is 1 and TxSa4SEL (register 0xn130h) is 1. Bit 7 is transmitted in frame 2 of the CRC-4 multiframe, bit 6 is in frame 4, etc.

TABLE 61: TRANSMIT Sa5 REGISTER

Register 38 TRANSMIT Sa5 REGISTER (TSA5R) 0xn134

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TxSa5[7:0]	R/W	11111111	**Sa5** The content of this register sources the transmit Sa5 bits while TxSa5ENB (register 0xn10Ah) is 1 and TxSa5SEL (register 0xn130h) is 1. Bit 7 is transmitted in frame 2 of the CRC-4 multiframe, bit 6 is in frame 4, etc.

TABLE 62: TRANSMIT Sa6 REGISTER

Register 39 TRANSMIT Sa6 REGISTER (TSA6R) 0xn135

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TxSa6[7:0]	R/W	11111111	**Sa6** The content of this register sources the transmit Sa6 bits while TxSa6ENB (register 0xn10Ah) is 1 and TxSa6SEL (register 0xn130h) is 1. Bit 7 is transmitted in frame 2 of the CRC-4 multiframe, bit 6 is in frame 4, etc.

TABLE 63: TRANSMIT Sa7 REGISTER

Register 40 TRANSMIT Sa7 REGISTER (TSA7R) 0xn136

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TxSa7[7:0]	R/W	11111111	**Sa7** The content of this register sources the transmit Sa7 bits while TxSa7ENB (register 0xn10Ah) is 1 and TxSa7SEL (register 0xn130h) is 1. Bit 7 is transmitted in frame 2 of the CRC-4 multiframe, bit 6 is in frame 4, etc.

TABLE 64: TRANSMIT Sa8 REGISTER

Register 41 TRANSMIT Sa8 REGISTER (TSA8R) 0xn137

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TxSa8[7:0]	R/W	11111111	**Sa8** The content of this register sources the transmit Sa8 bits while TxSa8ENB (register 0xn10Ah) is 1 and TxSa8SEL (register 0xn130h) is 1. Bit 7 is transmitted in frame 2 of the CRC-4 multiframe, bit 6 is in frame 4, etc.

TABLE 65: RECEIVE SA4 REGISTER

Register 42 **RECEIVE SA4 REGISTER (RSA4R)** **0xn13B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxSa4[7:0]	RO	11111111	**Sa4** The content of this register stores the received Sa4 bits if RxSa4ENB (register 0xn10Ch) is 1. Bit 7 is received in frame 2 of the CRC-4 multiframe, bit 6 is in frame 4, etc.

TABLE 66: RECEIVE SA5 REGISTER

Register 43 **RECEIVE SA5 REGISTER (RSA5R)** **0xn13C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxSa5[7:0]	RO	11111111	**Sa5** The content of this register stores the received Sa5 bits if RxSa5ENB (register 0xn10Ch) is 1. Bit 7 is received in frame 2 of the CRC-4 multiframe, bit 6 is in frame 4, etc.

TABLE 67: RECEIVE SA6 REGISTER

REGISTER 44 **RECEIVE SA6 REGISTER (RSA6R)** **0xn13D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxSa6[7:0]	RO	11111111	**Sa6** The content of this register stores the received Sa6 bits if RxSa6ENB (register 0xn10Ch) is 1. Bit 7 is received in frame 2 of the CRC-4 multiframe, bit 6 is in frame 4, etc.

TABLE 68: RECEIVE SA7 REGISTER

REGISTER 45 **RECEIVE SA7 REGISTER (RSA7R)** **0xn13E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxSa7[7:0]	RO	11111111	**Sa7** The content of this register stores the received Sa7 bits if RxSa7ENB (register 0xn10Ch) is 1. Bit 7 is received in frame 2 of the CRC-4 multiframe, bit 6 is in frame 4, etc.

TABLE 69: RECEIVE SA8 REGISTER

REGISTER 46 **RECEIVE SA8 REGISTER (RSA8R)** **0xn13F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxSa8[7:0]	RO	11111111	**Sa8** The content of this register stores the received Sa8 bits if RxSa8ENB (register 0xn10Ch) is 1. Bit 7 is received in frame 2 of the CRC-4 multiframe, bit 6 is in frame 4, etc.

TABLE 70: DATA LINK CONTROL REGISTER

REGISTER 19 **DATA LINK CONTROL REGISTER 2 (DLCR2)** **HEX ADDRESS: 0XN143**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SLC-96	R/W	0	**SLC®96 Enable, 6 bit for ESF** If SLC®96 framing is selected, setting this bit high will enable SLC®96 data link transmission; Otherwise, the regular SF framing bits are transmitted. In ESF framing mode, setting this bit high will cause facility data link to transmit/receive SLC®96-like message.
6	MOSA	R/W	0	**MOS Abort Enable/Disable Select** This Read/Write bit-field is used to configure the transmit HDLC2 controller to automatically transmit an abort sequence anytime it transitions from the MOS mode to the BOS mode. 0 = Transmit HDLC2 Controller inserts an MOS abort sequence if the MOS message is interrupted 1 = Prevents Transmit HDLC2 Controller from inserting an MOS abort sequence.
5	Rx_FCS_DIS	R/W	0	**Receive FCS Verification Disable** Enables/Disables Receive HDLC2 Controller's computation and verification of the FCS value in the incoming LAPD message frame 0 = Verifies FCS value of each MOS frame. 1 = Does not verify FCS value of each MOS frame.
4	AutoRx	R/W	0	**Auto Receive LAPD Message** Configures the Rx HDLC2 Controller to discard any incoming LAPD Message frame that exactly match which is currently stored in the Rx HDLC2 buffer. 0 = Disabled 1 = Enables this feature.
3	Tx_ABORT	R/W	0	**Transmit ABORT** Configures the Tx HDLC2 Controller to transmit an ABORT sequence (string of 7 or more consecutive 1's) to the Remote terminal. 0 = Tx HDLC2 Controller operates normally 1 = Tx HDLC2 Controller inserts an ABORT sequence into the data link channel.
2	Tx_IDLE	R/W	0	**Transmit Idle (Flag Sequence Byte)** Configures the Tx HDLC2 controller to transmit a string of Flag Sequence octets (0X7E) in the data link channel to the Remote terminal. 0 = Tx HDLC2 Controller resumes transmitting data to the Remote terminal 1 = Tx HDLC2 Controller transmits a string of Flag Sequence bytes. ***NOTE:*** *This bit-field is ignored if the Tx HDLC2 controller is operating in the BOS Mode - bit-field 0(MOS/BOS) within this register is set to 0.*
1	Tx_FCS_EN	R/W	0	**Transmit LAPD Message with FCS** Configure HDLC2 Controller to include/not include FCS octets in the outbound LAPD message frames. 0 = Does not include FCS octets into the outbound LAPD message frame. 1 = Inserts FCS octets into the outbound LAPD message frame. ***NOTE:*** *This bit-field is ignored if the transmit HDLC2 controller has been configured to operate in the BOS mode.*
0	MOS/$\overline{\text{BOS}}$	R/W	0	**Message Oriented Signaling/Bit Oriented Signaling Select** Specifies whether the TxRx HDLC2 Controller will be transmitting and receiving LAPD message frames (MOS) or Bit Oriented Signal (BOS) messages. 0 = Tx/Rx HDLC2 Controller transmits and receives BOS messages. 1 = Tx/Rx HDLC2 Controller transmits and receives MOS messages.

TABLE 71: TRANSMIT DATA LINK BYTE COUNT REGISTER

REGISTER 20 **TRANSMIT DATA LINK BYTE COUNT REGISTER 2 (TDLBCR2)** **HEX ADDRESS: 0XN144**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	BUFAVAL//BUFSEL	R/W	0	**Transmit HDLC2 Buffer Available/Buffer Select** Specifies which of the two Tx HDLC2 Buffers that the Tx HDLC2 controller should read from to generate the next outbound HDLC2 message. 0 = transmits message data residing in Tx HDLC2 Buffer 0. 1 = transmits message data residing in Tx HDLC2 buffer 1. ***NOTE:*** *If one of these Tx HDLC2 buffers contain a message which has yet to be completely read-in and processed for transmission by the Tx HDLC2 controller, then this bit-field will automatically reflect the value corresponding to the available buffer. Changing this bit-field to the in-use buffer is not permitted.*
6	TDLBC6	R/W	0	**Transmit HDLC2 Message - Byte Count** Depends on whether an MOS or BOS message is being transmitted to the Remote Terminal Equipment ***If BOS message is being transmitted*:** These bit fields contain the number of repetitions the BOS message must be transmitted before the Tx HDLC2 controller generates the TxEOT interrupt and halts transmission. If these fields are set to 00000000, then the BOS message will be transmitted for an indefinite number of times. ***If MOS message is being transmitted:*** These bit fields contain the length, in number of octets, of the message to be transmitted.
5	TDLBC5	R/W	0	
4	TDLBC4	R/W	0	
3	TDLBC3	R/W	0	
2	TDLBC2	R/W	0	
1	TDLBC1	R/W	0	
0	TDLBC0	R/W	0	

TABLE 72: RECEIVE DATA LINK BYTE COUNT REGISTER

REGISTER 21 **RECEIVE DATA LINK BYTE COUNT REGISTER 2 (RDLBCR2)** **HEX ADDRESS: 0XN145**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RBUFPTR	R/W	0	**Receive HDLC2 Buffer-Pointer** Identifies which RxHDLC2 buffer contains the newly received HDLC2 message. 0 = HDLC2 message is stored in Rx HDLC2 Buffer 0. 1 = HDLC2 message is stored in Rx HDLC2 Buffer 1.
6	RDLBC6	R/W	0	**Receive HDLC Message - byte count** **In MOS Mode** These seven bit-fields contain the size in bytes of the HDLC2 message that has been extracted and written into the Rx HDLC2 buffer. In BOS Mode These bits should be set to the value of the message repetitions before each receive interrupt. If ithey are set to “0”, no RxEOT interrupt will be generated.
5	RDLBC5	R/W	0	
4	RDLBC4	R/W	0	
3	RDLBC3	R/W	0	
2	RDLBC2	R/W	0	
1	RDLBC1	R/W	0	
0	RDLBC0	R/W	0	

TABLE 73: DATA LINK CONTROL REGISTER

REGISTER 19 **DATA LINK CONTROL REGISTER 3 (DLCR3)** **HEX ADDRESS: 0XN153**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SLC-96	R/W	0	**SLC®96 Enable, 6 bit for ESF** If SLC®96 framing is selected, setting this bit high will enable SLC®96 data link transmission; Otherwise, the regular SF framing bits are transmitted. In ESF framing mode, setting this bit high will cause facility data link to transmit/receive SLC®96-like message.
6	MOSA	R/W	0	**MOS Abort Enable/Disable Select** This Read/Write bit-field is used to configure the transmit HDLC3 controller to automatically transmit an abort sequence anytime it transitions from the MOS mode to the BOS mode. 0 = Transmit HDLC3 Controller inserts an MOS abort sequence if the MOS message is interrupted 1 = Prevents Transmit HDLC3 Controller from inserting an MOS abort sequence.
5	Rx_FCS_DIS	R/W	0	**Receive FCS Verification Disable** Enables/Disables Receive HDLC3 Controller's computation and verification of the FCS value in the incoming LAPD message frame 0 = Verifies FCS value of each MOS frame. 1 = Does not verify FCS value of each MOS frame.
4	AutoRx	R/W	0	**Auto Receive LAPD Message** Configures the Rx HDLC3 Controller to discard any incoming LAPD Message frame that exactly match which is currently stored in the Rx HDLC3 buffer. 0 = Disabled 1 = Enables this feature.
3	Tx_ABORT	R/W	0	**Transmit ABORT** Configures the Tx HDLC3 Controller to transmit an ABORT sequence (string of 7 or more consecutive 1's) to the Remote terminal. 0 = Tx HDLC3 Controller operates normally 1 = Tx HDLC3 Controller inserts an ABORT sequence into the data link channel.
2	Tx_IDLE	R/W	0	**Transmit Idle (Flag Sequence Byte)** Configures the Tx HDLC3 controller to transmit a string of Flag Sequence octets (0X7E) in the data link channel to the Remote terminal. 0 = Tx HDLC3 Controller resumes transmitting data to the Remote terminal 1 = Tx HDLC3 Controller transmits a string of Flag Sequence bytes. ***NOTE:*** *This bit-field is ignored if the Tx HDLC3 controller is operating in the BOS Mode - bit-field 0(MOS/BOS) within this register is set to 0.*
1	Tx_FCS_EN	R/W	0	**Transmit LAPD Message with FCS** Configure HDLC3 Controller to include/not include FCS octets in the outbound LAPD message frames. 0 = Does not include FCS octets into the outbound LAPD message frame. 1 = Inserts FCS octets into the outbound LAPD message frame. ***NOTE:*** *This bit-field is ignored if the transmit HDLC3 controller has been configured to operate in the BOS mode.*
0	MOS/$\overline{\text{BOS}}$	R/W	0	**Message Oriented Signaling/Bit Oriented Signaling Select** Specifies whether the TxRx HDLC3 Controller will be transmitting and receiving LAPD message frames (MOS) or Bit Oriented Signal (BOS) messages. 0 = Tx/Rx HDLC3 Controller transmits and receives BOS messages. 1 = Tx/Rx HDLC3 Controller transmits and receives MOS messages.

TABLE 74: TRANSMIT DATA LINK BYTE COUNT REGISTER

REGISTER 20 **TRANSMIT DATA LINK BYTE COUNT REGISTER 3 (TDLBCR3)** **HEX ADDRESS: 0XN154**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	BUFAVAL//BUFSEL	R/W	0	**Transmit HDLC3 Buffer Available/Buffer Select** Specifies which of the two Tx HDLC3 Buffers that the Tx HDLC3 controller should read from to generate the next outbound HDLC3 message. 0 = transmits message data residing in Tx HDLC3 Buffer 0. 1 = transmits message data residing in Tx HDLC3 buffer 1. ***NOTE:*** *If one of these Tx HDLC3 buffers contain a message which has yet to be completely read-in and processed for transmission by the Tx HDLC3 controller, then this bit-field will automatically reflect the value corresponding to the available buffer. Changing this bit-field to the in-use buffer is not permitted.*
6	TDLBC6	R/W	0	**Transmit HDLC3 Message - Byte Count** Depends on whether an MOS or BOS message is being transmitted to the Remote Terminal Equipment ***If BOS message is being transmitted*:** These bit fields contain the number of repetitions the BOS message must be transmitted before the Tx HDLC3 controller generates the TxEOT interrupt and halts transmission. If these fields are set to 00000000, then the BOS message will be transmitted for an indefinite number of times. ***If MOS message is being transmitted:*** These bit fields contain the length, in number of octets, of the message to be transmitted.
5	TDLBC5	R/W	0	
4	TDLBC4	R/W	0	
3	TDLBC3	R/W	0	
2	TDLBC2	R/W	0	
1	TDLBC1	R/W	0	
0	TDLBC0	R/W	0	

TABLE 75: RECEIVE DATA LINK BYTE COUNT REGISTER

REGISTER 21 **RECEIVE DATA LINK BYTE COUNT REGISTER 3 (RDLBCR3)** **HEX ADDRESS: 0XN155**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RBUFPTR	R/W	0	**Receive HDLC3 Buffer-Pointer** Identifies which RxHDLC3 buffer contains the newly received HDLC3 message. 0 = HDLC3 message is stored in Rx HDLC3 Buffer 0. 1 = HDLC3 message is stored in Rx HDLC3 Buffer 1.
6	RDLBC6	R/W	0	**Receive HDLC Message - byte count** **In MOS Mode** These seven bit-fields contain the size in bytes of the HDLC3 message that has been extracted and written into the Rx HDLC3 buffer. In BOS Mode These bits should be set to the value of the message repetitions before each receive interrupt. If ithey are set to “0”, no RxEOT interrupt will be generated.
5	RDLBC5	R/W	0	
4	RDLBC4	R/W	0	
3	RDLBC3	R/W	0	
2	RDLBC2	R/W	0	
1	RDLBC1	R/W	0	
0	RDLBC0	R/W	0	

TABLE 76: DEVICE ID REGISTER

REGISTER 47 **DEVICE ID REGISTER (DEVID)** **0XN1FE**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	DEVID[7:0]	RO	00110100	**DEVID** This register is used to identify the XRT86L34 Framer/LIU. The contents of this regitster are 0x35h.

TABLE 77: TRANSMIT CHANNEL CONTROL REGISTER 0 TO 31 E1 MODE

REGISTER 49-80 E1 TRANSMIT CHANNEL CONTROL REGISTER 0-31 (TCCR 0-31) HEX ADDRESS: 0XN300 TO 0XN31F

BIT	MODE	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	E1	LAPDcntl	R/W	10	**LAPD Control** These bits select which LAPD controller is to be activated. 00 = LAPD1 01 = LAPD2 10 = TxDE[1:0] will determine the data source for the D/E Time Slots 11 = LAPD3
5-4		Reserved	-	-	**Reserved**
3-0		TxCond(3:0)	R/W	0	**Transmit Channel Conditioning for Timeslot 0 to 31** Replaces the contents of timeslot 1 octet (PCM data within the next out-bound frame) with signaling codes as follows. **0x0 =** Contents of timeslot octet unchanged prior to transmission to Remote Terminal Equipment. Contents are transmitted without modification as received via the TxSer_n input pin. **0x1 =** All 8 bits of the timeslot octet are inverted (1's complement) prior to transmission to the Remote Terminal Equipment. This selection is equivalent to executing the following logic operation with each timeslot 1 octet: **TX_TIME_SLOT_OCTET=(TE_TIME_SLOT_OCTET) XOR 0xFF** **0x2 =** The even bits of the timeslot octet are inverted prior to trans mission to the Remote Terminal Equipment. This selection is equivalent to executing the following logic operation: **TX_TIME_SLOT_OCTET=(TE_TIME_SLOT_OCTET) XOR 0xAA** **0x3 =** The odd bits of the time slot octet are inverted prior to trans mission to the Remote Terminal Equipment. This selection is equivalent to executing the following logic operation: **TX_TIME_SLOT_OCTET=(TE_TIME_SLOT_OCTET) XOR 0x55** **0x4** = The contents of the timeslot octet will be substituted with the 8 -bit value in Programmable User Code Register, prior to transmission to the Remote Terminal Equipment. **0x5 =** The contents of the timeslot octet will be substituted with the value 0xFF (BUSY) prior to transmission to the Remote Terminal Equipment. **0X6 =** The contents of the timeslot octet will be substituted with the value 0xD5 (VACANT 0V) prior to transmission to the Remote Terminal Equipment. **0X7 =** The BUSY TS(111#_####) code replaces the input data for transmission. (##### is Timeslot number.) **0X8 =** The BUSY 00 code replaces the input data for transmission **0X9 =** The A-Law Digital Milliwatt pattern replaces the input data for transmission. **0XA =** The μ-Law Digital Milliwatt pattern replaces the input data for transmission. **0xB** = The MSB (bit 1) of input data is inverted. **0xC** = All input data except MSB is inverted. **0xD** = PRBS, QRTS/X^{15} + X^{14} + 1. **0xE** = The input PCM data bit are unchanged. **0xF** = This is a D/E time slots. See transmit signaling and data link select register. (TSDLSR)

TABLE 78: TRANSMIT CHANNEL CONTROL REGISTER 0 TO 31 T1 MODE

REGISTER 49-80 T1 TRANSMIT CHANNEL CONTROL REGISTER 0-31 (TCCR 0-31) HEX ADDRESS: 0XN300 TO 0XN31F

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	LAPDcntl	R/W	10	**LAPD Control** These bits select which LAPD controller is to be activated. 00 = LAPD1 01 = LAPD2 10 = TxDE[1:0] will determine the data source for the D/E Time Slots 11 = LAPD3
5 - 4	TxZERO[1:0]	R/W	00	**Selects type of zero suppression** These bits select the zero code suppression used. 00 = No zero code suppression is used. 01 = AT&T bit 7 stuffing is used. 10 = GTE zero code suppression is used. Bit 8 is stuffed in non-signaling frame. Otherwise, bit 7 is stuffed in signaling frame if the signaling bit is zero. 11 = DDS zero code suppression is applied where 0x98 replaces the input data.

TABLE 78: TRANSMIT CHANNEL CONTROL REGISTER 0 TO 31 T1 MODE

REGISTER 49-80 T1 TRANSMIT CHANNEL CONTROL REGISTER 0-31 (TCCR 0-31) HEX ADDRESS: 0XN300 TO 0XN31F

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3-0	TxCond(3:0)	R/W	0	**Transmit Channel Conditioning for Timeslot 0 to 23** Replaces the contents of timeslot 1 octet (PCM data within the next out-bound frame) with signaling codes as follows. **0x0 =** Contents of timeslot octet unchanged prior to transmission to Remote Terminal Equipment. Contents are transmitted without modification as received via the TxSer_n input pin. **0x1 =** All 8 bits of the timeslot octet are inverted (1's complement) prior to transmission to the Remote Terminal Equipment. This selection is equivalent to executing the following logic operation with each timeslot 1 octet: **TX_TIME_SLOT_OCTET=(TE_TIME_SLOT_OCTET) XOR 0xFF** **0x2 =** The even bits of the timeslot octet are inverted prior to trans mission to the Remote Terminal Equipment. This selection is equivalent to executing the following logic operation: **TX_TIME_SLOT_OCTET=(TE_TIME_SLOT_OCTET) XOR 0xAA** **0x3 =** The odd bits of the time slot octet are inverted prior to trans mission to the Remote Terminal Equipment. This selection is equivalent to executing the following logic operation: **TX_TIME_SLOT_OCTET=(TE_TIME_SLOT_OCTET) XOR 0x55** **0x4** = The contents of the timeslot octet will be substituted with the 8 -bit value in Programmable User Code Register, prior to transmission to the Remote Terminal Equipment. **0x5 =** The contents of the timeslot octet will be substituted with the value 0xFF (BUSY) prior to transmission to the Remote Terminal Equipment. **0X6 =** The contents of the timeslot octet will be substituted with the value 0xD5 (VACANT 0V) prior to transmission to the Remote Terminal Equipment. **0X7 =** The BUSY TS(111#_####) code replaces the input data for transmission. (##### is Timeslot number.) **0X8 =** The BUSY 00 code replaces the input data for transmission **0X9 =** The A-Law Digital Milliwatt pattern replaces the input data for transmission. **0XA =** The µ-Law Digital Milliwatt pattern replaces the input data for transmission. **0xB** = The MSB (bit 1) of input data is inverted. **0xC** = All input data except MSB is inverted. **0xD** = PRBS, QRTS/X^{15} + X^{14} + 1. **0xE** = The input PCM data bit are unchanged. **0xF** = This is a D/E time slots. See transmit signaling and data link select register. (TSDLSR)

TABLE 79: USER CODE REGISTER 0 TO 31

REGISTER 81-112 USER CODE REGISTER 0 (UCR 0-31) HEX ADDRESS: 0XN320 TO 0XN33F

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0		R/W	0	Programmable User code.

TABLE 80: TRANSMIT SIGNALING CONTROL REGISTER X - E1 MODE

REGISTER 113-144 - E1 TRANSMIT SIGNALING CONTROL REGISTER X (TSCR) HEX ADDRESS: 0XN340 TO 0XN35F

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	A (x)	R/W	0 (1)	**Signaling bit A or x bit** A,B,C,D: These are programmable signaling information. *Note: Time slot 16 of frame 0 is controlled by TSCR0 (for 0 bits) and TSCR16 (for xyxx bits).*
6	B (y)	R/W	0 (0)	**Signaling bit B or y bit**
5	C (x)	R/W	0 (1)	**Signaling bit C or x bit**
4	D (x)	R/W	0 (1)	**Signaling bit D or x bit**
3	Reserved	-	-	**Reserved**
2	Reserved	-	-	**Reserved**
1	TxSIGSRC[1]	R/W	0	**Channel signaling control** These bits determine the selection of signaling conditioning. 00 = No signaling data is inserted into input PCM data (passthrough). 01 = Signaling data is inserted from TSCRs. 10 = Signaling data is inserted from TxOH input while TxMUXEN=0 and TxIMODE[1:0]=00, otherwise is inserted from TxSIG input. 11 = No signaling. For xyxx bits only, x's are from TSCR and y is the alarm condition.
0	TxSIGSRC[0]	R/W	0	

TABLE 81: TRANSMIT SIGNALING CONTROL REGISTER X - T1 MODE

REGISTER 113-144 - T1 TRANSMIT SIGNALING CONTROL REGISTER X (TSCR) (0-23) HEX ADDRESS: 0XN340 TO 0XN35F

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	A (x)	R/W	0 (1)	**Signaling bit A** A,B,C,D: These are programmable signaling information.
6	B (y)	R/W	0 (0)	**Signaling bit B**
5	C (x)	R/W	0 (1)	**Signaling bit C**
4	D (x)	R/W	0 (1)	**Signaling bit D**
3	Reserved	-	-	**Reserved**
2	Rob_Enb	R/W	0	**Robbed-bit signaling enable** This bit enables Robbed-bit signaling transmission. 0 = Robbed-bit is disabled. 1 = Robbed-bit is enabled
1	TxSIGSRC[1]	R/W	0	**Channel signaling control** These bits determine the selection of signaling conditioning. 00 = No signaling data is inserted into input PCM data. 01 = Signaling data is inserted from TSCRs. 10 = Signaling data is inserted from TxSig input. 11 = No signaling.
0	TxSIGSRC[0]	R/W	0	

TABLE 82: RECEIVE CHANNEL CONTROL REGISTER X (RCCR 0-31) - E1 MODE

REGISTER 145-176 E1 RECEIVE CHANNEL CONTROL REGISTER X (RCCR 0-31) HEX ADDRESS: 0XN360 TO 0XN37F

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	LAPDcntl	R/W	10	**LAPD Control** These bits select which LAPD controller is to be activated. 00 = LAPD1 01 = LAPD2 10 = RxDE[1:0] will determine the data source for the D/E Time Slots 11 = LAPD3
5-4	Reserved	-	-	**Reserved**
3	RxCOND[3]	R/W	0	**Selects Data Conditioning** These bits determines the type of data condition applying to input PCM data. 0x0 = The input PCM data is unchanged. 0x1 = All 8 bits of the PCM channel data are inverted. 0x2 = The even bits of input data are inverted. 0x3 = The odd bits of input data are inverted. 0x4 = Data in User Code Register shown in Table 3-27 replaces the input data. 0x5 = BUSY FF code (0xFF)) replaces the input data. 0x6 = BUSY 0Vcode (0xD5) replaces the input data. 0x7 = BUSY TS (111#_####) replaces the input data; ##### is Timeslot number. 0x8 = BUSY 00 (0x00) replaces the input data. 0x9 = The A-law digital milliwatt pattern replaces the input data. 0xA = The m-law digital milliwatt pattern replaces the input data. 0xB = The MSB (bit 1) of input data is inverted. 0xC = All input data except MSB is inverted. 0xD = PRBS, QRTS/X^{15} + X^{14} +1. 0xE = The input PCM data bit are unchanged. 0xF = This is a D/E time slots. See receive Signaling data link select register 12. (RS&DLSR)
2	RxCOND[2]	R/W	0	
1	RxCOND[1]	R/W	0	
0	RxCOND[0]	R/W	0	

TABLE 83: RECEIVE CHANNEL CONTROL REGISTER X (RCCR 0-23) - T1 MODE

REGISTER 145-176 - T1 RECEIVE CHANNEL CONTROL REGISTER X (RCCR 0-23) HEX ADDRESS: 0XN360 TO 0XN37F

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	LAPDcntl	R/W	10	**LAPD Control** These bits select which LAPD controller is to be activated. 00 = LAPD1 01 = LAPD2 10 = RxDE[1:0] will determine the data source for the D/E Time Slots 11 = LAPD3
5	RxZERO[1]	R/W	0	**Selects Type of Zero Suppression** These bits select the zero code suppression used. 00 = No zero code suppression is used. 01 = AT&T bit 7 stuffing is used. 10 = GTE zero code suppression is used. Bit 8 is stuffed in non-signaling frame. Otherwise, bit 7 is stuffed in signaling frame if the signaling bit is zero. 11 = DDS zero code suppression is applied.
4	RxZERO[0]	R/W	0	
3	RxCOND[3]	R/W	0	**Selects Data Conditioning** These bits determines the type of data condition applying to input PCM data. 0x0 = The input PCM data is unchanged. 0x1 = All 8 bits of the PCM channel data are inverted. 0x2 = The even bits of input data are inverted. 0x3 = The odd bits of input data are inverted. 0x4 = Data in User (IDLE) Code Register (Table 3?49) replaces the input data for transmission. 0x5 = BUSY code (0x7F)) replaces the input data for transmission. 0x6 = VACANT code (0xFF) replaces the input data for transmission. 0x7 = BUSY TS (111#_####) replaces the input data for transmission; ##### is Timeslot number. 0x8 = MOOF (0x1A) replaces the input data for transmission. 0x9 = The A-law digital milliwatt pattern replaces the input data. 0xA = The m-law digital milliwatt pattern replaces the input data. 0xB = The MSB (bit 1) of input data is inverted. 0xC = All input data except MSB is inverted. 0xD = PRBS, QRTS/$X^{15} + X^{14} + 1$. 0xE = The input PCM data bit are unchanged. 0xF = This is a D/E time slots. See receive signaling data link select register 12. (RS&DLSR)
2	RxCOND[2]	R/W	0	
1	RxCOND[1]	R/W	0	
0	RxCOND[0]	R/W	0	

TABLE 84: RECEIVE USER CODE REGISTER X (RUCR 0-31)

REGISTER 177-208 RECEIVE USER CODE REGISTER X (RUCR 0-31) HEX ADDRESS: 0XN380 TO 0XN39F

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RxUSER[7]	R/W	1	**Programmable USER code**
6	RxUSER[6]	R/W	1	
5	RxUSER[5]	R/W	1	
4	RxUSER[4]	R/W	1	
3	RxUSER[3]	R/W	1	
2	RxUSER[2]	R/W	1	
1	RxUSER[1]	R/W	1	
0	RxUSER[0]	R/W	1	

TABLE 85: RECEIVE SIGNALING CONTROL REGISTER X (RSCR) (0-31)

REGISTER 209-240 RECEIVE SIGNALING CONTROL REGISTER X (RSCR) (0-31) HEX ADDRESS: 0XN3A0 TO 0XN3BF

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
6	SIGC_ENB	R/W	0	**Signaling substitution enable** This bit enables signaling substitution. 0 = Substitution is disabled. 1 = Substitution is enabled.
5	OH_ENB	R/W	0	**Signaling OH interface output enable** This bit enables outputting signaling through overhead interface. The information in receive signaling array registers is output to receive overhead interface. 0 = Output is disabled. 1 = Output is enabled.
4	DEB_ENB	R/W	0	**Per-channel debounce enable** This bit enables signaling debounce feature. 0 = Debounce is disabled. 1 = Debounce is enabled.
3	RxSIGC[1]	R/W	0	**Signaling conditioning** These bits control per-channel signaling substitution. 00 = Substitutes all signaling bits with one. 01 = Enables 16-code (SIG16-A,B,C,D) signaling substitution. 10 = Enables 4-code (SIG4-A,B) signaling substitution. 11 = Enables 2-code (SIG2-A) signaling substitution.
2	RxSIGC[0]	R/W	0	
1	RxSIGE[1]	R/W	0	**Signaling extraction.** These bits determines the extracted signaling coding. 00 = No signaling is extracted. 01 = Extracts 16-code signaling. 10 = Extracts 4-code signaling. 11 = Extracts 2-code signaling.
0	RxSIGE[0]	R/W	0	

TABLE 86: RECEIVE SUBSTITUTION SIGNALING REGISTER (RSSR) E1 MODE

REGISTER 241-272 E1 MODE RECEIVE SUBSTITUTION SIGNALING REGISTER (RSSR) HEX ADDRESS 0XN3C0 TO 0XN3DF

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
6	SIG2-A	R/W	0	2-code signaling A
5	SIG4-B	R/W	0	4-code signaling B
4	SIG4-A	R/W	0	4-code signaling A
3	SIG16-D	R/W	0	16-code signaling D
2	SIG16-C	R/W	0	16-code signaling C
1	SIG16-B	R/W	0	16-code signaling B
0	SIG16-A	R/W	0	16-code signaling A

TABLE 87: LAPD BUFFER 0 CONTROL REGISTER

REGISTER 241-272 LAPD BUFFER 0 CONTROL REGISTER (LAPDBCR0) HEX ADDRESS: 0XN600 TO 0XN660

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	LAPD Buffer 0	R/W	0	**LAPD Buffer 0 (96-Bytes)** This register is used to transmit and receive LAPD messages within buffer 0 of the HDLC controller chosen in the LAPD Select Register (0xn11B). When writing to buffer 0, the message is inserted into the outgoing LAPD frame and the data cannot be retrieved. After detecting the Rx end of transfer interrupt (RxEOT), the extracted LAPD message is available to be read. ***NOTE:*** *When writing or reading from Buffer 0, the register is automatically incremented such that 0xn600 can be written to or read from continuously.*

TABLE 88: LAPD BUFFER 1 CONTROL REGISTER

REGISTER 241-272 LAPD BUFFER 0 CONTROL REGISTER (LAPDBCR1) HEX ADDRESS: 0XN700 TO 0XN760

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	LAPD Buffer 1	R/W	0	**LAPD Buffer 1 (96-Bytes)** This register is used to transmit and receive LAPD messages within buffer 1 of the HDLC controller chosen in the LAPD Select Register (0xn11B). When writing to buffer 1, the message is inserted into the outgoing LAPD frame and the data cannot be retrieved. After detecting the Rx end of transfer interrupt, the extracted LAPD message is available to be read. ***NOTE:*** *When writing or reading from Buffer 1, the register is automatically incremented such that 0xn700 can be written to or read from continuously.*

TABLE 89: RECEIVE SUBSTITUTION SIGNALING REGISTER (RSSR) T1 MODE

REGISTER 241-272 - T1 RECEIVE SUBSTITUTION SIGNALING REGISTER (RSSR) HEX ADDRESS: 0XN3C0 TO 0XN3DF

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Reserved	-	-	**Reserved**
3	SIG16-A, 4-A, 2-A	R/W	0	**16-code signaling A 4-code signaling A 2-code signaling A**
2	SIG16-B, 4-B, 2-A	R/W	0	**16-code signaling B 4-code signaling B 2-code signaling A**
1	SIG16-C, 4-A, 2-A	R/W	0	**16-code signaling C 4-code signaling A 2-code signaling A**
0	SIG16-D, 4-B, 2-A	R/W	0	**16-code signaling D 4-code signaling B 2-code signaling A**

TABLE 90: RECEIVE SIGNALING ARRAY REGISTER 0 TO 31

REGISTER 273-304 RECEIVE SIGNALING ARRAY REGISTER (RSAR 0-31) HEX ADDRESS: 0XN500 TO 0XN51F

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Reserved	-	-	**Reserved**
3	A	R/W	0	Reflects the most recently received signaling value (A,B,C,D) associated with timeslot 0 to 31. ***NOTE:*** *The content of this register only has meaning when the framer is using Channel Associated Signaling.*
2	B	R/W	0	
1	C	R/W	0	
0	D	R/W	0	

TABLE 91: PMON T1/E1 RECEIVE LINE CODE (BIPOLAR) VIOLATION COUNTER

REGISTER 305 PMON RECEIVE LINE CODE (BIPOLAR) VIOLATION COUNTER (RLCVCMSB) HEX ADDRESS: 0XN900

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Reserved	-	-	**Reserved**
3-0	RxLCV Count - High Byte	RUR	0	These four Reset Upon Read bits along with PMON Receive Line Code Violation Counter - LSB, provides a 12-bit representation of the number of LIne Code violations that have been detected by the Receive Framer block since the last read of these registers. Lower 8 bits. This register contains the lowest four bits within this 12 bit expression

TABLE 92: PMON T1/E1 RECEIVE LINE CODE (BIPOLAR) VIOLATION COUNTER

REGISTER 306 PMON RECEIVE LINE CODE (BIPOLAR) VIOLATION COUNTER (RLCVCLSB) HEX ADDRESS: 0XN901

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxLCV Count - Low Byte	RUR	0	These eight Reset Upon Read bits along with PMON Receive Line Code Violation Counter - MSB, provides 12-bit representation of the number of LIne Code violations that have been detected by Receive Framer Block since the last read of these registers. Upper 4 bits. This register contains the upper 8 bits within this 12 bit expression.

TABLE 93: PMON T1/E1 RECEIVE FRAMING ALIGNMENT BIT ERROR COUNTER

REGISTER 307 PMON RECEIVE FRAMING ALIGNMENT ERROR COUNTER (RFAECLSB) HEX ADDRESS: 0XN902

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Framing Alignment Error Count - High Byte	RUR	0	These eight Reset Upon Read bits along with PMON E1 Receive Framing Alignment Bit Error Counter- LSB, provides a 12-bit representation of the number of Framing Alignment errors that have been detected by Receive E1 Framer number n since the last read of these registers. This register contains the upper 8bits within this 12-bit expression.

TABLE 94: PMON T1/E1 RECEIVE FRAMING ALIGNMENT BIT ERROR COUNTER

REGISTER 308 PMON RECEIVE FRAMING ALIGNMENT BIT ERROR COUNTER (RFAB-ECMSB) HEX ADDRESS: 0XN903

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Reserved	-	-	**Reserved**
3-0	Framing Alignment Error Count - Low Byte	RUR	0	These four Reset Upon Read bits along with PMON E1 Receive Framing Alignment Bit Error Counter- MSB, provides 12-bit representation of the number of Framing Alignment errors that have been detected by Receive E1 Framer Block since the last read of these register. This register contains the lowest four bits within this 12-bit expression

TABLE 95: PMON T1/E1 RECEIVE SEVERELY ERRORED FRAME COUNTER

REGISTER 309 PMON RECEIVE SEVERELY ERRORED FRAME COUNTER (RSEFC) HEX ADDRESS: 0XN904

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Severely Errored Frame Count	RUR	0	Severely Errored 8-bit frame accumulation Counter ***Note: A severely errored frame event is defined as the occurrence of two consecutive errored frame alignment signals that are not responsible for loss of frame alignment.***

TABLE 96: PMON T1/E1 RECEIVE CRC-4 BLOCK ERROR COUNTER - MSB

REGISTER 310 PMON RECEIVE SYNCHRONIZATION BIT BLOCK ERROR COUNTER (RSBBECMSB) HEX ADDRESS: 0XN905

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	CRC-4 Block Error Count - High Byte	RUR	0	These eight Reset Upon Read bits along with PMON E1 Receive CRC-4 Block Error Counter - LSB, provides a 10-bit representation of the number of CRC-4 Block errors detected by Receive E1 Framer Block since the last read of these registers. This register contains the upper eight bits of this 10 bit expression

TABLE 97: PMON T1/E1 RECEIVE CRC-4 BLOCK ERROR COUNTER - LSB

REGISTER 311 PMON RECEIVE SYNCHRONIZATION BIT BLOCK ERROR COUNTER (RSBBECLSB) HEX ADDRESS: 0XN907

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-2	Reserved	-	-	**Reserved**
1-0	CRC-4 Block Error Count - Low Byte	RUR	0	These two Reset upon Read bits along with PMON E1 Receive CRC-4 Block Error Counter - MSB, provides a 10-bit representation of the number of CRC-4 Block errors that have been detected by a Receive E1 Framer Block since the last read of these registers. This register contains the lower two bits within this 10 bit expression. *Note: Counter contains the 10-bit synchronization bit error event. A synchronization bit error event is defined as a CRC-4 error received. Counter is disabled during loss of sync at either the Frame/FAS or ESF/CRC4 level, but it will not be disabled if loss of multiframe sync occurs at the CAS level.*

TABLE 98: PMON T1/E1 RECEIVE FAR-END BLOCK ERROR COUNTER - MSB

REGISTER 312 PMON RECEIVE FAR-END BLOCK ERROR COUNTER (E1RFEBECMSB) HEX ADDRESS: 0XN908

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Far-End Block Error Count - High Byte	RUR	0	These eight Reset Upon Read bits along with PMON E1 Receive Far-End Block Error Counter - LSB, provides a 10-bit representation of the number of Far End Block Error events that have been detected by the Receive E1 Framer Block since the last read of these registers. This register contains the upper eight bits within this 10 bit expression.

TABLE 99: PMON T1/E1 RECEIVE FAR END BLOCK ERROR COUNTER

REGISTER 313 PMON RECEIVE FAR END BLOCK ERROR COUNTER (RFEBECLSB) HEX ADDRESS: 0XN908

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-2	Reserved	-	-	**Reserved**
1-0	Far-End Block Error Count -Low Byte	RUR	0	These two Reset Upon Read bits along with PMON E1 Receive Far-End Block Error Counter - MSB, provides a 10-bit representation of the number of Far End Block Error events that have been detected by the Receive E1 Framer Block since the last read of these registers. This register contains the lower two bits within this 10 bit expression. ***Note: Counter contains the 10-bit far-end block error event. Counter will increment once each time the received E-bit is set to zero. The counter is disabled during loss of sync at either the FAS or CRC-4 level and it will continue to count if loss of multiframe sync occurs at the CAS level.***

TABLE 100: PMON T1/E1 RECEIVE SLIP COUNTER

REGISTER 314 PMON RECEIVE SLIP COUNTER (RSC) HEX ADDRESS: 0XN909

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Slip Count	RUR	0	Note: counter contains the 8-bit receive buffer slip event. A slip event is defined as a replication or deletion of a T1/E1 frame by the receiving slip buffer. ***Note: A 12 bit counter which counts the occurrence of a bipolar violation on the receive data line. This counter is of sufficient length so that the probability of counter saturation over a one second interval at a 10 -3-Bit Error Rate (BER) is less than 0.001%.***

TABLE 101: PMON T1/E1 RECEIVE LOSS OF FRAME COUNTER

REGISTER 315 PMON RECEIVE LOSS OF FRAME COUNTER (RLFC) HEX ADDRESS: 0XN90A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Loss of Frame Counts	RUR	0	***Note: LOFC is a count of the number of times a "Loss Of FAS Frame" has been declared. This counter provides the capability to measure an accumulation of short failure events.***

TABLE 102: PMON T1/E1 RECEIVE CHANGE OF FRAME ALIGNMENT COUNTER

REGISTER 316 PMON RECEIVE CHANGE OF FRAME ALIGNMENT COUNTER (RCFAC) HEX ADDRESS: 0XN90B

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	COFA Count	RUR	0	Change of Frame Alignment Accumulation counter. ***Note: COFA is declared when the newly-locked framing is different from the one offered by off-line framer.***

TABLE 103: PMON LAPD T1/E1 FRAME CHECK SEQUENCE ERROR COUNTER

REGISTER 317 PMON LAPD FRAME CHECK SEQUENCE ERROR COUNTER (FCSEC) HEX ADDRESS: 0XN90C

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	FCS Error Count	RUR	0	Frame Check Sequence error Accumulation Counter. ***Note: Counter accumulates the times of occurrence of receive frame check sequence error detected by LAPD controller.***

TABLE 104: T1/E1 PRBS BIT ERROR COUNTER MSB

REGISTER 318 **T1/E1 PRBS BIT ERROR COUNTER MSB** **HEX ADDRESS: 0XN90D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	PRBSE[15]	RUR	0	**Most significant bits of PRBS bit error Accumulation counter**
6	PRBSE[14]	RUR	0	
5	PRBSE[13]	RUR	0	
4	PRBSE[12]	RUR	0	
3	PRBSE[11]	RUR	0	
2	PRBSE[10]	RUR	0	
1	PRBSE[9]	RUR	0	
0	PRBSE[8]	RUR	0	

TABLE 105: T1/E1 PRBS BIT ERROR COUNTER LSB

REGISTER 319 **T1/E1 PRBS BIT ERROR COUNTER LSB** **HEX ADDRESS: 0XN90E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	PRBSE[7]	RUR	0	**Least significant byte of PRBS bit error accumulation counter.**
6	PRBSE[6]	RUR	0	
5	PRBSE[5]	RUR	0	
4	PRBSE[4]	RUR	0	
3	PRBSE[3]	RUR	0	
2	PRBSE[2]	RUR	0	
1	PRBSE[1]	RUR	0	
0	PRBSE[0]	RUR	0	

TABLE 106: T1/E1 TRANSMIT SLIP COUNTER

REGISTER 320 **T1/E1 TRANSMIT SLIP COUNTER (T1/E1TSC)** **HEX ADDRESS: 0XN90F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSLIP[7]	RUR	0	**Slip accumulation counter.**
6	TxSLIP[6]	RUR	0	
5	TxSLIP[5]	RUR	0	
4	TxSLIP[4]	RUR	0	
3	TxSLIP[3]	RUR	0	
2	TxSLIP[2]	RUR	0	
1	TxSLIP[1]	RUR	0	
0	TxSLIP[0]	RUR	0	

TABLE 107: BLOCK INTERRUPT STATUS REGISTER

REGISTER 321 **BLOCK INTERRUPT STATUS REGISTER (BISR)** **HEX ADDRESS: 0XNB00**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Sa6	RO	0	**Sa6 Interrupt Status**
6	LBCODE	RO	0	**Loopback Code Interrupt**
5	RxClkLOS	RUR	0	**RxClk Los Interrupt Status** Indicates if Framer n has experienced a Loss of Recovered Clock interrupt since last read of this register. 0 = Loss of Recovered Clock interrupt has not occurred since last read of this register 1 = Loss of Recovered Clock interrupt has occurred since last read of this register.
4	ONESEC	RUR	0	**One Second Interrupt Status** Indicates if the XRT86L34 has experienced a One Second interrupt since the last read of this register. 0 = No outstanding One Second interrupts awaiting service 1 = Outstanding One Second interrupt awaits service
3	HDLC	RO	0	**HDLC Block Interrupt Status** Indicates if the HDLC block has an interrupt request awaiting service. 0 = No outstanding interrupt requests awaiting service 1 = HDLC Block has an interrupt request awaiting service. Interrupt Service routine should branch to and read Data LInk Status Register (address xA,06). ***NOTE:*** *This bit-field will be reset to 0 after the microprocessor has performed a read to the Data Link Status Register.*
2	SLIP	RO	0	**Slip Buffer Block Interrupt Status** Indicates if the Slip Buffer block has any outstanding interrupt requests awaiting service. 0 = No outstanding interrupts awaiting service 1 = Slip Buffer block has an interrupt awaiting service. Interrupt Service routine should branch to and read Slip Buffer Interrupt Status register (address 0xXA,0x09. ***NOTE:*** *This bit-field will be reset to 0 after the microprocessor has performed a read of the Slip Buffer Interrupt Status Register.*
1	ALARM	RO	0	**Alarm & Error Block Interrupt Status** Indicates if the Alarm & Error Block has any outstanding interrupts that are awaiting service. 0 = No outstanding interrupts awaiting service 1 = Alarm & Error Block has an interrupt awaiting service. Interrupt SerStatus Register (address xA,02) ***NOTE:*** *This bit-field will be reset to 0 after the microprocessor has performed a read of the Alarm & Error Interrupt Status register.*
0	T1/E1 FRAME	RO	0	**T1/E1 Framer Block Interrupt Status** Indicates if an T1/E1 Frame Status interrupt request is awaiting service. 0 = No T1/E1 Frame Status interrupt is pending 1 = T1/E1 Framer Status interrupt is awaiting service.

TABLE 108: BLOCK INTERRUPT ENABLE REGISTER

REGISTER 322 **BLOCK INTERRUPT ENABLE REGISTER (BIER)** **HEX ADDRESS: 0XNB01**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SA6_ENB	R/W	0	**SA6 interrupt enable**
6	LBCODE_ENB	R/W	0	**Loopback code interrupt enable**
5	RXCLKLOSS	R/W	0	**RxLineClk Loss Interrupt Enable** 0 = Disables interrupt 1 = Enables interrupt
4	ONESEC_ENB	R/W	0	**One Second Interrupt Enable** 0 = Disables interrupt 1 = Enables Interrupt
3	HDLC_ENB	R/W	0	**HDLC Block Interrupt Enable** 0 = Disables all HDLC Block interrupts 1 = Enables HDLC Block (for interrupt generation) at the block level
2	SLIP_ENB	R/W	0	**Slip Buffer Block Interrupt Enable** 0 = Disables all Slip Buffer Block Interrupts 1 = Enables Slip Buffer Block at the block level
1	ALARM_ENB	R/W	0	**Alarm & Error Block Interrupt Enable** 0 = Disables all Alarm & Error Block interrupts 1 = Enables Alarm & Error block at the block level
0	T1/E1FRAME_ENB	R/W	0	**T1/E1 Frame Block Enable** 0 = Disables all Frame Block interrupts 1 = Enables the Frame Block at the block level

TABLE 109: ALARM & ERROR INTERRUPT STATUS REGISTER

REGISTER 323 **ALARM & ERROR INTERRUPT STATUS REGISTER (AEISR)** **HEX ADDRESS: 0XNB02**

BIT	MODE	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	E1/T1	RxLOF State	RO	0	**Receive Loss Of Frame State** Reflects a current Loss of Framing condition as detected by the Receive T1/E1 Framer. 0 = Receive Framer not declaring Loss of Framing condition 1 = Receive Framer declaring Loss of Framing condition
6	E1/T1	RxAIS State	RO	0	**Receive Alarm Indication Status State** This Read Only bit field indicates whether or not the receive T1/E1 Frame is currently detecting an AIS pattern in the incoming data stream. 0 = Receive Framer not detecting AIS pattern in incoming T1/E1 data stream 1 = Receive Framer detecting AIS pattern in incoming T1/E1 data stream
5	E1	RxMYEL Status	RUR	0	**Receipt of CAS Multiframe Yellow Alarm Interrupt Status.** The Receive E1 Framer will set this bit-field to 1 if it detects the CAS Multiframe Yellow Alarm in the incoming E1 data stream. 0 = Receipt of CAS Multiframe Yellow Alarm interrupt has not occurred since the last read of this register. 1 = Receipt of CAS Multiframe Yellow Alarm interrupt has occurred since the last read of this register.
5	T1	RxYEL_State	R	0	**Yellow Alarm State** Indicates a yellow alarm has been received. 0 = No yellow Alarm is Received 1 = Yellow alarm is received

TABLE 109: ALARM & ERROR INTERRUPT STATUS REGISTER

REGISTER 323 **ALARM & ERROR INTERRUPT STATUS REGISTER (AEISR)** **HEX ADDRESS: 0XNB02**

BIT	MODE	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	E1/T1	LOS Status	RUR	0	**Loss of Signal Interrupt Status.** The Receive E1 Framer will set this bit-field to 1 if it detects a consecutive string of 0's at the RxPOX_n and RxNEG_n input pins for 32 bit period. 0 = LOS Interrupt has not occurred since the last read of this register 1 = LOS Interrupt has occurred since the last read of this register
3	E1/T1	LCV Int Status	RUR	0	**Line Code Violation Interrupt Status**. The Receive LIU Interrupt Block will set this bit-field to 1 if it detects a Line Code Violation in the incoming E1 data stream. 0 = Line Code Violation interrupt has not occurred since the last read of this register. 1 = Line Code Violation interrupt has occurred since the last read of this register.
2	E1/T1	RxLOF Status	RUR	0	**Change in Receive Loss of Frame Condition Interrupt Status**. The receive E1 Framer block will set this bit-field to 1 if the Receive E1 framer has transition into the In-Frame condition or Loss of Frame condition. 0 = Change in RxLOF Interrupt has not occurred since the last read of this register 1 = Change in RxLOF Interrupt has occurred since the last read of this register
1	E1/T1	RxAIS Status	RUR	0	**Change in Receive AIS Condition Interrupt Status**. The Receive E1 Framer will generate the Change in AIS Condition interrupt if it starts to detect the AIS pattern in the incoming data stream or if it no longer detects the AIS pattern in the incoming data stream. 0 = Change in AIS Condition Interrupt has not occurred since the last read of this register 1 = Change in AIS Condition Interrupt has occurred since the last read of this register
0	E1/T1	RxYEL Status	RUR	0	**Receipt of FAS Frame Yellow Alarm Interrupt Status.** The Receive E1 Framer will generate the FAS Frame Yellow Alarm interrupt if it detects the FAS Frame Yellow Alarm in the incoming E1 data stream. 0 = FAS Frame Yellow Alarm interrupt has not occurred 1 = FAS Frame Yellow Alarm interrupt has occurred since the last read of this register.

TABLE 110: ALARM & ERROR INTERRUPT ENABLE REGISTER - E1 MODE

REGISTER 324 E1 MODE ALARM & ERROR INTERRUPT ENABLE REGISTER (AEIER) HEX ADDRESS: 0XNB03

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	Reserved	-	-	**Reserved**
5	RxMYEL ENB	R/W	0	**Multiframe Yellow alarm state change interrupt enable** Enables the generation of an interrupt when the yellow alarm has been received. 0 = A multiframe yellow alarm (y bit equals to 1) will not generate an interrupt. 1 = A multiframe yellow alarm will generate an interrupt.
4	LOS ENB	R/W	0	**Loss Of Signal interrupt enable** Enables the interrupt generation when the loss of signal has been detected. 0 = Disables the interrupt generation of LOS detection. 1 = Enables the interrupt generation of LOS detection
3	BPV ENB	R/W	0	**Bipolar violation interrupt enable** Enables the interrupt generation of a bipolar violation. 0 = Disables the interrupt generation of a bipolar violation condition. 1 = Enables the interrupt generation of a bipolar violation condition.
2	RxLOF ENB	R/W	0	**Red alarm state change interrupt enable** Enables the interrupt generation when the change state of red alarm has been detected. 0 = Disables the interrupt generation of loss of frame detection. 1 = Enables the interrupt generation of loss of frame detection.
1	RxAIS ENB	R/W	0	**AIS state change interrupt enable** Enables the generation of an interrupt when the change state of AIS event has been detected. 0 = The state change of AIS does not generate an interrupt. 1 = The state change of AIS does generate an interrupt.
0	RxYEL ENB	R/W	0	**Yellow alarm state change interrupt enable** Enables the generation of an interrupt when the yellow alarm has been received. 0 = A yellow alarm (A bit equals to 1) will not generate an interrupt. 1 = A yellow alarm will generate an interrupt

TABLE 111: ALARM & ERROR INTERRUPT ENABLE REGISTER -T1 MODE

REGISTER 324 T1 MODE **ALARM & ERROR INTERRUPT ENABLE REGISTER (AEIER)** **HEX ADDRESS: 0XNB03**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-5	Reserved	-	-	**Reserved**
4	LOS ENB	R/W	0	**Loss Of Signal interrupt enable** Enables the interrupt generation when the loss of signal has been detected. 0 = Disables the interrupt generation of LOS detection. 1 = Enables the interrupt generation of LOS detection.
3	BPV ENB	R/W	0	**Bipolar violation interrupt enable** Enables the interrupt generation of a bipolar violation. 0 = Disables the interrupt generation of a bipolar violation condition. 1 = Enables the interrupt generation of a bipolar violation condition.
2	RxRED ENB	R/W	0	**Red Alarm State Change Interrupt Enable** Enables the interrupt generation when the change state of red alarm has been detected. 0 = Disables the interrupt generation of framing mimic detection. 1 = Enables the interrupt generation of framing mimic detection.
1	RxAIS ENB	R/W	0	**AIS state change interrupt enable** Enable the generation of an interrupt when the change state of AIS event has been detected. 0 = The state change of AIS does not generate an interrupt. 1 = The state change of AIS does generate an interrupt
0	RxYEL ENB	R/W	0	**Yellow alarm state change interrupt enable** Enables the generation of an interrupt when the change state of yellow alarm has been detected. 0 = Any state change of yellow alarm will not generate an interrupt. 1 = Changing state of yellow alarm will generate an interrupt.

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TABLE 112: FRAMER INTERRUPT STATUS REGISTER E1 MODE

REGISTER 325 E1 MODE **FRAMER INTERRUPT STATUS REGISTER (FISR)** **HEX ADDRESS: 0XNB04**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	COMFA Status **E1 Only**	RUR	0	**Change in CAS Multiframe Alignment Interrupt Status** 0 = Change in CAS Multiframe Alignment Interrupt has not occurred since the last read of this register 1 = Change in CAS Multiframe Alignment Interrupt has occurred since the last read of this register
6	NBIT Status **E1 Only**	RUR	0	**Change in National Bits Interrupt Status** The Receive E1 Framer will generate this interrupt if it has detected a change in the National Bits in the incoming non-FAS E1 Frames. 0 = Change in National Bits Interrupt has not occurred since the last read of this register 1 = Change in National Bits Interrupt has occurred since the last read of this register.
5	SIG Status	RUR	0	**Change in CAS Signaling Interrupt Status** The Receive E1 Framer will generate this interrupt if it detects a change in the four-bit signaling values for any one of the 30 voice channels. 0 = Change in CAS Signaling Interrupt has not occurred since the last read of this register 1 = Change in CAS Signaling Interrupt has occurred since the last read of this register.
4	COFA Status	RUR	0	**Change of FAS Frame Alignment Interrupt Status** 0 = Change in FAS Frame Alignment interrupt has not occurred since the last read of this register 1 = Change in FAS Frame Alignment interrupt has occurred since the last read of this register
3	IF Status	RUR	0	**Change of In Frame Condition Interrupt Status**
2	FMD Status	RUR	0	
1	Sync Error Status	RUR	0	**CRC-4 Error Interrupt Status.** The Receive E1Framer will declare this interrupt if it detects an error in the CRC-4 bits within a given sub-multiframe. 0 = Sync Error has not occurred since the last read of this register 1 = Sync Error has occurred since the last read of this register
0	Framing Error Status	RUR	0	0 = Framing Bit Error interrupt has not occurred since the last read of this register 1 = Framing Bit Error interrupt has occurred since the last read of this register

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TABLE 113: FRAMER INTERRUPT STATUS REGISTER T1 MODE

REGISTER 325 T1 MODE **FRAMER INTERRUPT STATUS REGISTER (FISR)** **HEX ADDRESS: 0XNB04**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
5	SIG	RUR/ WC	0	**Signaling updated** This bit indicates the occurrence of state change of any signaling channel. 0 = No state change occurs of any signaling. 1 = Change of signaling state occurs.
4	COFA	RUR/ WC	0	**Change of Frame Alignment** This bit is used to indicate that the receive synchronization signal has changed alignment with respect to its last multiframe position. 0 = No COFA occurs. 1 = COFA occurs.
3	IF	RUR/ WC	0	**In-frame state** This bit indicates the occurrence of state change of in-frame indication. 0 = No state change occurs of in-frame indication. 1 = In-frame indication has changed state.
2	FMD	RUR/ WC	0	**Frame Mimic state change** This bit indicates the occurrence of state change of framing mimic detection. 0 = No state change occurs of framing mimic detection. 1 = Framing mimic detection has changed state.
1	SE	RUR/ WC	0	**Synchronization bit error** This bit indicates the occurrence of synchronization bit error event. 0 = No synchronization bit error occurs. 1 = Synchronization bit error occurs.
0	FE	RUR/ WC	0	**Framing error** This bit is used to indicate that one or more frame alignment bit error have occurred. This bit doesn't not necessarily indicate that synchronization has been lost. 0 = No framing bit error occurs. 1 = Framing bit error occurs.

TABLE 114: FRAMER INTERRUPT ENABLE REGISTER E1 MODE

REGISTER 326 E1 MODE **FRAMER INTERRUPT ENABLE REGISTER (FIER)** **HEX ADDRESS: 0XNB05**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	COMFA ENB - E1 Only	R/W	0	**Change in CAS Multiframe Alignment Interrupt Enable - E1 only** 0 = Disables the Change in CAS Multiframe Alignment Interrupt 1 = Enables the Change in CAS Multiframe Alignment Interrupt
6	NBIT ENB - E1 Only	R/W	0	**Change in National Bits Interrupt Enable - E1 only** 0 = Disables the Change in National Bits Interrupt 1 = Enables the Change in National Bits Interrupt
5	SIG ENB	R/W	0	**Change in CAS Signaling Bits Interrupt Enable** 0 = Disables the Change in CAS Signaling Bits Interrupt Enable 1 = Enables the Change in CAS Signaling Bits Interrupt Enable
4	COFA ENB	R/W	0	**Change in FAS Framing Alignment Interrupt Enable** 0 = Disables the Change in FAS Framing Alignment Interrupt Enable 1 = Enables the Change in FAS Framing Alignment Interrupt Enable
3	IF ENB	R/w	0	**IF Enable**
2	FMD ENB	R/W	0	**FMD Enable**
1	SE_ENB	R/W	0	**Sync (CRC-4) Error Interrupt Enable** 0 = Sync Error Interrupt Disabled 1 = Sync Error Interrupt Enabled
0	FE_ENB	R/W0	0	**Framing Bit Error Interrupt Enable** 0 = Disables the Framing Bit Error Interrupt 1 = Enables the Framing Bit Error Interrupt

TABLE 115: FRAMER INTERRUPT ENABLE REGISTER T1 MODE

REGISTER 326 T1 MODE **FRAMER INTERRUPT ENABLE REGISTER (FIER)** **HEX ADDRESS: 0XNB05**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
5	SIG_ENB	R/W	0	This bits enables the generation of an interrupt when any signaling channel has changed state. 0 = Change of signaling data does not generate an interrupt. 1 = Change of signaling data does generate an interrupt.
4	COFA_ENB	R/W	0	Setting this bit will enable the interrupt generation when the frame search logic determines that frame alignment has been reached and that the new alignment differs from the previous alignment. 0 = Disables the interrupt generation of COFA detection. 1 = Enables the interrupt generation of COFA detection.
3	IF_ENB	R/W	0	**IF Enable** Setting this bit will enable the interrupt generation of an in-frame recognition. 0 = Disables the interrupt generation of an in-frame detection. 1 = Enables the interrupt generation of an in-frame detection.
2	FMD_ENB	R/W	0	**FMD Enable** Setting this bit will enable the interrupt generation when the frame search logic detects the presence of framing bit mimics. 0 = Disables the interrupt generation of framing mimic detection. 1 = Enables the interrupt generation of framing mimic detection.
1	SE_ENB	R/W	0	**Sync (CRC-4) Error Interrupt Enable** Setting this bit will enable the generation of an interrupt when a synchronization bit error event has been detected. A synchronization bit error event is defined as CRC-4 error. 0 = The detection of synchronization bit errors does not generate an interrupt. 1 = The detection of synchronization bit errors does generate an interrupt
0	FE_ENB	R/W0	0	**Framing Bit Error Interrupt Enable** This bits enables the generation of an interrupt when a framing bit error has been detected. 0 = Any error in the framing bits does not generate an interrupt. 1 = A error in the framing bits does generate an interrupt.

TABLE 116: DATA LINK STATUS REGISTER 1

REGISTER 327 **DATA LINK STATUS REGISTER 1 (DLSR1)** **HEX ADDRESS: 0XNB06**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	MSG TYPE	RUR	0	**HDLC1 Message Type Identifier** Indicates type of data link message received by Rx HDLC1 Controller 0 = Bit Oriented Signaling type data link message received 1 = Message Oriented Signaling type data link message received
6	TxSOT	RUR	0	**Transmit HDLC1 Start of Transmission Interrupt Status** Indicates if the Transmit HDLC1 Start of Transmission Interrupt has occurred since the last read of this register. Transmit HDLC1 Controller will declare this interrupt when it has started to transmit a data link message. 0 = Transmit HDLC1 Start of Transmission interrupt has not occurred since the last read of this register 1 = Transmit HDLC1 Start of Transmission interrupt has occurred since the last read of this register.
5	RxSOT	RUR	0	**Receive HDLC1 Start of Reception Interrupt Status** Indicates if the Receive HDLC1 Start of Reception interrupt has occurred since the last read of this register. Receive HDLC1 Controller will declare this interrupt when it has started to receive a data link message. 0 = Receive HDLC1 Start of Reception interrupt has not occurred since the last read of this register 1 = Receive HDLC1 Start of Reception interrupt has occurred since the last read of this register
4	TxEOT	RUR	0	**Transmit HDLC1 End of Transmission Interrupt Status** Indicates if the Transmit HDLC1 End of Transmission Interrupt has occurred since the last read of this register. Transmit HDLC1 Controller will declare this interrupt when it has completed its transmission of a data link message. 0 = Transmit HDLC1 End of Transmission interrupt has not occurred since the last read of this register 1 = Transmit HDLC1 End of Transmission interrupt has occurred since the last read of this register
3	RxEOT	RUR	0	**Receive HDLC1 Controller End of Reception Interrupt Status** Indicates if Receive HDLC1 End of Reception Interrupt has occurred since the last read of this register. Receive HDLC1 Controller will declare this interrupt once it has completely received a full data link message. 0 = Receive HDLC1 End of Reception interrupt has not occurred since the last read of this register 1 = Receive HDLC1 End of Reception Interrupt has occurred since the last read of this register
2	FCS Error	RUR	0	**FCS Error Interrupt Status** Indicates if the FCS Error Interrupt has occurred since the last read of this register. Receive HDLC1 Controller will declare this interrupt if it detects an error in the most recently received data message. 0 = FCS Error interrupt has not occurred since last read of this register 1 = FCS Error interrupt has occurred since last read of this register
1	Rx ABORT	RUR	0	**Receipt of Abort Sequence Interrupt Status** Indicates if the Receipt of Abort interrupt has occurred since last read of this register. Receive HDLC1 Controller will declare this interrupt if it detects a string of seven (7) consecutive 1's in the incoming data link channel. 0 = Receipt of Abort Sequence interrupt has not occurred since last read of this register 1 = Receipt of Abort Sequence interrupt has occurred since last read of this register

TABLE 116: DATA LINK STATUS REGISTER 1

REGISTER 327 **DATA LINK STATUS REGISTER 1 (DLSR1)** **HEX ADDRESS: 0XNB06**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	RxIDLE	RUR	0	**Receipt of Idle Sequence Interrupt Status** Indicates if the Receipt of Idle Sequence interrupt has occurred since the last read of this register. The Receive HDLC1 Controller will declare this interrupt if it detects the flag sequence octet (0x7E) in the incoming data link channel. 0 = Receipt of Idle Sequence interrupt has not occurred since last read of this register 1 = Receipt of Idle Sequence interrupt has occurred since last read of this register.

TABLE 117: DATA LINK INTERRUPT ENABLE REGISTER 1

REGISTER 328 **DATA LINK INTERRUPT ENABLE REGISTER 1 (DLIER1)** **HEX ADDRESS: 0XNB07**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	**Reserved**
6	TxSOT ENB	R/W	0	**Transmit HDLC1 Start of Transmission Interrupt Enable** 0 = Disables the Transmit HDLC1 Start of Transmission interrupt 1 = Enables the Transmit HDLC1 Start of Transmission interrupt
5	RxSOT ENB	R/W	0	**Receive HDLC1 Start of Reception Interrupt Enable** 0 = Disables the Receive HDLC1 Start of Reception interrupt 1 = Enables the Receive HDLC1 Start of Reception interrupt
4	TxEOT ENB	R/W	0	**Transmit HDLC1 End of Transmission Interrupt Enable** 0 = Disables the Transmit HDLC1 End of Transmission interrupt 1 = Enables the Transmit HDLC1 End of Transmission interrupt
3	RxEOT ENB	R/W	0	**Receive HDLC1 End of Reception Interrupt Enable** 0 = Disables the Receive HDLC1 End of Reception interrupt 1 = Enables the Receive HDLC1 End of Reception interrupt
2	FCS ERR ENB	R/W	0	**FCS Error Interrupt Enable** 0 = Disables FCS Error interrupt 1 = Enables FCS Error interrupt
1	RxABORT ENB	R/W	0	**Receipt of Abort Sequence Interrupt Enable** 0 = Disables Receipt of Abort Sequence interrupt 1 = Enables Receive of Abort Sequence interrupt
0	RxIDLE ENB	R/W	0	**Receipt of Idle Sequence Interrupt Enable** 0 = Disables Receipt of Idle Sequence interrupt 1 = Enables Receipt of Idle Sequence interrupt

TABLE 118: SLIP BUFFER INTERRUPT STATUS REGISTER (SBSR)

REGISTER 329 **SLIP BUFFER INTERRUPT STATUS REGISTER (SBSR)** **HEX ADDRESS: 0XNB08**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSB_FULL	RUR/ WC	0	**Slip buffer fills & a frame is deleted** This bit is set when the elastic store fills and a frame is deleted.
6	TxSB_EMPT	RUR/ WC	0	**Slip buffer empties and a frame is repeated** This bit is set when the elastic store empties and a frame is repeated.
5	TxSB_SLIP	RUR/ WC	0	**Receive slips** This bit is set when the slip buffer slips.
4	96LOCK	R	0	**SLC®96 is in sync** This bit indicates that SLC96 is in sync.
3	MLOCK	R	0	**Multiframe is in Sync** This bit indicates that multiframe is in sync.
2	SB_FULL	RUR/ WC	0	**Slip buffer fills & a frame is deleted** This bit is set when the elastic store fills and a frame is deleted.
1	SB_EMPT	RUR/ WC	0	**Slip buffer empties and a frame is repeated** This bit is set when the elastic store empties and a frame is repeated.
0	SB_SLIP	RUR/ WC	0	**Receive slips** This bit is set when the slip buffer slips.

TABLE 119: SLIP BUFFER INTERRUPT ENABLE REGISTER (SBIER)

REGISTER 330 **SLIP BUFFER INTERRUPT ENABLE REGISTER (SBIER)** **HEX ADDRESS: 0XNB09**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxFULL_ENB	R/W	0	**Tx Interrupt Enable bit for slip buffer full** Setting this bit enables interrupt when the elastic store fills and a frame is deleted.
6	TxEMPT_ENB	R/W	0	**Tx Interrupt Enable bit for slip buffer empty** Setting this bit enables interrupt when the elastic store empties and a frame is repeated.
5	TxSLIP_ENB	R/W	0	**Tx Interrupt Enable bit for Slip buffer slip** Setting this bit enables interrupt when the slip buffer slips.
4-3	Reserved	-	-	**Reserved**
2	FULL_ENB	R/W	0	**Interrupt Enable bit for slip buffer full** Setting this bit enables interrupt when the elastic store fills and a frame is deleted.
1	EMPT_ENB	R/W	0	**Interrupt Enable bit for slip buffer empty** Setting this bit enables interrupt when the elastic store empties and a frame is repeated.
0	SLIP_ENB	R/W	0	**Interrupt Enable bit for Slip buffer slip** Setting this bit enables interrupt when the slip buffer slips.

TABLE 120: RECEIVE LOOPBACK CODE INTERRUPT AND STATUS REGISTER (RLCISR)

REGISTER 331 RECEIVE LOOPBACK CODE INTERRUPT AND STATUS REGISTER (RLCISR) HEX ADDRESS: 0XNB0A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	AUXPSTAT	R	0	**AUXP state** This bit indicates the status of receive AUXP pattern.
6	AUXPINT	RUR/WC	0	**AUXP state change interrupt** 1 = Indicates the receive AUXP status has changed.
5	NONCRCSTAT	R	0	**CRC-4-to-non-CRC-4 interworking status** This bit indicates the status of CRC-4 interworking status in MODENB mode. 1 = CRC-4-to-non-CRC-4 interworking is established.
4	NONCRCINT	RUR/WC	0	**CRC-4-to-non-CRC-4 interworking interrupt** 1 = Indicates the interworking status has changed.
3	RXASTAT	R	0	**Receive activation status** This bit indicates the status of receive activation process. 1 = Indicates the loopback code activation is received.
2	RXDSTAT	R	0	**Receive deactivation status** This bit indicates the status of receive deactivation process. 1 = Indicates the loopback code deactivation is received.
1	RXAINT	RUR/WC	0	**Receive activation interrupt** 1 = Indicates the loopback code activation status has changed.
0	RXDINT	RUR/WC	0	**Receive deactivation interrupt** 1 = Indicates the loopback code deactivation status has changed.

TABLE 121: RECEIVE LOOPBACK CODE INTERRUPT ENABLE REGISTER (RLCIER)

REGISTER 332 RECEIVE LOOPBACK CODE INTERRUPT ENABLE REGISTER (RLCIER) HEX ADDRESS: 0XNB0B

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
6	AUXPINTENB	R/W	0	**AUXP interrupt enable** 1 = Enables the receive AUXP detect interrupt.
5	Reserved	-	-	**Reserved**
4	NONCRCENB	R/W	0	**CRC-4 interworking interrupt enable** 1 = Enables the CRC-4-non-CRC-4 interworking interrupt.
3-2	Reserved	-	-	**Reserved**
1	RXAENB	R/W	0	**Receive activation interrupt enable** 1 = Enables the loopback code activation interrupt.
0	RXDENB	R/W	0	**Receive deactivation interrupt enable** 1 = Enables the loopback code deactivation interrupt.

TABLE 122: RECEIVE SA INTERRUPT REGISTER (RSAIR)

REGISTER 333 **RECEIVE SA INTERRUPT REGISTER (RSAIR)** **HEX ADDRESS: 0XNB0C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SA6_1111	R/W	0	**Debounced Sa6 = 1111 received** 1 = Indicates a debounced Sa6 = 1111 has been received.
6	SA6_1110	R/W	0	**Debounced Sa6 = 1110 received** 1 = Indicates a debounced Sa6 = 1111 has been received.
5	SA6_1100	R/W	0	**Debounced Sa6 = 1100 received** 1 = Indicates a debounced Sa6 = 1111 has been received.
4	SA6_1010	R/W	0	**Debounced Sa6 = 1010 received** 1 = Indicates a debounced Sa6 = 1010 has been received.
3	SA6_1000	R/W	0	**Debounced Sa6 = 1000 received** 1 = Indicates a debounced Sa6 = 1111 has been received.
2	SA6_001x	R/W	0	**Debounced Sa6 = 001x received** 1 = Indicates a debounced Sa6 = 1111 has been received.
1	SA6_other	R/W	0	**Debounced Sa6 = other received** 1 = Indicates a debounced Sa6 equals to other combination received.
0	SA6_0000	R/W	0	**Debounced Sa6 = 0000 received** 1 = Indicates a debounced Sa6 = 0000 has been received.

TABLE 123: RECEIVE SA INTERRUPT ENABLE REGISTER (RSAIER)

REGISTER 334 **RECEIVE SA INTERRUPT ENABLE REGISTER (RSAIER)** **HEX ADDRESS: 0XNB0D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SA6_1111_ENB	R/W	0	**Debounced Sa6 = 1111 received enable** 1 = Indicates a debounced Sa6 = 1111 has been received.
6	SA6_1110_ENB	R/W	0	**Debounced Sa6 = 1110 received enable** 1 = Enables the generation of an interrupt when a debounced Sa6 = 1111 has been received.
5	SA6_1100_ENB	R/W	0	**Debounced Sa6 = 1100 received enable** 1 = Enables the generation of an interrupt when a debounced Sa6 = 1111 has been received.
4	SA6_1010_ENB	R/W	0	**Debounced Sa6 = 1010 received enable** 1 = Enables the generation of an interrupt when a debounced Sa6 = 1111 has been received.
3	SA6_1000_ENB	R/W	0	**Debounced Sa6 = 1000 received enable** 1 = Enables the generation of an interrupt when a debounced Sa6 = 1111 has been received.
2	SA6_001x_ENB	R/W	0	**Debounced Sa6 = 001x received enable** 1 = Enables the generation of an interrupt when a debounced Sa6 = 1111 has been received.
1	SA6_other_ENB	R/W	0	**Debounced Sa6 = other received enable** 1 = Enables the generation of an interrupt when a debounced Sa6 equals to other combinations received.
0	SA6_0000_ENB	R/W	0	**Debounced Sa6 = 0000 received enable** 1 = Enables the generation of an interrupt when a debounced Sa6 = 0000 has been received.

TABLE 124: EXCESSIVE ZERO STATUS REGISTER

REGISTER 334 **EXCESSIVE ZERO STATUS REGISTER (EXZSR)** **HEX ADDRESS: 0XNB0E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	EXZ_STATUS	RUR	0	**Excessive Zero State Change** 0 = No change in status 1 = Change in status has occured

TABLE 125: EXCESSIVE ZERO ENABLE REGISTER

REGISTER 334 **EXCESSIVE ZERO ENABLE REGISTER (EXZER)** **HEX ADDRESS: 0XNB0F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	EXZ_ENB	R/W	0	**Excessive Zero Interrupt Enable** 0 = Disabled 1 = Enable excessiver zero interrupt generation

TABLE 126: SS7 STATUS REGISTER FOR LAPD1

REGISTER 334 SS7 STATUS REGISTER FOR LAPD1 (SS7SR1) HEX ADDRESS: 0XNB10

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	SS7_1_STATUS	RUR	0	**SS7 Interrupt Status for LAPD1** 0 = No change in status 1 = Change in status has occured

TABLE 127: SS7 ENABLE REGISTER FOR LAPD1

REGISTER 334 SS7 ENABLE REGISTER FOR LAPD1 (SS7ER1) HEX ADDRESS: 0XNB11

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	SS7_1_ENB	R/W	0	**SS7 Interrupt Enable for LAPD1** 0 = Disabled 1 = Enable SS7 interrupt generation if more than 276 bytes are received within the LAPD1 message

TABLE 128: DATA LINK STATUS REGISTER 2

REGISTER 327 **DATA LINK STATUS REGISTER 2 (DLSR2)** **HEX ADDRESS: 0XNB16**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	MSG TYPE	RUR	0	**HDLC2 Message Type Identifier** Indicates type of data link message received by Rx HDLC2 Controller 0 = Bit Oriented Signaling type data link message received 1 = Message Oriented Signaling type data link message received
6	TxSOT	RUR	0	**Transmit HDLC2 Start of Transmission Interrupt Status** Indicates if the Transmit HDLC2 Start of Transmission Interrupt has occurred since the last read of this register. Transmit HDLC2 Controller will declare this interrupt when it has started to transmit a data link message. 0 = Transmit HDLC2 Start of Transmission interrupt has not occurred since the last read of this register 1 = Transmit HDLC2 Start of Transmission interrupt has occurred since the last read of this register.
5	RxSOT	RUR	0	**Receive HDLC2 Start of Reception Interrupt Status** Indicates if the Receive HDLC2 Start of Reception interrupt has occurred since the last read of this register. Receive HDLC2 Controller will declare this interrupt when it has started to receive a data link message. 0 = Receive HDLC2 Start of Reception interrupt has not occurred since the last read of this register 1 = Receive HDLC2 Start of Reception interrupt has occurred since the last read of this register
4	TxEOT	RUR	0	**Transmit HDLC2 End of Transmission Interrupt Status** Indicates if the Transmit HDLC2 End of Transmission Interrupt has occurred since the last read of this register. Transmit HDLC2 Controller will declare this interrupt when it has completed its transmission of a data link message. 0 = Transmit HDLC2 End of Transmission interrupt has not occurred since the last read of this register 1 = Transmit HDLC2 End of Transmission interrupt has occurred since the last read of this register
3	RxEOT	RUR	0	**Receive HDLC2 Controller End of Reception Interrupt Status** Indicates if Receive HDLC2 End of Reception Interrupt has occurred since the last read of this register. Receive HDLC2 Controller will declare this interrupt once it has completely received a full data link message. 0 = Receive HDLC2 End of Reception interrupt has not occurred since the last read of this register 1 = Receive HDLC2 End of Reception Interrupt has occurred since the last read of this register
2	FCS Error	RUR	0	**FCS Error Interrupt Status** Indicates if the FCS Error Interrupt has occurred since the last read of this register. Receive HDLC2 Controller will declare this interrupt if it detects an error in the most recently received data message. 0 = FCS Error interrupt has not occurred since last read of this register 1 = FCS Error interrupt has occurred since last read of this register
1	Rx ABORT	RUR	0	**Receipt of Abort Sequence Interrupt Status** Indicates if the Receipt of Abort interrupt has occurred since last read of this register. Receive HDLC2 Controller will declare this interrupt if it detects a string of seven (7) consecutive 1's in the incoming data link channel. 0 = Receipt of Abort Sequence interrupt has not occurred since last read of this register 1 = Receipt of Abort Sequence interrupt has occurred since last read of this register

TABLE 128: DATA LINK STATUS REGISTER 2

REGISTER 327 **DATA LINK STATUS REGISTER 2 (DLSR2)** **HEX ADDRESS: 0XNB16**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	RxIDLE	RUR	0	**Receipt of Idle Sequence Interrupt Status** Indicates if the Receipt of Idle Sequence interrupt has occurred since the last read of this register. The Receive HDLC2 Controller will declare this interrupt if it detects the flag sequence octet (0x7E) in the incoming data link channel. 0 = Receipt of Idle Sequence interrupt has not occurred since last read of this register 1 = Receipt of Idle Sequence interrupt has occurred since last read of this register.

TABLE 129: DATA LINK INTERRUPT ENABLE REGISTER 2

REGISTER 328 **DATA LINK INTERRUPT ENABLE REGISTER 2 (DLIER2)** **HEX ADDRESS: 0XNB17**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	**Reserved**
6	TxSOT ENB	R/W	0	**Transmit HDLC2 Start of Transmission Interrupt Enable** 0 = Disables the Transmit HDLC2 Start of Transmission interrupt 1 = Enables the Transmit HDLC2 Start of Transmission interrupt
5	RxSOT ENB	R/W	0	**Receive HDLC2 Start of Reception Interrupt Enable** 0 = Disables the Receive HDLC2 Start of Reception interrupt 1 = Enables the Receive HDLC2 Start of Reception interrupt
4	TxEOT ENB	R/W	0	**Transmit HDLC2 End of Transmission Interrupt Enable** 0 = Disables the Transmit HDLC2 End of Transmission interrupt 1 = Enables the Transmit HDLC2 End of Transmission interrupt
3	RxEOT ENB	R/W	0	**Receive HDLC2 End of Reception Interrupt Enable** 0 = Disables the Receive HDLC2 End of Reception interrupt 1 = Enables the Receive HDLC2 End of Reception interrupt
2	FCS ERR ENB	R/W	0	**FCS Error Interrupt Enable** 0 = Disables FCS Error interrupt 1 = Enables FCS Error interrupt
1	RxABORT ENB	R/W	0	**Receipt of Abort Sequence Interrupt Enable** 0 = Disables Receipt of Abort Sequence interrupt 1 = Enables Receive of Abort Sequence interrupt
0	RxIDLE ENB	R/W	0	**Receipt of Idle Sequence Interrupt Enable** 0 = Disables Receipt of Idle Sequence interrupt 1 = Enables Receipt of Idle Sequence interrupt

TABLE 130: SS7 STATUS REGISTER FOR LAPD2

REGISTER 334 **SS7 STATUS REGISTER FOR LAPD2 (SS7SR2)** **HEX ADDRESS: 0XNB18**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	SS7_2_STATUS	RUR	0	**SS7 Interrupt Status for LAPD2** 0 = No change in status 1 = Change in status has occured

TABLE 131: SS7 ENABLE REGISTER FOR LAPD2

REGISTER 334 **SS7 ENABLE REGISTER FOR LAPD2 (SS7SR2)** **HEX ADDRESS: 0XNB19**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	SS7_2_ENB	R/W	0	**SS7 Interrupt Enable for LAPD2** 0 = Disabled 1 = Enable SS7 interrupt generation if more than 276 bytes are received within the LAPD2 message

TABLE 132: DATA LINK STATUS REGISTER 3

REGISTER 327 **DATA LINK STATUS REGISTER 3 (DLSR3)** **HEX ADDRESS: 0XNB26**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	MSG TYPE	RUR	0	**HDLC3 Message Type Identifier** Indicates type of data link message received by Rx HDLC3 Controller 0 = Bit Oriented Signaling type data link message received 1 = Message Oriented Signaling type data link message received
6	TxSOT	RUR	0	**Transmit HDLC3 Start of Transmission Interrupt Status** Indicates if the Transmit HDLC3 Start of Transmission Interrupt has occurred since the last read of this register. Transmit HDLC3 Controller will declare this interrupt when it has started to transmit a data link message. 0 = Transmit HDLC3 Start of Transmission interrupt has not occurred since the last read of this register 1 = Transmit HDLC3 Start of Transmission interrupt has occurred since the last read of this register.
5	RxSOT	RUR	0	**Receive HDLC3 Start of Reception Interrupt Status** Indicates if the Receive HDLC3 Start of Reception interrupt has occurred since the last read of this register. Receive HDLC3 Controller will declare this interrupt when it has started to receive a data link message. 0 = Receive HDLC3 Start of Reception interrupt has not occurred since the last read of this register 1 = Receive HDLC3 Start of Reception interrupt has occurred since the last read of this register
4	TxEOT	RUR	0	**Transmit HDLC3 End of Transmission Interrupt Status** Indicates if the Transmit HDLC3 End of Transmission Interrupt has occurred since the last read of this register. Transmit HDLC3 Controller will declare this interrupt when it has completed its transmission of a data link message. 0 = Transmit HDLC3 End of Transmission interrupt has not occurred since the last read of this register 1 = Transmit HDLC3 End of Transmission interrupt has occurred since the last read of this register
3	RxEOT	RUR	0	**Receive HDLC3 Controller End of Reception Interrupt Status** Indicates if Receive HDLC3 End of Reception Interrupt has occurred since the last read of this register. Receive HDLC3 Controller will declare this interrupt once it has completely received a full data link message. 0 = Receive HDLC3 End of Reception interrupt has not occurred since the last read of this register 1 = Receive HDLC3 End of Reception Interrupt has occurred since the last read of this register
2	FCS Error	RUR	0	**FCS Error Interrupt Status** Indicates if the FCS Error Interrupt has occurred since the last read of this register. Receive HDLC3 Controller will declare this interrupt if it detects an error in the most recently received data message. 0 = FCS Error interrupt has not occurred since last read of this register 1 = FCS Error interrupt has occurred since last read of this register
1	Rx ABORT	RUR	0	**Receipt of Abort Sequence Interrupt Status** Indicates if the Receipt of Abort interrupt has occurred since last read of this register. Receive HDLC3 Controller will declare this interrupt if it detects a string of seven (7) consecutive 1's in the incoming data link channel. 0 = Receipt of Abort Sequence interrupt has not occurred since last read of this register 1 = Receipt of Abort Sequence interrupt has occurred since last read of this register

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	RxIDLE	RUR	0	**Receipt of Idle Sequence Interrupt Status** Indicates if the Receipt of Idle Sequence interrupt has occurred since the last read of this register. The Receive HDLC2 Controller will declare this interrupt if it detects the flag sequence octet (0x7E) in the incoming data link channel. 0 = Receipt of Idle Sequence interrupt has not occurred since last read of this register 1 = Receipt of Idle Sequence interrupt has occurred since last read of this register.

TABLE 133: DATA LINK INTERRUPT ENABLE REGISTER 3

REGISTER 328 **DATA LINK INTERRUPT ENABLE REGISTER 3 (DLIER3)** **HEX ADDRESS: 0XNB27**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	**Reserved**
6	TxSOT ENB	R/W	0	**Transmit HDLC3 Start of Transmission Interrupt Enable** 0 = Disables the Transmit HDLC3 Start of Transmission interrupt 1 = Enables the Transmit HDLC3 Start of Transmission interrupt
5	RxSOT ENB	R/W	0	**Receive HDLC3 Start of Reception Interrupt Enable** 0 = Disables the Receive HDLC3 Start of Reception interrupt 1 = Enables the Receive HDLC3 Start of Reception interrupt
4	TxEOT ENB	R/W	0	**Transmit HDLC3 End of Transmission Interrupt Enable** 0 = Disables the Transmit HDLC3 End of Transmission interrupt 1 = Enables the Transmit HDLC3 End of Transmission interrupt
3	RxEOT ENB	R/W	0	**Receive HDLC3 End of Reception Interrupt Enable** 0 = Disables the Receive HDLC3 End of Reception interrupt 1 = Enables the Receive HDLC3 End of Reception interrupt
2	FCS ERR ENB	R/W	0	**FCS Error Interrupt Enable** 0 = Disables FCS Error interrupt 1 = Enables FCS Error interrupt
1	RxABORT ENB	R/W	0	**Receipt of Abort Sequence Interrupt Enable** 0 = Disables Receipt of Abort Sequence interrupt 1 = Enables Receive of Abort Sequence interrupt
0	RxIDLE ENB	R/W	0	**Receipt of Idle Sequence Interrupt Enable** 0 = Disables Receipt of Idle Sequence interrupt 1 = Enables Receipt of Idle Sequence interrupt

TABLE 134: SS7 STATUS REGISTER FOR LAPD3

REGISTER 334 **SS7 STATUS REGISTER FOR LAPD3 (SS7SR3)** **HEX ADDRESS: 0XNB28**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	SS7_3_STATUS	RUR	0	**SS7 Interrupt Status for LAPD3** 0 = No change in status 1 = Change in status has occured

TABLE 135: SS7 ENABLE REGISTER FOR LAPD3

TABLE 136: REGISTER 334 SS7 ENABLE REGISTER FOR LAPD3 (SS7SR3) HEX ADDRESS: 0XNB29

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	SS7_3_ENB	R/W	0	**SS7 Interrupt Enable for LAPD3** 0 = Disabled 1 = Enable SS7 interrupt generation if more than 276 bytes are received within the LAPD3 message

TABLE 137: CUSTOMER INSTALLATION ALARM STATUS REGISTER

REGISTER 334 CUSTOMER INSTALLATION ALARM STATUS REGISTER (CIASR) HEX ADDRESS: 0XNB40

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
[7:6]	Reserved	-	-	These bits are reserved
5	RxAIS-CI_state	R/W	0	**Rx AIS-CI State** 0 = No AIS-CI state detected 1 = AIS-CI state detected
4	RxRAI-CI_state	R/W	0	**Rx RAI-CI State** 0 = No RAI-CI state detected 1 = RAI-CI state detected
[3:2]	Reserved	-	-	These bits are reserved
1	RxAIS-CI	RUR	0	**Rx AIS-CI State Change** 0 = No change in status 1 = Change of status has occured
0	RxRAI-CI	RUR	0	**Rx RAI-CI State Change** 0 = No change in status 1 = Change of status has occured

TABLE 138: CUSTOMER INSTALLATION ALARM STATUS REGISTER

REGISTER 334 CUSTOMER INSTALLATION ALARM INTERRUPT ENABLE REGISTER (CIAIER) HEX ADDRESS: 0XNB41

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RxAIS-CI_ENB	R/W	0	**Rx AIS-CI Interrupt Generation Enable** 0 = Disabled 1 - Enable Rx AIS-CI Interrupt Generation
0	RxRAI-CI_ENB	R/W	0	**Rx RAI-CI Interrupt Generation Enable** 0 = Disabled 1 - Enable Rx RAI-CI Interrupt Generation

1.5 THE INTERRUPT STRUCTURE WITHIN THE FRAMER

The XRT86L34 Framer is equipped with a sophisticated Interrupt Servicing Structure. This Interrupt Structure includes an Interrupt Request output pin INT, numerous Interrupt Enable Registers and numerous Interrupt Status Registers.

The Interrupt Servicing Structure, within the XRT86L34 Framer contains three levels of hierarchy:

- The Framer Level
- The Block Level
- The Source Level.

The Framer Interrupt Structure has been carefully designed to allow the user to quickly determine the exact source of this interrupt (with minimal latency) which will aid the mC/mP in determining the which interrupt service routine to call up in order to eliminate or properly respond to the condition(s) causing the interrupt.

The XRT86L34 Framer comes equipped with registers to support the servicing of this wide array of potential "interrupt request" sources. Table 139 lists the possible conditions that can generate interrupts.

TABLE 139: LIST OF THE POSSIBLE CONDITIONS THAT CAN GENERATE INTERRUPTS, IN EACH FRAMER

INTERRUPT BLOCK	INTERRUPTING CONDITION
Framer Level	Loss of RxLineClk Signal· One Second Interrupt
HDLC Controller Block	Transmit HDLC - Start of Transmission Receive HDLC - Start of Reception Transmit HDLC - End of Transmission Receive HDLC - End of Reception FCS Error Receipt of Abort Sequence Receipt of Idle Sequence
Slip Buffer Block	Slip Buffer Full Slip Buffer Empty Slip Buffer - Slip
Alarm & Error Block	Receipt of CAS Multi-frame Yellow Alarm Detection of Loss of Signal Condition Detection of Line Code Violation Change in Receive Loss of Framer Condition Change in Receive AIS Condition Receipt of FAS Frame Yellow Alarm
T1/E1 Frame Block	Change in CAS Multi-Frame Alignment Change in National Bits· Change in CAS Signaling Bits Change in FAS Frame Alignment· Change in the "In Frame" Condition Detection of "Frame Mimicking Data" Detection of Sync (CRC-4/CRC-6) Errors Detection of Framing Bit Errors

General Flow of Interrupt Servicing

When any of the conditions presented in Table 139 occur, (if their Interrupt is enabled), then the Framer generates an interrupt request to the mP/mC by asserting the active-low interrupt request output pin, INT. Shortly after the local mC/mP has detected the activated INT signal, it will enter into the appropriate user-supplied interrupt service routine. The first task for the mP/mC, while running this interrupt service routine, may be to isolate the source of the interrupt request down to the device level (e.g, the Framer IC), if multiple peripheral ICs exist in the user's system. However, once the interrupting peripheral device has been identified, the next task for the mP/mC is to determine exactly what feature of functional section within the device requested the interrupt.

Determine the Framer(s) Requesting the Interrupt

If the interrupting device turns out to be the Framer, then the mP/mC must determine which of the eight framer channels requested the interrupt. Hence, upon reaching this state, one of the very first things that the mP/mC must do within the user Framer interrupt service routine, is to perform a read of each of the Block Interrupt Status Registers within all of the Framer channels that have been enabled for Interrupt Generation via their respective Interrupt Control Registers.

Table 140 lists the Address for the Block Interrupt Status Registers associated with each of the Framer channels within the Framer.

TABLE 140: ADDRESS OF THE BLOCK INTERRUPT STATUS REGISTERS

FRAMER NUMBER	ADDRESS OF BLOCK INTERRUPT STATUS REGISTER
0	0x0B02
1	0x1B02
2	0x2B02
3	0x3B02
4	0x4B02
5	0x5B02
6	0x6B02
7	0x7B02

The bit-format of each of these Block Interrupt Status Registers is listed below.

TABLE 141: BLOCK INTERRUPT STATUS REGISTER

REGISTER 321 **BLOCK INTERRUPT STATUS REGISTER (BISR)** **HEX ADDRESS: 0XNB00**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Sa6	RO	0	**Sa6 Interrupt Status**
7-6	LBCODE	RO	0	**Loopback Code Interrupt**
5	RxClkLOS	RUR	0	**RxClk Los Interrupt Status** Indicates if Framer n has experienced a Loss of Recovered Clock interrupt since last read of this register. 0 = Loss of Recovered Clock interrupt has not occurred since last read of this register 1 = Loss of Recovered Clock interrupt has occurred since last read of this register.
4	ONESEC	RUR	0	**One Second Interrupt Status** Indicates if the XRT86L34 has experienced a One Second interrupt since the last read of this register. 0 = No outstanding One Second interrupts awaiting service 1 = Outstanding One Second interrupt awaits service
3	HDLC	RO	0	**HDLC Block Interrupt Status** Indicates if the HDLC block has an interrupt request awaiting service. 0 = No outstanding interrupt requests awaiting service 1 = HDLC Block has an interrupt request awaiting service. Interrupt Service routine should branch to and read Data LInk Status Register (address xA,06). ***NOTE:*** *This bit-field will be reset to 0 after the microprocessor has performed a read to the Data Link Status Register.*
2	SLIP	RO	0	**Slip Buffer Block Interrupt Status** Indicates if the Slip Buffer block has any outstanding interrupt requests awaiting service. 0 = No outstanding interrupts awaiting service 1 = Slip Buffer block has an interrupt awaiting service. Interrupt Service routine should branch to and read Slip Buffer Interrupt Status register (address 0xXA,0x09. ***NOTE:*** *This bit-field will be reset to 0 after the microprocessor has performed a read of the Slip Buffer Interrupt Status Register.*
1	ALARM	RO	0	**Alarm & Error Block Interrupt Status** Indicates if the Alarm & Error Block has any outstanding interrupts that are awaiting service. 0 = No outstanding interrupts awaiting service 1 = Alarm & Error Block has an interrupt awaiting service. Interrupt SerStatus Register (address xA,02) ***NOTE:*** *This bit-field will be reset to 0 after the microprocessor has performed a read of the Alarm & Error Interrupt Status register.*
0	T1/E1 FRAME	RO	0	**T1/E1 Framer Block Interrupt Status** Indicates if an T1/E1 Frame Status interrupt request is awaiting service. 0 = No T1/E1 Frame Status interrupt is pending 1 = T1/E1 Framer Status interrupt is awaiting service.

For a given Framer, the Block Interrupt Status Register presents the "Interrupt Request" status of each "Interrupt Block" within the Framer. The purpose of the "Block Interrupt Status Register" is to help the mP/mC identify which "Interrupt Block(s) have requested the interrupt. Whichever bit(s) are asserted, in this register, identifies which block(s) have experienced an "interrupt generating" condition, as presented in Table 141. Once the

mP/mC has read this register, it can determine which "branch" within the interrupt service routine that it must follow; in order to properly service this interrupt.

The Framer IC further supports the "Interrupt Block" Hierarchy by providing the "Block Interrupt Enable Register. The bit-format of this register is identical to that for the "Block Interrupt Status Register", and is presented below for the sake of completeness.

TABLE 142: BLOCK INTERRUPT ENABLE REGISTER

REGISTER 322 **BLOCK INTERRUPT ENABLE REGISTER (BIER)** **HEX ADDRESS: 0XNB01**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SA6_ENB	R/W	0	**SA6 interrupt enable**
6	LBCODE_ENB	R/W	0	**Loopback code interrupt enable**
5	RXCLKLOSS	R/W	0	**RxLineClk Loss Interrupt Enable** 0 = Disables interrupt 1 = Enables interrupt
4	ONESEC_ENB	R/W	0	**One Second Interrupt Enable** 0 = Disables interrupt 1 = Enables Interrupt
3	HDLC_ENB	R/W	0	**HDLC Block Interrupt Enable** 0 = Disables all HDLC Block interrupts 1 = Enables HDLC Block (for interrupt generation) at the block level
2	SLIP_ENB	R/W	0	**Slip Buffer Block Interrupt Enable** 0 = Disables all Slip Buffer Block Interrupts 1 = Enables Slip Buffer Block at the block level
1	ALARM_ENB	R/W	0	**Alarm & Error Block Interrupt Enable** 0 = Disables all Alarm & Error Block interrupts 1 = Enables Alarm & Error block at the block level
0	T1/E1FRAME_ENB	R/W	0	**T1/E1 Frame Block Enable** 0 = Disables all Frame Block interrupts 1 = Enables the Frame Block at the block level

The Block Interrupt Enable Register permits the user to individually enable or disable the interrupt requesting capability of each of the "interrupt blocks" within the Framer. If a particular bit-field, within this register contains the value "0"; then the corresponding functional block has been disabled from generating any interrupt requests.

The procedures for configuring, enabling and servicing interrupts for each of these hierarchical levels is discussed below.

1.5.1 Configuring the Interrupt System, at the Framer Level

The XRT86L34 Framer IC permits the user to enable or disable each of the Eight Framers for interrupt generation. Further, the chip permits the user to make the following configuration selection.

1. Whether the "source-level" Interrupt Status bits are "Reset-upon-Read" or "Write-to-Clear".
2. Whether or not an "activated interrupt" is automatically cleared.

1.5.1.1 Enabling/Disabling the Framer for Interrupt Generation

Each of the eight (8) Framers of the XRT86L34 Framer can be enabled or disabled for interrupt generation. This selection is made by writing the appropriate “0” or “1” to bit 0 (INTRUP_EN) of the "Interrupt Control Register" corresponding to that framer, (see Table 143.)

TABLE 143: INTERRUPT CONTROL REGISTER

REGISTER 26 **INTERRUPT CONTROL REGISTER (ICR)** **HEX ADDRESS: 0XN11A**

BIT	MODE	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-3		Reserved	-	-	**Reserved**
2		INT_WC_RUR	R/W	0	**Interrupt Write-to-Clear or Reset-upon-Read Select** Configures Interrupt Status bits to either RUR or Write-to-Clear 0=Interrupt Status bit RUR 1=Interrupt Status bit Write-to-Clear
1		ENBCLR	R/W	0	**Interrupt Enable Auto Clear** 0=Interrupt Enable bits are not cleared after status reading 1=Interrupt Enable bits are cleared after status reading
0		INTRUP_ENB	R/W	0	**Interrupt Enable for Framer_n** Enables Framer n for Interrupt Generation. 0 = Disables corresponding framer block for Interrupt Generation 1 = Enables corresponding framer block for Interrupt Generation

Setting this bit-field to "0" disables all interrupts within the Framer. Setting this bit-field to "1" enables the Framer for interrupt generation (at the Framer Level).

NOTE: *It is important to note that setting this bit-field to "1" does not enable all of the interrupts within the Framer. A given interrupt must also be enabled at the block and source-level, before it is enabled for interrupt generation.*

1.5.1.2 Configuring the "Interrupt Status Bits", within a given Framer to be "Reset-upon-Read" or "Write-to-Clear".

The XRT86L34 Source-Level Interrupt Status Register bits can be configured to be either "Reset-upon-Read" or "Write-to-Clear". If the user configures the Interrupt Status Registers to be "Reset-upon-Read", then when the mP/mC is reading the interrupt status register, the following will happen.

1. The contents of the Source-Level Interrupt Status Register will automatically be reset to "0x00", following the read operation.
2. The Interrupt Request Output pin ($\overline{INT}$) will automatically toggle false (or "high") upon reading the Interrupt Status Register containing the last activated interrupt status bit.

If the user configures the Interrupt Status Registers to be "Write-to-Clear", then when the mP/mC is reading the interrupt status register, the following will happen.

1. The contents of the Source-Level Interrupt Status Register will not be cleared to "0x00", following the read operation. The mP/mC will have to write 0x00 to the interrupt status register in order to reset the contents of the register to 0x00.
2. Reading the Interrupt Status Register, which contains the activated bit(s) will not cause the "Interrupt Request Output" pin ($\overline{INT}$) to toggle false. The Interrupt Request Output pin will not toggle false until the mP/mC has written 0x00 into this register. (Hence, the Interrupt Service Routine must include this write operation).

The Interrupt Status Register (associated with a given framer) can be configured to be either "Reset-upon-Read" or "Write-to-Clear" by writing the appropriate value into Bit 2, within the Interrupt Control Register as indicated in Table 143.

Writing a "0" into this bit-field configures the Interrupt Status registers to be "Reset-upon-Read"(RUR). Conversely, writing a "1" into this bit-field configures the Interrupt Status registers to be "Write-to-Clear".

1.5.1.3 Automatic Reset of Interrupt Enable Bits

Occasionally, the user's system (which includes the Framer IC), may experience a fault condition, such that a "Framer Interrupt Condition" will continuously exist. If this particular interrupt has been enabled (within the Framer), then the Framer will generate an interrupt request to the mP/mC. Afterwards, the mP/mC will attempt to service this interrupt by reading the appropriate Block-level and Source-Level Interrupt Status Register. Ad-

ditionally, the local mP/mC will attempt to perform some "system-related" tasks in order to try to resolve these conditions causing the interrupt. After the local mC/mP has attempted all of these things, the Framer IC will negate the $\overline{INT}$ output pin. However, because this system fault still remains, the condition causing the Framer to issue this interrupt also exists. Consequently, the Framer IC will generate another interrupt request, which forces the mP/mC to once again attempt to service this interrupt. This phenomenon quickly results in the local mP/mC being "tied up" in a continuous cycle of executing this one interrupt service routine. Consequently, the mP/mC (along with portions of the overall system) now becomes non-functional.

In order to prevent this phenomenon from ever occurring, the Framer IC can be configured to automatically reset the "interrupt enable" bits, following their activation. This feature can be implemented by writing the appropriate value to bit 1 of the "Interrupt Control Register" as indicated in Table 143.

Writing a "1" to this bit-field configures the Framer to reset a given interrupt following activation. Writing a "0" to this bit-field configures the Framer to leave the interrupt enabled, following its activation.

1.6 PROGRAMMING THE LINE INTERFACE UNIT (LIU SECTION)

Channel Control Registers

TABLE 144: MICROPROCESSOR REGISTER #335, BIT DESCRIPTION

REGISTER ADDRESS 0X0F00H 0X0F10H 0X0F20H 0X0F30H 0X0F40H 0X0F50H 0X0F60H 0X0F70H	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			
D7	Reserved	**This Bit Is Not Used**	R/W	0
D6	Reserved	**This Bit Is Not Used**	R/W	
D5	RXON_n	**Receiver ON:** Writing a “1” into this bit location turns on the Receive Section of channel n. Writing a “0” shuts off the Receiver Section of channel n.	R/W	0
D4	EQC4_n	**Equalizer Control bit 4:** This bit together with EQC[3:0] are used for controlling transmit pulse shaping, transmit line build-out (LBO) and receive monitoring for either T1 or E1 Modes of operation. See Table 145.	R/W	0
D3	EQC3_n	**Equalizer Control bit 3:** See bit D4 description for function of this bit	R/W	0
D2	EQC2_n	**Equalizer Control bit 2:** See bit D4 description for function of this bit	R/W	0
D1	EQC1_n	**Equalizer Control bit 1:** See bit D4 description for function of this bit	R/W	0
D0	EQC0_n	**Equalizer Control bit 0:** See bit D4 description for function of this bit	R/W	0

TABLE 145: EQUALIZER CONTROL AND TRANSMIT LINE BUILD OUT

EQC[4:0]	T1/E1 MODE/RECEIVE SENSITIVITY	TRANSMIT LBO	CABLE
0x00h	T1 Long Haul/36dB	0dB	100Ω TP
0x01h	T1 Long Haul/36dB	-7.5dB	100Ω TP
0x02h	T1 Long Haul/36dB	-15dB	100Ω TP
0x03h	T1 Long Haul/36dB	-22.5dB	100Ω TP
0x04h	T1 Long Haul/45dB	0dB	100Ω TP
0x05h	T1 Long Haul/45dB	-7.5dB	100Ω TP
0x06h	T1 Long Haul/45dB	-15dB	100Ω TP
0x07h	T1 Long Haul/45dB	-22.5dB	100Ω TP
0x08h	T1 Short Haul/15dB	0 to 133 feet (0.6dB)	100Ω TP
0x09h	T1 Short Haul/15dB	133 to 266 feet (1.2dB)	100Ω TP
0x0Ah	T1 Short Haul/15dB	266 to 399 feet (1.8dB)	100Ω TP
0x0Bh	T1 Short Haul/15dB	399 to 533 feet (2.4dB)	100Ω TP
0x0Ch	T1 Short Haul/15dB	533 to 655 feet (3.0dB)	100Ω TP
0x0Dh	T1 Short Haul/15dB	Arbitrary Pulse	100Ω TP
0x0Eh	T1 Gain Mode/29dB	0 to 133 feet (0.6dB)	100Ω TP
0x0Fh	T1 Gain Mode/29dB	133 to 266 feet (1.2dB)	100Ω TP
0x10h	T1 Gain Mode/29dB	266 to 399 feet (1.8dB)	100Ω TP
0x11h	T1 Gain Mode/29dB	399 to 533 feet (2.4dB)	100Ω TP
0x12h	T1 Gain Mode/29dB	533 to 655 feet (3.0dB)	100Ω TP
0x13h	T1 Gain Mode/29dB	Arbitrary Pulse	100Ω TP
0x14h	T1 Gain Mode/29dB	0dB	100Ω TP
0x15h	T1 Gain Mode/29dB	-7.5dB	100Ω TP
0x16h	T1 Gain Mode/29dB	-15dB	100Ω TP
0x17h	T1 Gain Mode/29dB	-22.5dB	100Ω TP
0x18h	E1 Long Haul/36dB	ITU G.703	75Ω Coax
0x19h	E1 Long Haul/36dB	ITU G.703	120Ω TP
0x1Ah	E1 Long Haul/45dB	ITU G.703	75Ω Coax
0x1Bh	E1 Long Haul/45dB	ITU G.703	120Ω TP
0x1Ch	E1 Short Haul/15dB	ITU G.703	75Ω Coax
0x1Dh	E1 Short Haul/15dB	ITU G.703	120Ω TP
0x1Eh	E1 Gain Mode/29dB	ITU G.703	75Ω Coax
0x1Fh	E1 Gain Mode/29dB	ITU G.703	120Ω TP

TABLE 146: MICROPROCESSOR REGISTER #336, BIT DESCRIPTION

REGISTER ADDRESS 0X0F01H 0X0F11H 0X0F21H 0X0F31H 0X0F41H 0X0F51H 0X0F61H 0X0F71H	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			
D7	RXTSEL_n	**Receiver Termination Select:** In **Host** mode, this bit is used to select between the internal termination and "High" impedance modes for the receiver according to the following table; **RXTSEL** / **RX Termination** **0** / **"High" Impedance** **1** / **Internal**	R/W	0
D6	TXTSEL_n	**Transmit Termination Select:** In **Host** mode, this bit is used to select between the internal termination and "High" impedance modes for the transmitter according to the following table; **TXTSEL** / **TX Termination** **0** / **"High" Impedance** **1** / **Internal**	R/W	0
D5	TERSEL1_n	**Termination Impedance Select1:** In **Host** mode and in internal termination mode, (TXTSEL = "1" and RXTSEL = "1") TERSEL[1:0] control the transmit and receive termination impedance according to the following table; **TERSEL1** / **TERSEL0** / **Termination** 0 / 0 / 100Ω 0 / 1 / 110Ω 1 / 0 / 75Ω 1 / 1 / 120Ω In the internal termination mode, the receiver termination of each receiver is realized completely by internal resistors or by the combination of internal and one fixed external resistor. In the internal termination mode, the transmitter output should be AC coupled to the transformer.	R/W	0

TABLE 146: MICROPROCESSOR REGISTER #336, BIT DESCRIPTION

<table>
<tr><td>D4</td><td>TERSEL0_n</td><td>Termination Impedance Select bit 0:</td><td>R/W</td><td>0</td></tr>
<tr><td>D3</td><td>RxJASEL_n</td><td>Receive Jitter Attenuator Enable
The bit is used to enable the receive jitter attenuator.
“0” = Disabled
“1” = Enable the Receive Jitter Attenuator</td><td>R/W</td><td>0</td></tr>
<tr><td>D2</td><td>TxJASEL_n</td><td>Transmit Jitter Attenuator Enable
The bit is used to enable the transmit jitter attenuator.
“0” = Disabled
“1” = Enable the Transmit Jitter Attenuator</td><td>R/W</td><td>0</td></tr>
<tr><td>D1</td><td>JABW_n</td><td>Jitter Attenuator Bandwidth Select: In E1 mode, set this bit to “1” to select a 1.5Hz Bandwidth for the Jitter Attenuator. The FIFO length will be automatically set to 64 bits. Set this bit to “0” to select 10Hz Bandwidth for the Jitter Attenuator in E1 mode. In T1 mode the Jitter Attenuator Bandwidth is permanently set to 3Hz, and the state of this bit has no effect on the Bandwidth.
<table>
<tr><th>Mode</th><th>JABW bit D1</th><th>FIFOS_n bit D0</th><th>JA B-W Hz</th><th>FIFO Size</th></tr>
<tr><td>T1</td><td>0</td><td>0</td><td>3</td><td>32</td></tr>
<tr><td>T1</td><td>0</td><td>1</td><td>3</td><td>64</td></tr>
<tr><td>T1</td><td>1</td><td>0</td><td>3</td><td>32</td></tr>
<tr><td>T1</td><td>1</td><td>1</td><td>3</td><td>64</td></tr>
<tr><td>E1</td><td>0</td><td>0</td><td>10</td><td>32</td></tr>
<tr><td>E1</td><td>0</td><td>1</td><td>10</td><td>64</td></tr>
<tr><td>E1</td><td>1</td><td>0</td><td>1.5</td><td>64</td></tr>
<tr><td>E1</td><td>1</td><td>1</td><td>1.5</td><td>64</td></tr>
</table></td><td>R/W</td><td>0</td></tr>
<tr><td>D0</td><td>FIFOS_n</td><td>FIFO Size Select: See table of bit D1 above for the function of this bit.</td><td>R/W</td><td>0</td></tr>
</table>

TABLE 147: MICROPROCESSOR REGISTER #337, BIT DESCRIPTION

<table>
<tr><th>REGISTER ADDRESS
0X0F02H
0X0F12H
0X0F22H
0X0F32H
0X0F42H
0X0F52H
0X0F62H
0X0F72H</th><th>CHANNEL_n
CHANNEL_0
CHANNEL_1
CHANNEL_2
CHANNEL_3
CHANNEL_4
CHANNEL_5
CHANNEL_6
CHANNEL_7</th><th rowspan="2">FUNCTION</th><th rowspan="2">REGISTER TYPE</th><th rowspan="2">RESET VALUE</th></tr>
<tr><th>BIT #</th><th>NAME</th></tr>
<tr><td>D7</td><td>INVQRSS_n</td><td>Invert QRSS Pattern: When TQRSS is active, Writing a “1” to this bit inverts the polarity of transmitted QRSS pattern. Writing a “0” sends the QRSS pattern with no inversion.</td><td>R/W</td><td>0</td></tr>
</table>

TABLE 147: MICROPROCESSOR REGISTER #337, BIT DESCRIPTION

<table>
<tr><td>D6</td><td>TXTEST2_n</td><td>Transmit Test Pattern bit 2: This bit together with TXTEST1 and TXTEST0 are used to generate and transmit test patterns according to the following table:

<table>
<tr><th>TXTEST2</th><th>TXTEST1</th><th>TXTEST0</th><th>Test Pattern</th></tr>
<tr><td>0</td><td>X</td><td>X</td><td>No Pattern</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>TDQRSS</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>TAOS</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>TLUC</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>TLDC</td></tr>
</table>

TDQRSS (Transmit/Detect Quasi-Random Signal): This condition when activated enables Quasi-Random Signal Source generation and detection for the selected channel number n. In a T1 system QRSS pattern is a 2^{20}-1 pseudo-random bit sequence (PRBS) with no more than 14 consecutive zeros. In a E1 system, QRSS is a 2^{15}-1 PRBS pattern.
TAOS (Transmit All Ones): Activating this condition enables the transmission of an All Ones Pattern from the selected channel number n.
TLUC (Transmit Network Loop-Up Code): Activating this condition enables the Network Loop-Up Code of “00001” to be transmitted to the line for the selected channel number n. When Network Loop-Up code is being transmitted, the XRT86L34 will ignore the Automatic Loop-Code detection and Remote Loop-Back activation (NLCDE1 =“1”, NLCDE0 =“1”, if activated) in order to avoid activating Remote Digital Loop-Back automatically when the remote terminal responds to the Loop-Back request.
TLDC (Transmit Network Loop-Down Code): Activating this condition enables the network Loop-Down Code of “001” to be transmitted to the line for the selected channel number n.</td><td>R/W</td><td>0</td></tr>
<tr><td>D5</td><td>TXTEST1_n</td><td>Transmit Test pattern bit 1: See description of bit D6 for the function of this bit.</td><td>R/W</td><td>0</td></tr>
<tr><td>D4</td><td>TXTEST0_n</td><td>Transmit Test Pattern bit 0: See description of bit D6 for the function of this bit.</td><td>R/W</td><td>0</td></tr>
<tr><td>D3</td><td>TXON_n</td><td>Transmitter ON: Writing a “1” into this bit location turns on the Transmit Section of channel n. Writing a “0” shuts off the Transmit Section of channel n. In this mode, TTIP_n and TRING_n driver outputs will be tri-stated for power reduction or redundancy applications.</td><td>R/W</td><td>0</td></tr>
</table>

TABLE 147: MICROPROCESSOR REGISTER #337, BIT DESCRIPTION

D2	LOOP2_n	**Loop-Back control bit 2:** This bit together with the LOOP1 and LOOP0 bits control the Loop-Back modes of the LIU section of the chip according to the following table: **LOOP2** / **LOOP1** / **LOOP0** / **Loop-Back Mode** 0 / X / X / No Loop-Back 1 / 0 / 0 / Dual Loop-Back 1 / 0 / 1 / Analog Loop-Back 1 / 1 / 0 / Remote Loop-Back 1 / 1 / 1 / Digital Loop-Back		
D1	LOOP1_n	**Loop-Back control bit 1:** See description of bit D2 for the function of this bit.	R/W	0
D0	LOOP0_n	**Loop-Back control bit 0:** See description of bit D2 for the function of this bit.	R/W	0

TABLE 148: MICROPROCESSOR REGISTER #338, BIT DESCRIPTION

REGISTER ADDRESS **0X0F03H** **0X0F13H** **0X0F23H** **0X0F33H** **0X0F43H** **0X0F53H** **0X0F63H** **0X0F73H**	**CHANNEL_n** **CHANNEL_0** **CHANNEL_1** **CHANNEL_2** **CHANNEL_3** **CHANNEL_4** **CHANNEL_5** **CHANNEL_6** **CHANNEL_7**	**FUNCTION**	**REGISTER TYPE**	**RESET VALUE**
BIT #	**NAME**			

TABLE 148: MICROPROCESSOR REGISTER #338, BIT DESCRIPTION

<table>
<tr><td>D7</td><td>NLCDE1_n</td><td>Network Loop Code Detection Enable Bit 1:
This bit together with NLCDE0_n control the Loop-Code detection of each channel.
<table><tr><th>NLCDE1</th><th>NLCDE0</th><th>Function</th></tr><tr><td>0</td><td>0</td><td>Disable Loop-code detection</td></tr><tr><td>0</td><td>1</td><td>Detect Loop-Up code in receive data</td></tr><tr><td>1</td><td>0</td><td>Detect Loop-Down code in receive data</td></tr><tr><td>1</td><td>1</td><td>Automatic Loop-Code detection</td></tr></table>When NLCDE1 =”0” and NLCDE0 = “1” or NLCDE1 = “1” and NLCDE0 = “0”, the chip is manually programmed to monitor the receive data for the Loop-Up or Loop-Down code respectively.When the presence of the “00001” or “001” pattern is detected for more than 5 seconds, the status of the NLCD bit is set to “1” and if the NLCD interrupt is enabled, an interrupt is initiated.The Host has the option to control the Loop-Back function manually.
Setting the NLCDE1 = “1” and NLCDE0 = “1” enables the Automatic Loop-Code detection and Remote Loop-Back activation mode. As this mode is initiated, the state of the NLCD interface bit is reset to “0” and the chip is programmed to monitor the receive data for the Loop-Up code. If the “00001” pattern is detected for longer than 5 seconds, the NLCD bit is set “1”, Remote Loop-Back is activated and the chip is automatically programmed to monitor the receive data for the Loop-Down code. The NLCD bit stays set even after the chip stops receiving the Loop-Up code. The Remote Loop-Back condition is removed when the chip receives the Loop-Down code for more than 5 seconds or if the Automatic Loop-Code detection mode is terminated.</td><td>R/W</td><td>0</td></tr>
<tr><td>D6</td><td>NLCDE0_n</td><td>Network Loop Code Detection Enable Bit 0:
See description of D7 for function of this bit.</td><td>R/W</td><td>0</td></tr>
<tr><td>D5</td><td>Reserved</td><td>This Bit Is Not Used</td><td>R/W</td><td>0</td></tr>
<tr><td>D4</td><td>RXRES1_n</td><td>Receive External Resistor Control Pin 1: In Host mode, this bit along with the RXRES0_n bit selects the value of the external Receive fixed resistor according to the following table;
<table><tr><th>RXRES1_n</th><th>RXRES0_n</th><th>Required Fixed External RX Resistor</th></tr><tr><td>0</td><td>0</td><td>No external Fixed Resistor</td></tr><tr><td>0</td><td>1</td><td>240Ω</td></tr><tr><td>1</td><td>0</td><td>210Ω</td></tr><tr><td>1</td><td>1</td><td>150Ω</td></tr></table></td><td>R/W</td><td>0</td></tr>
<tr><td>D3</td><td>RXRES0_n</td><td>Receive External Resistor Control Pin 0: For function of this bit see description of D4 the RXRES1_n bit.</td><td>R/W</td><td>0</td></tr>
</table>

TABLE 148: MICROPROCESSOR REGISTER #338, BIT DESCRIPTION

D2	INSBPV_n	**Insert Bipolar Violation:** When this bit transitions from "0" to "1", a bipolar violation is inserted in the transmitted data stream of the selected channel number n. Bipolar violation can be inserted either in the QRSS pattern, or input data when operating in single-rail mode. The state of this bit is sampled on the rising edge of the respective TCLK_n. ***NOTE:*** *To ensure the insertion of a bipolar violation, a "0" should be written in this bit location before writing a "1".*	R/W	0
D1	INSBER_n	**Insert Bit Error:** With TDQRSS enabled, when this bit transitions from "0" to "1", a bit error will be inserted in the transmitted QRSS pattern of the selected channel number n. The state of this bit is sampled on the rising edge of the respective TCLK_n. ***NOTE:*** *To ensure the insertion of bit error, a "0" should be written in this bit location before writing a "1".*	R/W	0
D0	Reserved	**This Bit Is Not Used**	R/W	0

TABLE 149: MICROPROCESSOR REGISTER #339, BIT DESCRIPTION

REGISTER ADDRESS **0X0F04H** **0X0F14H** **0X0F24H** **0X0F34H** **0X0F44H** **0X0F54H** **0X0F64H** **0X0F74H**	**CHANNEL_n** **CHANNEL_0** **CHANNEL_1** **CHANNEL_2** **CHANNEL_3** **CHANNEL_4** **CHANNEL_5** **CHANNEL_6** **CHANNEL_7**	**FUNCTION**	**REGISTER TYPE**	**RESET VALUE**
BIT #	**NAME**			
D7	Reserved	**This Bit Is Not Used**	RO	0
D6	DMOIE_n	**DMO Interrupt Enable:** Writing a "1" to this bit enables DMO interrupt generation, writing a "0" masks it.	R/W	0
D5	FLSIE_n	**FIFO Limit Status Interrupt Enable:** Writing a "1" to this bit enables interrupt generation when the FIFO limit is within to 3 bits, writing a "0" to masks it.	R/W	0
D4	LCVIE_n	**Line Code Violation Interrupt Enable:** Writing a "1" to this bit enables Line Code Violation interrupt generation, writing a "0" masks it.	R/W	0
D3	NLCDIE_n	**Network Loop-Code Detection Interrupt Enable:** Writing a "1" to this bit enables Network Loop-code detection interrupt generation, writing a "0" masks it.	R/W	0
D2	AISDIE_n	**AIS Interrupt Enable:** Writing a "1" to this bit enables Alarm Indication Signal detection interrupt generation, writing a "0" masks it.	R/W	0

TABLE 149: MICROPROCESSOR REGISTER #339, BIT DESCRIPTION

D1	RLOSIE_n	**Receive Loss of Signal Interrupt Enable:** Writing a "1" to this bit enables Loss of Receive Signal interrupt generation, writing a "0" masks it.	R/W	0
D0	QRPDIE_n	**QRSS Pattern Detection Interrupt Enable:** Writing a "1" to this bit enables QRSS pattern detection interrupt generation, writing a "0" masks it.	R/W	0

TABLE 150: MICROPROCESSOR REGISTER #340, BIT DESCRIPTION

REGISTER ADDRESS **0x0F05H** **0x0F15H** **0x0F25H** **0x0F35H** **0x0F45H** **0x0F55H** **0x0F65H** **0x0F75H**	**CHANNEL_n** **CHANNEL_0** **CHANNEL_1** **CHANNEL_2** **CHANNEL_3** **CHANNEL_4** **CHANNEL_5** **CHANNEL_6** **CHANNEL_7**	**FUNCTION**	**REGISTER TYPE**	**RESET VALUE**
BIT #	**NAME**			
D7	Reserved		RO	0
D6	DMO_n	**Driver Monitor Output:** This bit is set to a "1" to indicate transmit driver failure is detected. The value of this bit is based on the current status of DMO for the corresponding channel. If the DMOIE bit is enabled, any transition on this bit will generate an Interrupt.	RO	0
D5	FLS_n	**FIFO Limit Status:** This bit is set to a "1" to indicate that the jitter attenuator read/write FIFO pointers are within +/- 3 bits. If the FLSIE bit is enabled, any transition on this bit will generate an Interrupt.	RO	0
D4	LCV_n	**Line Code Violation:** This bit is set to a "1" to indicate that the receiver of channel n is currently detecting a Line Code Violation or an excessive number of zeros in the B8ZS or HDB3 modes. If the LCVIE bit is enabled, any transition on this bit will generate an Interrupt.	RO	0

TABLE 150: MICROPROCESSOR REGISTER #340, BIT DESCRIPTION

D3	NLCD_n	**Network Loop-Code Detection:** This bit operates differently in the Manual or the Automatic Network Loop-Code detection modes. **In the Manual Loop-Code detection mode**, (NLCDE1 = "0" and NLCDE0 = "1" or NLCDE1 = "1" and NLCDE0 = "0") this bit gets set to "1" as soon as the Loop-Up ("00001") or Loop-Down ("001") code is detected in the receive data for longer than 5 seconds. The NLCD bit stays in the "1" state for as long as the chip detects the presence of the Loop-code in the receive data and it is reset to "0" as soon as it stops receiving it. In this mode, if the NLCD interrupt is enabled, the chip will initiate an interrupt on every transition of the NLCD. **When the Automatic Loop-code detection mode,** (NLCDE1 = "1" and NLCDE0 ="1") is initiated, the state of the NLCD interface bit is reset to "0" and the chip is programmed to monitor the receive input data for the Loop-Up code. This bit is set to a "1" to indicate that the Network Loop Code is detected for more than 5 seconds. Simultaneously the Remote Loop-Back condition is automatically activated and the chip is programmed to monitor the receive data for the Network Loop Down code. The NLCD bit stays in the "1" state for as long as the Remote Loop-Back condition is in effect even if the chip stops receiving the Loop-Up code. Remote Loop-Back is removed if the chip detects the "001" pattern for longer than 5 seconds in the receive data.Detecting the "001" pattern also results in resetting the NLCD interface bit and initiating an interrupt provided the NLCD interrupt enable bit is active. **When programmed in Automatic detection mode,** the NLCD interface bit stays "High" for the entire time the Remote Loop-Back is active and initiate an interrupt anytime the status of the NLCD bit changes. In this mode, the **Host** can monitor the state of the NLCD bit to determine if the Remote Loop-Back is activated.	RO	0
D2	AISD_n	**Alarm Indication Signal Detect:** This bit is set to a "1" to indicate All Ones Signal is detected by the receiver. The value of this bit is based on the current status of Alarm Indication Signal detector of channel n. If the AISDIE bit is enabled, any transition on this bit will generate an Interrupt.	RO	0
D1	RLOS_n	**Receive Loss of Signal:** This bit is set to a "1" to indicate that the receive input signal is lost. The value of this bit is based on the current status of the receive input signal of channel n. If the RLOSIE bit is enabled, any transition on this bit will generate an Interrupt.	RO	0
D0	QRPD_n	**Quasi-random Pattern Detection:** This bit is set to a "1" to indicate the receiver is currently in synchronization with QRSS pattern. The value of this bit is based on the current status of Quasi-random pattern detector of channel n. If the QRPDIE bit is enabled, any transition on this bit will generate an Interrupt.	RO	0

TABLE 151: MICROPROCESSOR REGISTER #341, BIT DESCRIPTION

REGISTER ADDRESS 0x0F06H 0x0F16H 0x0F26H 0x0F36H 0x0F46H 0x0F56H 0x0F66H 0x0F76H	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			
D7	Reserved		RO	0
D6	DMOIS_n	**Driver Monitor Output Interrupt Status:** This bit is set to a "1" every time the DMO status has changed since last read. ***NOTE:*** *This bit is reset upon read.*	RUR	0
D5	FLSIS_n	**FIFO Limit Interrupt Status:** This bit is set to a "1" every time when FIFO Limit (Read/Write pointer with +/- 3 bits apart) status has changed since last read. ***NOTE:*** *This bit is reset upon read.*	RUR	0
D4	LCVIS_n	**Line Code Violation Interrupt Status:** This bit is set to a "1" every time when LCV status has changed since last read. ***NOTE:*** *This bit is reset upon read.*	RUR	0
D3	NLCDIS_n	**Network Loop-Code Detection Interrupt Status:** This bit is set to a "1" every time when NLCD status has changed since last read. ***NOTE:*** *This bit is reset upon read.*	RUR	0
D2	AISDIS_n	**AIS Detection Interrupt Status:** This bit is set to a "1" every time when AISD status has changed since last read. ***NOTE:*** *This bit is reset upon read.*	RUR	0
D1	RLOSIS_n	**Receive Loss of Signal Interrupt Status:** This bit is set to a "1" every time RLOS status has changed since last read. ***NOTE:*** *This bit is reset upon read.*	RUR	0
D0	QRPDIS_n	**Quasi-Random Pattern Detection Interrupt Status:** This bit is set to a "1" every time when QRPD status has changed since last read. ***NOTE:*** *This bit is reset upon read.*	RUR	0

TABLE 152: MICROPROCESSOR REGISTER #342, BIT DESCRIPTION

REGISTER ADDRESS 0X0F07H 0X0F17H 0X0F27H 0X0F37H 0X0F47H 0X0F57H 0X0F67H 0X0F77H	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			
D7	Reserved		RO	0
D6	Reserved		RO	0
D5	CLOS5_n	**Cable Loss bit 5:** CLOS[5:0]_n are the six bit receive selective equalizer setting which is also a binary word that represents the cable attenuation indication within ±1dB. CLOS5_n is the most significant bit (MSB) and CLOS0_n is the least significant bit (LSB).	RO	0
D4	CLOS4_n	**Cable Loss bit 4:** See description of D5 for function of this bit.	RO	0
D3	CLOS3_n	**Cable Loss bit 3:** See description of D5 for function of this bit.	RO	0
D2	CLOS2_n	**Cable Loss bit 2:** See description of D5 for function of this bit.	RO	0
D1	CLOS1_n	**Cable Loss bit 1:** See description of D5 for function of this bit.	RO	0
D0	CLOS0_n	**Cable Loss bit 0:** See description of D5 for function of this bit.	RO	0

TABLE 153: MICROPROCESSOR REGISTER #343, BIT DESCRIPTION

REGISTER ADDRESS 0X0F08H 0X0F18H 0X0F28H 0X0F38H 0X0F48H 0X0F58H 0X0F68H 0X0F78H	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			

TABLE 153: MICROPROCESSOR REGISTER #343, BIT DESCRIPTION

D7	Reserved		R/W	0
D6-D0	B6S1_n - B0S1_n	**Arbitrary Transmit Pulse Shape, Segment 1:**The shape of each channel's transmitted pulse can be made independently user programmable by selecting "Arbitrary Pulse" mode. The arbitrary pulse is divided into eight time segments whose combined duration is equal to one period of MCLK. This 7 bit number represents the amplitude of the nth channel's arbitrary pulse during the first time segment. B6S1_n-B0S1_n is in signed magnitude format with B6S1_n as the sign bit and B0S1_n as the least significant bit (LSB).	R/W	0

TABLE 154: MICROPROCESSOR REGISTER #344, BIT DESCRIPTION

REGISTER ADDRESS	**CHANNEL_n**	**FUNCTION**	**REGISTER TYPE**	**RESET VALUE**
0X0F09H	**CHANNEL_0**			
0X0F19H	**CHANNEL_1**			
0X0F29H	**CHANNEL_2**			
0X0F39H	**CHANNEL_3**			
0X0F49H	**CHANNEL_4**			
0X0F59H	**CHANNEL_5**			
0X0F69H	**CHANNEL_6**			
0X0F79H	**CHANNEL_7**			
BIT #	**NAME**			
D7	Reserved		R/W	0
D6-D0	B6S2_n - B0S2_n	**Arbitrary Transmit Pulse Shape, Segment 2** The shape of each channel's transmitted pulse can be made independently user programmable by selecting "Arbitrary Pulse" mode. The arbitrary pulse is divided into eight time segments whose combined duration is equal to one period of MCLK. This 7 bit number represents the amplitude of the nth channel's arbitrary pulse during the second time segment. B6S2_n-B0S2_n is in signed magnitude format with B6S2_n as the sign bit and B0S2_n as the least significant bit (LSB).	R/W	0

TABLE 155: MICROPROCESSOR REGISTER #345, BIT DESCRIPTION

REGISTER ADDRESS	**CHANNEL_n**	**FUNCTION**	**REGISTER TYPE**	**RESET VALUE**
0X0F0AH	**CHANNEL_0**			
0X0F1AH	**CHANNEL_1**			
0X0F2AH	**CHANNEL_2**			
0X0F3AH	**CHANNEL_3**			
0X0F4AH	**CHANNEL_4**			
0X0F5AH	**CHANNEL_5**			
0X0F6AH	**CHANNEL_6**			
0X0F7AH	**CHANNEL_7**			
BIT #	**NAME**			

TABLE 155: MICROPROCESSOR REGISTER #345, BIT DESCRIPTION

D7	Reserved		R/W	0
D6-D0	B6S3_n - B0S3_n	**Arbitrary Transmit Pulse Shape, Segment 3** The shape of each channel's transmitted pulse can be made independently user programmable by selecting "Arbitrary Pulse" mode. The arbitrary pulse is divided into eight time segments whose combined duration is equal to one period of MCLK. This 7 bit number represents the amplitude of the nth channel's arbitrary pulse during the third time segment. B6S3_n-B0S3_n is in signed magnitude format with B6S3_n as the sign bit and B0S3_n as the least significant bit (LSB).	R/W	0

TABLE 156: MICROPROCESSOR REGISTER #346, BIT DESCRIPTION

REGISTER ADDRESS 0X0F0BH 0X0F1BH 0X0F2BH 0X0F3BH 0X0F4BH 0X0F5BH 0X0F6BH 0X0F7BH	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			
D7	Reserved		R/W	0
D6-D0	B6S4_n - B0S4_n	**Arbitrary Transmit Pulse Shape, Segment 4** The shape of each channel's transmitted pulse can be made independently user programmable by selecting "Arbitrary Pulse" mode. The arbitrary pulse is divided into eight time segments whose combined duration is equal to one period of MCLK. This 7 bit number represents the amplitude of the nth channel's arbitrary pulse during the fourth time segment. B6S4_n-B0S4_n is in signed magnitude format with B6S4_n as the sign bit and B0S4_n as the least significant bit (LSB).	R/W	0

TABLE 157: MICROPROCESSOR REGISTER #347, BIT DESCRIPTION

REGISTER ADDRESS 0X0F0CH 0X0F1CH 0X0F2CH 0X0F3CH 0X0F4CH 0X0F5CH 0X0F6CH 0X0F7CH	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			

TABLE 157: MICROPROCESSOR REGISTER #347, BIT DESCRIPTION

D7	Reserved		R/W	0
D6-D0	B6S5_n - B0S5_n	**Arbitrary Transmit Pulse Shape, Segment 5** The shape of each channel's transmitted pulse can be made independently user programmable by selecting "Arbitrary Pulse" mode. The arbitrary pulse is divided into eight time segments whose combined duration is equal to one period of MCLK. This 7 bit number represents the amplitude of the nth channel's arbitrary pulse during the fifth time segment. B6S5_n-B0S5_n is in signed magnitude format with B6S5_n as the sign bit and B0S5_n as the least significant bit (LSB).	R/W	0

TABLE 158: MICROPROCESSOR REGISTER #348, BIT DESCRIPTION

REGISTER ADDRESS 0X0F0DH 0X0F1DH 0X0F2DH 0X0F3DH 0X0F4DH 0X0F5DH 0X0F6DH 0X0F7DH	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			
D7	Reserved		R/W	0
D6-D0	B6S6_n - B0S6_n	**Arbitrary Transmit Pulse Shape, Segment 6** The shape of each channel's transmitted pulse can be made independently user programmable by selecting "Arbitrary Pulse" mode. The arbitrary pulse is divided into eight time segments whose combined duration is equal to one period of MCLK. This 7 bit number represents the amplitude of the nth channel's arbitrary pulse during the sixth time segment. B6S6_n-B0S6_n is in signed magnitude format with B6S6_n as the sign bit and B0S6_n as the least significant bit (LSB).	R/W	0

TABLE 159: MICROPROCESSOR REGISTER #349, BIT DESCRIPTION

REGISTER ADDRESS 0X0F0EH 0X0F1EH 0X0F2EH 0X0F3EH 0X0F4EH 0X0F5EH 0X0F6EH 0X0F7EH	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			

TABLE 159: MICROPROCESSOR REGISTER #349, BIT DESCRIPTION

D7	Reserved		R/W	0
D6-D0	B6S7_n - B0S7_n	**Arbitrary Transmit Pulse Shape, Segment 7** The shape of each channel's transmitted pulse can be made independently user programmable by selecting "Arbitrary Pulse" mode. The arbitrary pulse is divided into eight time segments whose combined duration is equal to one period of MCLK. This 7 bit number represents the amplitude of the nth channel's arbitrary pulse during the seventh time segment. B6S7_n-B0S7_n is in signed magnitude format with B6S7_n as the sign bit and B0S7_n as the least significant bit (LSB).	R/W	0

TABLE 160: MICROPROCESSOR REGISTER #350, BIT DESCRIPTION

REGISTER ADDRESS **0X0F0FH** **0X0F1FH** **0X0F2FH** **0X0F3FH** **0X0F4FH** **0X0F5FH** **0X0F6FH** **0X0F7FH**	**CHANNEL_n** **CHANNEL_0** **CHANNEL_1** **CHANNEL_2** **CHANNEL_3** **CHANNEL_4** **CHANNEL_5** **CHANNEL_6** **CHANNEL_7**	**FUNCTION**	**REGISTER TYPE**	**RESET VALUE**
BIT #	**NAME**			
D7	Reserved		R/W	0
D6-D0	B6S8_n - B0S8_n	**Arbitrary Transmit Pulse Shape, Segment 8** The shape of each channel's transmitted pulse can be made independently user programmable by selecting "Arbitrary Pulse" mode. The arbitrary pulse is divided into eight time segments whose combined duration is equal to one period of MCLK. This 7 bit number represents the amplitude of the nth channel's arbitrary pulse during the eighth time segment. B6S8_n-B0S8_n is in signed magnitude format with B6S8_n as the sign bit and B0S8_n as the least significant bit (LSB).	R/W	0

TABLE 161: MICROPROCESSOR REGISTER #559, BIT DESCRIPTION

REGISTER ADDRESS 0X0FE0H / BIT #	NAME	FUNCTION	REGISTER TYPE	RESET VALUE
D7	Reserved	**This Bit Is Not Used**	R/W	0
D6	ATAOS	**Automatic Transmit All Ones Upon RLOS:** Writing a “1” to this bit enables the automatic transmission of All "Ones" data to the line for the channel that detects an RLOS condition. Writing a “0” disables this feature.	R/W	0
D5	Reserved	**This Bit Is Not Used**	R/W	0
D4	Reserved	**This Bit Is Not Used**	R/W	0
D3	Reserved	**This Bit Is Not Used**	R/W	0
D2	Reserved	**This Bit Is Not Used**		0
D1	GIE	**Global Interrupt Enable:** Writing a “1” to this bit globally enables interrupt generation for all channels. Writing a “0” disables interrupt generation.	R/W	0
D0	SRESET	**Software Reset µP Registers:** Writing a “1” to this bit longer than 10µs initiates a device reset through the microprocessor interface. All internal circuits are placed in the reset state with this bit set to a “1” except the microprocessor register bits.	R/W	0

TABLE 162: MICROPROCESSOR REGISTER #560, BIT DESCRIPTION

REGISTER ADDRESS 0X0FE1H / BIT #	NAME	FUNCTION	REGISTER TYPE	RESET VALUE
D7	Reserved		R/W	0
D6	Reserved		R/W	0
D5 D4	Guage1 Guage0	**Wire Gauge Selector Bit 1:** This bit together with bit D6 are used to select wire gauge size as shown in the table below.	R/W	0 0
D3	Reserved	**This Bit Is Not Used**	R/W	0

GAUGE1	GAUGE0	Wire Size
0	0	22 and 24 Gauge
0	1	22 Gauge
1	0	24 Gauge
1	1	26 Gauge

TABLE 162: MICROPROCESSOR REGISTER #560, BIT DESCRIPTION

D2	RXMUTE	**Receive Output Mute:** Writing a "1" to this bit, mutes receive outputs at the framer block to a "0" state for any channel that detects an RLOS condition. ***NOTE:*** *The receive clock is not muted.*	R/W	0
D1	EXLOS	**Extended LOS:** Writing a "1" to this bit extends the number of zeros at the receive input of each channel before RLOS is declared to 4096 bits. Writing a "0" reverts to the normal mode (175+75 bits for T1 and 32 bits for E1).	R/W	0
D0	ICT	**In-Circuit-Testing:** Writing a "1" to this bit configures all the output pins of the chip in high impedance mode for In-Circuit-Testing.	R/W	0

TABLE 163: MICROPROCESSOR REGISTER #561, BIT DESCRIPTION

REGISTER ADDRESS 0X0FE2H BIT #	NAME	FUNCTION	REGISTER TYPE	RESET VALUE
D7	Reserved	**This Bit Is Not Used**	R/W	0
D6	Reserved	**This Bit Is Not Used**	R/W	0
D5-D0	Reserved	**This Bit Is Not Used**	R/W	0

TABLE 164: MICROPROCESSOR REGISTER #563, BIT DESCRIPTION

REGISTER ADDRESS 0X0FE4H BIT #	NAME	FUNCTION	REGISTER TYPE	RESET VALUE
D7 D6	MCLKnT11 MCLKnT10	**Master T1 Output Clock Reference** These two bits are used to select the programmable output clock reference for T1MCLKnOUT. "00" = 1.544MHz "01" = 3.088MHz "10" = 6.176MHz "11" = 12.352MHz	R/W	0 0
D5 D4	MCLKnE11 MCLKnE10	**Master E1 Output Clock Reference** These two bits are used to select the programmable output clock reference for E1MCLKnOUT. "00" = 2.048MHz "01" = 4.096MHz "10" = 8.192MHz "11" = 16.384MHz	R/W	0 0
D3	Reserved	**This Bit Is Not Used.**	R/W	0
D2	Reserved	**This Bit Is Not Used.**	R/W	0

TABLE 164: MICROPROCESSOR REGISTER #563, BIT DESCRIPTION

D1	Reserved	**This Bit Is Not Used.**	R/W	0
D0	Reserved	**This Bit Is Not Used.**	R/W	0

TABLE 165: MICROPROCESSOR REGISTER #568, BIT DESCRIPTION

REGISTER ADDRESS 0X0FE9H BIT #	NAME	FUNCTION	REGISTER TYPE	RESET VALUE
D7	Reserved	**This Bit Is Not Used.**	R/W	0
D6	Reserved	**This Bit Is Not Used.**	R/W	0
D5	Reserved	**This Bit Is Not Used.**	R/W	0
D4	Reserved	**This Bit Is Not Used.**	R/W	0
D3 D2 D1 D0	CLKSEL3 CLKSEL2 CLKSEL1 CLKSEL0	**Clock Select Input** CLKSEL[3:0] is used to select the input clock source to be used as the internal timing reference for MCLKIN. “0000” = 2.048MHz “0001” = 1.544MHz “0010” = 8kHz “0011” = 16kHz “0100” = 56kHz “0101” = 64kHz “0110” = 128kHz “0111” = 256kHz “1000” = 4.096MHz “1001” = 3.088MHz “1010” = 8.192MHz “1011” = 6.176MHz “1100” = 16.384MHz “1101” = 12.352MHz “1110” = 2.048MHz “1111” = 1.544MHz	R/W	0 0 0 0

TABLE 166: MICROPROCESSOR REGISTER #569, BIT DESCRIPTION

REGISTER ADDRESS 0X0FEAH BIT #	NAME	FUNCTION	REGISTER TYPE	RESET VALUE
D7	GCHIS7	**Global Channel 7 Interrupt Status Indicator** This bit indicates that a change in status on Channel 7 has occured regarding any interrupt generation that has been enabled. This register is Reset Upon Read.	RUR	0

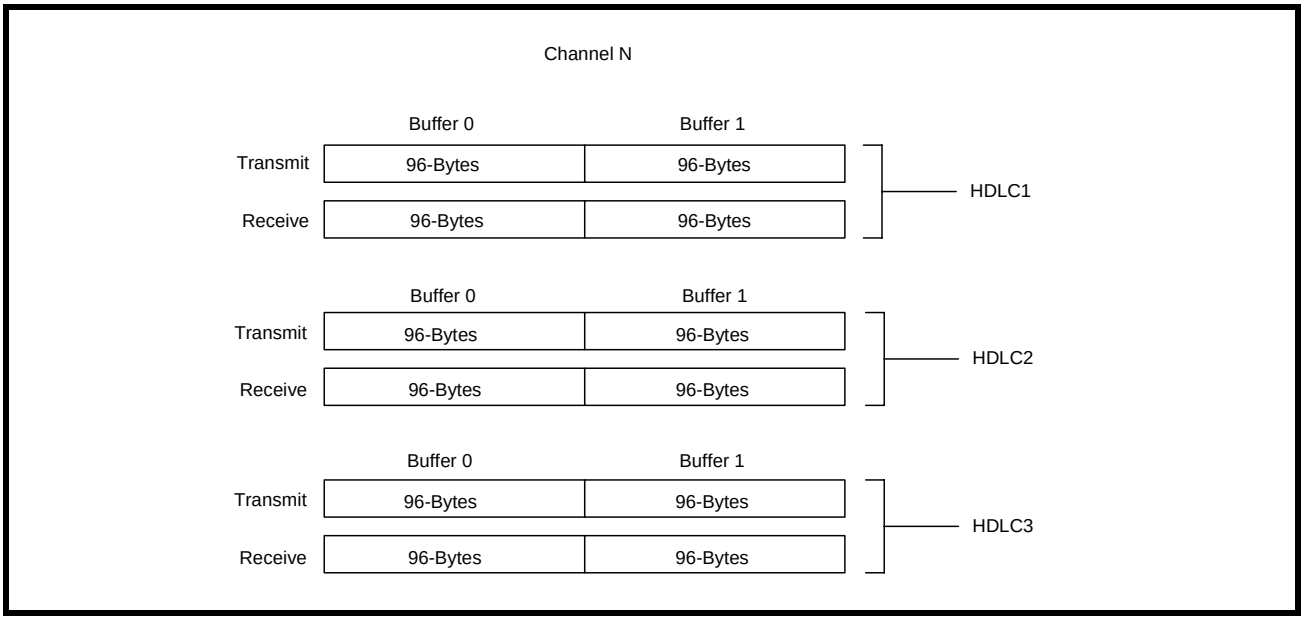
TABLE 166: MICROPROCESSOR REGISTER #569, BIT DESCRIPTION

D6	GCHIS6	**Global Channel 6 Interrupt Status Indicator** This bit indicates that a change in status on Channel 6 has occured regarding any interrupt generation that has been enabled. This register is Reset Upon Read.	RUR	0
D5	GCHIS5	**Global Channel 5 Interrupt Status Indicator** This bit indicates that a change in status on Channel 5 has occured regarding any interrupt generation that has been enabled. This register is Reset Upon Read.	RUR	0
D4	GCHIS4	**Global Channel 4 Interrupt Status Indicator** This bit indicates that a change in status on Channel 4 has occured regarding any interrupt generation that has been enabled. This register is Reset Upon Read.	RUR	0
D3	GCHIS3	**Global Channel 3 Interrupt Status Indicator** This bit indicates that a change in status on Channel 3 has occured regarding any interrupt generation that has been enabled. This register is Reset Upon Read.	RUR	0
D2	GCHIS2	**Global Channel 2 Interrupt Status Indicator** This bit indicates that a change in status on Channel 2 has occured regarding any interrupt generation that has been enabled. This register is Reset Upon Read.	RUR	0
D1	GCHIS1	**Global Channel 1 Interrupt Status Indicator** This bit indicates that a change in status on Channel 1 has occured regarding any interrupt generation that has been enabled. This register is Reset Upon Read.	RUR	0
D0	GCHIS0	**Global Channel 0 Interrupt Status Indicator** This bit indicates that a change in status on Channel 0 has occured regarding any interrupt generation that has been enabled. This register is Reset Upon Read.	RUR	0

2.0 HDLC CONTROLLERS AND LAPD

The purpose of the HDLC controllers is to allow messages to be stored for transport in the outbound transmit framer block or extracted from the receive framer block through the LAPD interface. Each channel within the Framer has 3 independent HDLC controllers. Each HDLC controller has two 96-Byte buffers for Transmit and two 96-Byte buffers for Receive. The buffers are used to insert messages into the out going data stream for Transmit or to extract messages from the incoming data stream from the Receive path. Total, there are twelve 96-Byte buffers per channel. This allows multiple HDLC messages to be transported to and from EXAR's framing device. The following sections describe the procedure for transporting LAPD messages using HDLC controller 1. HDLC controller 2 and HDLC controller 3 are implemented in the same manner, each having individual control registers. See the register map/descriptions for more details.

FIGURE 7. HDLC CONTROLLERS



2.1 DS1 TRANSMIT HDLC CONTROLLER BLOCK

2.1.1 Description of the DS1 Transmit HDLC Controller Block

Thre transmit framer block can insert data link information to outbound DS1 frames. The data link information in DS1 framing format can be inserted from:

- DS1 Transmit Overhead Input Interface Block
- DS1 Transmit HDLC Controller
- DS1 Transmit Serial Input Interface

The Transmit Data Link Source Select [1:0] bits, within the Transmit Data Link Select Register (TSDLSR) determine source of the data link bits (Facility Data Link (FDL) bits in ESF framing format mode, Signaling Framing (Fs) bits in SLC®96 framing format mode and Remote Signaling (R) bits in T1DM framing format mode) to be inserted into the outgoing DS1 frames.

The table below shows configuration of the Transmit Data Link Source Select [1:0] bits of the Transmit Data Link Select Register (TSDLSR).

TRANSMIT DATA LINK SELECT REGISTER (TSDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Data Link Source Select [1:0]	R/W	00 - The data link bits are inserted into the framer through the Transmit HDLC Controller/SLC-96 Fs bits. 01 - The data link bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins. 10 - The data link bits are inserted into the framer through the Transmit Overhead Input Interface via the TxOH_n pins. 11 - The data link bits are forced into 1.

If the Transmit Data Link Source Select bits of the Transmit Data Link Select Register are set to 00, the Transmit HDLC Controller block becomes input source of the data link bits in outgoing DS1 frames.

Each of the framers contains 3 DS1 Transmit High-level Data Link Controller (HDLC) blocks. The function of these blocks is to provide a serial data link channel in DS1 mode through the following:

- Facility Data Link (FDL) bits in ESF framing format mode
- Signaling Framing (Fs) bits in SLC®96 framing format mode
- Remote Signaling (R) bits in T1DM framing format mode
- D or E signaling timeslot channel

Data link bits are automatically inserted into the Facility Data Link (FDL) bits in ESF framing format mode, Signaling Framing (Fs) bits in SLC®96 framing format mode and Remote Signaling (R) bits in T1DM framing format mode or forced to 1 by the framer. Additionally, the user can define any one of the twenty-four DS0 timeslots to be D or E channel. We will discuss how to configure XRT86L34 to transmit data link information through D or E channels in a later section.

Each DS1 Transmit HDLC Controller block contains three major functional modules associated with DS1 framing formats. They are the:

- SLC®96 Data Link Controller
- LAPD Controller
- Bit-Oriented Signaling Processor.

There are two 96-byte transmit message buffers in shared memory for each of the 3 HDLC controllers to transmit data link information. When one message buffer is filled up, the Transmit HDLC Controller automatically switches to the next message buffer to load data link messages. These two message buffers ping-pong among each other for data link message transmission.

The SLC®96 Enable bit and the LAPD Enable bit of the Data Link Control Register (DLCR) determines which one of the three functions is performed by the Transmit HDLC Controller block. The table below shows configuration of the SLC®96 Enable bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) ADDRESS = 0XN113H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	SLC®96 Enable	R/W	0 - In SLC®96 framing mode, the data link transmission is disabled. The framer transmits the regular SF framing bits. In ESF framing mode, the framer transmits regular ESF framing bits and Facility Data Link (FDL) bits. 1 - In SLC®96 framing mode, the data link transmission is enabled. In ESF framing mode, the framer transmits SLC®96-like message in the Facility Data Link bits.

The table below shows configuration of the LAPD Enable bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (ADDRESS = 0XN113H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	LAPD Enable	R/W	0 - The Transmit HDLC Controller will send out Bit-Oriented Signaling (BOS) message. 1 - The Transmit HDLC Controller will send out LAPD protocol or so-called Message-Oriented Signaling (MOS) message.

2.1.2 How to configure XRT86L34 to transmit data link information through D or E Channels

The XRT86L34 can configure any one or ones of the twenty-four DS0 channels to be D or E channels. D channel is used primarily for data link applications. E channel is used primarily for signaling for circuit switching with multiple access configurations.

The Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of each channel determine whether that particular channel is configured as D or E channel. These bits also determine what type of data or signaling conditioning is applied to each channel.

TRANSMIT CHANNEL CONTROL REGISTER (TCCR) (ADDRESS = 0XN300H - 0XN31FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Transmit Data Conditioning Select	R/W	1111 - This channel is configured as D or E timeslot.

If the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register of a particular timeslot are set to 1111, that timeslot is configured as a D or E timeslot.

Any D or E timeslot can be configured to take data link information from the following sources:

- DS1 Transmit Overhead Output Interface Block
- DS1 Transmit HDLC Controller Block
- DS1 Transmit Serial Output Interface Block
- DS1 Transmit Fractional Input Interface Block

The Transmit D or E Channel Source Select [1:0] bits of the Transmit Data Link Select Register (TSDLSR) determines which one of the above-mentioned modules to be input sources of D or E timeslot. The table below shows configuration of the Transmit D or E Channel Source Select [1:0] bits of the Transmit Data Link Select Register (TSDLSR).

TRANSMIT DATA LINK SELECT REGISTER (TSDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Transmit D or E Channel Source Select [1:0]	R/W	00 - The data link bits are inserted into the D or E channel through the Transmit Serial Data input Interface via the TxSer_n pins. 01 - The data link bits are inserted into the D or E channel through the Transmit HDLC Controller. 10 - The data link bits are inserted into the D or E channel through the Transmit Serial Data input Interface via the TxSer_n pins. 11 - The data link bits are inserted into the D or E channel through the Transmit Fractional T1 Input Interface via the TxFrT1_n pins.

For the Transmit HDLC Controller to be input source of D or E channel, the Transmit D or E Channel Source Select [1:0] bits of the Transmit Data Link Select Register has to be set to 01.

2.1.3 Transmit BOS (Bit Oriented Signaling) Processor

The Transmit BOS Processor handles transmission of BOS messages through the DS1 data link channel. It determines how many repetitions a certain BOS message will be transmitted. It also inserts BOS IDLE flag sequence and ABORT sequence to be transmitted on the data link channel. In the later sections, we will discuss BOS message format and how to transmit BOS message.

2.1.3.1 Description of BOS

Bit-Oriented Signaling message is a sixteen-bit pattern carries the form of:

(0d5d4d3d2d1d0011111111)

Where d5 is the MSB and d0 is the LSB. The rightmost "1" is transmitted first. Bit-Oriented Signaling message is classified into the following two groups:

- Priority Codeword Message
- Command and Response Information

Priority Codeword message is preemptive and has the highest priority among all data link information. Priority Codeword information indicates a condition that is affecting the quality of service and thus shall be transmitted until the condition no longer exists. The duration of transmission should not be less than one second. Priority codeword information may be interrupted by software for 100 milliseconds to send maintenance commands with a minimum interval of one second between interruptions. Yellow alarm (00000000 11111111) is the only priority message defined in standard.

Command and response information is transmitted to perform various functions. The BOS Processor send command and response message by transmitting a minimum of 10 repetitions of the appropriate codeword pattern. Command and response data transmission initiates action at the remote end, while the remote end will respond by sending Bit-Oriented response message to acknowledge the received commands. The activation and deactivation of line loop-back and payload loop-back functions are this type of signal.

2.1.3.2 How to configure the BOS Processor Block to transmit BOS

This section describes how to configure the BOS Processor Block to transmit BOS message in a step-by-step basis.

2.1.3.2.1 Step 1: Find out the next available transmit data link buffer

To transmit a bit-oriented signal, a repeating message is sent of the form (0d5d4d3d2d1d0011111111), where the "d5d4d3d2d1d0" represents a six-bit message. The user is recommended to read Transmit Data Link Byte Count Register for next available transmit data link buffer number.

The table below shows how content of the Buffer Enable bit of the Transmit Data Link Byte Count Register (TDLBCR) determines what the next available transmit data link buffer number is.

TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR) (ADDRESS = 0XN114H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Buffer Select	R	0 - The next available transmit data link buffer for sending out BOS or MOS message is Buffer 0. 1 - The next available transmit data link buffer for sending out BOS or MOS message is Buffer 1.

2.1.3.2.2 Step 2: Write BOS Message into transmit data link buffer

After finding out the next available transmit data link buffer, the user should write the eight bits message that are to be transmitted in the form (0d5d4d3d2d1d00) to the first location of the next available transmit data link buffer. The writing of these buffers is through the LAPD Buffer 0 indirect data registers and the LAPD Buffer1 indirect data registers. LAPD Buffer 0 and 1 indirect data registers have addresses 0xn600H and 0xn700H respectively. There is no indirect address register for transmit data link buffer 0 and 1.

A microcontroller WRITE access to the LAPD Buffer indirect data registers will access the transmit data link buffer and a microcontroller READ will access the receive data link buffers. The very first WRITE access to the LAPD Buffer indirect data register will always be direct to location 0 within the transmit data link buffer.

For example, if the BOS Message to be sent is (101011) and the next available transmit data link buffer of Channel n is 1. The user should write pattern (01010110) into transmit data link buffer 1 of Channel n. The following microprocessor access to the framer should be done:

WR n7H 56H

2.1.3.2.3 Step 3: Program BOS Message transmission repetitions

The user should program the value of message transmission repetitions into the Transmit Data Link Byte Count Register. The framer will transmit the BOS message the same number of times as was stored in the Transmit Data Link Byte Count Register (TDLBCR) before generating the Transmit End of Transfer (TxEOT) interrupts. If the value stored inside the Transmit Data Link Byte Count Register (TDLBCR) is set to 0, the message will be transmitted indefinitely and no Transmit End of Transfer interrupt will be generated.

The table below shows configurations of the Transmit Data Link Byte Count [6:0] bits the Transmit Data Link Byte Count Register (TDLBCR).

TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR) (ADDRESS = 0XN114H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6-0	Transmit Data Link Byte Count [6:0]	R/W	Value of these bits determines how many times a BOS message pattern will be transmitted by the framer before generating the Transmit End of Transfer (TxEOT) interrupt. ***NOTE:*** *If these bits are set to 0, the BOS message will be transmitted indefinitely and no Transmit End of Transfer interrupts will be generated.*

2.1.3.2.4 Step 4: Configure BOS Message transmission control bits

Configuration of the Data Link Control Register determines whether the BOS Processor will insert IDLE flag character or ABORT sequence to the data link channel. It also determines how the transition between MOS mode to BOS mode is done.

If the IDLE Insertion bit of the Data Link Control Register is set, repeated flags of value 0x7E are transmitted as soon as the current operation is finished (defined by the value in Transmit Data Link Byte Count Register). However, if the Transmit Data Link Byte Count value is zero, the framer will not force a flag sequence on to the data link channel.

The table below shows configurations of the IDLE Insertion bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (ADDRESS = 0XN113H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	IDLE Insertion	R/W	0 - No flag sequence is sent on the data link channel. 1 - The framer forces a flag sequence of value 0x7E onto the data link channel.

If the ABORT bit of the Data Link Control Register is set, a BOS abort sequence (9 consecutive ones) is transmitted on the data link channel following by all-one transmission. In other words, all data link bits will be set to 1 after the transmission of the current message byte.

The table below shows configurations of the ABORT bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (ADDRESS = 0XN113H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	ABORT	R/W	0 - No ABORT sequence is sent on the data link channel. 1 - The framer forces an ABORT sequence of pattern (111111111) onto the data link channel. All data link bits will be set to 1 after sending the ABORT sequence.

Switching the data link channel from MOS mode to BOS mode while a message is being transmitted will interrupt the message after the octet in progress is transmitted. If the MOS ABORT bit of the Data Link Control Register is set, a MOS ABORT sequence (a zero followed by 7 ones) will be inserted before switching. Switching the data link from BOS to LAPD will not take place until the current operation completes if Transmit BOS byte count is not set to zero initially. If the Transmit BOS byte count value is set to zero, the transition from BOS mode to MOS mode will take place right after finishing the current message octet.

The table below shows configurations of the MOS ABORT bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (ADDRESS = 0XN113H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	MOS ABORT	R/W	0 - The framer forces an MOS ABORT sequence of one zero and seven ones (01111111) onto the data link channel during the transition from MOS mode to BOS mode. 1 - No MOS ABORT sequence is sent on the data link channel during the transition from MOS mode to BOS mode.

2.1.3.2.5 Step 5: Enable transmit BOS message interrupts

The BOS Processor can generate a couple of interrupts indicating the status of BOS message transmission to the microprocessor. These are the Transmit Start of Transfer (TxSOT) interrupt and the Transmit End of Transfer (TxEOT) interrupt.

To enable these interrupts, the Transmit Start of Transfer Enable bit and the Transmit End of Transfer Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Transmit Start of Transfer Enable bit and the Transmit End of Transfer Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (ADDRESS = 0XNB07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Transmit Start of Transfer Enable	R/W	0 - The Transmit Start of Transfer interrupt is disabled. 1 - The Transmit Start of Transfer interrupt is enabled.
4	Transmit End of Transfer Enable	R/W	0 - The Transmit End of Transfer interrupt is disabled. 1 - The Transmit End of Transfer interrupt is enabled.

The table below shows configurations of the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	HDLC Controller Interrupt Enable	R/W	0 - Every interrupt generated by the HDLC Controller is disabled. 1 - Every interrupt generated by the HDLC Controller is enabled.

When these interrupt enable bits are set and the BOS message is transmitted to the data link channel, the BOS Processor changes the Transmit Start of Transfer and Transmit End of Transfer status bits of the Data Link Status Register (DLSR). These two status indicators are valid until the Data Link Status Register is read. Reading these register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Transmit Start of Transfer and Transmit End of Transfer status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (ADDRESS = 0XNB06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Transmit Start of Transfer	RUR / WC	0 - There is no data link message to be sent to the data link channel. 1 - The HDLC Controller will send a data link message to the data link channel.
4	Transmit End of Transfer	RUR / WC	0 - No data link message was sent to the data link channel. 1 - The HDLC Controller finished sending a data link message to the data link channel.

2.1.3.2.6 Step 6: BOS message transmission

A zero is then written into the LAPD enable bit of Data Link Control Register, which sets the transmitter to Bit-Oriented mode and kicks off the transmission process. The LAPD Controller latches these control bits of the Data Link Control Register and send a Transmit Start of Transfer interrupt (TxSOT) to the microprocessor to indicate that a BOS message will be send. After the required number of times of BOS message is sent, the LAPD Controller generates an Transmit End of Transfer interrupt (TxEOT) to the microprocessor to indicate that the BOS message transmission comes to an end.

The table below shows configurations of the LAPD Enable bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (ADDRESS = 0XN113H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	LAPD Enable	R/W	0 - The Transmit HDLC Controller will send out Bit-Oriented Signaling (BOS) message. 1 - The Transmit HDLC Controller will send out LAPD protocol or so-called Message-Oriented Signaling (MOS) message.

2.1.4 Transmit MOS (Message Oriented Signaling) or LAPD Controller

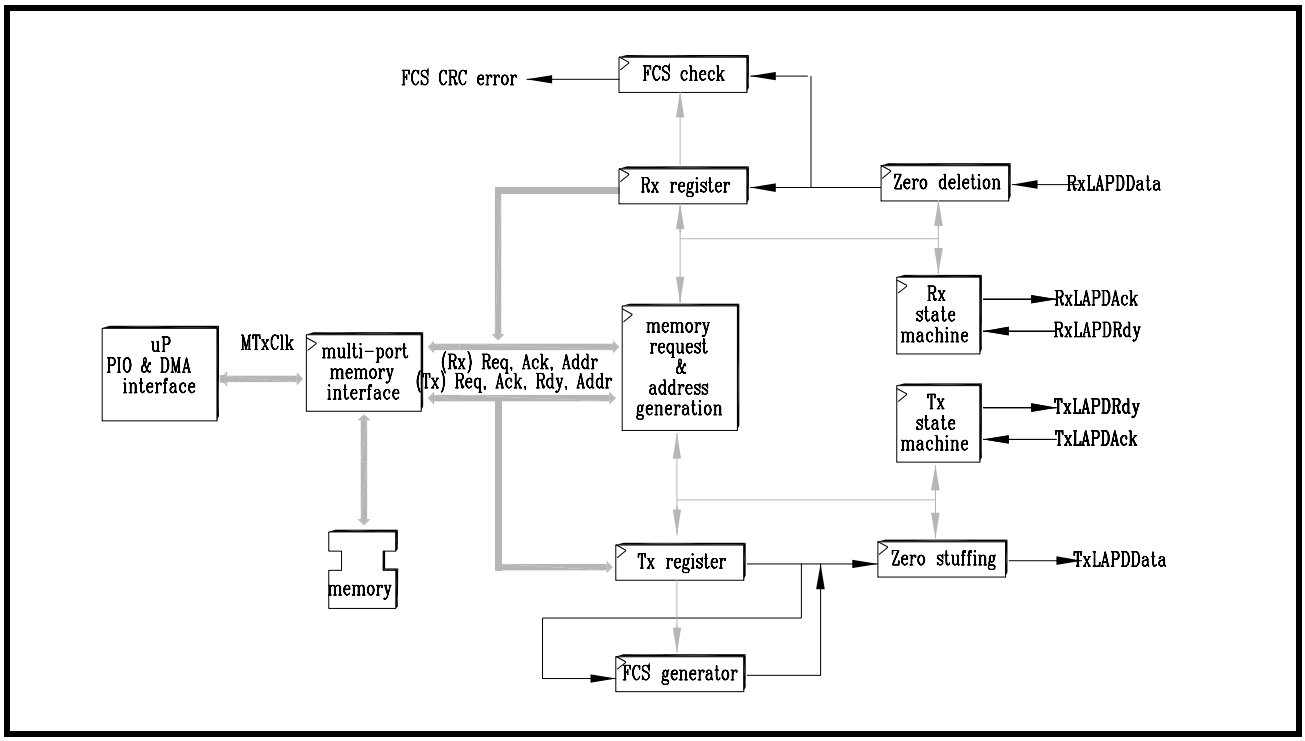
The Transmit LAPD controller implements the Message-Oriented protocol based on ITU Recommendation Q.921 Link Access Procedures on the D-channel (LAPD) type of protocol. It provides the following functions:

- Zero stuffing
- T1/E1 transmitter interface

- Transmit message buffer access
- Frame check sequence generation
- IDLE flag insertion
- ABORT sequence generation

Two 96-byte buffers in shared memory are allocated for LAPD transmitter to reduce the frequency of microprocessor interrupts and alleviate the response time requirement for microprocessor to handle each interrupt. There are no restrictions on the length of the message. However the 96-byte buffer is deep enough to hold one entire LAPD path or test signal identification message. Figure 8 depicts the block diagram of both transmit and receive LAPD controller.

FIGURE 8. LAPD CONTROLLER



In the later sections, we will briefly discuss MOS message format and how to configure the LAPD Controller to transmit MOS message.

2.1.4.1 Discussion of MOS

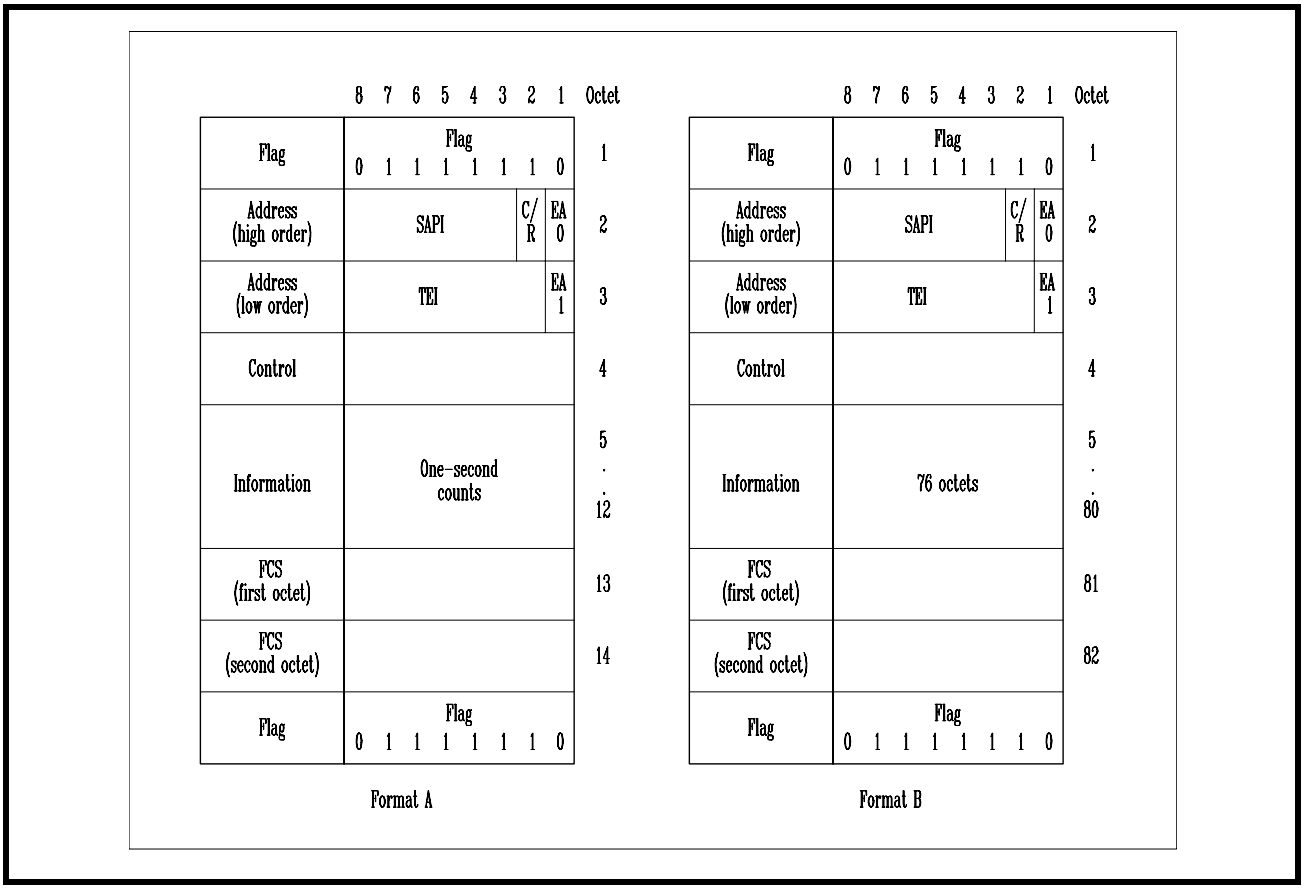
Message-Oriented signals (MOS) sent by the transmit LAPD Controller are messages conforming to ITU Recommendation Q.921 LAPD protocol as defined below.

Two types of Message-Oriented signals are defined. One is a periodic performance report generated by the source or sink T1/E1 terminals as defined by ANSI T1.403. The other is a path or test signal identification message that may be optionally generated by a terminal or intermediate equipment on a T1/E1 circuit.

Message-oriented signals shall use the frame structure, field definitions and elements of procedure of the LAPD protocol defined in ITU recommendation Q.921 except the address field. Performance information is carried by Message-Oriented signal using LAPD protocol. The message structures of the periodic performance

report and path or test signal identification message are shown in Figure 9 in format A and format B respectively.

FIGURE 9. LAPD FRAME STRUCTURE



2.1.4.1.1 Periodic Performance Report

The ANSI T1.403 standard requires that the status of the transmission quality be reported every one-second interval. The one-second timing may be derived from the DS1 signal or from a separate equally accurate (±32ppm) source. The phase of the one-second periods with respect to the occurrence of error events is arbitrary; that is, the one-second timing does not depend on the time of occurrence of any error event. A total of four seconds of information is transmitted so that recovery operations may be initiated in case an error corrupts a message.

Counts of events shall be accumulated in each contiguous one-second interval. At the end of each one-second interval, a modulo-4 counter shall be incremented, and the appropriate performance bits shall be set in bytes 5 and 6 in Format A. These octets and the octets that carry the performance bits of the preceding three one-second intervals form the periodic performance report.

The periodic performance report is made up of 14 bytes of data. Bytes 1 to 4, 13, and 14 are the message header and bytes 5 to 12 contain data regarding the four most-recent one-second intervals. The periodic performance report message uses the SAPI/TEI value of 14.

2.1.4.1.2 Transmission-Error Event

Occurrences of transmission-error events indicate the quality of transmission. The occurrences that shall be detected and reported are:

- CRC Error Event: A CRC-6 error event is the occurrence of a received CRC code that is not identical to the corresponding locally calculated code.

- Severely Errored Framing Event: A severely-errored-framing event is the occurrence of two or more framing-bit-pattern errors within a 3-ms period. Contiguous 3-ms intervals shall be examined. The 3-ms period may coincide with the ESF. The severely-errored-framing event, while similar in form to criteria for declaring a terminal has lost framing, is only designed as a performance indicator; existing terminal out-of-frame criteria will continue to serve as the basis for terminal alarms.
- Frame-Synchronization-Bit Error Event: A frame-synchronization-bit-error event is the occurrence of a received framing-bit-pattern not meeting the severely-errored-framing event criteria.
- Line-Code Violation event: A line-code violation event is a bipolar violation of the incoming data. A line-code violation event for an B8ZS-coded signal is the occurrence of a received excessive zeros (EXZ) or a bipolar violation that is not part of a zero-substitution code.
- Controlled Slip Event: A controlled-slip event is a replication, or deletion, of a T1 frame by the receiving terminal. A controlled slip may occur when there is a difference between the timing of a synchronous receiving terminal and the received signal.

2.1.4.1.3 Path and Test Signal Identification Message

The path identification message is used to identify the path between the source terminal and the sink terminal. The test signal identification message is used by test signal generating equipment. Both identification messages are made up of 82 bytes of data. Byte 1 to 4, 81 and 82 are the message header and bytes 5 to 80 contain six data elements. These messages use the SAPI/TEI value of 15 to differentiate themselves from the performance report message.

2.1.4.1.4 Frame Structure

The message structure of message-oriented signal is shown in Figure 9. Two format types are shown in the figure: format A for frames which are sending performance report message and format B for frames which containing a path or test signal identification message. The following abbreviations are used:

- SAPI: Service Access Point Identifier
- C/R: Command or Response
- EA: Extended Address
- TEI: Terminal Endpoint Identifier
- FCS: Frame Check Sequence

2.1.4.1.5 Flag Sequence

All frames shall start and end with the flag sequence consisting of one 0 bit followed by six contiguous 1 bits and one 0 bit. The flag preceding the address field is defined as the opening flag. The flag following the Frame Check Sequence (FCS) field is defined as the closing flag. The closing flag may also serve as the opening flag of the next frame, in some applications. However, all receivers must be able to accommodate receipt of one or more consecutive flags.

2.1.4.1.6 Address Field

The address field consists of two octets. A single octet address field is reserved for LAPB operation in order to allow a single LAPB data link connection to be multiplexed along with LAPD data link connections.

2.1.4.1.7 Address Field Extension bit (EA)

The address field range is extended by reserving bit 1 of the address field octets to indicate the final octet of the address field. The presence of a 1 in bit 1 of an address field octet signals that it is the final octet of the address field. The double octet address field for LAPD operation shall have bit 1 of the first octet set to a 0 and bit 1 of the second octet set to 1.

2.1.4.1.8 Command or Response bit (C/R)

The Command or Response bit identifies a frame as either a command or a response. The user side shall send commands with the C/R bit set to 0, and responses with the C/R bit set to 1. The network side shall do the opposite; That is, commands are sent with C/R bit set to 1, and responses are sent with C/R bit set to 0.

2.1.4.1.9 Service Access Point Identifier (SAPI)

The Service Access Point Identifier identifies a point at which data link layer services are preceded by a data link layer entity type to a layer 3 or management entity. Consequently, the SAPI specifies a data link layer entity

type that should process a data link layer frame and also a layer 3 or management entity, which is to receive information carried by the data link layer frame. The SAPI allows 64 service access points to be specified, where bit 3 of the address field octet containing the SAPI is the least significant binary digit and bit 8 is the most significant. SAPI values are 14 and 15 for performance report message and path or test signal identification message respectively.

2.1.4.1.10 Terminal Endpoint Identifier (TEI)

The TEI sub-field allows 128 values where bit 2 of the address field octet containing the TEI is the least significant binary digit and bit 8 is the most significant binary digit. The TEI sub-field bit pattern 111 1111 (=127) is defined as the group TEI. The group TEI is assigned permanently to the broadcast data link connection associated with the addressed Service Access Point (SAP). TEI values other than 127 are used for the point-to-point data link connections associated with the addressed SAP. Non-automatic TEI values (0-63) are selected by the user, and their allocation is the responsibility of the user. The network automatically selects and allocates TEI values (64-126).

2.1.4.1.11 Control Field

The control field identifies the type of frame which will be either a command or response. The control field shall consist of one or two octets. Three types of control field formats are specified: 2-octet numbered information transfer (I format), 2-octet supervisory functions (S format), and single-octet unnumbered information transfers and control functions (U format). The control field for T1/E1 message is categorized as a single-octet unacknowledged information transfer having the value 0x03.

2.1.4.1.12 Frame Check Sequence (FCS) Field

The source of either the performance report or an identification message shall generate the frame check sequence. The FCS field shall be a 16-bit sequence. It shall be the ones complement of the sum (modulo 2) of:

- The remainder of xk (x15 + x14 + x13 + x12 + x11 + x10 + x9 + x8 + x7 + x6 + x5 + x4 + x3 + x2 + x + 1) divided (modulo 2) by the generator polynomial x16 + x12 + x5 + 1, where k is the number of bits in the frame existing between, but not including, the final bit of the opening flag and the first bit of the FCS, excluding bits inserted for transparency, and
- The remainder of the division (modulo 2) by the generator polynomial x16 + x12 + x5 + 1, of the product of x16 by the content of the frame existing between, but not including, the final bit of the opening flag and the first bit of the FCS, excluding bits inserted for transparency.

As a typical implementation at the transmitter, the initial content of the register of the device computing the remainder of the division is preset to all 1s and is then modified by division by the generator polynomial on the address, control and information fields; the ones complement of the resulting remainder is transmitted as the 16-bit FCS.

As a typical implementation at the receiver, the initial content of the register of the device computing the remainder is preset to all 1s. The final remainder, after multiplication by x16 and then division (modulo 2) by the generator polynomial x16 + x12 + x5 + 1 of the serial incoming protected bits and the FCS, will be 0001110100001111 (x15 through x0, respectively) in the absence of transmission errors.

2.1.4.1.13 Transparency (Zero Stuffing)

A transmitting data link layer entity shall examine the frame content between the opening and closing flag sequences, (address, control, information and FCS field) and shall insert a 0 bit after all sequences of five contiguous 1 bits (including the last five bits of the FCS) to ensure that an IDLE flag or an Abort sequence is not simulated within the frame. A receiving data link layer entity shall examine the frame contents between the opening and closing flag sequences and shall discard any 0 bit which directly follows five contiguous 1 bits.

2.1.4.2 How to configure the Transmit HDLC Controller Block to transmit MOS

This section describes how to configure the LAPD Controller Block to transmit MOS message in a step-by-step basis.

2.1.4.2.1 Step 1: Find out the next available transmit data link buffer

To transmit MOS message, the user is recommended to read Transmit Data Link Byte Count Register for next available transmit buffer number.

The table below shows how contents of the Buffer Enable bit of the Transmit Data Link Byte Count Register (TDLBCR) determines what the next available transmit buffer number is.

TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR) (ADDRESS = 0XN114H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Buffer Select	R	0 - The next available transmit buffer for sending out BOS or MOS message is Buffer 0. 1 - The next available transmit buffer for sending out BOS or MOS message is Buffer 1.

2.1.4.2.2 Step 2: Write MOS Message into transmit data link buffer

After finding out the next available transmit buffer, the user should write the entire message data to the available transmit data link buffer via PIO or DMA access. The writing of these buffers is through the LAPD Buffer 0 indirect data registers and the LAPD Buffer1 indirect data registers. LAPD Buffer 0 and 1 indirect data registers have addresses 0xn600H and 0xn700H respectively. There is no indirect address register for transmit data link buffer 0 and 1.

A microcontroller WRITE access to the LAPD Buffer indirect data registers will access the transmit data link buffer and a microcontroller READ will access the receive data link buffers. The very first WRITE access to the LAPD Buffer indirect data register will always be direct to location 0 within the transmit data link buffer. The next WRITE access to the LAPD Buffer indirect data register will be direct to location 1 within the transmit data link buffer and so on, until all 96 bytes of the transmit buffer is filled.

For example, if the first byte of the MOS message to be sent is (01010110) and the next available transmit data link buffer of Channel n is 1. The user should write pattern (01010110) into transmit data link buffer 1 of Channel n. The following microprocessor access to the framer should be done:

WR n7H 56H

The first byte of MOS message is written into location 0 of the transmit data link buffer. If the next byte of the MOS message is (10100101), the user should perform another microprocessor WRITE access:

WR n7H A5H

The second byte of MOS message is written into location 1 of the transmit data link buffer. The WRITE access should be repeated until the entire block of MOS message is written into the transmit buffer or the transmit buffer is completely filled.

2.1.4.2.3 Step 3: Program the Transmit Data Link Byte Count Register

The user should program byte count of the MOS message into the Transmit Data Link Byte Count Register after the whole block of data is present in the buffer memory.

The table below shows configurations of the Transmit Data Link Byte Count [6:0] bits the Transmit Data Link Byte Count Register (TDLBCR).

TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR) (ADDRESS = 0XN114H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6-0	Transmit Data Link Byte Count [6:0]	R/W	Value of these bits determines length of the MOS message pattern to be transmitted by the framer before generating the Transmit End of Transfer (TxEOT) interrupt.

2.1.4.2.4 Step 4: Configure MOS Message transmission control bits

Configuration of the Data Link Control Register determines whether the LAPD Controller will insert IDLE flag character, FCS or ABORT sequence to the data link channel. It also determines how the transition between MOS mode to BOS mode is done.

If the IDLE Insertion bit of the Data Link Control Register is set, repeated flags of value 0x7E are transmitted as soon as the current operation is finished (defined by the value in Transmit Data Link Byte Count Register). The IDLE bit must be set to 1 at the last block of transfer to enable FCS and flag insertion for message completion.

The table below shows configurations of the IDLE Insertion bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (ADDRESS = 0XN113H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	IDLE Insertion	R/W	0 - No flag sequence is sent on the data link channel. 1 - The framer forces a flag sequence of value 0x7E onto the data link channel.

NOTE: *If the entire message is longer than 96-byte in length or more than one full block of message has to be transmitted, the IDLE Insertion bit should not be set to one until the last block of message has to be sent.*

If the FCS Insertion bit of the Data Link Control Register (DLCR) is set to high, the LAPD Controller will calculate and insert the frame check sequence to the last block of the transmitted message.

The table below shows configurations of the FCS Insertion bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (ADDRESS = 0XN113H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	FCS Insertion	R/W	0 - No FCS will be inserted into the last block of the transmitted MOS message. 1 - The LAPD Controller will calculate and insert the FCS into the last block of the transmitted MOS message.

If the FCS is not enabled at the end of a message, the controller will return to sending IDLE flags immediately after the last octet is transmitted. This permits the use of a programmable FCS, which may be used for diagnostic tests or other test applications.

To abort a transmitting message, the LAPD Controller sets the ABORT bit in Data Link Control Register to 1. This bit is cleared after the LAPD transmitter finishes sending the message octet in progress. The transmitter then transmit an ABORT sequence of one zero followed by seven ones (01111111) before goes to idle if the IDLE bit is set. The transmitter will keep transmitting IDLE flag characters until it is instructed otherwise.

The table below shows configurations of the ABORT bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (ADDRESS = 0XN113H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	ABORT	R/W	0 - No ABORT sequence is sent on the data link channel. 1 - The framer forces an ABORT sequence of pattern (111111 10) onto the data link channel. IDLE flag pattern will be transmitted after the ABORT sequence is sent.

Switching the data link channel from MOS mode to BOS mode while a message is being transmitted will interrupt the message after the octet in progress is transmitted. If the MOS ABORT bit of the Data Link Control Register is set, a MOS ABORT sequence (a zero followed by 7 ones) will be inserted before switching. Switching the data link from BOS to LAPD will not take place until the current operation completes if Transmit BOS byte count is not set to zero initially. If the Transmit BOS byte count value is set to zero, the transition from BOS mode to MOS mode will take place right after finishing the current message octet.

The table below shows configurations of the MOS ABORT bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (ADDRESS = 0XN113H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	MOS ABORT	R/W	0 - The framer forces an MOS ABORT sequence of one zero and seven ones [0111 1111] onto the data link channel during the transition from MOS mode to BOS mode. 1 - No MOS ABORT sequence is sent on the data link channel during the transition from MOS mode to BOS mode.

2.1.4.2.5 Step 5: Enable transmit MOS message interrupts

The LAPD Controller can generate a couple of interrupts indicating the status of MOS message transmission to the microprocessor. These are the Transmit Start of Transfer (TxSOT) interrupt and the Transmit End of Transfer (TxEOT) interrupt.

To enable these interrupts, the Transmit Start of Transfer Enable bit and the Transmit End of Transfer Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Transmit Start of Transfer Enable bit and the Transmit End of Transfer Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (ADDRESS = 0XNB07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Transmit Start of Transfer Enable	R/W	0 - The Transmit Start of Transfer interrupt is disabled. 1 - The Transmit Start of Transfer interrupt is enabled.
4	Transmit End of Transfer Enable	R/W	0 - The Transmit End of Transfer interrupt is disabled. 1 - The Transmit End of Transfer interrupt is enabled.

The table below shows configurations of the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	HDLC Controller Interrupt Enable	R/W	0 - Every interrupt generated by the HDLC Controller is disabled. 1 - Every interrupt generated by the HDLC Controller is enabled.

When these interrupt enable bits are set and the MOS message is transmitted to the data link channel, the LAPD Controller changes the Transmit Start of Transfer and Transmit End of Transfer status bits of the Data Link Status Register (DLSR). These two status indicators are valid until the Data Link Status Register is read. Reading these register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Transmit Start of Transfer and Transmit End of Transfer status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (ADDRESS = 0XNB06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Transmit Start of Transfer	RUR / WC	0 - There is no data link message to be sent to the data link channel. 1 - The HDLC Controller will send a data link message to the data link channel.
4	Transmit End of Transfer	RUR / WC	0 - No data link message was sent to the data link channel. 1 - The HDLC Controller finished sending a data link message to the data link channel.

2.1.4.2.6 Step 6: MOS message transmission

A one is then written into the LAPD enable bit of Data Link Control Register, which sets the transmitter to Message-Oriented mode and kicks off the transmission process. The LAPD controller latches these control bits of the Data Link Control Register and send a Transmit Start of Transfer interrupt (TxSOT) to the microprocessor to indicate that an MOS message will be send.

The LAPD transmitter will then transmit the open flag character (01111110) in the data link bit position first followed by the entire message. If the message is longer than 96 bytes or more than one full block of data are to be transmitted, the alternating buffer usage approach will provide more adequate time to allow the writing of the message in the Ping-Pong buffers without overwriting good data in the transmitting buffer or repeating data because it was written too late. User must fill in data fast enough in Ping-Pong buffer concatenation scenario to avoid automatic flag insertion between two blocks of data that will cause far-end FCS errors.

After the entire MOS message is sent, the LAPD Controller generates the Transmit End of Transfer (TxEOT) interrupt to the microprocessor indicating that the MOS message transmission is over.

The table below shows configurations of the LAPD Enable bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (ADDRESS = 0XN113H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	LAPD Enable	R/W	0 - The Transmit HDLC Controller will send out Bit-Oriented Signaling (BOS) message. 1 - The Transmit HDLC Controller will send out LAPD protocol or so-called Message-Oriented Signaling (MOS) message.

2.1.5 Transmit SLCâ96 Data link Controller

The SLC®96 T1 format is invented by AT&T and is used between the Digital Switch and a SLC®96 formatted remote terminal. The purpose of the SLC®96 product is to provide standard telephone service or Plain Old Telephone Service (POTS) in areas of high subscriber density but back-haul the traffic over T1 facilities.

To support the SLC®96 formatted remote terminal equipment, which is likely in an underground location, the T1s needed methods to:

- Indicate equipment failures of the equipment to maintenance personal
- Indicate failures of the POTS lines
- Test the POTS lines
- Provide redundancy on the T1s

The SLC®96 framing format is a D4 Super-frame (SF) format with specialized data link information bits. These data link information bits take the position of the Super-frame Alignment (Fs) bit positions. These bits consist of:

- Concentrator bits (C, bit position 1 to 11)
- First Spoiler bits (FS, bit position 12 to 14)
- Maintenance bits (M, bit position 15 to 17)
- Alarm bits (A, bit position 18 to 19)
- Protection Line Switch bits (S, bit position 20 to 23)
- Second Spoiler bit (SS, bit position 24)
- Resynchronization pattern (000111000111)

In SLCâ96 mode, six six-bit data will generate one 9-ms frame of the SLCâ96 message format. The format of the data link message is given in BELLCORE TR-TSY-000008. To select this mode, the Framing Select bits of the Framing Select Register (FSR) must be set to binary number 100. The table below shows configuration of the Framing Select bits of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (ADDRESS = 0XN107H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2-0	T1 Framing Select	R/W	**T1 Framing Select:** These READ/WRITE bit-fields allow the user to select one of the five T1 framing formats supported by the framer. These framing formats include ESF, SLC®96, SF, N and T1DM mode. **NOTE:** *Changing of framing format will automatically force the framer to RESYNC.*

Framing Format	Bit 2	Bit 1	Bit 0
ESF	0	X	X
SLC®96	1	0	0
SF	1	0	1
N	1	1	0
T1DM	1	1	1

When SLC®96 mode is enabled, the Fs bit is replaced by the data link message read from memory at the beginning of each D4 super-frame. The XRT86L34 allocates two 6-byte buffers to provide the SLC®96 Data Link Controller an alternating access mechanism for information transmission. The bit ordering and usage is shown in the following table; and the LSB is sent first. Note that these registers are memory-based storage and they need to be initialized.

TRANSMIT SLC®96 MESSAGE REGISTERS

BITBYTE	5	4	3	2	1	0
1	0	1	1	1	0	0
2	C1	1	1	1	0	0
3	C7	C6	C5	C4	C3	C2
4	1	0	C11	C10	C9	C8
5	A2	A1	M3	M2	M1	0
6	0	1	S4	S3	S2	S1

Each register is read out of memory once every six SF super-frames. The memory holding these registers owns a shared memory structure that is used by multiple devices. These include DS1 transmit module, DS1 receive module, Transmit LAPD Controller, Transmit SLCâ96 Data Link controller, Bit-Oriented Signaling Processor, Receive LAPD Controller, Receive SLCâ96 Data Link Controller, Receive Bit-Oriented Signaling Processor and microprocessor interface module.

2.1.5.1 How to configure the SLC®96 Data Link Controller to transmit SLC®96 Data Link Messages

This section describes how to configure the SLC®96 Data Link Controller to transmit SLC®96 Data Link message in a step-by-step basis.

2.1.5.1.1 Step 1: Find out the next available transmit data link buffer

To transmit SLC®96 Data Link message, the user is recommended to read Transmit Data Link Byte Count Register for next available transmit buffer number.

The table below shows how contents of the Buffer Enable bit of the Transmit Data Link Byte Count Register (TDLBCR) determines what the next available transmit buffer number is.

TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR) (ADDRESS = 0XN114H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Buffer Select	R	0 - The next available transmit buffer for sending out BOS or MOS message is Buffer 0. 1 - The next available transmit buffer for sending out BOS or MOS message is Buffer 1.

2.1.5.1.2 Step 2: Write SLC®96 Data Link Message into transmit data link buffer

After finding out the next available transmit buffer, the user should write the entire message data to the available transmit data link buffer via PIO or DMA access. The writing of these buffers is through the LAPD Buffer 0 indirect data registers and the LAPD Buffer1 indirect data registers. LAPD Buffer 0 and 1 indirect data registers have addresses 0xn600H and 0xn700H respectively. There is no indirect address register for transmit data link buffer 0 and 1.

A microcontroller WRITE access to the LAPD Buffer indirect data registers will access the transmit data link buffer and a microcontroller READ will access the receive data link buffers. The very first WRITE access to the LAPD Buffer indirect data register will always be direct to location 0 within the transmit data link buffer. The next WRITE access to the LAPD Buffer indirect data register will be direct to location 1 within the transmit data link buffer and so on, until all 96 bytes of the transmit buffer is filled.

For example, if the first byte of the SLC®96 Data Link message to be sent is (101011) and the next available transmit data link buffer of Channel n is 1. The user should write pattern (00101011) into transmit data link buffer 1 of Channel n. The following microprocessor access to the framer should be done:

WR n7H 2BH

The first byte of the SLC®96 Data Link message is written into location 0 of the transmit data link buffer. If the next byte of the data link message is (101001), the user should perform another microprocessor WRITE access of pattern (00101001):

WR n7H 29H

The second byte of data link message is written into location 1 of the transmit data link buffer. The WRITE access should be repeated until all six bytes of SLC®96 Data Link message is written into the transmit buffer or the transmit buffer is completely filled.

2.1.5.1.3 Step 3: Enable transmit data link message interrupt

The SLC®96 Data Link Controller can generate the Transmit Start of Transfer (TxSOT) interrupt indicating the status of data link message transmission to the microprocessor. To enable this interrupt, the Transmit Start of Transfer Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Transmit Start of Transfer Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (ADDRESS = 0XNB07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Transmit Start of Transfer Enable	R/W	0 - The Transmit Start of Transfer interrupt is disabled. 1 - The Transmit Start of Transfer interrupt is enabled.

The table below shows configurations of the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	HDLC Controller Interrupt Enable	R/W	0 - Every interrupt generated by the HDLC Controller is disabled. 1 - Every interrupt generated by the HDLC Controller is enabled.

When this interrupt enable bit is set and the SLC®96 Data Link message is transmitted to the data link channel, the SLC®96 Data Link Controller changes the Transmit Start of Transfer status bits of the Data Link Status Register (DLSR). This status indicator is valid until the Data Link Status Register is read. Reading this register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Transmit Start of Transfer and Transmit End of Transfer status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (ADDRESS = 0XNB06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Transmit Start of Transfer	RUR / WC	0 - There is no data link message to be sent to the data link channel. 1 - The SLC®96 Data Link Controller will send SLC®96 data link message to the data link channel.

2.1.5.1.4 Step 4: Program the Data Link Control Register to activate SLC®96 Data Link Transmission

The SLC®96 Enable bit and the LAPD Enable bit of the Data Link Control Register (DLCR) determines which one of the three functions is performed by the Transmit HDLC Controller block. The table below shows configuration of the SLC®96 Enable bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (ADDRESS = 0XN113H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	SLC®96 Enable	R/W	0 - In SLC®96 framing mode, the data link transmission is disabled. The framer transmits the regular SF framing bits. In ESF framing mode, the framer transmits regular ESF framing bits and Facility Data Link (FDL) bits. 1 - In SLC®96 framing mode, the data link transmission is enabled. In ESF framing mode, the framer transmits SLC®96-like message in the Facility Data Link bits.

The table below shows configuration of the LAPD Enable bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (ADDRESS = 0XN113H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	LAPD Enable	R/W	0 - The Transmit HDLC Controller will send out Bit-Oriented Signaling (BOS) message. 1 - The Transmit HDLC Controller will send out LAPD protocol or so-called Message-Oriented Signaling (MOS) message.

To enable SLC®96 data link transmission, the user has to set both of the SLC®96 Enable bit and the LAPD Enable bit of the Data Link Control Register to 1.

Without inputting new message, the data link controller will loop on the same message over and over again. To force the data link to output all ones is done by setting the ABORT bit in Data Link Control Register to 1. This operation takes place after the current message finishes transmitting. The table below shows configurations of the ABORT bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (ADDRESS = 0XN113H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	ABORT	R/W	0 - No ABORT sequence is sent on the data link channel. 1 - The framer forces an ABORT sequence of pattern (111111 10) onto the data link channel.

Setting the SLCâ96 bit low will switch the data link back to transfer normal framing bits after the current message transmit completes.

2.2 AUTOMATIC PERFORMANCE REPORT (APR)

The APR feature allows the system to transmit PMON status within a LAPD Framing format A at one second intervals or within a single shot report. The data octets 5 through 12 within the LAPD frame are replaced with the PMON status for the previous one second interval.

TABLE 167: FRAMING FORMAT FOR PMON STATUS INSERTED WITHIN LAPD BY INITIATING APR

Octet Number	8	7	6	5	4	3	2	1	Time (s)
1	Flag = 01111110								
2	SAPI = 001110						CR	EA=0	
3	TEI = 0000000							EA=1	
4	Control = 00000011 = Unacknowledged Frame								
5	G3	LV	G4	U1	U2	G5	SL	G6	T_0
6	FE	SE	LB	G1	R	G2	Nm	Ni	
7	G3	LV	G4	U1	U2	G5	SL	G6	T_0 - 1
8	FE	SE	LB	G1	R	G2	Nm	Ni	
9	G3	LV	G4	U1	U2	G5	SL	G6	T_0 - 2
10	FE	SE	LB	G1	R	G2	Nm	Ni	
11	G3	LV	G4	U1	U2	G5	SL	G6	T_0 - 3
12	FE	SE	LB	G1	R	G2	Nm	Ni	
13	FCS								
14									
15	Flag = 01111110								

NOTE: *The right most bit (bit 1) is transmitted first for all fields except for the two bytes of the FCS that are transmitted left most bit (bit 8) first.*

2.2.1 Bit Value Interpretation

G1 = 1 if number of CRC error events is equal to 1

G2 = 1 if number of CRC error events is greater than 1 or equal to 5

G3 = 1 if number of CRC error events is greater than 5 or equal to 10

G4 = 1 if number of CRC error events is greater than 10 or equal to 100

G5 = 1 if number of CRC error events is greater than 100 or equal to 319

G6 = 1 if number of CRC error events is equal to 320

SE = 1 if a severely errored framing event occurs (FE shall be 0)

FE = 1 if a framing synchronization bit error event occurs (SE shall be 0)

LV = 1 if a line code violation event occurs

SL = 1 if slip event within the slip buffer occurs

LB = 1 if payload loopback is activated

U1 = Not Used (default = 0)

U2 = Not Used (default = 0)

R = Not Used (default = 0)

NmNi = One second report module 4 count

2.3 DS1 Receive HDLC Controller Block

2.3.1 Description of the DS1 Receive HDLC Controller Block

XRT86L34 allows user to extract data link information from incoming DS1 frames. The data link information in DS1raming format mode can be extracted to the following:

- DS1 Receive Overhead Output Interface Block
- DS1 Receive HDLC Controller
- DS1 Receive Serial Output Interface

The Receive Data Link Source Select [1:0] bits, within the Receive Data Link Select Register (RSDLSR) determine destinations of the data link bits (Facility Data Link (FDL) bits in ESF framing format mode, Signaling Framing (Fs) bits in SLC®96 framing format mode and Remote Signaling (R) bits in T1DM framing format mode) extracted from the incoming DS1 frames.

The table below shows configuration of the Receive Data Link Source Select [1:0] bits of the Receive Data Link Select Register (RSDLSR).

RECEIVE DATA LINK SELECT REGISTER (RSDLSR) (ADDRESS = 0XN10CH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Receive Data Link Source Select [1:0]	R/W	00 - The data link bits extracted from the incoming DS1 frame are sent to the Receive HDLC Controller. 01 - The data link bits extracted from the incoming DS1 frame are sent to the Receive Serial Data Output Interface via the RxSer_n pins. 10 - The data link bits extracted from the incoming DS1 frame are sent to the Receive Overhead Output Interface via the RxOH_n pins. 11 - The data link bits are forced into 1.

If the Receive Data Link Source Select bits of the Receive Data Link Select Register are set to 00, the Receive HDLC Controller block becomes output destination of the data link bits in incoming DS1 frames.

Each of the four framers within the XRT86L34 device contains a DS1 Receive High-level Data Link Controller (HDLC) block. The function of this block is to establish a serial data link channel in DS1 mode through the following:

- Facility Data Link (FDL) bits in ESF framing format mode
- Signaling Framing (Fs) bits in SLC®96 framing format mode
- Remote Signaling (R) bits in T1DM framing format mode
- D or E signaling timeslot channel

Data link bits are automatically inserted into the Facility Data Link (FDL) bits in ESF framing format mode, Signaling Framing (Fs) bits in SLC®96 framing format mode and Remote Signaling (R) bits in T1DM framing format mode or forced to 1 by the framer. Additionally, XRT86L34 allows the user to define any one of ones of the twenty-four DS0 timeslots to be D or E channel. We will discuss how to configure XRT86L34 to Receive data link information through D or E channels in later section.

The DS1 Receive HDLC Controller block contains three major functional modules associated with DS1 framing formats. They are the:

- SLC®96 Data Link Controller
- LAPD Controller
- Bit-Oriented Signaling Processor.

There are two 96-byte receive message buffer in shared memory for each of the four framers to receive data link information. When one message buffer is filled up, the DS1 Receive HDLC Controller automatically switches to the next message buffer to store data link messages. These two message buffers ping-pong among each other for data link message storage.

The SLC®96 Enable bit and the Message Type bit of the Data Link Status Register (DLSR) determines which one of the three messages is received and processed by the Receive HDLC Controller block.

The table below shows configuration of the SLC®96 Enable bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (ADDRESS = 0XN113H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	SLC®96 Enable	R/W	0 - In SLC®96 framing mode, the data link transmission is disabled. The framer receives the regular SF framing bits. In ESF framing mode, the framer receives regular ESF framing bits and Facility Data Link (FDL) bits. 1 - In SLC®96 framing mode, the data link transmission is enabled. In ESF framing mode, the framer receives SLC®96-like message in the Facility Data Link bits.

The table below shows configuration of the Message Type bit of the Data Link Status Register (DLSR).

DATA LINK STATUS REGISTER (DLSR) (ADDRESS = 0XNB06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Message Type	RUR / WC	0 - The Receive HDLC Controller receives and processes Bit-Oriented Signaling (BOS) message. 1 - The Receive HDLC Controller receives and processes LAPD protocol or Message-Oriented Signaling (MOS) message.

2.3.2 How to configure XRT86L34 to Receive data link information through D or E Channels

The XRT86L34 can configure any one or ones of the twenty-four DS0 channels to be D or E channels. D channel is used primarily for data link applications. E channel is used primarily for signaling for circuit switching with multiple access configurations.

The Receive Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of each channel determine whether that particular channel is configured as D or E channel. These bits also determine what type of data or signaling conditioning is applied to each channel.

RECEIVE CHANNEL CONTROL REGISTER (RCCR) (ADDRESS = 0XN360H - 0XN37FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Receive Conditioning Select	R/W	1111 - This channel is configured as D or E timeslot.

If the Receive Conditioning Select [3:0] bits of the Receive Channel Control Register of a particular timeslot are set to 1111, that timeslot is configured as a D or E timeslot.

Any D or E timeslot can be configured to direct data link information to the following destinations:

- DS1 Receive Overhead Output Interface Block
- DS1 Receive HDLC Controller Block
- DS1 Receive Serial Output Interface Block
- DS1 Receive Fractional Output Interface Block

The Receive D or E Channel Source Select [1:0] bits of the Receive Data Link Select Register (RSDLSR) determines which one of the above-mentioned modules to be output destinations of D or E timeslot. The table be-

low shows configuration of the Receive D or E Channel Source Select [1:0] bits of the Receive Data Link Select Register (RSDLSR).

RECEIVE DATA LINK SELECT REGISTER (RSDLSR) (ADDRESS = 0XN10CH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Receive D or E Channel Source Select [1:0]	R/W	00 - The data link bits extracted form the D or E channel of incoming DS1 frame are inserted into the Receive Serial Data Output Interface via the RxSer_n pins. 01 - The data link bits extracted form the D or E channel of incoming DS1 frame are inserted into the Receive HDLC Controller. 10 - The data link bits extracted form the D or E channel of incoming DS1 frame are inserted into the Receive Fractional T1 Output Interface via the RxFrT1_n pins. 11 - The data link bits extracted form the D or E channel of incoming DS1 frame are inserted into the Receive Serial Data Output Interface via the RxSer_n pins.

For the Receive HDLC Controller to be output destination of D or E channel, the Receive D or E Channel Source Select [1:0] bits of the Receive Data Link Select Register has to be set to 01.

2.3.3 Receive BOS (Bit Oriented Signaling) Processor

The Receive BOS Processor handles receiving and processing of BOS messages through the DS1 data link channel. It generates Receive End of Transfer (RxEOT) interrupt each time a BOS message is received and stores the BOS message into the receive message buffer. In the later section, we will discuss how to configure the BOS Processor Block to receive BOS message.

2.3.3.1 How to configure the BOS Processor Block to receive BOS

This section describes how to configure the BOS Processor Block to receive BOS message and how to read out the BOS message. The operation of the receive BOS Processor is interrupt-driven. When a BOS message is received, message octet is written to the next receive data link message buffer opposite to that last used. The receive BOS Processor generates interrupts to the microprocessor notifying it that a BOS message is received. The BOS message can then be extracted from the appropriate receive data link buffer.

2.3.3.1.1 Step 1: Enable receive BOS message interrupts

The BOS Processor can generate a couple of interrupts indicating the status of BOS message received to the microprocessor. These are the Receive Start of Transfer (RxSOT) interrupt and the Receive End of Transfer (RxEOT) interrupt.

To enable these interrupts, the Receive Start of Transfer Enable bit and the Receive End of Transfer Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Start of Transfer Enable bit and the Receive End of Transfer Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (ADDRESS = 0XNB07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Start of Transfer Enable	R/W	0 - The Receive Start of Transfer interrupt is disabled. 1 - The Receive Start of Transfer interrupt is enabled.
3	Receive End of Transfer Enable	R/W	0 - The Receive End of Transfer interrupt is disabled. 1 - The Receive End of Transfer interrupt is enabled.

The table below shows configurations of the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	HDLC Controller Interrupt Enable	R/W	0 - Every interrupt generated by the HDLC Controller is disabled. 1 - Every interrupt generated by the HDLC Controller is enabled.

When these interrupt enable bits are set and the BOS message is received in the data link channel, the BOS Processor changes the Receive Start of Transfer and Receive End of Transfer status bits of the Data Link Status Register (DLSR). These two status indicators are valid until the Data Link Status Register is read. Reading these register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Start of Transfer and Receive End of Transfer status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (ADDRESS = 0XNB06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Start of Transfer	RUR / WC	0 - There is no data link message in the data link channel. 1 - The HDLC Controller began to receive a data link message in the data link channel.
3	Receive End of Transfer	RUR / WC	0 - No data link message was present in the data link channel. 1 - The HDLC Controller finished receiving a data link message in the data link channel.

The BOS Processor can also generate interrupts when either the BOS ABORT sequence (nine consecutive ones) or the IDLE flag character (hexadecimal value of 0x7EH) is received in the data link channel to the microprocessor. These are the Receive ABORT Sequence (RxABORT) interrupt and the Receive IDLE Flag Sequence (RxIDLE) interrupt.

To enable these interrupts, the Receive ABORT Sequence Enable bit and the Receive IDLE Flag Sequence Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive ABORT Sequence Enable bit and the Receive IDLE Flag Sequence Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (ADDRESS = 0XNB07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive ABORT Sequence Enable	R/W	0 - The Receive ABORT Sequence interrupt is disabled. 1 - The Receive ABORT Sequence interrupt is enabled.
0	Receive IDLE Flag Sequence Enable	R/W	0 - The Receive IDLE Flag Sequence interrupt is disabled. 1 - The Receive IDLE Flag Sequence interrupt is enabled.

When these interrupt enable bits are set and the BOS ABORT sequence or IDLE Flag Sequence is received in the data link channel, the BOS Processor changes the Receive ABORT Sequence and Receive IDLE Flag Sequence status bits of the Data Link Status Register (DLSR). These two status indicators are valid until the Data Link Status Register is read. Reading these register clears the associated interrupt if Reset Upon Read is se-

lected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive ABORT Sequence and Receive IDLE Flag Sequence status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (ADDRESS = 0XNB06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive ABORT Sequence	RUR / WC	0 - There is no BOS ABORT sequence received in the data link channel. 1 - The HDLC Controller receives BOS ABORT sequence in the data link channel.
0	Receive IDLE Flag Sequence	RUR / WC	0 - The message received in the data link channel is BOS message. 1 - The message received in the data link channel is MOS message.

2.3.3.1.2 Step 2: Find out the next available receive data link buffer

To transmit a bit-oriented signal, a repeating message is sent of the form (0d5d4d3d2d1d0011111111), where the "d5d4d3d2d1d0" represents a six-bit message. When receiving a BOS message, the received message octet is written to the next available receive data link buffer in the form of (0d5d4d3d2d1d00). The user is recommended to read Receive Data Link Byte Count Register for next available receive data link buffer number.

The table below shows how contents of the Receive Buffer Pointer bit of the Receive Data Link Byte Count Register (RDLBCR) determines what the next available receive data link buffer number is.

RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR) (ADDRESS = 0XN115H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Buffer Pointer	R	0 - The next available receive data link buffer for reading out BOS or MOS message is Buffer 0. 1 - The next available receive data link buffer for reading out BOS or MOS message is Buffer 1.

2.3.3.1.3 Step 3: Program BOS Message receiving repetitions

The user should program the value of message receiving repetitions into the Receive Data Link Byte Count Register. The framer will receive the BOS message the same number of times as was stored in the Receive Data Link Byte Count Register (RDLBCR) before generating the Receive End of Transfer (RxEOT) interrupts. If the value stored inside the Receive Data Link Byte Count Register (RDLBCR) is set to 0, the message will be received indefinitely and no Receive End of Transfer interrupt will be generated.

The table below shows configurations of the Receive Data Link Byte Count [6:0] bits the Receive Data Link Byte Count Register (RDLBCR).

RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR) (ADDRESS = 0XN115H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6-0	Receive Data Link Byte Count [6:0]	R/W	Value of these bits determines how many times a BOS message pattern will be received by the framer before generating the Receive End of Transfer (TxEOT) interrupt. ***NOTE:*** *If these bits are set to 0, the BOS message will be received indefinitely and no Receive End of Transfer interrupts will be generated.*

2.3.3.1.4 Step 4: Read BOS Message from receive data link buffer

Upon detection of the Receive End of Transfer (RxEOT) interrupt, the user should read the Message Type bit of the Data Link Status Register (DLSR) to find out what is the type of message received.

The table below shows how contents of the Message Type bit of the Data Link Status Register (DLSR) determines what the type of message received in the data link channel is.

DATA LINK STATUS REGISTER (DLSR) (ADDRESS = 0XNB06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Message Type	RUR / WC	0 - There is no BOS ABORT sequence received in the data link channel. 1 - The HDLC Controller receives BOS ABORT sequence in the data link channel.

After determined that the received message is a BOS one, the use should read eight bits message from the first location of the next available receive data link buffer. The reading of these buffers is through the LAPD Buffer 0 indirect data registers and the LAPD Buffer1 indirect data registers. LAPD Buffer 0 and 1 indirect data registers have addresses 0xn600H and 0xn700H respectively. There is no indirect address register for receive data link buffer 0 and 1.

A microcontroller WRITE access to the LAPD Buffer indirect data registers will access the receive data link buffer and a microcontroller READ will access the receive data link buffers. The very first READ access to the LAPD Buffer indirect data register will always be direct to location 0 within the receive data link buffer.

For example, if the BOS Message to received is (101011) and the next available receive data link buffer of Channel n is 1. The user should be able to read pattern (01010110) from receive data link buffer 1 of Channel n. The following microprocessor access to the framer should be done:

RD n7H

The result of the READ access should be 0x56H.

2.3.4 Receive LAPD Controller

The receive LAPD controller implements the Message-Oriented protocol based on ITU Recommendation Q.921 Link Access Procedures on the D-channel (LAPD) type of protocol. It provides the following functions:

- Zero deletion
- Pattern recognition for IDLE flag detection
- Pattern recognition for ABORT sequence detection
- Frame check sequence verification
- T1 receiver interface
- Receive data link message buffer access

Two 96-byte buffers in shared memory are allocated for receive LAPD Controller to reduce the frequency of microprocessor interrupts and alleviate the response time requirement for microprocessor to handle each interrupt. There are no restrictions on the length of the message received. However, the 96-byte buffer is deep enough to hold one entire LAPD path or test signal identification message.

The following section discuss how to configure the receive LAPD Controller to receive and extract MOS messages.

2.3.4.1 How to configure the Receive HDLC Controller Block to receive MOS message

This section describes how to configure the LAPD Controller Block to receive and extract MOS message in a step-by-step basis.

The operation of the receive LAPD Controller is interrupt-driven. When an MOS message is receiving, message octets are written to the next receive data link message buffer opposite to that last used. Each time the receiving data link message buffer is filled, a RxEOT interrupt is issued if it is enabled. This process continues until an ABORT sequence is received or an IDLE flag is received.

An interrupt is issued when one of the following conditions occurs and the corresponding interrupt enable bit is set.

- The RxSOT is set when the beginning of a data link message is received (the first non-flag message).
- The RxEOT is set when the end of a data link block is received.
- The RxIDLE is set if an IDLE flag sequence (b01111110) is received on the data link after either an ABORT sequence is received or a complete message is received.
- The RxABORT is set when an ABORT sequence is received.
- The FCS_ERR is issued when an erroneous frame check sequence is detected at the end of a message or an idle flag is received that is not octet aligned.

2.3.4.1.1 Step 1: Enable receive MOS message interrupts

The receive LAPD Controller can generate a couple of interrupts indicating the status of MOS message received to the microprocessor. These are the Receive Start of Transfer (RxSOT) interrupt and the Receive End of Transfer (RxEOT) interrupt.

To enable these interrupts, the Receive Start of Transfer Enable bit and the Receive End of Transfer Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Start of Transfer Enable bit and the Receive End of Transfer Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (ADDRESS = 0XNB07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Start of Transfer Enable	R/W	0 - The Receive Start of Transfer interrupt is disabled. 1 - The Receive Start of Transfer interrupt is enabled.
3	Receive End of Transfer Enable	R/W	0 - The Receive End of Transfer interrupt is disabled. 1 - The Receive End of Transfer interrupt is enabled.

The table below shows configurations of the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	HDLC Controller Interrupt Enable	R/W	0 - Every interrupt generated by the HDLC Controller is disabled. 1 - Every interrupt generated by the HDLC Controller is enabled.

When these interrupt enable bits are set and the MOS message is received in the data link channel, the LAPD Controller changes the Receive Start of Transfer and Receive End of Transfer status bits of the Data Link Status Register (DLSR). These two status indicators are valid until the Data Link Status Register is read. Reading these register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Start of Transfer and Receive End of Transfer status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (ADDRESS = 0XNB06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Start of Transfer	RUR / WC	0 - There is no data link message in the data link channel. 1 - The HDLC Controller began to receive a data link message in the data link channel.
3	Receive End of Transfer	RUR / WC	0 - No data link message was present in the data link channel. 1 - The HDLC Controller finished receiving a data link message in the data link channel.

The LAPD Controller can also generate interrupts when either the MOS ABORT sequence (seven consecutive ones) or the IDLE flag character (hexadecimal value of 0x7EH) is received in the data link channel to the microprocessor. These are the Receive ABORT Sequence (RxABORT) interrupt and the Receive IDLE Flag Sequence (RxIDLE) interrupt.

To enable these interrupts, the Receive ABORT Sequence Enable bit and the Receive IDLE Flag Sequence Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive ABORT Sequence Enable bit and the Receive IDLE Flag Sequence Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (ADDRESS = 0XNB07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive ABORT Sequence Enable	R/W	0 - The Receive ABORT Sequence interrupt is disabled. 1 - The Receive ABORT Sequence interrupt is enabled.
0	Receive IDLE Flag Sequence Enable	R/W	0 - The Receive IDLE Flag Sequence interrupt is disabled. 1 - The Receive IDLE Flag Sequence interrupt is enabled.

When these interrupt enable bits are set and the MOS ABORT sequence or IDLE Flag Sequence is received in the data link channel, the LAPD Controller changes the Receive ABORT Sequence and Receive IDLE Flag Sequence status bits of the Data Link Status Register (DLSR). These two status indicators are valid until the Data Link Status Register is read. Reading these register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive ABORT Sequence and Receive IDLE Flag Sequence status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (ADDRESS = 0XNB06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive ABORT Sequence	RUR / WC	0 - There is no BOS ABORT sequence received in the data link channel. 1 - The HDLC Controller receives MOS ABORT sequence in the data link channel.
0	Receive IDLE Flag Sequence	RUR / WC	0 - The message received in the data link channel is BOS message. 1 - The message received in the data link channel is MOS message.

Finally, the LAPD Controller generates Frame Check Sequence Error (FCS_ERR) interrupt when an erroneous frame check sequence is detected at the end of a message or an IDLE flag is received that is not octet aligned.

To enable this interrupt, the Frame Check Sequence Error Detection Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Frame Check Sequence Error Detection Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (ADDRESS = 0XNB07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Frame Check Sequence Error Detection Enable	R/W	0 - The Frame Check Sequence Error Detection interrupt is disabled. 1 - The Frame Check Sequence Error Detection interrupt is enabled.

When the Frame Check Sequence Error Detection interrupt enable bits is set and an erroneous frame check sequence is detected at the end of a message, the LAPD Controller changes the Frame Check Sequence Error Detection status bits of the Data Link Status Register (DLSR). This status indicator is valid until the Data Link Status Register is read. Reading this register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset this status indicator.

The table below shows the Frame Check Sequence Error Detection status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (ADDRESS = 0XNB06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Frame Check Sequence Error Detection	RUR / WC	0 - There is no FCS error detected in the data link channel. 1 - The HDLC Controller receives an erroneous FCS in the data link channel.

2.3.4.1.2 Step 2: Find out the next available receive data link buffer

When the LAPD Controller is receiving MOS message, the received message octets are written to the next available receive data link buffer. The user is recommended to read Receive Data Link Byte Count Register for next available receive data link buffer number.

The table below shows how contents of the Receive Buffer Pointer bit of the Receive Data Link Byte Count Register (RDLBCR) determines what the next available receive data link buffer number is.

RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR) (ADDRESS = 0XN115H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Buffer Pointer	R	0 - The next available receive data link buffer for reading out BOS or MOS message is Buffer 0. 1 - The next available receive data link buffer for reading out BOS or MOS message is Buffer 1.

2.3.4.1.3 Step 3: Reading the Receive Data Link Byte Count Register

The user should read the length of MOS message from the Receive Data Link Byte Count Register. The receive LAPD Controller increments the Receive Data Link Byte Count Register value when each octet of MOS

message is received. After the Receive End of Transfer (RxEOT) interrupt is generated, the Receive Data Link Byte Count Register should contain the length of entire MOS message.

The table below shows configurations of the Receive Data Link Byte Count [6:0] bits of the Receive Data Link Byte Count Register (RDLBCR).

RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR) (ADDRESS = 0XN115H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6-0	Receive Data Link Byte Count [6:0]	R	Value of these bits determines how many times a BOS message pattern will be received by the framer before generating the Receive End of Transfer (TxEOT) interrupt.

2.3.4.1.4 Step 4: Read MOS Message from receive data link buffer

Upon detection of the Receive End of Transfer (RxEOT) interrupt, the user should read the Message Type bit of the Data Link Status Register (DLSR) to find out what is the type of message received.

The table below shows how contents of the Message Type bit of the Data Link Status Register (DLSR) determines what the type of message received in the data link channel is.

DATA LINK STATUS REGISTER (DLSR) (ADDRESS = 0XNB06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Message Type	RUR / WC	0 - Message received in the data link channel is BOS. 1 - Message received in the data link channel is MOS.

After determined that the received message is an MOS one, the use should read the entire message from the available receive data link buffer. The reading of these buffers is through the LAPD Buffer 0 indirect data registers and the LAPD Buffer1 indirect data registers. LAPD Buffer 0 and 1 indirect data registers have addresses 0xn600H and 0xn700H respectively. There is no indirect address register for receive data link buffer 0 and 1.

A microcontroller WRITE access to the LAPD Buffer indirect data registers will access the receive data link buffer and a microcontroller READ will access the receive data link buffers. The very first READ access to the LAPD Buffer indirect data register will always be direct to location 0 within the receive data link buffer.

For example, if the first octet of the MOS Message received is (10101100) and the next available receive data link buffer of Channel n is 1. The user should be able to read pattern (01010110) from receive data link buffer 1 of Channel n. The following microprocessor access to the framer should be done:

RD n700H

The result of the READ access should be 0xACH.

2.3.5 Receive SLCâ96 Data link Controller

This section describes how to configure the Receive SLC®96 Data Link Controller block to receive SLC®96 Data Link message and how to read out the message from the receive data link message buffer. The operation of the Receive SLC®96 Data Link Controller is interrupt-driven. When a 36-bit SLC®96 Data Link message is received, message octet is written to the next receive data link message buffer opposite to that last used. The receive SLC®96 Data Link Controller generates interrupts to the microprocessor notifying it that a message is received. The data link message can then be extracted from the appropriate receive data link buffer.

In order to enable this mode of operation, the framing mode must be set to SLC®96. The XRT86L34 allocates two 6-byte buffers to provide SLC®96 Data Link Controller an alternating access mechanism for information

received. The bit ordering and usage is shown in the following table. The bits 7 and 6 are forced to 0 by the SLC®96 Data Link Controller.

RECEIVE SLC®96 MESSAGE REGISTERS

BITBYTE	7	6	5	4	3	2	1	0
1/7	0	0	0	1	1	1	0	0
2/8	0	0	C1	1	1	1	0	0
3/9	0	0	C7	C6	C5	C4	C3	C2
4/10	0	0	1	0	C11	C10	C9	C8
5/11	0	0	A2	A1	M3	M2	M1	0
6/12	0	0	0	1	S4	S3	S2	S1

2.3.5.1 How to configure the SLC®96 Data Link Controller to receive SLC®96 Data Link Messages

This section describes how to configure the SLC®96 Data Link Controller to receive SLC®96 Data Link message in a step-by-step basis.

The operation of the receive SLC®96 Data Link Controller is interrupt-driven. When an SLC®96 Data Link message is receiving, message octets are written to the next receive data link message buffer opposite to that last used. Every time the SLC®96 Data Link controller receives a 36-bit SLC®96 data link message, an RxEOT interrupt is issued if it is enabled. This process continues until an ABORT sequence is received.

An interrupt is issued when one of the following conditions occurs and the corresponding interrupt enable bit is set.

- The RxSOT is set when the beginning of a data link message is received.
- The RxEOT is set when the end of a data link block is received.
- The RxABORT is set when an ABORT sequence is received.

2.3.5.1.1 Step 1: Enable receive SLC®96 Data Link message interrupts

The receive SLC®96 Data Link Controller can generate a couple of interrupts indicating the status of SLC®96 message received to the microprocessor. These are the Receive Start of Transfer (RxSOT) interrupt and the Receive End of Transfer (RxEOT) interrupt.

To enable these interrupts, the Receive Start of Transfer Enable bit and the Receive End of Transfer Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Start of Transfer Enable bit and the Receive End of Transfer Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (ADDRESS = 0XNB07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Start of Transfer Enable	R/W	0 - The Receive Start of Transfer interrupt is disabled. 1 - The Receive Start of Transfer interrupt is enabled.
3	Receive End of Transfer Enable	R/W	0 - The Receive End of Transfer interrupt is disabled. 1 - The Receive End of Transfer interrupt is enabled.

The table below shows configurations of the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	HDLC Controller Interrupt Enable	R/W	0 - Every interrupt generated by the HDLC Controller is disabled. 1 - Every interrupt generated by the HDLC Controller is enabled.

When these interrupt enable bits are set and the SLC®96 message is received in the data link channel, the SLC®96 Data Link Controller changes the Receive Start of Transfer and Receive End of Transfer status bits of the Data Link Status Register (DLSR). These two status indicators are valid until the Data Link Status Register is read. Reading these register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Start of Transfer and Receive End of Transfer status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (ADDRESS = 0XNB06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Start of Transfer	RUR / WC	0 - There is no data link message in the data link channel. 1 - The SLC®96 Data Link Controller began to receive a data link message in the data link channel.
3	Receive End of Transfer	RUR / WC	0 - No data link message was present in the data link channel. 1 - The SLC®96 Data Link Controller finished receiving a data link message in the data link channel.

The SLC®96 Data Link Controller can also generate interrupts when the ABORT sequence is received in the data link channel to the microprocessor. This is the Receive ABORT Sequence (RxABORT).

To enable this interrupt, the Receive ABORT Sequence Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive ABORT Sequence Enable bit and the Receive IDLE Flag Sequence Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (ADDRESS = 0XNB07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive ABORT Sequence Enable	R/W	0 - The Receive ABORT Sequence interrupt is disabled. 1 - The Receive ABORT Sequence interrupt is enabled.

When these interrupt enable bits are set and the SLC®96 ABORT sequence is received in the data link channel, the SLC®96 Data Link Controller changes the Receive ABORT Sequence status bit of the Data Link Status Register (DLSR). This status indicator is valid until the Data Link Status Register is read. Reading the register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive ABORT Sequence status bit of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (ADDRESS = 0XNB06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive ABORT Sequence	RUR / WC	0 - There is no BOS ABORT sequence received in the data link channel. 1 - The SLC®96 Data Link Controller receives ABORT sequence in the data link channel.

2.3.5.1.2 Step 2: Find out the next available receive data link buffer

When the SLC®96 Data Link Controller is receiving SLC®96 message, the received message octets are written to the next available receive data link buffer. The user is recommended to read Receive Data Link Byte Count Register for next available receive data link buffer number.

The table below shows how contents of the Receive Buffer Pointer bit of the Receive Data Link Byte Count Register (RDLBCR) determines what the next available receive data link buffer number is.

RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR) (ADDRESS = 0XN115H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Buffer Pointer	R	0 - The next available receive data link buffer for reading out data link message is Buffer 0. 1 - The next available receive data link buffer for reading out data link message is Buffer 1.

2.3.5.1.3 Step 3: Read SLC®96 Data LInk Message from receive data link buffer

Upon detection of the Receive End of Transfer (RxEOT) interrupt, the use should read the entire SLC®96 Data Link message from the available receive data link buffer. The reading of these buffers is through the LAPD Buffer 0 indirect data registers and the LAPD Buffer1 indirect data registers. LAPD Buffer 0 and 1 indirect data registers have addresses 0xn600H and 0xn700H respectively. There is no indirect address register for receive data link buffer 0 and 1.

A microcontroller WRITE access to the LAPD Buffer indirect data registers will access the receive data link buffer and a microcontroller READ will access the receive data link buffers. The very first READ access to the LAPD Buffer indirect data register will always be direct to location 0 within the receive data link buffer.

For example, if the first octet of the SLC®96 Message received is (00101011) and the next available receive data link buffer of Channel n is 1. The user should be able to read pattern (00101011) from receive data link buffer 1 of Channel n. The following microprocessor access to the framer should be done:

RD n700H

The result of the READ access should be 0x2BH.

2.4 SS7 (SIGNALING SYSTEM NUMBER 7)

To support SS7 specifications while receiving LAPD messages, EXAR's Framer will generate an interrupt (if SS7 is enabled) once the HDLC controllers have received more than 276 bytes within two flag sequences (0x7E) of a LAPD message. Each HDLC controller supports SS7. For example: To enable SS7 for all HDLC controllers, registers 0xnB11 (LAPD1), 0xnB19 (LAPD2), 0xnB29 (LAPD3) must be set to 0x01.

2.5 E1 TRANSMIT HDLC CONTROLLER BLOCK

2.5.1 Description of the E1 Transmit HDLC Controller Block

XRT86L34 allows user to insert data link information to outbound E1 frames. The data link information in E1 framing format mode can be inserted from:

- E1 Transmit Overhead Input Interface Block

- E1 Transmit HDLC Controller
- E1 Transmit Serial Input Interface

The Transmit Data Link Source Select [1:0] bits, within the Synchronization MUX Register (SMR) determine source of the data link bits to be inserted into the outgoing E1 frames.

The table below shows configuration of the Transmit Data Link Source Select [1:0] bits of the Synchronization MUX Register (SMR).

SYNCHRONIZATION MUX REGISTER (SMR) (ADDRESS = 0XN109H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Transmit Data Link Source Select [1:0]	R/W	00 - The data link bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins. 01 - The data link bits are inserted into the framer through the Transmit HDLC Controller. 10 - The data link bits are inserted into the framer through the Transmit Overhead Input Interface via the TxOH_n pins. 11 - The data link bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins.

If the Transmit Data Link Source Select bits of the Transmit Data Link Select Register are set to 01, the Transmit HDLC Controller block becomes input source of the data link bits in outgoing E1 frames.

Each of the four framers within the XRT86L34 device contains an E1 Transmit High-level Data Link Controller (HDLC) block. The function of this block is to provide a serial data link channel in E1 mode through the following:

- The National bits (Sa4 through Sa8) of Timeslot 0 of non-FAS frame
- Timeslot 16 octet when the framer is in Common Channel Signaling mode
- D or E signaling timeslot channel

We will discuss how to configure XRT86L34 to transmit data link information through each of these data link channels in later sections.

The E1 Transmit HDLC Controller block contains two major functional modules associated with E1 framing formats. They are the LAPD Controller and the Bit-Oriented Signaling Processor.

There are two 96-byte transmit message buffers in shared memory for each of the four framers to transmit data link information. When one message buffer is filled up, the Transmit HDLC Controller automatically switches to the next message buffer to load data link messages. These two message buffers ping-pong among each other for data link message transmission.

The LAPD Enable bit of the Data Link Control Register (DLCR) determines whether the Transmit HDLC Controller block should perform as the LAPD Controller or the BOS Processor.

The table below shows configuration of the LAPD Enable bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (ADDRESS = 0XN113H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	LAPD Enable	R/W	0 - The Transmit HDLC Controller will send out Bit-Oriented Signaling (BOS) message. 1 - The Transmit HDLC Controller will send out LAPD protocol or so-called Message-Oriented Signaling (MOS) message.

2.5.2 How to configure XRT86L34 to transmit data link information through the National bits (Sa4 through Sa8)

As mentioned in previous section, the National bits (Sa4 through Sa8) of Timeslot 0 of non-FAS frame can be used to transmit data link information in E1 mode.

The XRT86L34 allows the user to decide on the following:

- Whether the National bits will be used to carry the data link information bits.
- How many of the National Bits will be used to carry the Data Link information bits.
- Which of these National Bits will be used to carry the Data Link information bits.

The Transmit Signaling and Data Link Control [2:0] bits of the Transmit Signaling and Data Link Select Register (TSDLSR) determines if the National bits will be used to carry data link information. The table below shows configuration of the Transmit Signaling and Data Link Control [2:0] bits of the Transmit Signaling and Data Link Select Register (TSDLSR).

TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2-0	Transmit Signaling and Data Link Select	R/W	000 - The data link interface is source of the Sa4 through Sa8 Nation bits. 001 - The data link interface is source of the Sa4 through Sa8 Nation bits. 010 - The Sa4 through Sa8 Nation bits are forced to 1. 011 - The Sa4 through Sa8 Nation bits are forced to 1. 1xx - The Sa4 through Sa8 Nation bits are forced to 1.

If the Transmit Signaling and Data Link Select [2:0] bits of the Transmit Signaling and Data Link Select Register is set to 000 or 001, the data link interface becomes source of the Sa4 through Sa8 National bits.

The Transmit Sa Data Link Select bits of the Transmit Signaling and Data Link Select Register (TSDLSR) determine which ones of the National bits are configured as Data Link bits in E1 framing format mode. Depending upon the configuration of the Transmit Signaling and Data Link Select Register, either of the following cases may exists:

- None of the National bits are used to transport the Data Link information bits (That is, data link channel of XRT86L34 is inactive).
- Any combination of between 1 and all 5 of the National bits can be selected to transport the Data Link information bits.

The table below shows configuration of the Transmit Sa Data Link Select bits of the Transmit Signaling and Data Link Select Register (TSDLSR).

TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Transmit Sa8 Data Link Select	R/W	0 - Source of the Sa8 Nation bit is not from the data link interface. 1 - Source the Sa8 National bit from the data link interface.
6	Transmit Sa7 Data Link Select	R/W	0 - Source of the Sa7 Nation bit is not from the data link interface. 1 - Source the Sa7 National bit from the data link interface.
5	Transmit Sa6 Data Link Select	R/W	0 - Source of the Sa6 Nation bit is not from the data link interface. 1 - Source the Sa6 National bit from the data link interface.
4	Transmit Sa5 Data Link Select	R/W	0 - Source of the Sa5 Nation bit is not from the data link interface. 1 - Source the Sa5 National bit from the data link interface.
3	Transmit Sa4 Data Link Select	R/W	0 - Source of the Sa4 Nation bit is not from the data link interface. 1 - Source the Sa4 National bit from the data link interface.

2.5.3 How to configure XRT86L34 to transmit data link information through Timeslot 16 octet

In E1 mode, Timeslot 16 octet can be configured to transmit the following:

- Channel Associated Signaling (CAS) bits A, B, C and D
- Common Channel Signaling (CCS) bits

The Common Channel Signaling (CCS) messages are actually data link information applicable to all thirty-two timeslots of an E1 frame, thus the name Common Channel Signaling. The Transmit Signaling and Data Link Control [2:0] bits of the Transmit Signaling and Data Link Select Register (TSDLSR) determine if Timeslot octet will be used to carry data link information or CAS signals. The table below shows configuration of the Transmit Signaling and Data Link Control [2:0] bits of the Transmit Signaling and Data Link Select Register (TSDLSR).

TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2-0	Transmit Signaling and Data Link Select	R/W	000 - Timeslot 16 octet is taken directly from the Transmit Serial Input Interface through the TxSer_n pin. 001 - Timeslot 16 octet is taken directly from the Transmit Overhead Input Interface through the TxOH_n pin or the Transmit Signaling Control Register of Timeslot 16. 010 - Timeslot 16 octet is taken directly from the Transmit Serial Input Interface through the TxSer_n pin. 011 - Timeslot 16 octet is taken directly from the Transmit Overhead Input Interface through the TxOH_n pin or the Transmit Signaling Control Register of Timeslot 16. 1xx - Timeslot 16 octet is taken from the data link interface.

If the Transmit Signaling and Data Link Select [2:0] bits of the Transmit Signaling and Data Link Select Register are set to 1xx, the data link interface becomes source of the Timeslot 16 octet.

2.5.4 How to configure XRT86L34 to transmit data link information through D or E Channels

The XRT86L34 can configure any one or ones of the thirty-two E1 channels to be D or E channels except for Channel number 0. D channel is used primarily for data link applications. E channel is used primarily for signaling for circuit switching with multiple access configurations.

The Transmit Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of each channel determine whether that particular channel is configured as D or E channel. These bits also determine what type of data or signaling conditioning is applied to each channel.

TRANSMIT CHANNEL CONTROL REGISTER (TCCR) (ADDRESS = 0XN300H - 0XN31FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Transmit Conditioning Select	R/W	1111 - This channel is configured as D or E timeslot.

If the Transmit Conditioning Select [3:0] bits of the Transmit Channel Control Register of a particular timeslot are set to 1111, that timeslot is configured as a D or E timeslot.

NOTE: *Timeslot 0 can never be configured as D or E timeslot.*

2.5.5 Transmit BOS (Bit Oriented Signaling) Processor

The Transmit BOS Processor handles transmission of BOS messages through the E1 data link channel. It determines how many repetitions a certain BOS message will be transmitted. It also inserts BOS IDLE flag sequence and ABORT sequence to be transmitted on the data link channel. Please see Section ? for descriptions of BOS message format and how to transmit BOS message.

2.5.6 Transmit MOS (Message Oriented Signaling) or LAPD Controller

The Transmit LAPD controller implements the Message-Oriented protocol based on ITU Recommendation Q.921 Link Access Procedures on the D-channel (LAPD) type of protocol. It provides the following functions:

- Zero stuffing
- T1/E1 transmitter interface
- Transmit message buffer access
- Frame check sequence generation
- IDLE flag insertion
- ABORT sequence generation

Two 96-byte buffers in shared memory are allocated for LAPD transmitter to reduce the frequency of microprocessor interrupts and alleviate the response time requirement for microprocessor to handle each interrupt. There are no restrictions on the length of the message. However the 96-byte buffer is deep enough to hold one entire LAPD path or test signal identification message. Please see Section ? for descriptions of MOS message format and how to configure the LAPD Controller to transmit MOS message.

2.6 E1 RECEIVE HDLC CONTROLLER BLOCK

2.6.1 Description of the E1 Receive HDLC Controller Block

XRT86L34 detects and extracts data link information from incoming E1 frames. The data link information in E1 framing format mode can be extracted to:

- E1 Receive Overhead Output Interface Block
- E1 Receive HDLC Controller
- E1 Receive Serial Output Interface

The extracted data link information is routed to the E1 Receive Overhead Output Interface and the E1 Receive Serial Output Interface no matter whether the E1 Receive HDLC Controller module is activated or not.

Each of the framers within the XRT86L34 device contains 3 E1 Receive High-level Data Link Controller (HDLC) blocks. The function of these blocks is to establish a serial data link channel in E1 mode through the following:

- The National bits (Sa4 through Sa8) of Timeslot 0 of non-FAS frame
- Timeslot 16 octet when the framer is in Common Channel Signaling mode
- D or E signaling timeslot channel

We will discuss how to configure XRT86L34 to transmit data link information through each of these data link channels in later sections.

The E1 Transmit HDLC Controller block contains two major functional modules associated with E1 framing formats. They are the LAPD Controller and the Bit-Oriented Signaling Processor.

There are two 96-byte receive message buffer in shared memory for each of the four framers to receive data link information. When one message buffer is filled up, the E1 Receive HDLC Controller automatically switches to the next message buffer to store data link messages. These two message buffers ping-pong among each other for data link message storage.

The Message Type bit of the Data Link Status Register (DLSR) determines which one of the three messages is received and processed by the Receive HDLC Controller block.

The table below shows configuration of the Message Type bit of the Data Link Status Register (DLSR).

DATA LINK STATUS REGISTER (DLSR) (ADDRESS = 0XNB06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Message Type	RUR / WC	0 - The Receive HDLC Controller receives and processes Bit-Oriented Signaling (BOS) message. 1 - The Receive HDLC Controller receives and processes LAPD protocol or Message-Oriented Signaling (MOS) message.

2.6.2 How to configure XRT86L34 to receive data link information through the National bits (Sa4 through Sa8)

As mentioned in previous section, the National bits (Sa4 through Sa8) of Timeslot 0 of non-FAS frame can be used to receive data link information in E1 mode.

The XRT86L34 allows the user to decide on the following:

- Whether the National bits will be used to carry the data link information bits.
- How many of the National Bits will be used to carry the Data Link information bits.
- Which of these National Bits will be used to carry the Data Link information bits.

The Receive Signaling and Data Link Control [2:0] bits of the Receive Signaling and Data Link Select Register (RSDLSR) determines if the National bits will be used to carry data link information. The table below shows

configuration of the Receive Signaling and Data Link Control [2:0] bits of the Receive Signaling and Data Link Select Register (RSDLSR).

RECEIVE SIGNALING AND DATA LINK SELECT REGISTER (RSDLSR) (ADDRESS = 0XN10CH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2-0	Receive Signaling and Data Link Select	R/W	000 - The data link interface is destination of the Sa4 through Sa8 Nation bits. 001 - The data link interface is destination of the Sa4 through Sa8 Nation bits. 010 - The Sa4 through Sa8 Nation bits are forced to 1. 011 - The Sa4 through Sa8 Nation bits are forced to 1. 1xx - The Sa4 through Sa8 Nation bits are forced to 1.

If the Receive Signaling and Data Link Select [2:0] bits of the Receive Signaling and Data Link Select Register are set to 000 or 001, the data link interface becomes destination of the Sa4 through Sa8 National bits.

The Receive Sa Data Link Select bits of the Receive Signaling and Data Link Select Register (RSDLSR) determine which ones of the National bits are configured as Data Link bits in E1 framing format mode. Depending upon the configuration of the Receive Signaling and Data Link Select Register, either of the following cases may exists:

- None of the National bits are used to transport the Data Link information bits (That is, data link channel of XRT86L34 is inactive).
- Any combination of between 1 and all 5 of the National bits can be selected to transport the Data Link information bits.

The table below shows configuration of the Receive Sa Data Link Select bits of the Receive Signaling and Data Link Select Register (RSDLSR).

RECEIVE SIGNALING AND DATA LINK SELECT REGISTER (RSDLSR) (ADDRESS = 0XN10CH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Sa8 Data Link Select	R/W	0 - Destination of the Sa8 Nation bit is not the data link interface. 1 - Destination of the Sa8 National bit is the data link interface.
6	Receive Sa7 Data Link Select	R/W	0 - Destination of the Sa7 Nation bit is not the data link interface. 1 - Destination of the Sa7 National bit is the data link interface.
5	Receive Sa6 Data Link Select	R/W	0 - Destination of the Sa6 Nation bit is not the data link interface. 1 - Destination of the Sa6 National bit is the data link interface.
4	Receive Sa5 Data Link Select	R/W	0 - Destination of the Sa5 Nation bit is not the data link interface. 1 - Destination of the Sa5 National bit is the data link interface.
3	Receive Sa4 Data Link Select	R/W	0 - Destination of the Sa4 Nation bit is not the data link interface. 1 - Destination of the Sa4 National bit is the data link interface.

2.6.3 How to configure XRT86L34 to receive data link information through Timeslot 16 octet

In E1 mode, Timeslot 16 octet can be configured to receive the following:

- Channel Associated Signaling (CAS) bits A, B, C and D
- Common Channel Signaling (CCS) bits

The Common Channel Signaling (CCS) messages are actually data link information applicable to all thirty-two timeslots of an E1 frame, thus the name Common Channel Signaling. The Receive Signaling and Data Link Control [2:0] bits of the Receive Signaling and Data Link Select Register (RSDLSR) determine if Timeslot octet

will be used to carry data link information or CAS signals. The table below shows configuration of the Receive Signaling and Data Link Control [2:0] bits of the Receive Signaling and Data Link Select Register (RSDLSR).

RECEIVE SIGNALING AND DATA LINK SELECT REGISTER (RSDLSR) (ADDRESS = 0XN10CH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2-0	Receive Signaling and Data Link Select	R/W	000 - Timeslot 16 octet is extracted directly to the Receive Serial Output Interface through the RxSer_n pin. 001 - Timeslot 16 octet is extracted directly to the Receive Overhead Output Interface through the RxOH_n pin or the Receive Signaling Control Register of Timeslot 16. 010 - Timeslot 16 octet is extracted directly to the Receive Serial Output Interface through the RxSer_n pin. 011 - Timeslot 16 octet is extracted directly to the Receive Overhead Output Interface through the RxOH_n pin or the Receive Signaling Control Register of Timeslot 16. 1xx - Timeslot 16 octet is extracted to the data link interface.

If the Receive Signaling and Data Link Select [2:0] bits of the Receive Signaling and Data Link Select Register are set to 1xx, the data link interface becomes destination of the Timeslot 16 octet.

2.6.4 How to configure XRT86L34 to receive data link information through D or E Channels

The XRT86L34 can configure any one or ones of the thirty-two E1 channels to be D or E channels except for Channel number 0. D channel is used primarily for data link applications. E channel is used primarily for signaling for circuit switching with multiple access configurations.

The Receive Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of each channel determine whether that particular channel is configured as D or E channel. These bits also determine what type of data or signaling conditioning is applied to each channel.

RECEIVE CHANNEL CONTROL REGISTER (RCCR) (ADDRESS = 0XN360H - 0XN37FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Receive Conditioning Select	R/W	1111 - This channel is configured as D or E timeslot.

If the Receive Conditioning Select [3:0] bits of the Receive Channel Control Register of a particular timeslot are set to 1111, that timeslot is configured as a D or E timeslot.

NOTE: *Timeslot 0 can never be configured as D or E timeslot.*

2.6.5 Receive BOS (Bit Oriented Signaling) Processor

The Receive BOS Processor handles receiving and processing of BOS messages through the E1 data link channel. It generates Receive End of Transfer (RxEOT) interrupt each time a BOS message is received and stores the BOS message into the receive message buffer. Please see Section ? for how to configure the BOS Processor Block to receive BOS message.

2.6.6 Receive LAPD Controller

The receive LAPD controller implements the Message-Oriented protocol based on ITU Recommendation Q.921 Link Access Procedures on the D-channel (LAPD) type of protocol. It provides the following functions:

- Zero deletion
- Pattern recognition for IDLE flag detection
- Pattern recognition for ABORT sequence detection
- Frame check sequence verification

- T1 receiver interface
- Receive data link message buffer access

Two 96-byte buffers in shared memory are allocated for receive LAPD Controller to reduce the frequency of microprocessor interrupts and alleviate the response time requirement for microprocessor to handle each interrupt. There are no restrictions on the length of the message received. However, the 96-byte buffer is deep enough to hold one entire LAPD path or test signal identification message.

3.0 OVERHEAD INTERFACE BLOCK

The XRT86L34 has the ability to extract or insert DS1 data link information from or into the following:

- Facility Data Link (FDL) bits in ESF framing format mode
- Signaling Framing (Fs) bits in SLC®96 and N framing format mode
- Remote Signaling (R) bits in T1DM framing format mode

The source and destination of these inserted and extracted data link bits would be from either the internal HDLC Controller or the external device accessible through DS1 Overhead Interface Block. The operation of the Transmit Overhead Input Interface Block and the Receive Overhead Output Interface Block will be discussed separately.

3.1 DS1 TRANSMIT OVERHEAD INPUT INTERFACE BLOCK

3.1.1 Description of the DS1 Transmit Overhead Input Interface Block

The DS1 Transmit Overhead Input Interface Block will allow an external device to be the provider of the Facility Data Link (FDL) bits in ESF framing format mode, Signaling Framing (Fs) bits in the SLC96 and N framing format mode and Remote Signaling (R) bit in T1DM framing format mode. This interface provides interface signals and required interface timing to shift in proper data link information at proper time.

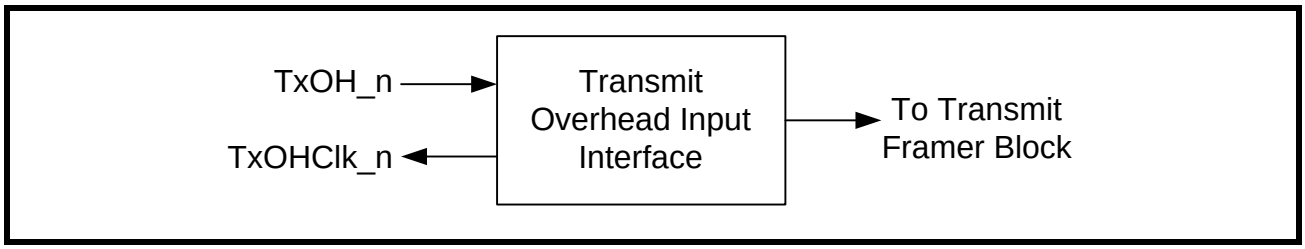
The Transmit Overhead Input Interface for a given Framer consists of two signals.

- TxOHClk_n: The Transmit Overhead Input Interface Clock Output signal
- TxOH_n: The Transmit Overhead Input Interface Input signal.

The Transmit Overhead Input Interface Clock Output pin (TxOHCLK_n) generates a rising clock edge for each data link bit position according to configuration of the framer. The Data Link equipment interfaced to the Transmit Overhead Input Interface block should update the data link bits on the TxOH_n line upon detection of the rising edge of TxOHClk_n. The Transmit Overhead Input Interface block will sample and latch the data link bits on the TxOH_n line on the falling edge of TxOHClk_n. The data link bits will be included and transmitted via the outgoing DS1 frames.

The figure below shows block diagram of the DS1 Transmit Overhead Input Interface of XRT86L34.

FIGURE 10. BLOCK DIAGRAM OF THE DS1 TRANSMIT OVERHEAD INPUT INTERFACE OF THE XRT86L34



3.1.2 Configure the DS1 Transmit Overhead Input Interface module as source of the Facility Data Link (FDL) bits in ESF framing format mode

The FDL bits in ESF framing format mode can be inserted from:

- DS1 Transmit Overhead Input Interface Block
- DS1 Transmit HDLC Controller
- DS1 Transmit Serial Input Interface.

The Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR) controls the insertion of data link bits into the FDL bits in ESF framing format mode. The table below shows configuration of the Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR).

TRANSMIT DATA LINK SELECT REGISTER (TDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Data Link Source Select	R/W	00 - The Facility Data Link bits are inserted into the framer through either the LAPD controller or the SLCâ96 buffer. 01 - The Facility Data Link bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins. 10 - The Facility Data Link bits are inserted into the framer through the Transmit Overhead Input Interface via the TxOH_n pins. 11 - The Facility Data Link bits are forced to one by the framer.

If the Transmit Data Link Source Select bits of the Transmit Data Link Select Register are set to 10, the Transmit Overhead Input Interface Block becomes input source of the FDL bits.

The XRT86L34 allows the user to select bandwidth of the Facility Data Link Channel in ESF framing format mode. The FDL can be either a 4KHz or 2KHz data link channel. The Transmit Data Link Bandwidth Select bits of the Transmit Data Link Select Register (TDLSR) determine the bandwidth of FDL channel in ESF framing format mode.

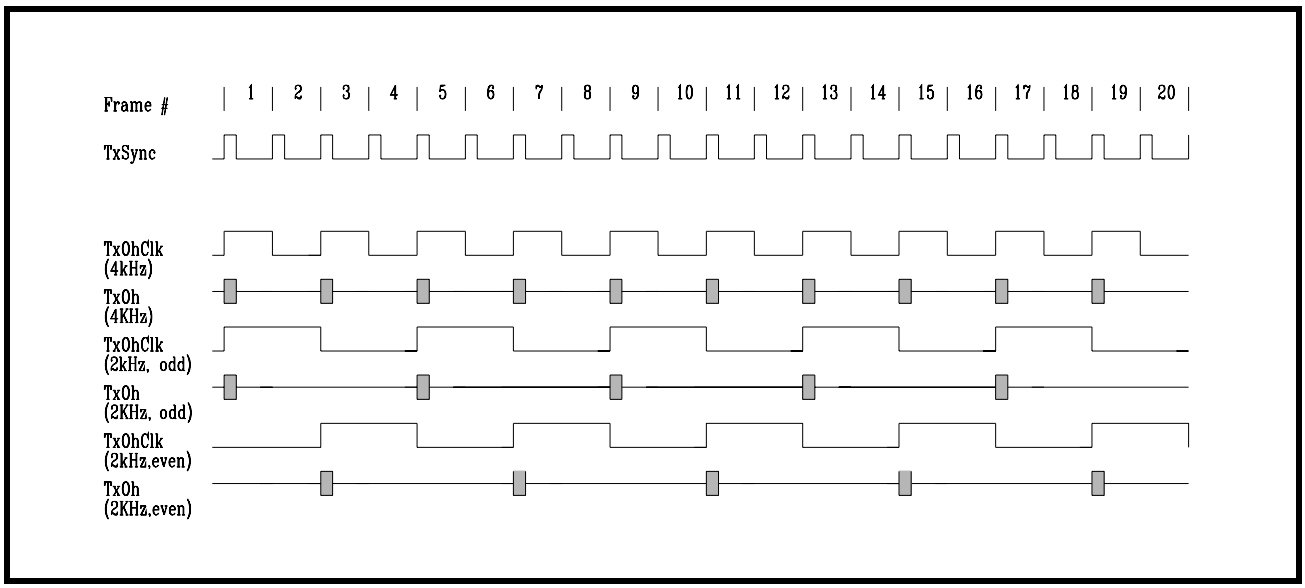
The table below shows configuration of the Transmit Data Link Bandwidth Select bits of the Transmit Data Link Select Register (TDLSR).)

TRANSMIT DATA LINK SELECT REGISTER (TDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	Transmit Data Link Bandwidth Select	R/W	00 - The Facility Data Link is a 4KHz channel. All available FDL bits (first bit of every other frame) are used as data link bits. 01 - The Facility Data Link is a 2KHz channel. Only the odd FDL bits (first bit of frame 1, 5, 9…) are used as data link bits. 10 - The Facility Data Link is a 2KHz channel. Only the even FDL bits (first bit of frame 3, 7, 11…) are used as data link bits.

Figure 11 below shows the timing diagram of the input and output signals associated with the DS1 Transmit Overhead Input Interface module in ESF framing format mode.

FIGURE 11. DS1 TRANSMIT OVERHEAD INPUT INTERFACE TIMING IN ESF FRAMING FORMAT MODE



3.1.3 Configure the DS1 Transmit Overhead Input Interface module as source of the Signaling Framing (Fs) bits in N or SLC®96 framing format mode

The Fs bits in SLC®96 and N framing format mode can be inserted from:

- DS1 Transmit Overhead Input Interface Block
- DS1 Transmit HDLC Controller
- DS1 Transmit Serial Input Interface.

The Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR) controls the insertion of data link bits into the Fs bits in N or SLC®96 framing format mode. The table below shows configuration of the Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR).

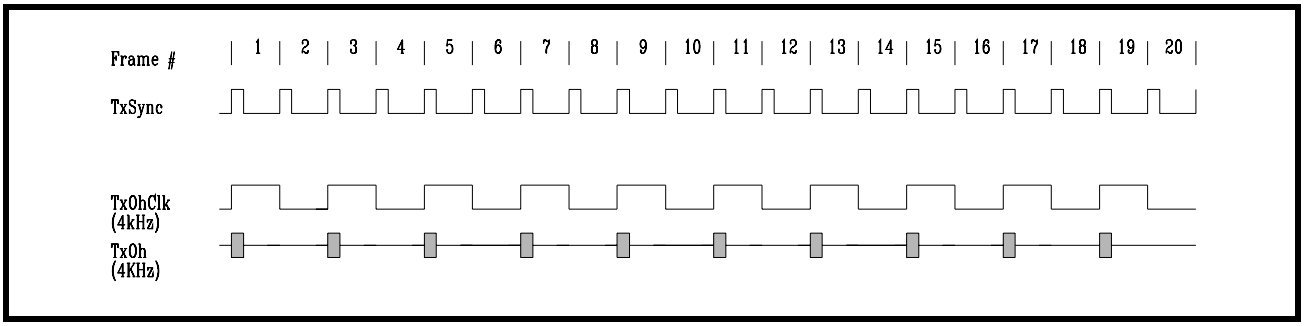
TRANSMIT DATA LINK SELECT REGISTER (TDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Data Link Source Select	R/W	00 - The Signaling Framing bits are inserted into the framer through either the LAPD controller or the SLCâ96 buffer. 01 - The Signaling Framing bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins. 10 - The Signaling Framing bits are inserted into the framer through the Transmit Overhead Input Interface via the TxOH_n pins. 11 - The Signaling Framing bits are forced to one by the framer.

If the Transmit Data Link Source Select bits of the Transmit Data Link Select Register are set to 10, the Transmit Overhead Input Interface Block becomes input source of the Fs bits.

Figure 12 below shows the timing diagram of the input and output signals associated with the DS1 Transmit Overhead Input Interface module in N or SLC®96 framing format mode.

FIGURE 12. DS1 TRANSMIT OVERHEAD INPUT TIMING IN N OR SLC®96 FRAMING FORMAT MODE



3.1.4 Configure the DS1 Transmit Overhead Input Interface module as source of the Remote Signaling (R) bits in T1DM framing format mode

The R bits in T1DM framing format mode can be inserted from:

- DS1 Transmit Overhead Input Interface Block
- DS1 Transmit HDLC Controller
- DS1 Transmit Serial Input Interface.

The Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR) controls the insertion of data link bits into the R bits in T1DM framing format mode. The table below shows configuration of the Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR).

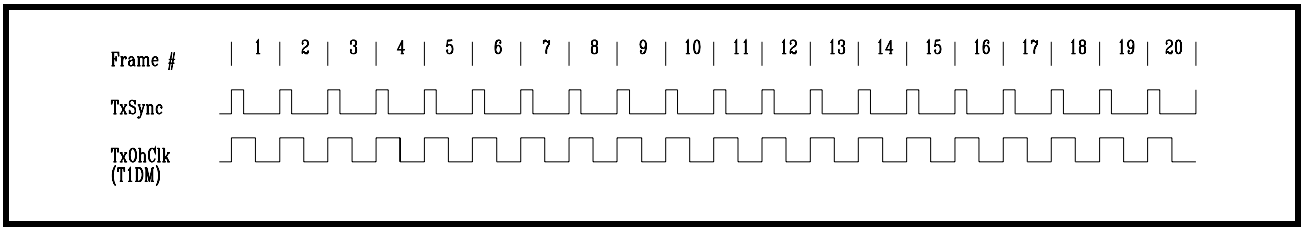
TRANSMIT DATA LINK SELECT REGISTER (TDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Data Link Source Select	R/W	00 - The Remote Signaling bits are inserted into the framer through either the LAPD controller or the SLCâ96 buffer. 01 - The Remote Signaling bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins. 10 - The Remote Signaling bits are inserted into the framer through the Transmit Overhead Input Interface via the TxOH_n pins. 11 - The Remote Signaling bits are forced to one by the framer.

If the Transmit Data Link Source Select bits of the Transmit Data Link Select Register are set to 10, the Transmit Overhead Input Interface Block becomes input source of the R bits. Since R bit presents in Timeslot 24 of every T1DM frame, therefore, bandwidth of T1DM data link channel is 8KHz.

Figure 13 below shows the timing diagram of the input and output signals associated with the DS1 Transmit Overhead Input Interface module in T1DM framing format mode.

FIGURE 13. DS1 TRANSMIT OVERHEAD INPUT INTERFACE MODULE IN T1DM FRAMING FORMAT MODE



3.2 DS1 RECEIVE OVERHEAD OUTPUT INTERFACE BLOCK

3.2.1 Description of the DS1 Receive Overhead Output Interface Block

The DS1 Receive Overhead Output Interface Block allows an external device to be the consumer of the Facility Data Link (FDL) bits in ESF framing format mode, Signaling Framing (Fs) bits in the SLC96 and N framing format mode and Remote Signaling (R) bit in T1DM framing format mode This interface provides interface signals and required interface timing to shift out proper data link information at proper time.

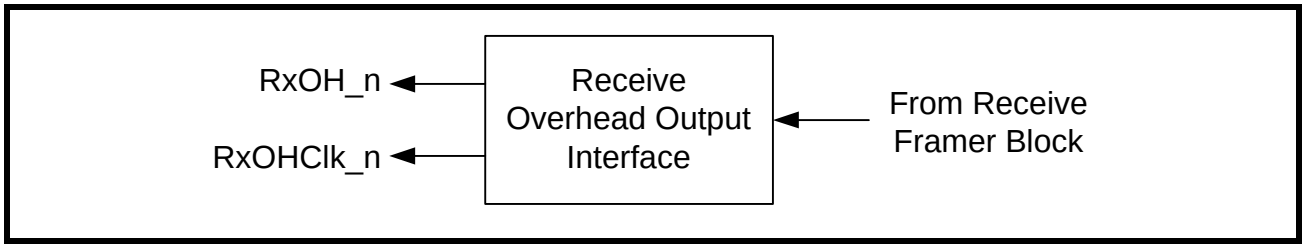
The Receive Overhead Output Interface for a given Framer consists of two signals.

- RxOHClk_n: The Receive Overhead Output Interface Clock Output signal
- RxOH_n: The Receive Overhead Output Interface Output signal.

The Receive Overhead Output Interface Clock Output pin (RxOHCLK_n) generates a rising clock edge for each data link bit position according to configuration of the framer. The data link bits extracted from the incoming T1 frames are outputted from the Receive Overhead Output Interface Output pin (RxOH_n) at the rising edge of RxOHClk_n. The Data Link equipment should sample and latch the data link bits at the falling edge of RxOHClk_n.

The figure below shows block diagram of the Receive Overhead Output Interface of XRT86L34.

FIGURE 14. BLOCK DIAGRAM OF THE DS1 RECEIVE OVERHEAD OUTPUT INTERFACE OF XRT86L34



3.2.2 Configure the DS1 Receive Overhead Output Interface module as destination of the Facility Data Link (FDL) bits in ESF framing format mode

The FDL bits in ESF framing format mode can be extracted to:

- DS1 Receive Overhead Output Interface Block
- DS1 Receive HDLC Controller
- DS1 Receive Serial Output Interface.

The Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR) controls the extraction of FDL bits in ESF framing format mode. The table below shows configuration of the Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR).

RECEIVE DATA LINK SELECT REGISTER (TDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Receive Data Link Destination Select	R/W	00 - The extracted Facility Data Link bits are stored in either the LAPD controller or the SLCâ96 buffer. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 01 - The extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 10 - The extracted Facility Data Link bits are outputted from the framer through the Receive Overhead Output Interface via the RxOH_n pins. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 11 - The Facility Data Link bits are forced to one by the framer.

If the Receive Data Link Source Select bits of the Receive Data Link Select Register are set to 10, the Receive Overhead Output Interface Block becomes Output source of the FDL bits.

The XRT86L34 allows the user to select bandwidth of the Facility Data Link Channel in ESF framing format mode. The FDL can be either a 4KHz or 2KHz data link channel. The Receive Data Link Bandwidth Select bits of the Receive Data Link Select Register (RDLSR) determine the bandwidth of FDL channel in ESF framing format mode.

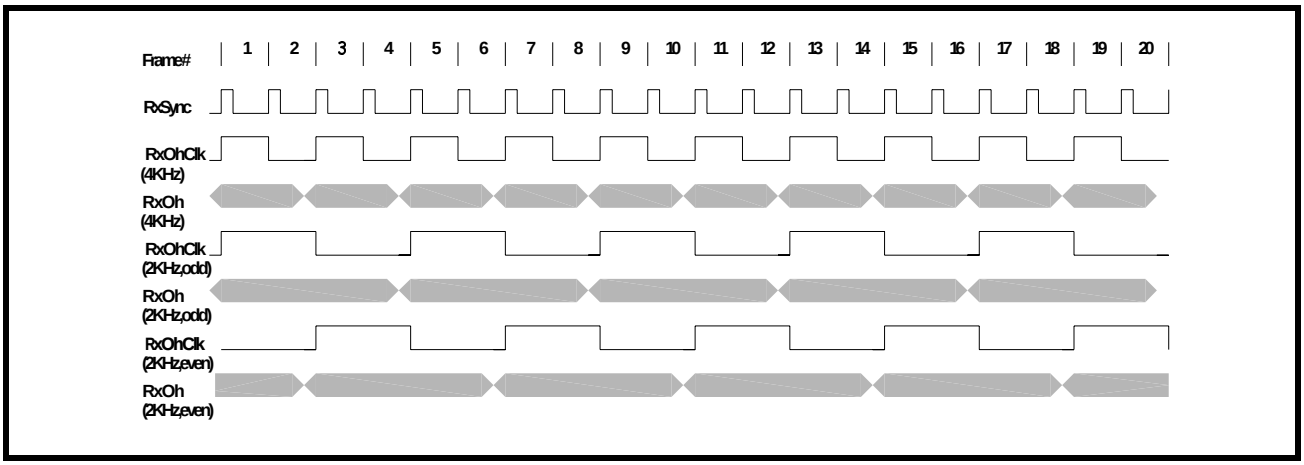
The table below shows configuration of the Receive Data Link Bandwidth Select bits of the Receive Data Link Select Register (TDLSR).

RECEIVE DATA LINK SELECT REGISTER (TDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	Receive Data Link Bandwidth Select	R/W	00 - The Facility Data Link is a 4KHz channel. All available FDL bits (first bit of every other frame) are used as data link bits. 01 - The Facility Data Link is a 2KHz channel. Only the odd FDL bits (first bit of frame 1, 5, 9…) are used as data link bits. 10 - The Facility Data Link is a 2KHz channel. Only the even FDL bits (first bit of frame 3, 7, 11…) are used as data link bits.

Figure 15 below shows the timing diagram of the Output and output signals associated with the DS1 Receive Overhead Output Interface module in ESF framing format mode.

FIGURE 15. DS1 RECEIVE OVERHEAD OUTPUT INTERFACE MODULE IN ESF FRAMING FORMAT MODE



3.2.3 Configure the DS1 Receive Overhead Output Interface module as destination of the Signaling Framing (Fs) bits in N or SLC®96 framing format mode

The Fs bits in SLC®96 and N framing format mode can be extracted to:

- DS1 Receive Overhead Output Interface Block
- DS1 Receive HDLC Controller
- DS1 Receive Serial Output Interface.

The Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR) controls the destination of Fs bits in N or SLC®96 framing format mode. The table below shows configuration of the Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR).

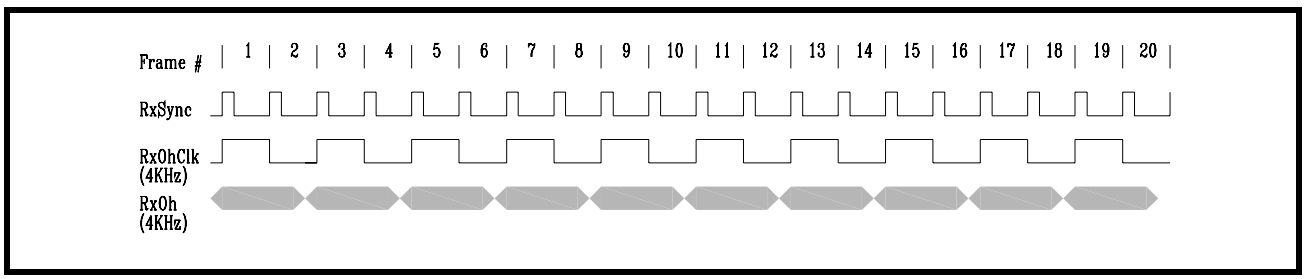
RECEIVE DATA LINK SELECT REGISTER (TDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Receive Data Link Source Select	R/W	00 - The extracted Facility Data Link bits are stored in either the LAPD controller or the SLCâ96 buffer. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 01 - The extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 10 - The extracted Facility Data Link bits are outputted from the framer through the Receive Overhead Output Interface via the RxOH_n pins. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 11 - The Facility Data Link bits are forced to one by the framer.

If the Receive Data Link Source Select bits of the Receive Data Link Select Register are set to 10, the Receive Overhead Output Interface Block outputs Fs bits extracted from the incoming T1 data stream.

Figure 16 below shows the timing diagram of the output signals associated with the DS1 Receive Overhead Output Interface module in N or SLC®96 framing format mode.

FIGURE 16. DS1 RECEIVE OVERHEAD OUTPUT INTERFACE TIMING IN N OR SLC®96 FRAMING FORMAT MODE



3.2.4 Configure the DS1 Receive Overhead Output Interface module as destination of the Remote Signaling (R) bits in T1DM framing format mode

The R bits in T1DM framing format mode can be extracted to:

- DS1 Receive Overhead Output Interface Block
- DS1 Receive HDLC Controller
- DS1 Receive Serial Output Interface.

The Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR) controls the destination of R bits in T1DM framing format mode. The table below shows configuration of the Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR).

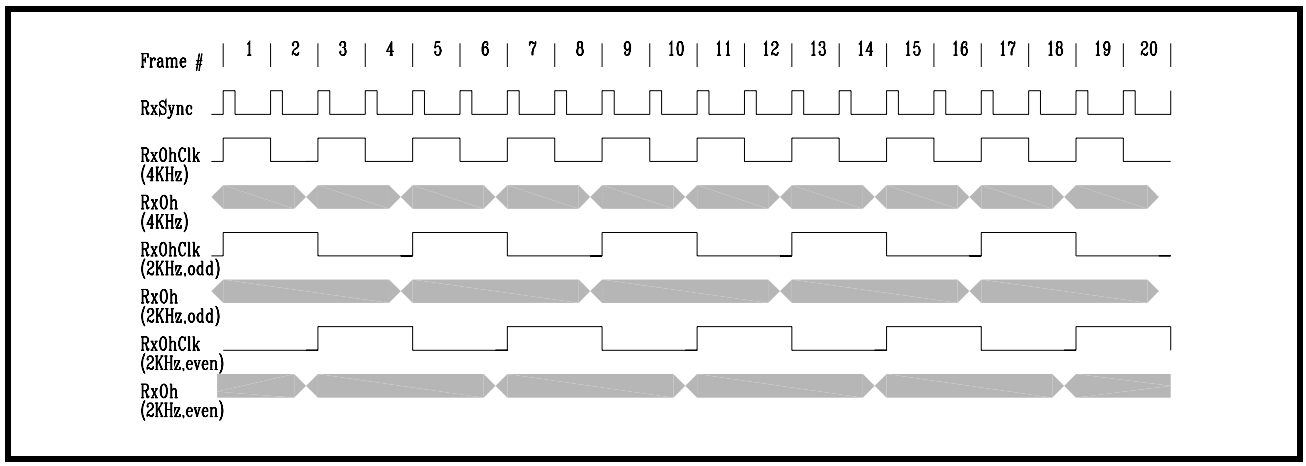
RECEIVE DATA LINK SELECT REGISTER (RDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Receive Data Link Source Select	R/W	00 - The extracted Facility Data Link bits are stored in either the LAPD controller or the SLC®96 buffer. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 01 - The extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 10 - The extracted Facility Data Link bits are outputted from the framer through the Receive Overhead Output Interface via the RxOH_n pins. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 11 - The Facility Data Link bits are forced to one by the framer.

If the Receive Data Link Source Select bits of the Receive Data Link Select Register are set to 10, the Receive Overhead Output Interface Block outputs the R bits extracted from the incoming T1 data stream. Since R bit presents in Timeslot 24 of every T1DM frame, therefore, bandwidth of T1DM data link channel is 8KHz.

Figure 17 below shows the timing diagram of the output signals associated with the DS1 Receive Overhead Output Interface module in T1DM framing format mode.

FIGURE 17. DS1 RECEIVE OVERHEAD OUTPUT INTERFACE TIMING IN T1DM FRAMING FORMAT MODE



3.3 E1 OVERHEAD INTERFACE BLOCK

The XRT86L34 has the ability to extract or insert E1 data link information from or into the E1 National bit sequence. The source and destination of these inserted and extracted data link bits would be from either the internal HDLC Controller or the external device accessible through E1 Overhead Interface Block. The operation of the Transmit Overhead Input Interface Block and the Receive Overhead Output Interface Block will be discussed separately.

3.4 E1 TRANSMIT OVERHEAD INPUT INTERFACE BLOCK

3.4.1 Description of the E1 Transmit Overhead Input Interface Block

The E1 Transmit Overhead Input Interface Block will allow an external device to be the provider of the E1 National bit sequence. This interface provides interface signals and required interface timing to shift in proper data link information at proper time.

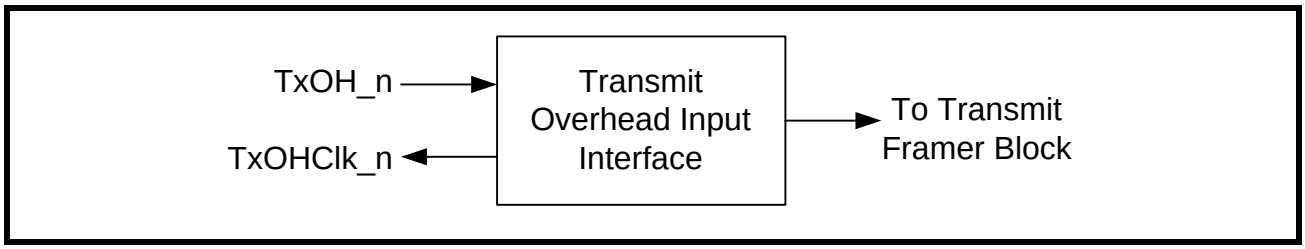
The Transmit Overhead Input Interface for a given Framer consists of two signals.

- TxOHClk_n: The Transmit Overhead Input Interface Clock Output signal
- TxOH_n: The Transmit Overhead Input Interface Input signal.

The Transmit Overhead Input Interface Clock Output pin (TxOHCLK_n) generates a rising clock edge for each National bit that is configured to carry Data Link information according to setting of the framer. The Data Link equipment interfaced to the Transmit Overhead Input Interface should update the data link bits on the TxOH_n line upon detection of the rising edge of TxOHClk_n. The Transmit Overhead Input Interface block will sample and latch the data link bits on the TxOH_n line on the falling edge of TxOHClk_n. The data link bits will be included in and transmitted via the outgoing E1 frames.

The figure below shows block diagram of the DS1 Transmit Overhead Input Interface of XRT86L34.

FIGURE 18. BLOCK DIAGRAM OF THE E1 TRANSMIT OVERHEAD INPUT INTERFACE OF XRT86L34



3.4.2 Configure the E1 Transmit Overhead Input Interface module as source of the National Bit Sequence in E1 framing format mode

The National Bit Sequence in E1 framing format mode can be inserted from:

- E1 Transmit Overhead Input Interface Block
- E1 Transmit HDLC Controller
- E1 Transmit Serial Input Interface

The purpose of the Transmit Overhead Input Interface is to permit Data Link equipment direct access to the Sa4 through Sa8 National bits that are to be transported via the outbound frames. The Transmit Data Link Source Select [1:0] bits, within the Synchronization MUX Register (SMR) determine source of the Sa4 through Sa8 National bits to be inserted into the outgoing E1 frames.

The table below shows configuration of the Transmit Data Link Source Select [1:0] bits of the Synchronization MUX Register (SMR).

SYNCHRONIZATION MUX REGISTER (SMR) (ADDRESS = 0XN109H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Transmit Data Link Source Select [1:0]	R/W	00 - The Sa4 through Sa8 National bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins. 01 - The Sa4 through Sa8 National bits are inserted into the framer through the Transmit LAPD Controller. 10 - The Sa4 through Sa8 National bits are inserted into the framer through the Transmit Overhead Input Interface via the TxOH_n pins. 11 - The Sa4 through Sa8 National bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins.

If the Transmit Data Link Source Select bits of the Transmit Data Link Select Register are set to 10, the Transmit Overhead Input Interface Block becomes input source of the FDL bits.

The XRT86L34 allows the user to decide on the following:

- How many of the National Bits will be used to carry the Data Link information bits

- Which of these National Bits will be used to carry the Data Link information bits.

The Transmit Sa Data Link Select bits of the Transmit Signaling and Data Link Select Register (TSDLSR) determine which ones of the National bits are configured as Data Link bits in E1 framing format mode. Depending upon the configuration of the Transmit Signaling and Data Link Select Register, either of the following cases may exists:

- None of the National bits are used to transport the Data Link information bits (That is, data link channel of XRT86L34 is inactive).
- Any combination of between 1 and all 5 of the National bits can be selected to transport the Data Link information bits.

The table below shows configuration of the Transmit Sa Data Link Select bits of the Transmit Signaling and Data Link Select Register (TSDLSR).

TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) (ADDRESS = 0XN10AH)

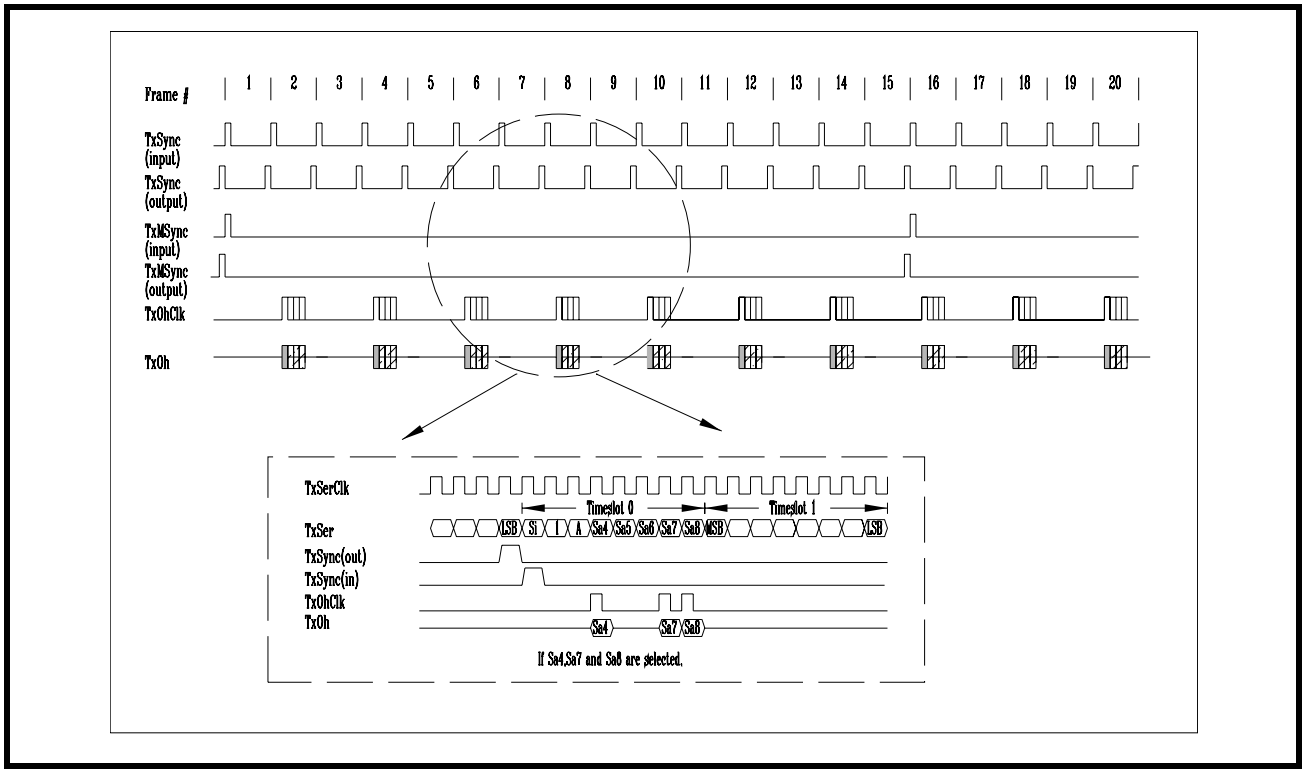
BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Transmit Sa8 Data Link Select	R/W	0 - Source of the Sa8 Nation bit is not from the data link interface. 1 - Source the Sa8 National bit from the data link interface.
6	Transmit Sa7 Data Link Select	R/W	0 - Source of the Sa7 Nation bit is not from the data link interface. 1 - Source the Sa7 National bit from the data link interface.
5	Transmit Sa6 Data Link Select	R/W	0 - Source of the Sa6 Nation bit is not from the data link interface. 1 - Source the Sa6 National bit from the data link interface.
4	Transmit Sa5 Data Link Select	R/W	0 - Source of the Sa5 Nation bit is not from the data link interface. 1 - Source the Sa5 National bit from the data link interface.
3	Transmit Sa4 Data Link Select	R/W	0 - Source of the Sa4 Nation bit is not from the data link interface. 1 - Source the Sa4 National bit from the data link interface.

For every Sa bit that is selected to carry Data Link information, the Transmit Overhead Input Interface will supply a clock pulse, via the TxOHClk_n output pin, such that:

- The Data Link equipment interfaced to the Transmit Overhead Input Interface should update the data on the TxOH_n line upon detection of the rising edge of TxOHClk_n.
- The Transmit Overhead Input Interface will sample and latch the data on the TxOH_n line on the falling edge of TxOHClk_n.

Figure 19 below shows the timing diagram of the input and output signals associated with the E1 Transmit Overhead Input Interface module in E1 framing format mode.

FIGURE 19. E1 TRANSMIT OVERHEAD INPUT INTERFACE TIMING



3.5 E1 RECEIVE OVERHEAD INTERFACE

3.5.1 Description of the E1 Receive Overhead Output Interface Block

The E1 Receive Overhead Output Interface Block will allow an external device to be the consumer of the E1 National bit sequence. This interface provides interface signals and required interface timing to shift out proper data link information at proper time.

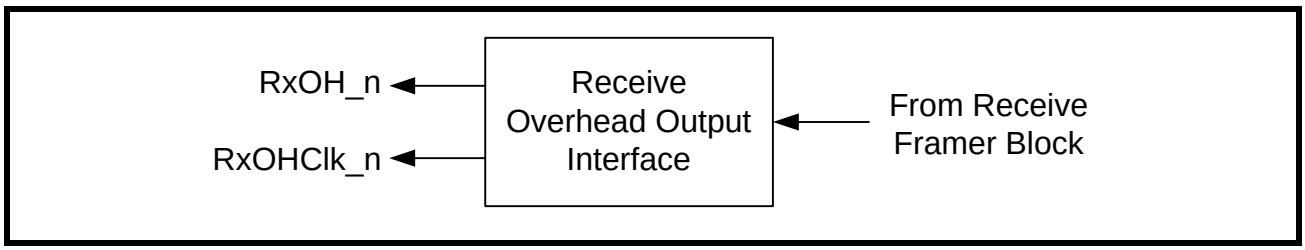
The Receive Overhead Output Interface for a given Framer consists of two signals.

- RxOHClk_n: The Receive Overhead Output Interface Clock Output signal
- RxOH_n: The Receive Overhead Output Interface Output signal.

The Receive Overhead Output Interface Clock Output pin (RxOHCLK_n) generates a rising clock edge for each National bit that is configured to carry Data Link information according to setting of the framer. The data link bits extracted from the incoming E1 frames are outputted from the Receive Overhead Output Interface Output pin (RxOH_n) before the rising edge of RxOHClk_n. The Data Link equipment should sample and latch the data link bits at the rising edge of RxOHClk_n.

The figure below shows block diagram of the Receive Overhead Output Interface of XRT86L34.

FIGURE 20. BLOCK DIAGRAM OF THE E1 RECEIVE OVERHEAD OUTPUT INTERFACE OF XRT86L34



3.5.2 Configure the E1 Receive Overhead Output Interface module as source of the National Bit Sequence in E1 framing format mode

The National Bit Sequence in E1 framing format mode can be extracted and directed to:

- E1 Receive Overhead Output Interface Block
- E1 Receive HDLC Controller
- E1 Receive Serial Output Interface

The purpose of the Receive Overhead Output Interface is to permit Data Link equipment to have direct access to the Sa4 through Sa8 National bits that are extracted from the incoming E1 frames. Independent of the availability of the E1 Receive HDLC Controller module, the XRT86L34 always output the received National bits through the Receive Overhead Output Interface block.

The XRT86L34 allows the user to decide on the following:

- How many of the National Bits is used to carry the Data Link information bits
- Which of these National Bits is used to carry the Data Link information bits.

The Receive Sa Data Link Select bits of the Receive Signaling and Data Link Select Register (TSDLSR) determine which ones of the National bits are configured as Data Link bits in E1 framing format mode. Depending upon the configuration of the Receive Signaling and Data Link Select Register, either of the following cases may exists:

- None of the received National bits are used to transport the Data Link information bits (That is, data link channel of XRT86L34 is inactive).
- Any combination of between 1 and all 5 of the received National bits are used to transport the Data Link information bits.

The table below shows configuration of the Receive Sa Data Link Select bits of the Receive Signaling and Data Link Select Register (RSDLSR).

RECEIVE SIGNALING AND DATA LINK SELECT REGISTER (RSDLSR) (ADDRESS = 0XN10CH)

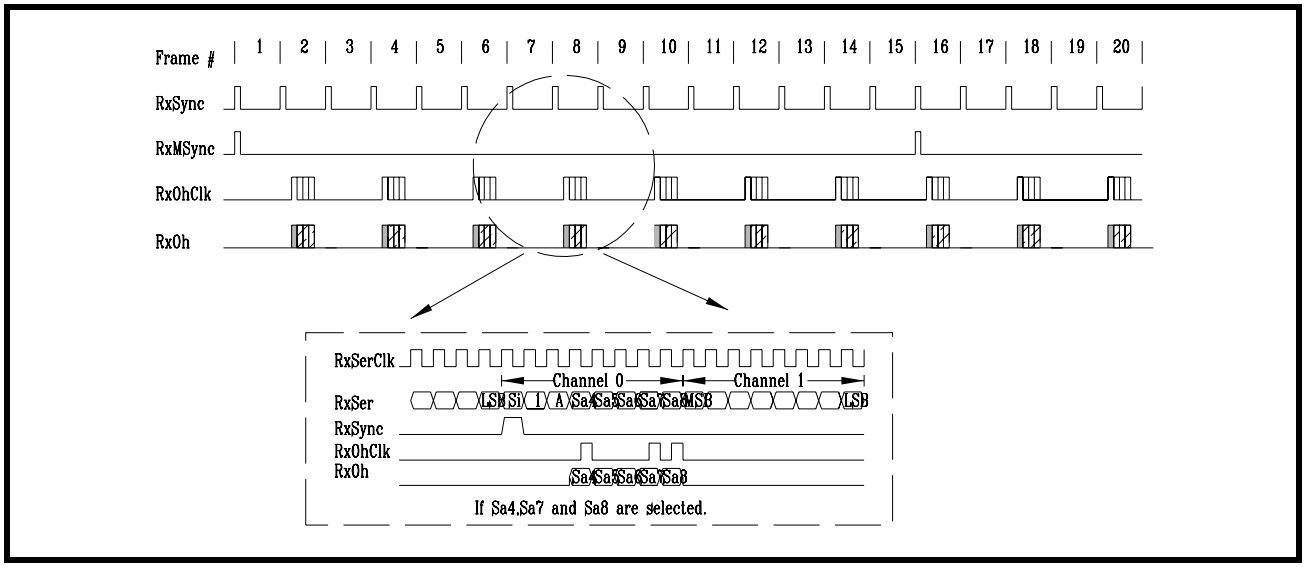
BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Sa8 Data Link Select	R/W	0 - The received Sa8 Nation bit is not extracted to the data link interface. 1 - The received Sa8 Nation bit is extracted to the data link interface.
6	Receive Sa7 Data Link Select	R/W	0 - The received Sa7 Nation bit is not extracted to the data link interface. 1 - The received Sa7 Nation bit is extracted to the data link interface.
5	Receive Sa6 Data Link Select	R/W	0 - The received Sa6 Nation bit is not extracted to the data link interface. 1 - The received Sa6 Nation bit is extracted to the data link interface.
4	Receive Sa5 Data Link Select	R/W	0 - The received Sa5 Nation bit is not extracted to the data link interface. 1 - The received Sa5 Nation bit is extracted to the data link interface.
3	Receive Sa4 Data Link Select	R/W	0 - The received Sa4 Nation bit is not extracted to the data link interface. 1 - The received Sa4 Nation bit is extracted to the data link interface.

For every received Sa bit that is determined to carry Data Link information, the Receive Overhead Output Interface will supply a clock pulse, via the RxOHClk_n output pin, such that:

- The Receive Overhead Output interface should update the data on the RxOH_n line before the rising edge of RxOHClk_n.
- The external Data Link equipment interfaced to the Receive Overhead Output Interface will sample and latch the data on the RxOH_n line on the rising edge of RxOHClk_n.

Figure 21 below shows the timing diagram of the output signals associated with the E1 Receive Overhead Output Interface module in E1 framing format mode.

FIGURE 21. E1 RECEIVE OVERHEAD OUTPUT INTERFACE TIMING



4.0 THE E1 TRANSMIT SECTION

4.1 THE E1 TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK

4.1.1 Description of the Transmit Payload Data Input Interface Block

Each of the four framers within the XRT86L34 device includes a Transmit Payload Data Input Interface block. The function of this block is to provide an interface to the local Terminal Equipment (for example, a Central Office or switching equipment) that has data to send to a "Far End" terminal over a DS1 or E1 transport medium.

The Payload Data Input Interface module (also known as the Back-plane Interface module) supports payload data to be taken from or presented to the system. In DS1 mode, supported data rates are 1.544Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 12.352Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s. In E1 mode, supported data rates are MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s.

The Transmit Payload Data Input Interface block supplies or accepts the following signals to the local Terminal Equipment circuitry:

- Transmit Serial Data Input (TxSer_n)
- Transmit Serial Clock (TxSerClk_n)
- Transmit Single-frame Synchronization Signal (TxSync_n)
- Transmit Multi-frame Synchronization Signal (TxMSync_n)
- Transmit Time-slot Indicator Clock (TxTSClk_n)
- Transmit Time-slot Indication Bits (TxTSb[4:0]_n)

The Transmit Serial Data is an input pin carrying payload, signaling and sometimes Data Link data supplied by the local Terminal Equipment to the XRT86L34 device.

The Transmit Serial Clock is an input or output signal used by the Transmit Payload Data Input Interface block to latch in incoming serial data from the local Terminal Equipment. The Transmit Clock Inversion bit of the Transmit Interface Control Register (TICR) determines at which edge of the Transmit Serial Clock would data transition on the Transmit Serial Data pin occur.

The table below shows configurations of the Transmit Clock Inversion bit of the Transmit Interface Control Register (TICR).

TRANSMIT INTERFACE CONTROL REGISTER (TICR) (ADDRESS = 0XN120H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Transmit Clock Inversion	R/W	0 - Serial data transition happens on rising edge of the Transmit Serial Clock. 1 - Serial data transition happens on falling edge of the Transmit Serial Clock.

Throughout the discussion of this datasheet, we assume that serial data transition happens on rising edge of the Transmit Serial Clock unless stated otherwise.

The Transmit Single-frame Synchronization signal is either input or output. When configure as input, it indicates beginning of an E1 frame. When configure as output, it indicates end of an E1 frame.

The Transmit Multi-frame Synchronization signal is either input or output. When configure as input, it indicates beginning of an E1 multi-frame. When configure as output, it indicates end of an E1 multi-frame.

The Transmit Input Clock signal is multiplexed into the Transmit Multi-frame Synchronization pin (TxMSync_n) of XRT86L34 device. When the framer is running at High-speed Back-plane Interface mode, the Transmit Input Clock functions as the timing source for the High-speed Back-plane Interface.

By connecting these signals with the local Terminal Equipment, the Transmit Payload Data Input Interface accepts payload data from the Terminal Equipment and routes it to the Transmit Framer module inside the device.

4.1.2 Brief Discussion of the Transmit Payload Data Input Interface Block Operating at XRT84V24 Compatible 2.048Mbit/s mode

If the framer is operating in normal 2.048Mbit/s Back-plane interface mode for E1, timing source of the transmit section can be one of the three clocks:

- Transmit Serial Input Clock
- OSCCLK Driven Divided Clock
- Recovered Receive Line Clock

The Transmit Timing Source Select [1:0] bits of the Clock Select Register (CSR) determine which clock is used as the timing source. The following table shows configurations of the Transmit Timing Source Select [1:0] bits of the Clock Select Register.

CLOCK SELECT REGISTER (CSR) (ADDRESS = 0XN100H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Timing Source Select	R/W	**Transmit Timing Source Select:** These two READ/WRITE bit-fields permit the user to select the timing source of Transmit section of the framer. When the Transmit Back-plane interface is operating at a clock rate of 2.048MHz for E1, these two READ/WRITE bit-fields also determine the direction of Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk). When the framer is operating at other Back-plane mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all inputs. 00 - The Recovered Receive Line Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 2.048MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer. 01 - The Transmit Serial Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 2.048MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all inputs. 10 - The OSCCLK Driven Divided clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 2.048MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer. 11 - The Recovered Receive Line Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 2.048MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer.

The Transmit Serial Clock (TxSerClk_n), Transmit Single-frame Synchronization Signal (TxSync_n) and Transmit Multi-frame Synchronization Signal (TxMSync_n) can be either inputs or outputs depend on the timing source of the Transmit section of the framer.

With the OSCCLK Driven Divided Clock or the Recovered Receive Line Clock being the timing source of the transmit section, the Transmit Serial Clock (TxSerClk_n), Transmit Single-frame Synchronization Signal (TxSync_n) and Transmit Multi-frame Synchronization Signal (TxMSync_n) are all outputs.

With the timing source of the transmit section being the Transmit Serial Input Clock, the Transmit Serial Clock (TxSerClk_n), Transmit Single-frame Synchronization Signal (TxSync_n) and Transmit Multi-frame Synchronization Signal (TxMSync_n) are all inputs.

The following table illustrates the input and output nature of these signals for different Transmit timing sources.

TRANSMIT TIMING SOURCE	TXSERCLK_N	TXSYNC_N	TXMSYNC_N
Terminal Equipment Driven TxSerClk	Input	Input	Input
OSCCLK Driven Divided Clock	Output	Output	Output
Recovered Receive Line Clock	Output	Output	Output

The Transmit Time-slot Indication Bits (TxTSb[4:0]_n) are multiplexed I/O pins. The functionality of these pins is governed by the value of Transmit Fractional E1 Input Enable bit of the Transmit Interface Control Register (TICR).

The following table illustrates the configurations of the Transmit Fractional E1 Input Enable bit.

TRANSMIT INTERFACE CONTROL REGISTER (TICR) (ADDRESS = 0XN120H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Transmit Fractional E1 Input Enable	R/W	0 - The Transmit Time-slot Indication bits (TxTSb[4:0] are outputting five-bit binary values of Time-slot number (0-31) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. The Transmit Time-slot Indicator Clock signal (TxTSClk_n) is a 256KHz clock that pulses HIGH for one E1 bit period whenever the Transmit Payload Data Input Interface block is accepting the LSB of each of the twenty-four time slots. 1 - The TxTSb[0]_n bit becomes the Transmit Fractional E1 Input signal (TxFrTD_n) which carries Fractional E1 payload data into the framer. The TxTSb[1]_n bit becomes the Transmit Signaling Data Input signal (TxSig_n) which is used to insert robbed-bit signaling data into the outbound E1 frame. The TxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-31) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. The TxTSb[3]_n bit becomes the Transmit Overhead Synchronization Pulse (TxOHSync_n) which is used to output an Overhead Synchronization Pulse that indicates the first bit of each E1multi-frame. The TxTSClk_n will output gaped fractional E1 clock that can be used by Terminal Equipment to clock out Fractional E1 payload data at rising edge of the clock. Or, The TxTSClk_n pin will be a clock enable signal to Transmit Fractional E1 Input signal (TxFrTD_n) when the un-gaped Transmit Serail Input Clock (TxSerClk_n) is used to clock in Fractional E1 Payload Data into the framer.

When configured to operate in normal condition (that is, when the Transmit Fractional E1 Input Enable bit is equal to zero), these bits reflect the five-bit binary value of the Time Slot number (0-31) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. TxTSb[4] represents the MSB of the binary value and TxTSb[0] represents the LSB.

When the Transmit Fractional E1 Input Enable bit is equal to one, the TxTSb[0]_n bit becomes the Transmit Fractional E1 Input signal (TxFrTD_n). This input pin carries Fractional E1 Input data to be inserted into the outbound E1 data stream. The Fraction E1 Input Interface allows certain time-slots of outbound E1 data stream to have a different source other than the local Terminal Equipment. Function of the Fractional E1 Input signal will be discussed in details in later sections.

When the Transmit Fractional E1 Input Enable bit is equal to one, the TxTSb[1]_n bit becomes the Transmit Signaling Data Input signal (TxSig_n). These input pins can be used to insert robbed-bit signaling data into the outbound E1 frame. Function of the Transmit Signaling Data Input signal will be discussed in details in later sections.

When the Transmit Fractional E1 Input Enable bit is equal to one, the TxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-31) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. MSB of the binary value is presented first and the LSB is presented last.

When the Transmit Fractional E1 Input Enable bit is equal to one, the TxTSb[3]_n bit becomes the Transmit Overhead Synchronization Pulse (TxOHSync_n). These pins can be used to output an Overhead Synchronization Pulse that indicates the first bit of each E1multi-frame. Function of the Transmit Overhead Synchronization Output signal will be discussed in details in later sections.

The TxTSb[4]_n bit is not multiplexed.

The table below shows functionality of the TxTSb[3:0] bits when the Transmit Fractional E1 Input bit is set to different values.

TRANSMIT FRACTIONAL E1 INPUT BIT = 0		TRANSMIT FRACTIONAL E1 INPUT BIT = 1	
TxTSb[0]	Output	TxFrTD	Input
TxTSb[1]	Output	TxSig	Input
TxTSb[2]	Output	TxTS	Output
TxTSb[3]	Output	TxOHSync	Output

The Transmit Time-slot Indicator Clock signal (TxTSClk_n) is a multi-function output pin. When configured to operate in normal condition (that is, when the Transmit Fractional E1 Input Enable bit is equal to zero), the TxTSClk_n is a 256KHz clock that pulses HIGH for one E1 bit period whenever the Transmit Payload Data Input Interface block is accepting the LSB of each of the twenty-four time slots. The local Terminal Equipment should use this clock signal to sample the TxTSb[0] through TxTSb[4] bits and identify the time-slot being processed via the Transmit Section of the framer.

When the Transmit Fractional E1 Input Enable bit is equal to one, the TxTSClk_n will output gaped fractional E1 clock at time-slots where Fractional E1 Input data is present. This clock can be used by Terminal Equipment to clock out Fractional E1 payload data at rising edge of the clock. The framer will then input Fractional E1 payload data using falling edge of the clock. Otherwise, this pin can be configured as a clock enable signal to Transmit Fractional E1 Input signal (TxFrTD_n) if the framer is set accordingly. In this way, Fractional E1 payload data is clocked into the framer using un-gaped Transmit Serail Input Clock (TxSerClk_n). A detailed discussion of the Fractional E1 Payload Data Input Interface can be found in later sections.

Both the Transmit Time-slot Indicator Clock (TxTSClk_n) and the Transmit Time-slot Indication Bits (TxTSbb[4:0]_n) are output signals in normal 2.048Mbit/s Back-plane mode regardless of the timing source of the Transmit Section of framer.

A detailed discussion of how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment using different timing sources can be found in the later sections.

4.1.2.1 Connect the Transmit Payload Data Input Interface block to the Local Terminal Equipment if Transmit Timing Source = TxSerClk_n

By setting the Transmit Timing Source [1:0] bits of the Clock Select Register to 01, the TxSerClk_n input signal is configured to be the timing source for the Transmit section of the framer. The Terminal Equipment should supply an external free-running clock with frequency of 2.048MHz to the TxSerClk_n input pin. The Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal are inputs to the framer.

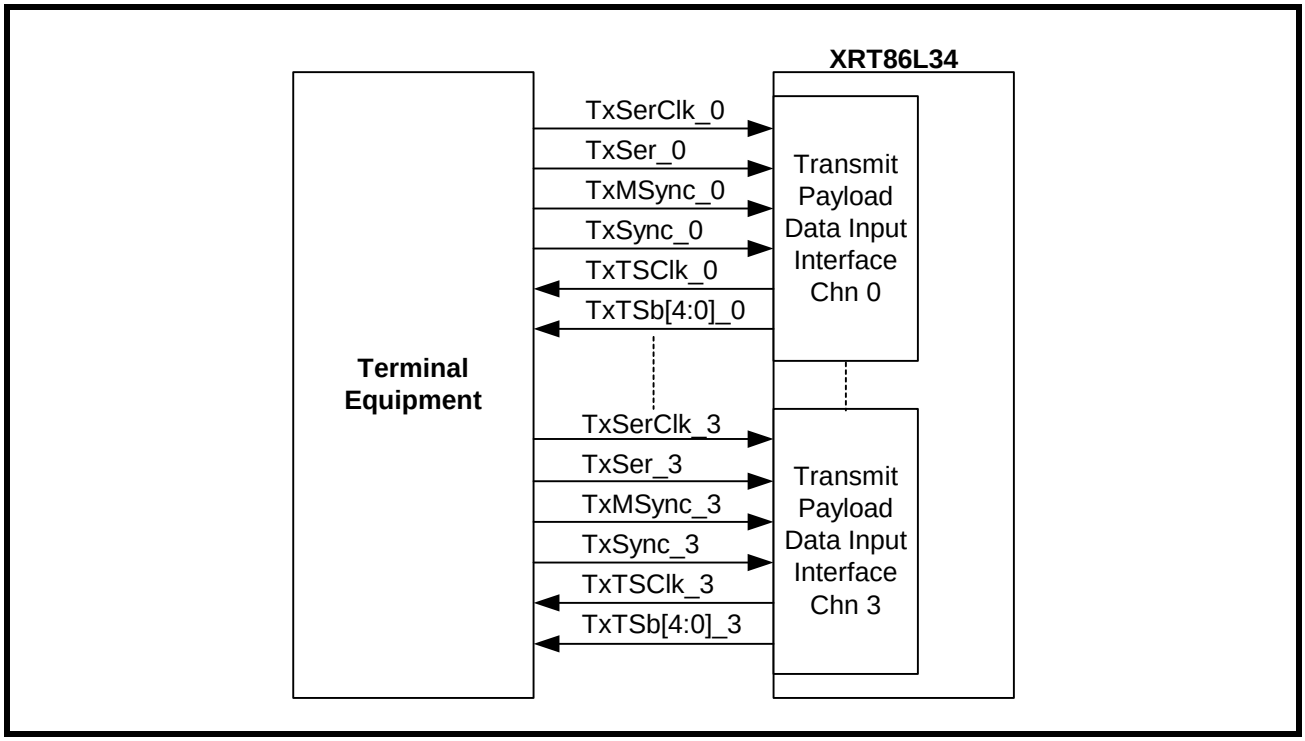
The Transmit Single-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the first bit position of each E1 frame. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of an E1 frame.

The Transmit Multi-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the first bit position of the first frame of an E1 multi-frame. By sampling the HIGH pulse on the Transmit Multi-frame Synchronization signal, the framer can position the beginning of an E1 super-frame.

It is the responsibility of the Terminal Equipment to provide serial input data through the TxSer_n pin aligned with the Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal.

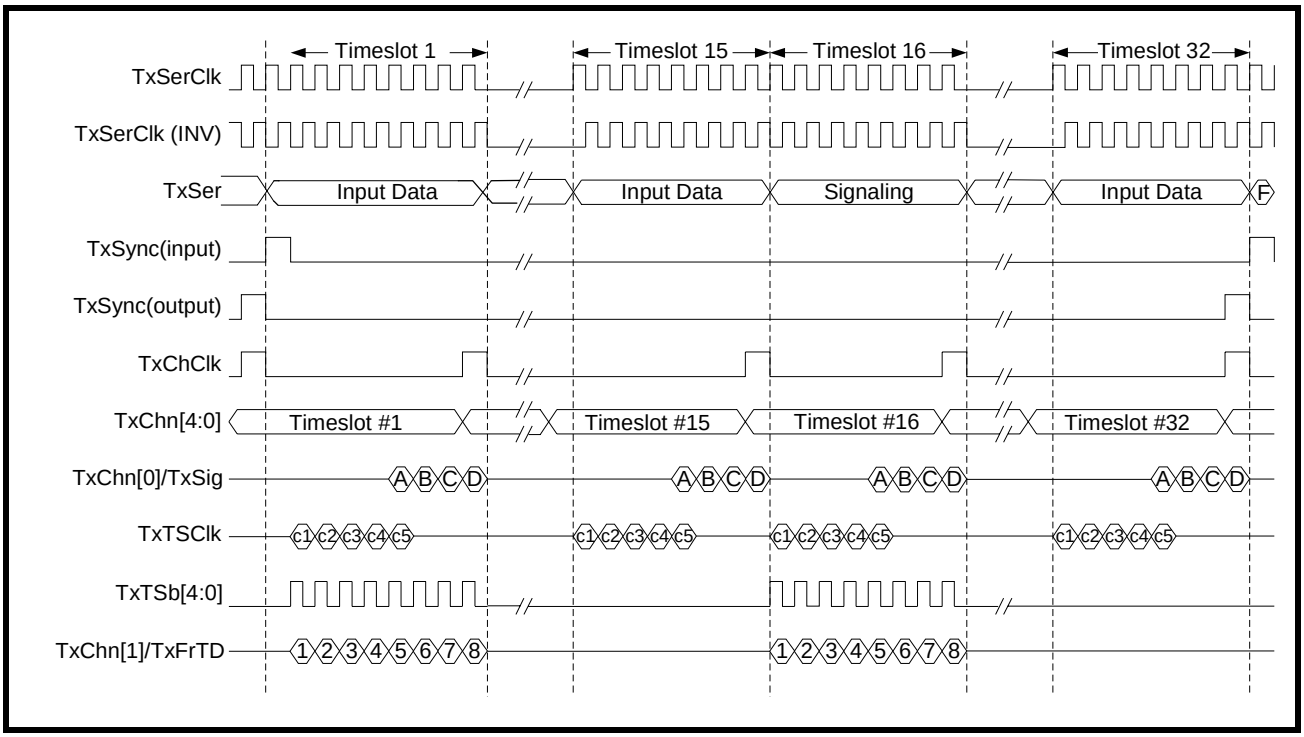
See Figure 22 below for how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment with the Transmit Serial clock being the timing source of transmit section.

FIGURE 22. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT WITH TXSERCLK_N AS TRANSMIT TIMING SOURCE



The following Figure 23 shows waveforms of the signals (TxSerClk_n, TxSer_n, TxSync_n, TxTSClk_n and TxTSb[4:0]_n) that connecting the Transmit Payload Data Input Interface block to the local Terminal Equipment with the Transmit Serial clock being the timing source of transmit section.

FIGURE 23. WAVEFORMS OF THE SIGNALS THAT CONNECT THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WITH THE TRANSMIT SERIAL CLOCK BEING THE TIMING SOURCE OF THE TRANSMIT SECTION



4.1.2.2 Connect the Transmit Payload Data Input Interface block to the Local Terminal Equipment if the Transmit Timing Source = OSCCLK

By setting the Transmit Timing Source [1:0] bits of the Clock Select Register (CSR) to 10, the OSCCLK Driven Divided clock is configured to be the timing source for the Transmit section of the framer. A free-running clock should apply to the OSCCLK input pin with frequencies of 16.384MHz, 32.768MHz and 65.536MHz depending on the setting of OSCCLK Frequency Select [1:0] bits of the Clock Select Register (CSR).

The free-running OSCCLK is divided inside the XRT86L34 and routed to all four framers. This OSCCLK Driven Divided Clock has to be 16.384MHz in frequency. When these bits are set to 00, the framer will internally divide the incoming OSCCLK by one. Therefore, the external oscillator clock applied to the OSCCLK pin should be 16.384MHz. When these bits are set to 01, the framer will internally divide the incoming OSCCLK by two. Therefore, the external oscillator clock applied to the OSCCLK pin should be 32.768MHz. When these bits are set to 10, the framer will internally divide the incoming OSCCLK by four. Therefore, the external oscillator clock applied to the OSCCLK pin should be 65.536MHz.

The following table shows configurations of the OSCCLK Frequency Select [1:0] bits of the Clock Select Register.

CLOCK SELECT REGISTER (CSR) (ADDRESS = 0XN100H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	OSCCLK Frequency Select	R/W	These two READ/WRITE bit-fields permit the user to select internal clock dividing logic of the framer depending on the frequency of incoming oscillator clock (OSCCLK). The frequency of internal clock used by the framer should be 16.384MHz. 00 - The framer will internally divide the incoming OSCCLK by one. Therefore, the external oscillator clock applied to the OSCCLK pin should be 16.384MHz. 01 - The framer will internally divide the incoming OSCCLK by two. Therefore, the external oscillator clock applied to the OSCCLK pin should be 32.768MHz. 10 - The framer will internally divide the incoming OSCCLK by four. Therefore, the external oscillator clock applied to the OSCCLK pin should be 65.536MHz.

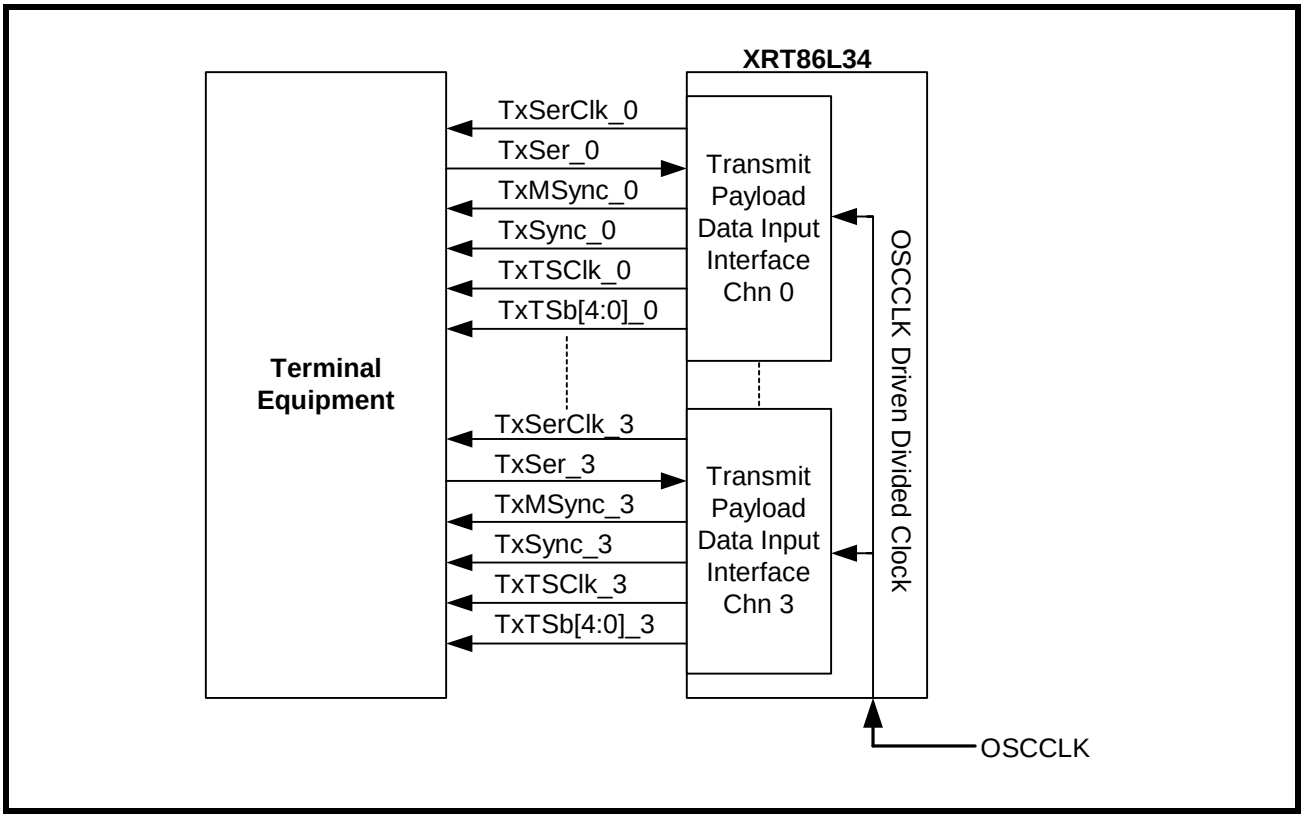
The Transmit Serial clock signal pin (TxSerClk_n) is output from the framer. The framer outputs a 2.048MHz clock through this pin to the local Terminal Equipment. The Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal are also automatically configured to be output signals.

The Transmit Single-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the last bit position of each E1 frame. By triggering on the HIGH pulse on the Transmit Single-frame Synchronization signal, the local Terminal Equipment can identify the end of an E1 frame and should start inserting payload data of the next E1 frame to the framer.

The Transmit Multi-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the last bit position of the last frame of an E1 multi-frame. By triggering on the HIGH pulse on the Transmit Multi-frame Synchronization signal, the local Terminal Equipment can identify the end of an E1 super-frame and should start inserting payload data of the next E1 multi-frame into the framer.

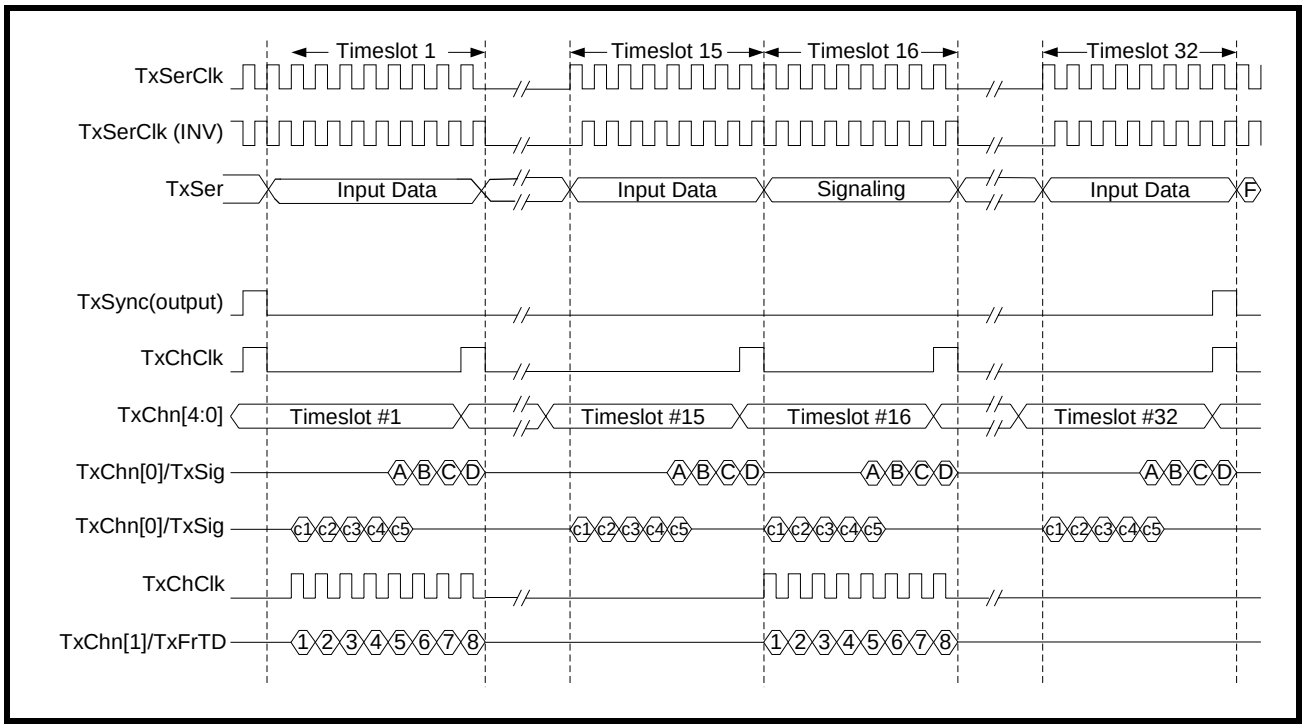
See Figure 24 for how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment with the OSCCLK Driven Divided clock as the timing source of transmit section.

FIGURE 24. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT WITH OSCCLK DRIVEN DIVIDED CLOCK AS TRANSMIT TIMING SOURCE



The following Figure 25 shows waveforms of the signals (TxSerClk_n, TxSer_n, TxSync_n, TxTSClk_n and TxTSb[4:0]_n) that connecting the Transmit Payload Data Input Interface block to the local Terminal Equipment with the OSCCLK Driven Divided clock as the timing source of transmit section.

FIGURE 25. WAVEFORMS OF THE SIGNALS CONNECTING THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WITH THE OSCCLK DRIVEN DIVIDED CLOCK AS THE TIMING SOURCE OF THE TRANSMIT SECTION



4.1.2.3 Connect the Transmit Payload Data Input Interface block to the Local Terminal Equipment for Loop-timing applications

If the Transmit Timing Source [1:0] bits of the Clock Select Register are set to 00 or 11, the Recovered Receive Line Clock is configured to be the timing source for the Transmit section of the framer. This is also known as the Loop-timing mode.

If the Clock Loss Detection Enable bit of the Clock Select Register is set to one, and if the Recovered Receive Line Clock from the LIU is lost, the framer will automatically begin to use the OSCCLK Driven Divided clock as transmit timing source until the LIU is able to regain clock recovery.

The following table shows configuration of the Clock Loss Detection Enable bit of the Clock Select Register (CSR).

CLOCK SELECT REGISTER (CSR) (ADDRESS = 0XN100H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Clock Loss Detection Enable	R/W	This READ/WRITE bit-field permits the user to enable the Clock Loss Detection logic for the framer when the Recovered Receive Line Clock is used as transmit timing source of the framer. 0 - The framer disables the Clock Loss Detection logic. 1 - The framer enables the Clock Loss Detection logic. If the Recovered Receive Line Clock is used as transmit timing source of the framer, and if clock recovered from the LIU is lost, the framer can detect loss of the Recovered Receive Line Clock. Upon detecting of this occurrence, the framer will automatically begin to use the OSCCLK Driven Divided clock as transmit timing source until the LIU is able to regain clock recovery. ***NOTE:*** *This bit-field is ignored if the TxSerClk or the OSCCLK Driven Divided Clock is chosen to be the timing source of Transmit Section of the framer.*

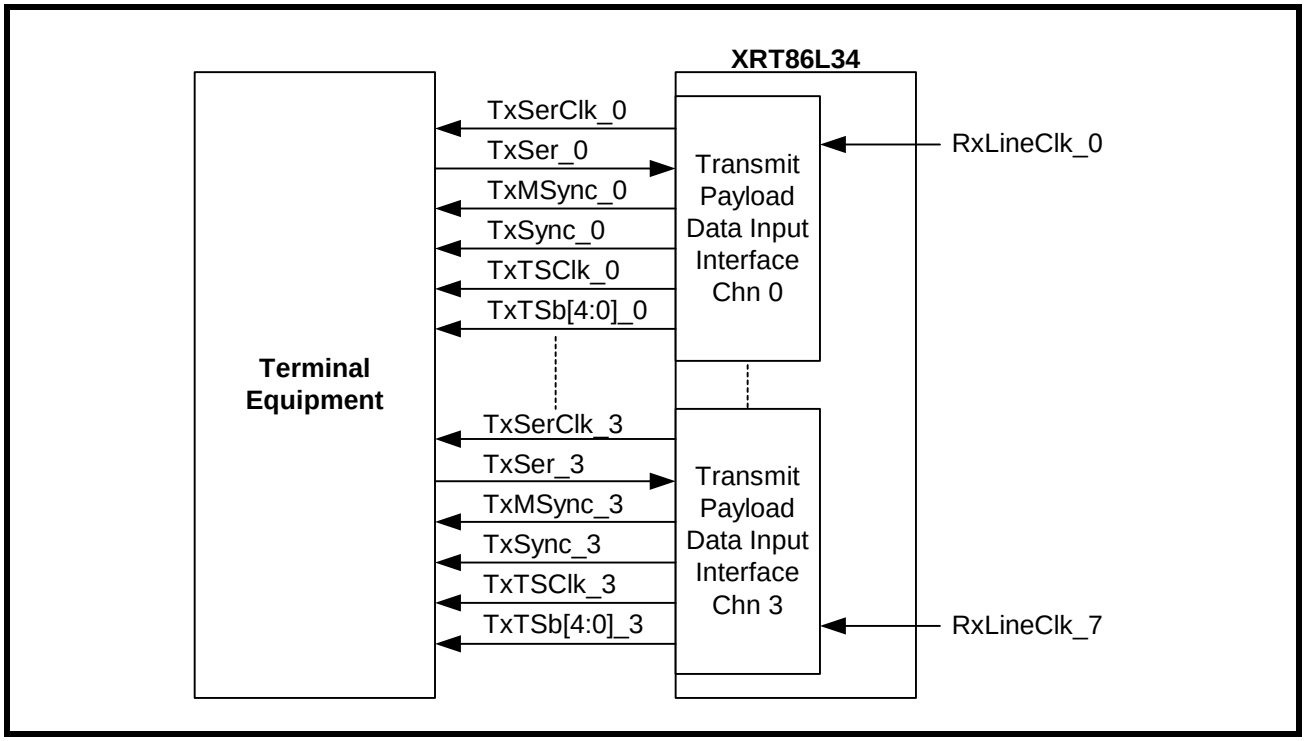
The Transmit Serial Clock signal pin (TxSerClk_n) is output from the framer. The XRT86L34 device routes the Recovered Receive Line Clock internally across the framer and output through the Transmit Serial Clock signal pin to the local Terminal Equipment. The Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal are automatically configured to be output signals.

The Transmit Single-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the last bit position of each E1 frame. By triggering on the HIGH pulse on the Transmit Single-frame Synchronization signal, the local Terminal Equipment can identify the end of an E1 frame and should start inserting payload data of the next E1 frame to the framer.

The Transmit Multi-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the last bit position of the last frame of an E1 multi-frame. By triggering on the HIGH pulse on the Transmit Multi-frame Synchronization signal, the local Terminal Equipment can identify the end of an E1 super-frame and should start inserting payload data of the next E1 multi-frame into the framer.

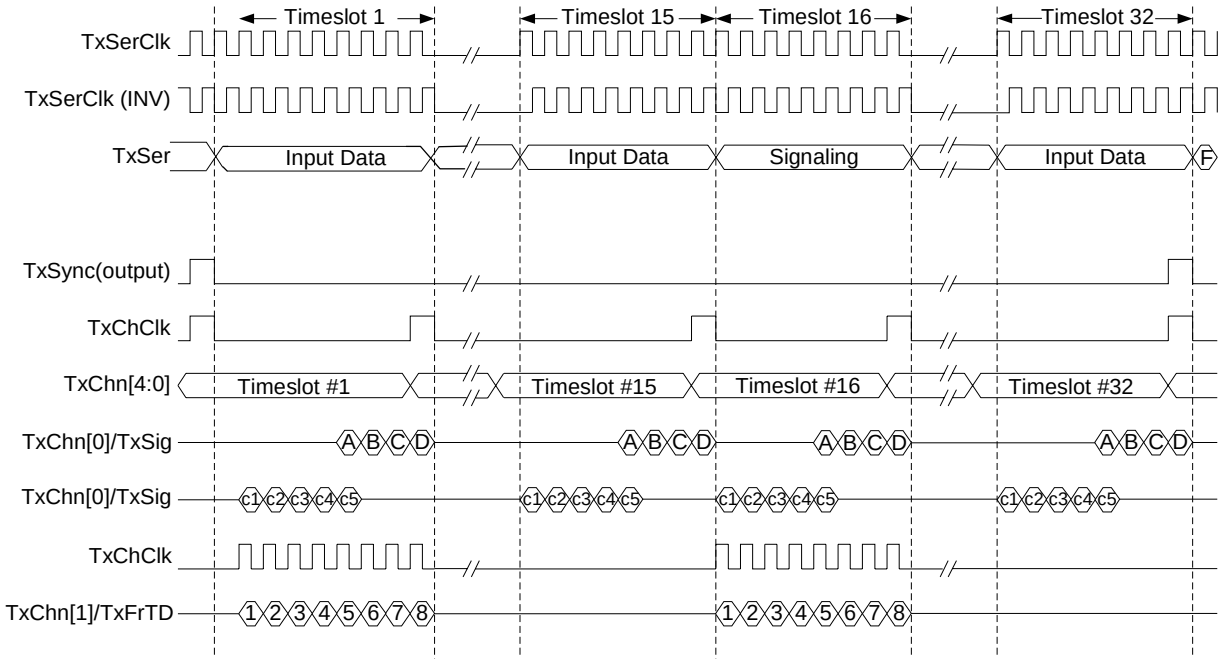
See Figure 26 for how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment with the Recovered Receive Line Clock being the timing source of transmit section.

FIGURE 26. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT WITH RECOVERED RECEIVE LINE CLOCK AS TRANSMIT TIMING SOURCE



The following Figure 27 shows waveforms of the signals (TxSerClk_n, TxSer_n, TxSync_n, TxTSClk_n and TxTSb[4:0]_n) that connecting the Transmit Payload Data Input Interface block to the local Terminal Equipment with the Recovered Receive Line Clock being the timing source of transmit section.

FIGURE 27. WAVERFORMS OF THE SIGNALS CONNECTING THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WITH THE RECOVERED RECEIVE LINE CLOCK BEING THE TIMING SOURCE OF TRANSMIT SECTION



4.2 TRANSMIT HIGH-SPEED BACK-PLANE INTERFACE

The High-speed Back-plane Interface supports payload data to be taken from or presented to the Terminal Equipment at different data rates. In E1 mode, supported High-speed data rates are MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s. The Transmit Multiplex Enable bit and the Transmit Interface Mode Select [1:0] bits of the Transmit Interface Control Register (TICR) determine the Transmit Back-plane Interface data rate.

The following table shows configurations of the Transmit Multiplex Enable bit and the Transmit Interface Mode Select [1:0] bits of the Transmit Interface Control Register (TICR).

TRANSMIT INTERFACE CONTROL REGISTER (TICR) (ADDRESS = 0XN120H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Transmit Multiplex Enable	R/W	0 - The Transmit Back-plane Interface block is configured to non-channel-multiplexed mode 1 - The Transmit Back-plane Interface block is configured to channel-multiplexed mode
1-0	Transmit Interface Mode Select	R/W	When combined with the Transmit Multiplex Enable bit, these bits determine the Transmit Back-plane Interface data rate.

The table below shows the combinations of Transmit Multiplex Enable bit and Transmit Interface Mode Select [1:0] bits and the resulting Transmit Back-plane Interface data rates.

TRANSMIT MULTIPLEX ENABLE BIT	TRANSMIT INTERFACE MODE SELECT BIT 1	TRANSMIT INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE
0	0	0	XRT84V24 Compatible 2.048Mbit/s
0	0	1	MVIP 2.048Mbit/s
0	1	0	4.096Mbit/s
0	1	1	8.192Mbit/s
1	0	0	-
1	0	1	Bit Multiplexed 16.384Mbit/s
1	1	0	HMVIP 16.384Mbit/s
1	1	1	H.100 16.384Mbit/s

When the Transmit Multiplex Enable bit is set to zero, the framer is configured in non-channel-multiplexed mode. The possible data rates are XRT84V24 Compatible 2.048Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s. In non-channel-multiplexed mode, payload data of each channel are taken from the Terminal Equipment separately. Each channel uses its own Transmit Serial Clock, Transmit Serial Data, Transmit Single-frame Synchronization signal and Transmit Multi-frame Synchronization signal as interface between the framer and the Terminal Equipment. Section 1.1.2.1, 1.1.2.2 and 1.1.2.3 provide details on how to connect the Transmit Payload Data Interface block with the Terminal Equipment when the Back-plane interface data rate is 1.544Mbit/s.

When the Back-plane interface data rate is MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s, the Transmit Serial Clock, Transmit Serial Data, Transmit Single-frame Synchronization signal and Transmit Multi-frame Synchronization signal are all configured as inputs. The Transmit Serial Clock is always an input clock with frequency of 2.048 MHz for all data rates. The TxMSync_n signal is configured as the Transmit Input Clock with frequencies of 2.048 MHz, 4.096 MHz and 8.192 MHz respectively. It serves as the primary clock source for the High-speed Back-plane Interface.

The table below summaries the clock frequencies of TxSerClk_n and TxInClk_n inputs when the framer is operating in non-multiplexed High-speed Back-plane mode.

TRANSMIT MULTIPLEX ENABLE BIT = 0

TRANSMIT INTERFACE MODE SELECT BIT 1	TRANSMIT INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE	TXSERCLK	TXMSYNC/TXINCLK
0	0	2.048Mbit/s	2.048 MHz	-
0	1	MVIP 2.048Mbit/s	2.048 MHz	2.048 MHz
1	0	4.096Mbit/s	2.048 MHz	4.096 MHz
1	1	8.192Mbit/s	2.048 MHz	8.192 MHz

When the Transmit Multiplex Enable bit is set to one, the framer is configured in channel-multiplexed mode. The possible data rates are bit-multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s and H.100 16.384Mbit/s. In channel-multiplexed mode, every four channels share the Transmit Serial Data and Transmit Single-frame Synchronization signal of one channel as interface between the framer and the local Terminal Equipment. The TxMSync_n signal of one channel is configured as the Transmit Input Clock with frequencies of 16.384 MHz. It serves as the primary clock source for the High-speed Back-plane Interface.

Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4. The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH at the beginning of the frame with data from Channel 0-3 multiplexed together. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH at the beginning of the frame with data from Channel 4-7 multiplexed together. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse. Additionally, each channel requires the local Terminal Equipment to provide a free-running 2.048 MHz clock into the Transmit Serial Clock input.

The table below summaries the clock frequencies of TxSerClk_n and TxInClk_n inputs when the framer is operating in multiplexed High-speed Back-plane mode.

TRANSMIT MULTIPLEX ENABLE BIT = 1

TRANSMIT INTERFACE MODE SELECT BIT 1	TRANSMIT INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE	TXSERCLK	TXMSYNC/TXCLK
0	0	-	-	-
0	1	Bit-multiplexed 16.384Mbit/s	2.048 MHz	16.384 MHz
1	0	HMVIP 16.384Mbit/s	2.048 MHz	16.384 MHz
1	1	H.100 16.384Mbit/s	2.048 MHz	16.384 MHz

The Transmit Serial Clock is always running at 1.544MHz for all the High-speed Back-plane Interface modes. It is automatically the timing source of the Transmit Section of the framer in High-speed Back-plane Interface mode.

The Transmit Single-frame Synchronization signal should pulse HIGH or LOW for one bit period at the First bit position of each E1 frame. Length of the bit period depends on data rate of the High-speed Back-plane Interface. The Transmit Synchronization Pulse Low bit of the Transmit Interface Control Register (TICR) determines whether the Transmit Single-frame Synchronization signal is HIGH active or LOW active.

The table below shows configurations of the Transmit Synchronization Pulse LOW bit of the Transmit Interface Control Register (TICR).

TRANSMIT INTERFACE CONTROL REGISTER (TICR)(ADDRESS = 0XN120H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Transmit Synchronization Pulse LOW	R/W	0 - The Transmit Single-frame Synchronization signal will pulse HIGH indicating the beginning of an E1 frame when the High-speed Back-plane Interface is running at a mode other than the XRT84V24 Compatible 2.048Mbit/s. 1 - The Transmit Single-frame Synchronization signal will pulse LOW indicating the beginning of an E1 frame when the High-speed Back-plane Interface is running at a mode other than the XRT84V24 Compatible 2.048Mbit/s.

Throughout the discussion of this datasheet, we assume that the Transmit Single-frame Synchronization signal pulses HIGH unless stated otherwise.

The TxMSync_n signal, which is a multiplexed I/O pin, no longer functions as the Transmit Multi-frame Synchronization Signal. Indeed, it becomes the Transmit Input Clock signal (TxInClk) of the High-speed Back-plane Interface of the framer. The local Terminal Equipment should provide a free-running clock with the same frequency as the High-speed Back-plane Interface to this input pin.

The following sections discuss details of how to operate the framer in different Back-plane interface speed mode and how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment.

4.2.0.1 E1 Transmit Input Interface - MVIP 2.048 MHz

When the Transmit Multiplex Enable bit is set to zero and the Transmit Interface Mode Select [1:0] bits are set to 01, the Transmit Back-plane interface of framer is running at a data rate of 2.048Mbit/s.

The interface consists of the following pins:

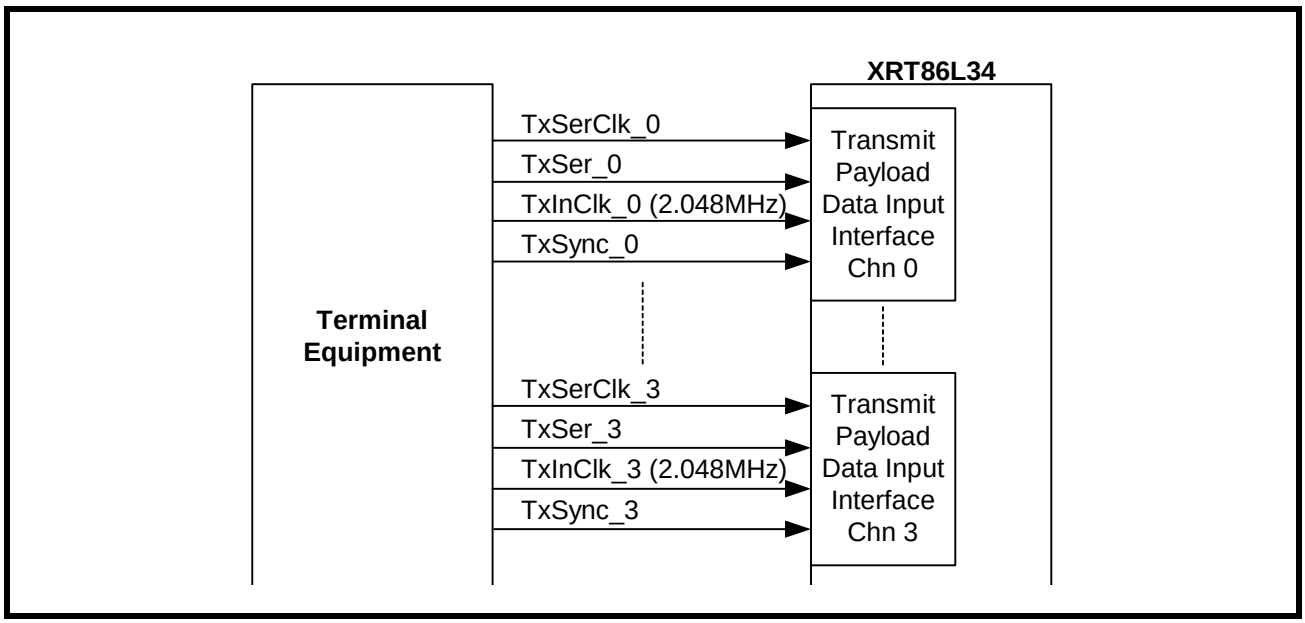
- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane interface is accepting data through TxSer_n at 2.048Mbit/s. The local Terminal Equipment supplies a free-running 2.048MHz clock to he Transmit Input Clock pin of the framer. The local Terminal Equipment also provides synchronized payload data at rising edge of the clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the Transmit Input Clock.

The Transmit Single-frame Synchronization input signal (TxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of an E1 frame. It is responsibility of the local Terminal Equipment to align the Transmit Single-frame Synchronization signal with serial data stream going into the framer.

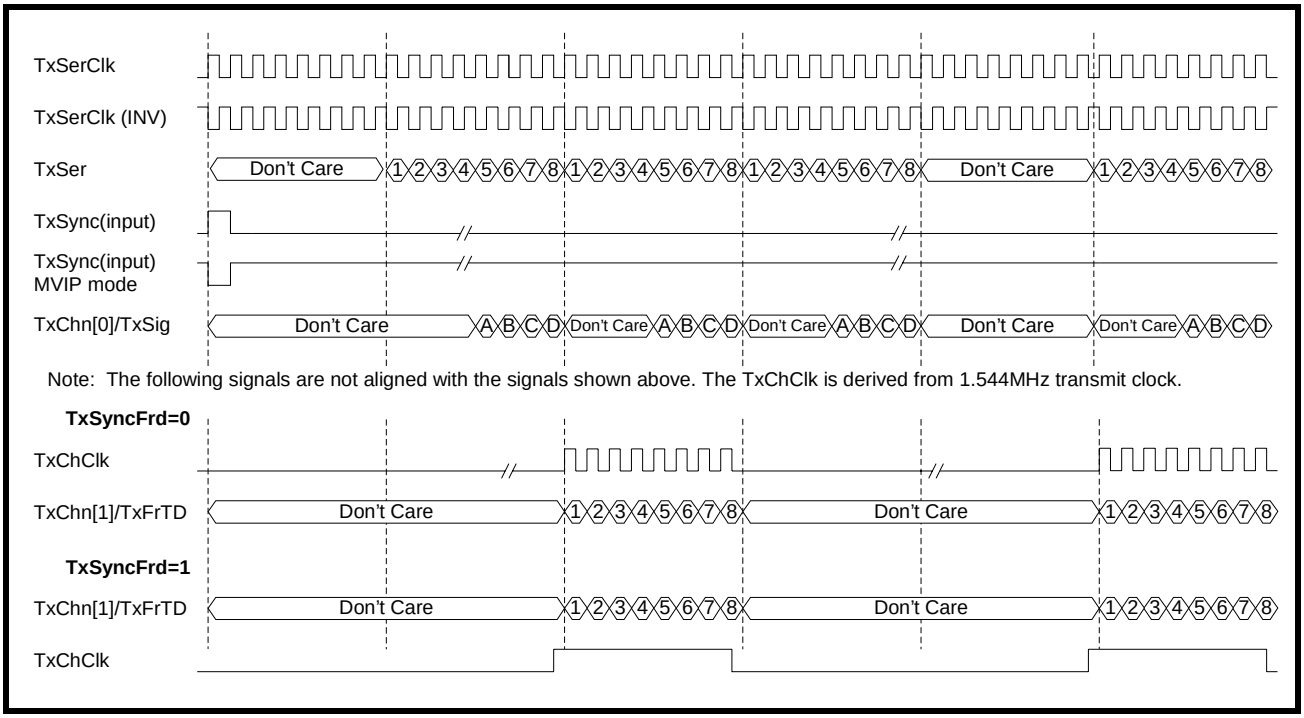
See Figure 28 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in MVIP 2.048Mbit/s mode.

FIGURE 28. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING MVIP 2.048MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at MVIP 2.048Mbit/s mode is shown in Figure 29.

FIGURE 29. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT MVIP 2.048MBIT/S



4.2.0.2 E1 Transmit Input Interface - 4.096 MHz

(This interface mode is the same as running at 2.048 MHz. The only difference is that the Transmit Input Clock runs two times faster at 4.096 MHz)

When the Transmit Multiplex Enable bit is set to zero and the Transmit Interface Mode Select [1:0] bits are set to 10, the Transmit Back-plane interface of framer is running at a clock rate of 4.096MHz.

The interface consists of the following pins:

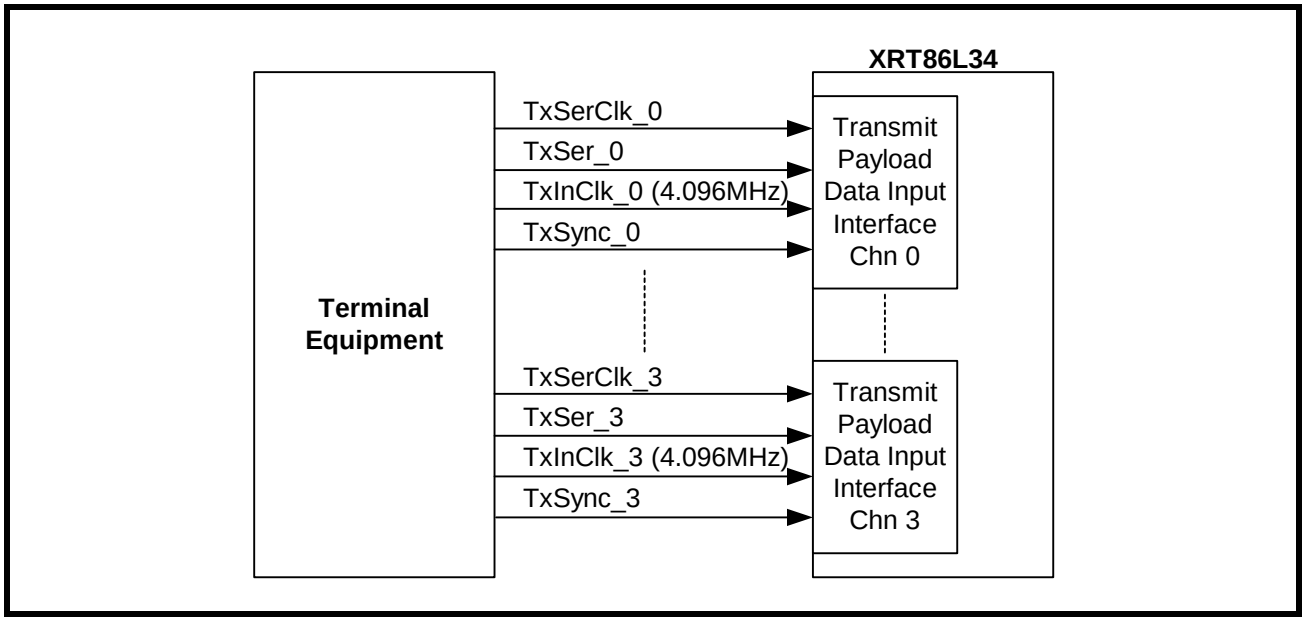
- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane interface is still accepting data through TxSer_n at an E1 equivalent data rate of 2.048Mbit/s. However, the local Terminal Equipment supplies a free-running 4.096MHz clock to the Transmit Input Clock pin of the framer. The local Terminal Equipment provides synchronized payload data at every other rising edge of the Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at every other falling edge of the clock.

Transmit Single-frame Synchronization input signal (TxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of an E1 frame. It is responsibility of the local Terminal Equipment to align the Transmit Single-frame Synchronization signal with serial data stream going into the framer.

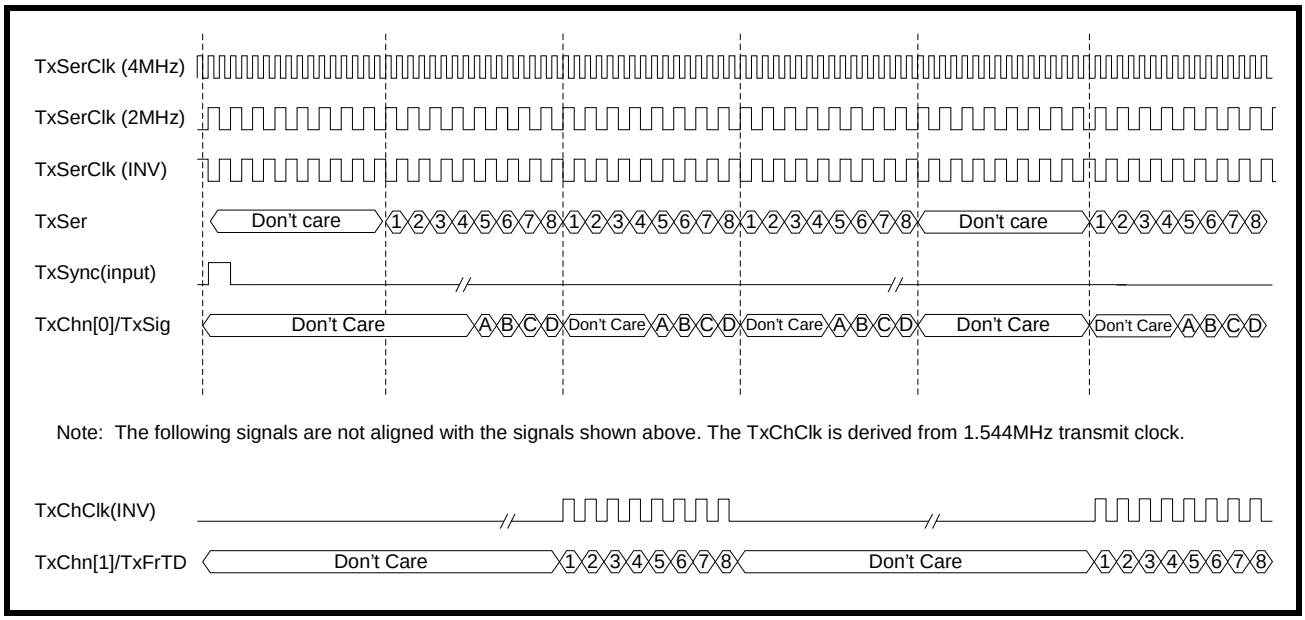
See Figure 30 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in 4.096Mbit/s mode.

FIGURE 30. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING 4.096MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at 4.096Mbit/s mode is shown in Figure 31.

FIGURE 31. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 4.096MBIT/S MODE



4.2.0.3 E1 Transmit Input Interface - 8.192 MHz

(This interface mode is the same as running at 2.048 MHz. The only difference is that the Transmit Input Clock runs four times faster at 8.192MHz)

When the Transmit Multiplex Enable bit is set to zero and the Transmit Interface Mode Select [1:0] bits are set to 11, the Transmit Back-plane interface of framer is running at a clock rate of 8.192MHz.

The interface consists of the following pins:

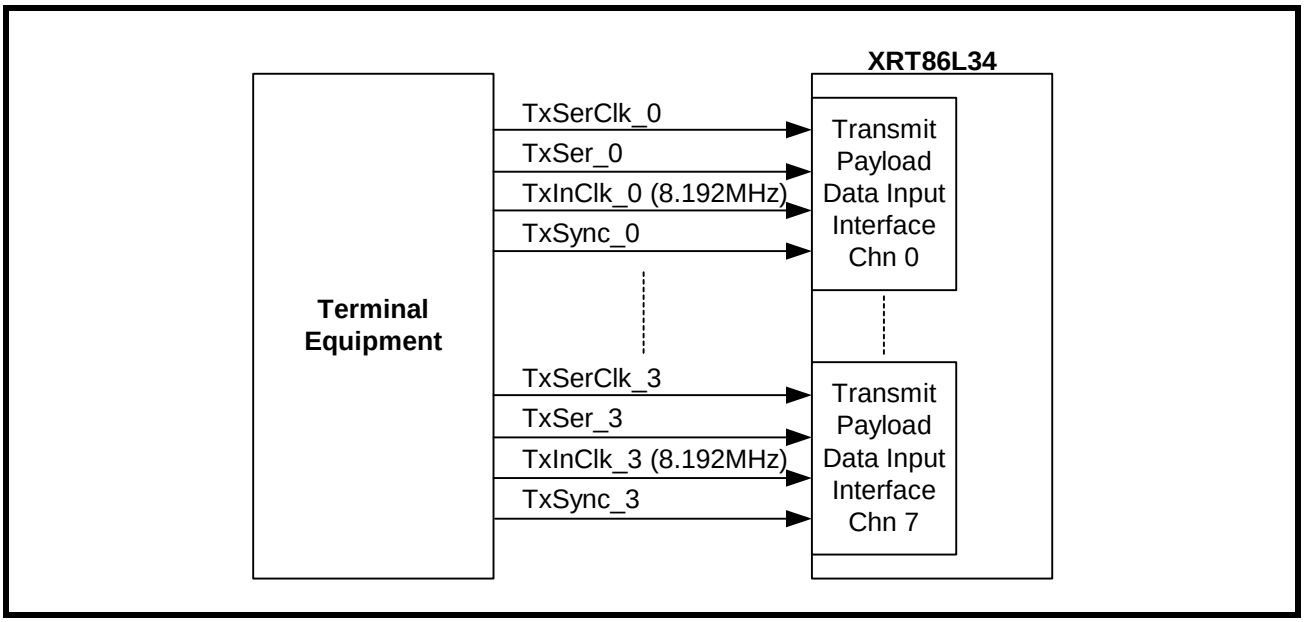
- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane interface is still accepting data through TxSer_n at an E1 equivalent data rate of 2.048Mbit/s. However, the local Terminal Equipment supplies a free-running 8.192MHz clock to the Transmit Input Clock pin of the framer. The local Terminal Equipment provides synchronized payload data at every other four rising edge of the Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at every other four falling edge of the clock.

The Transmit Single-frame Synchronization input signal (TxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of an E1 frame. It is responsibility of the local Terminal Equipment to align the Transmit Single-frame Synchronization signal with serial data stream going into the framer.

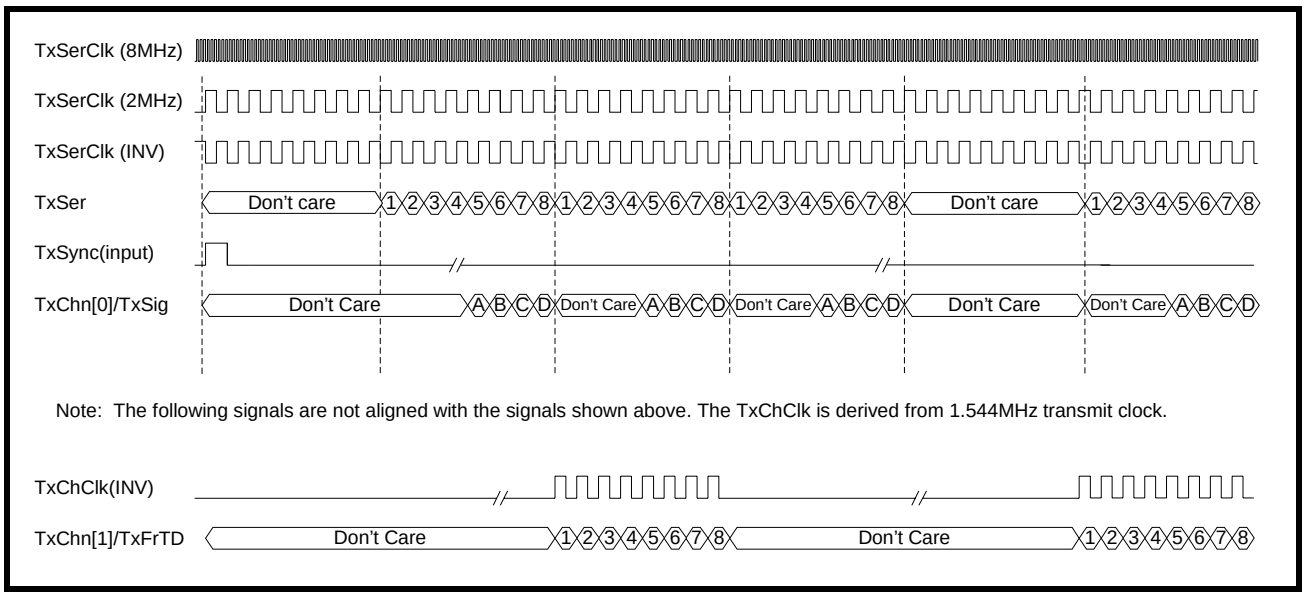
See Figure 32 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in 8.192Mbit/s mode.

FIGURE 32. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING 8.192MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at 8.192Mbit/s mode is shown in Figure 33.

FIGURE 33. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 8.192MBIT/S MODE



4.2.0.4 E1 Transmit Input Interface - Bit-Multiplexed 16.384Mbit/s

When the Transmit Multiplex Enable bit is set to one and the Transmit Interface Mode Select [1:0] bits are set to 01, the Transmit Back-plane interface of framer is running at a clock rate of 16.384MHz.

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane Interface is accepting data through TxSer_0 or TxSer_4 pins at 16.384Mbit/s. The local Terminal Equipment multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz is supplied to the Transmit Input Clock pin of Channel 0 and Channel 4 of the framer. The local Terminal Equipment provides multiplexed payload data at rising edge of this Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the clock.

The local Terminal Equipment maps four 2.048Mbit/s E1 data streams into this 16.384Mbit/s data stream as described below:

1. Payload data of four channels are repeated and grouped together in a bit-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the first payload bit of Timeslot 0 of Channel 1 and 2. The first payload bit of Timeslot 0 of Channel 3 is sent last.

After the first bits of Timeslot 0 of all four channels are sent, it comes the second bit of Timeslot 0 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	1_1	1_1	1_2	1_2	1_3	1_3

SECOND OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
2_0	2_0	2_1	2_1	2_2	2_2	2_3	2_3

X_Y: The Xth payload bit of Channel Y

2. The local Terminal Equipment also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream.

When the Terminal Equipment is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

FIFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	5_1	A_1	5_2	A_2	5_3	A_3

SIXTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
6_0	B_0	6_1	B_1	6_2	B_2	6_3	B_3

SEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
7_0	C_0	7_1	C_1	7_2	C_2	7_3	C_3

EIGHTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
8_0	D_0	8_1	D_1	8_2	D_2	8_3	D_3

X_Y: The Xth payload bit of Channel Y

A_Y: The signaling bit A of Channel Y

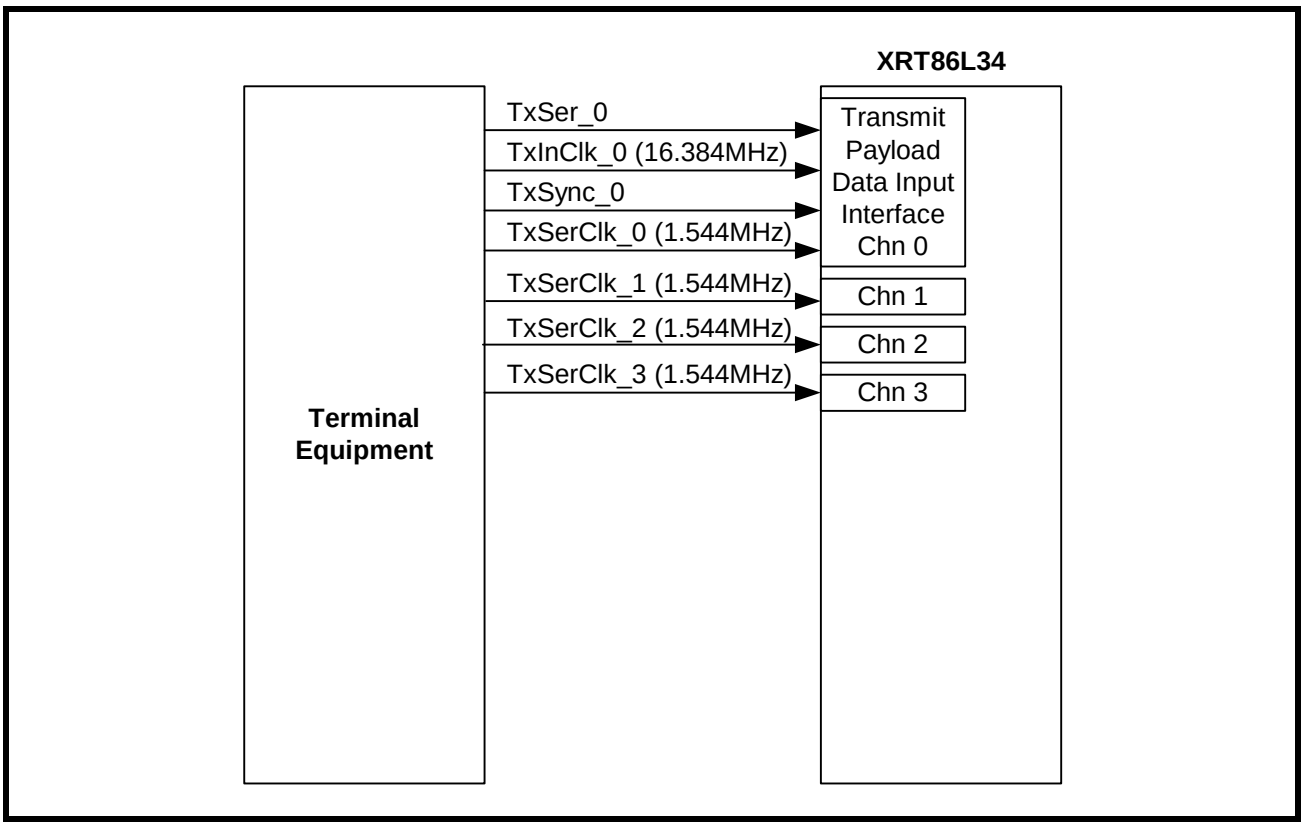
3. After the first octet of all four channels are sent, the local Terminal Equipment start sending the second octets following the same rules of Step 1 and 2.

The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH for one clock cycle at the first bit position of the data stream with data from Channel 0-3 multiplexed together. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH for one clock cycle at the first bit position of the data stream with data from Channel 4-7 multiplexed together. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed E1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT86L34 device and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

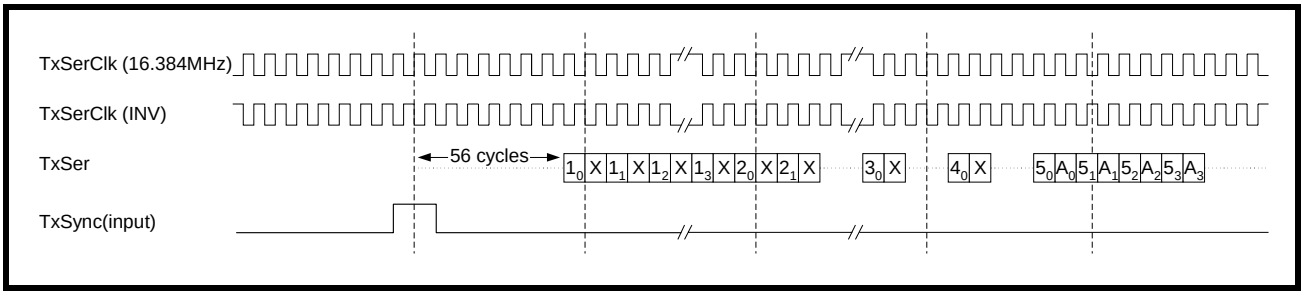
See Figure 34 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in Bit-multiplexed 16.384Mbit/s mode.

FIGURE 34. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 35 below when the framer is running at Bit-Multiplexed 16.384Mbit/s mode.

FIGURE 35. IMING SIGNAL WHEN THE FRAMER IS RUNNING AT BIT-MULTIPLEXED 16.384MBIT/S MODE



4.2.0.5 E1 Transmit Input Interface - HMVIP 16.384Mbit/s

When the Transmit Multiplex Enable bit is set to one and the Transmit Interface Mode Select [1:0] bits are set to 10, the Transmit Back-plane interface of framer is running at a clock rate of 16.384MHz.

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)

- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane Interface is accepting data through TxSer_0 or TxSer_4 pins at 16.384Mbit/s. The local Terminal Equipment multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz is supplied to the Transmit Input Clock pin of Channel 0 and Channel 4 of the framer. The local Terminal Equipment provides multiplexed payload data at rising edge of this Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the clock.

The local Terminal Equipment maps four 2.048Mbit/s E1 data streams into this 16.384Mbit/s data stream as described below:

1. Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Terminal Equipment will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent the last.

   After the payload bits of Timeslot 0 of all four channels are sent, it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

THIRD OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

FIFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

SEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

X_Y: The Xth payload bit of Channel Y

2. The local Terminal Equipment also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream.

When the Terminal Equipment is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

SECOND OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	6_0	B_0	7_0	C_0	8_0	D_0

FOURTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_1	A_1	6_1	B_1	7_1	C_1	8_1	D_1

SIXTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_2	A_2	6_2	B_2	7_2	C_2	8_2	D_2

EIGHTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_3	A_3	6_3	B_3	7_3	C_3	8_3	D_3

X_Y: The Xth payload bit of Channel Y

A_Y: The signaling bit A of Channel Y

3. After the first octet of all four channels are sent, the local Terminal Equipment start sending the second octets following the same rules of Step 1 and 2.

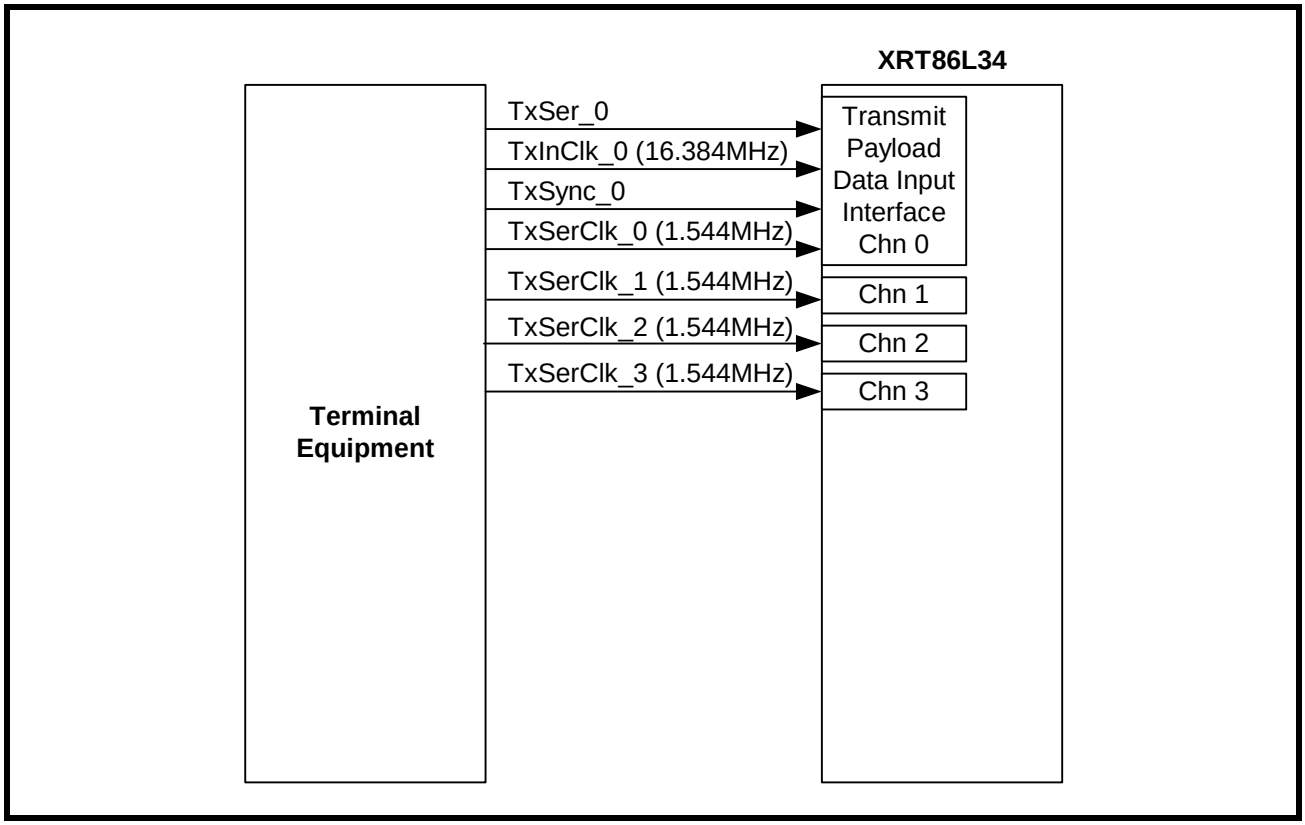
The Transmit Single-frame Synchronization signal should pulse HIGH for four clock cycles (the last two bit positions of the previous multiplexed frame and the first two bits of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH to identify the start of multiplexed data stream of Channel 4-7. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed E1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT86L34 device and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-run-

ning 2.048MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

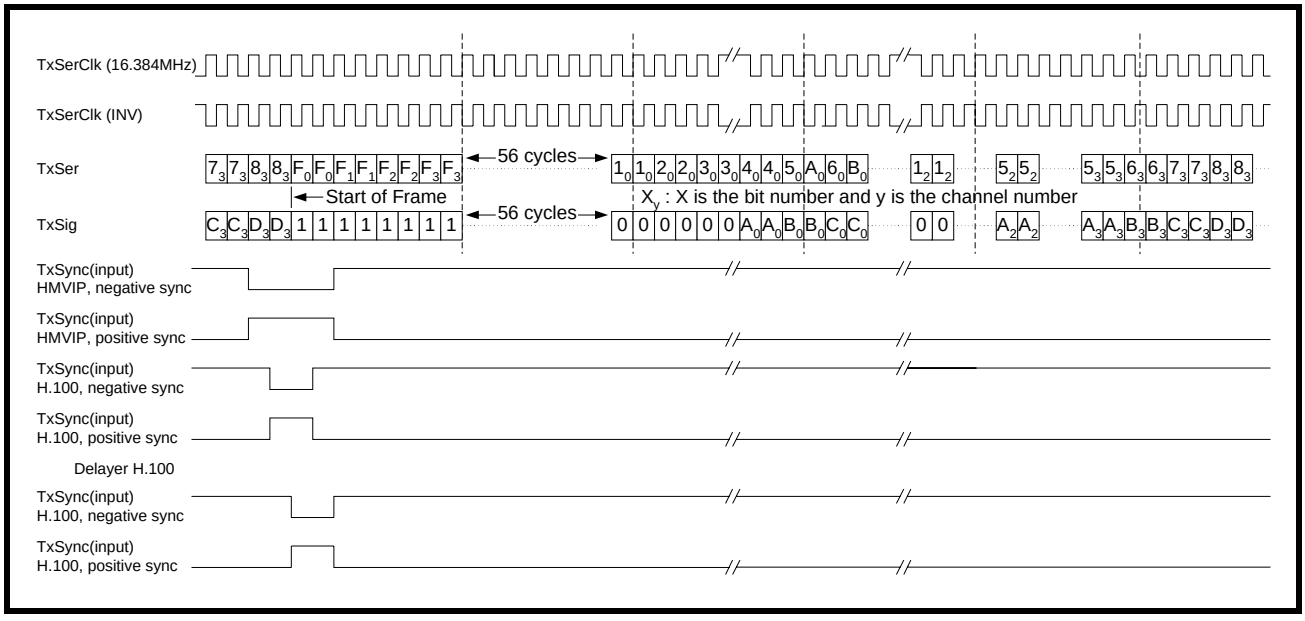
See Figure 36 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in HMVIP 16.384Mbit/s mode.

FIGURE 36. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 37 below when the framer is running at HMVIP 16.384Mbit/s mode.

FIGURE 37. TIMING SIGNAL WHEN THE FRAMER IS RUNNING AT HMVIP 16.384MBIT/S MODE



4.2.0.6 E1 Transmit Input Interface - H.100 16.384Mbit/s

When the Transmit Multiplex Enable bit is set to one and the Transmit Interface Mode Select [1:0] bits are set to 11, the Transmit Back-plane interface of framer is running at H.100 16.384Mbit/s mode.

(The HMVIP mode and the H.100 mode are essential the same except for the HIGH pulse position of the Transmit Single-frame Synchronization Signal)

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane Interface is accepting data through TxSer_0 or TxSer_4 pins at 16.384Mbit/s. The local Terminal Equipment multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz is supplied to the Transmit Input Clock pin of Channel 0 and Channel 4 of the framer. The local Terminal Equipment provides multiplexed payload data at rising edge of this Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the clock.

The local Terminal Equipment maps four 2.048Mbit/s E1 data streams into this 16.384Mbit/s data stream as described below:

1. Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Terminal Equipment will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent the last.

   After the payload bits of Timeslot 0 of all four channels are sent, it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

THIRD OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

FIFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

SEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

X_Y: The Xth payload bit of Channel Y

2. The local Terminal Equipment also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream.

When the Terminal Equipment is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

SECOND OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	6_0	B_0	7_0	C_0	8_0	D_0

FOURTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_1	A_1	6_1	B_1	7_1	C_1	8_1	D_1

SIXTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_2	A_2	6_2	B_2	7_2	C_2	8_2	D_2

EIGHTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_3	A_3	6_3	B_3	7_3	C_3	8_3	D_3

X_Y: The Xth payload bit of Channel Y

A_Y: The signaling bit A of Channel Y

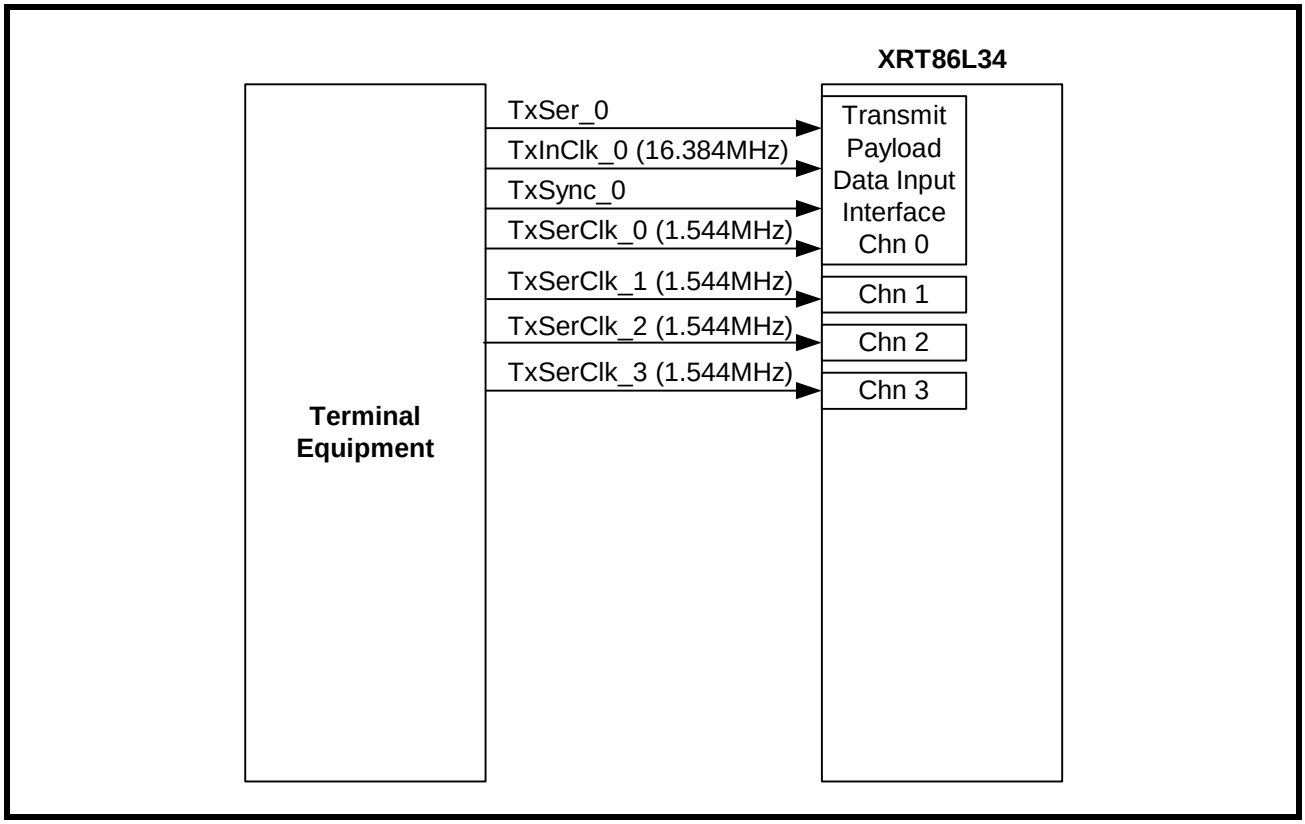
3. After the first octet of all four channels are sent, the local Terminal Equipment start sending the second octets following the same rules of Step 1 and 2.

The Transmit Single-frame Synchronization signal should pulse HIGH for two clock cycles (the last bit position of the previous multiplexed frame and the first bit position of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH to identify the start of multiplexed data stream of Channel 4-7. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed E1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT86L34 device and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-running 2.048MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

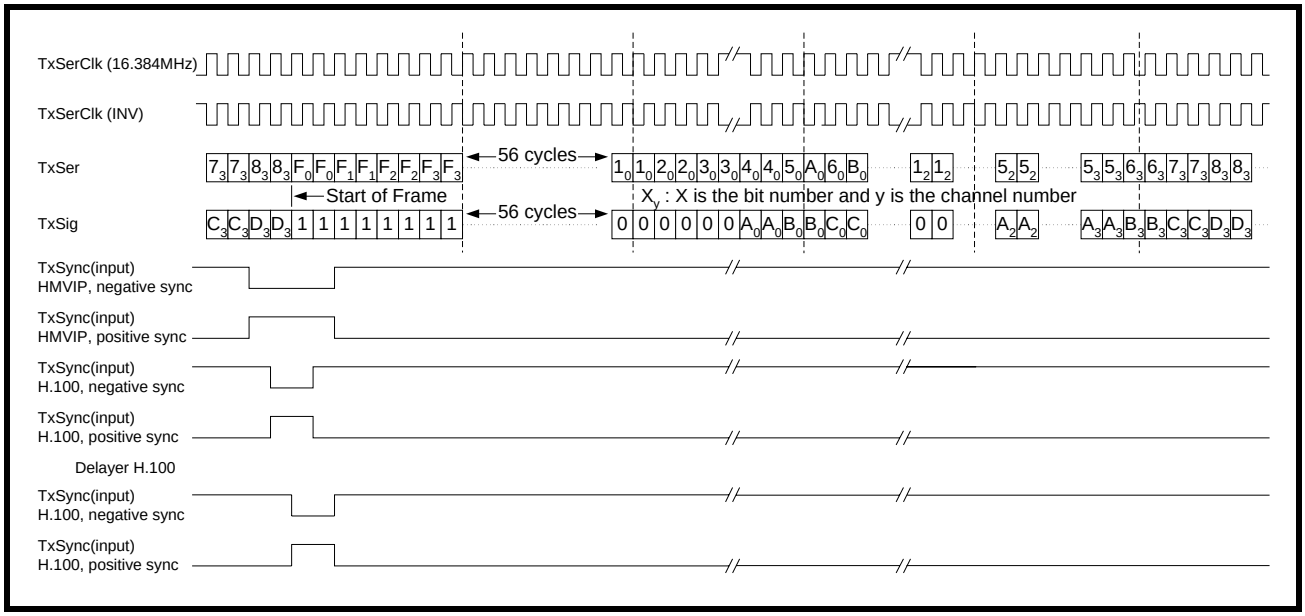
See Figure 38 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in HMVIP 16.384Mbit/s mode.

FIGURE 38. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 39 below when the framer is running at H.100 16.384Mbit/s mode.

FIGURE 39. TIMING SIGNAL WHEN THE FRAMER IS RUNNING AT H.100 16.384MBIT/S MODE



4.3 E1 TRANSMIT FRAMER BLOCK

4.3.1 How to Configure XRT86L34 to Operate in E1 Mode

The XRT86L34 Octal T1/E1/J1 Framer supports DS1, J1 or E1 framing modes. Since J1 standard is very similar to DS1 standard with a few minor changes, the J1 framing mode is included as a sub-set of the DS1 framing mode. All four framers within the XRT86L34 silicon can be individually configured to support DS1, J1 or E1 framing modes.

NOTE: *If transmitting section of one framer is configured to support either one of the framing modes, the receiving section is automatically configured to support the same framing modes.*

The T1/E1 Select bit of the Clock Select Register (CSR) controls which framing mode, that is, T1/J1 or E1, supported by the framer. The table below illustrates configurations of the T1/E1 Select bit of the Clock Select Register (CSR).

CLOCK SELECT REGISTER (CSR) (ADDRESS = 0XN100H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	T1/E1 Select	R/W	0 - The XRT86L34 framer is running in E1 mode. 1 - The XRT86L34 framer is running in T1 mode.

The purpose of the E1 Transmit Framer block is to embed and encode user payload data into frames and to route this E1 frame data to the Transmit E1 LIU Interface block. Please note that the XRT86L34 has four (4) individual E1 Transmit Framer blocks. Hence, the following description applies to all four of these individual Transmit E1 Framer blocks.

The purpose of the E1 Transmit Framer block is:

- To encode user data, inputted from the Terminal Equipment into a standard framing format.
- To provide individual data control and signaling conditioning of each DS0 channel.
- To support the transmission of HDLC messages, from the local transmitting terminal, to the remote receiving terminal.
- To transmit indications that the local receive framer has received error frames from the remote terminal.
- To transmit alarm condition indicators to the remote terminal.

The following sections discuss the functionalities of E1 Transmit Framer block in detail. We will also describe how to configure the XRT86L34 to transmit E1 frames according to system requirement of users.

4.3.2 How to Configure the Framer to Transmit and Receive Data in E1 Framing Format

The XRT86L34 Octal T1/E1/J1 Framer is designed to meet the requirement of ITU-T Recommendation G.704. The E1 framer supports the following:

- Frame Alignment Signal (FAS)
- CRC-4 Multi-frame

The ITU-T Recommendation G.704 also specifies two forms of signaling that can be supported by the E1 Transport medium:

- Channel Associated Signaling (CAS)
- Common Channel Signaling (CCS)

The XRT86L34 framer supports both CAS, CCS signaling format together with Clear Channel without signaling.

4.3.3 How to configure the framer to choose FAS searching algorithm

The XRT86L34 framer can use two algorithms to search for FAS pattern and thus declare FAS alignment synchronization. The FAS Selection bit of the Framing Select Register (FSR) allows the user to choose which one of the two algorithms for searching FAS frame alignment.

The table below shows configurations of the FAS Selection bit of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (ADDRESS = 0XN107H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	FAS Selection bit	R/W	This Read/Write bit field allows the user to determine which algorithm is used for searching FAS frame alignment pattern. When an FAS alignment pattern is found and locked, the XRT86L34 will generate Receive Synchronization (RxSync_n) pulse. 0 - Algorithm 1 is selected for searching FAS frame alignment pattern. 1 - Algorithm 2 is selected for searching FAS frame alignment pattern.

4.3.4 How to configure the framer to enable CRC-4 Multi-frame alignment and select the locking criteria

The CRC-4 Selection [1:0] bits of the Framing Select Register (FSR) enable the framer to search for CRC-4 Multi-frame alignment and select the criteria for locking the CRC-4 Multi-frame alignment.

The table below shows configurations of the CRC-4 Selection [1:0] bit of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (ADDRESS = 0XN107H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	CRC-4 Selection bit	R/W	Theses Read/Write bit fields allow the user to enable searching of CRC-4 Multi-frame alignment and determine what criteria are used for locking the CRC-4 Multi-frame alignment pattern. 00 - Searching of CRC-4 Multi-frame alignment is disabled. The XRT86L34 framer will not search for CRC-4 Multi-frame alignment and thus will not declare CRC-4 Multi-frame synchronization. No Receive CRC-4 Multi-frame Synchronization (RxCRCMsync_n) pulse will be generated by the framer. 01 - Searching of CRC-4 Multi-frame alignment is enabled. The XRT86L34 will search for and declare CRC-4 Multi-frame synchronization if:At least one valid CRC-4 Multi-frame alignment signal is observed within 8 ms. 10 - Searching of CRC-4 Multi-frame alignment is enabled. The XRT86L34 will search for and declare CRC-4 Multi-frame synchronization if:At least two valid CRC-4 Multi-frame alignment signals are observed within 8 ms. The time separating two CRC-4 Multi-frame alignment signals is multiple of 2 ms. 11 - Searching of CRC-4 Multi-frame alignment is enabled. The XRT86L34 will search for and declare CRC-4 Multi-frame synchronization if:At least three valid CRC-4 Multi-frame alignment signals are observed within 8 ms. The time separating two CRC-4 Multi-frame alignment signals is multiple of 2 ms.

4.3.5 How to configure the framer to enable CAS Multi-frame alignment

The XRT86L34 framer can use two algorithms to search for CAS Multi-frame alignment pattern. Upon detecting of CAS Multi-frame alignment pattern, the framer will declare CAS Multi-frame alignment synchronization and generate the Receive CAS Multi-frame synchronization pulse (RxCASMsync_n). The CAS Selection [1:0] bits of the Framing Select Register (FSR) enable the framer to search for CAS Multi-frame alignment.

The table below shows configurations of the CAS Selection [1:0] bit of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (ADDRESS = 0XN107H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	CAS Selection bit	R/W	These Read/Write bit fields allow the user to enable searching of CAS Multi-frame alignment and determine which algorithm of the two are used for locking the CAS Multi-frame alignment pattern. 00 - Searching of CAS Multi-frame alignment is disabled. The XRT86L34 framer will not search for CAS Multi-frame alignment and thus will not declare CAS Multi-frame synchronization. No Receive CAS Multi-frame Synchronization (RxCRCMsync_n) pulse will be generated by the framer. 01 - Searching of CAS Multi-frame alignment is enabled. The XRT86L34 will search for and declare CAS Multi-frame synchronization using Algorithm 1. 10 - Searching of CAS Multi-frame alignment is enabled. The XRT86L34 will search for and declare CAS Multi-frame synchronization using Algorithm 2 (G.732). 11 - Searching of CAS Multi-frame alignment is disabled. The XRT86L34 framer will not search for CAS Multi-frame alignment and thus will not declare CAS Multi-frame synchronization. No Receive CAS Multi-frame Synchronization (RxCRCMsync_n) pulse will be generated by the framer.

4.3.6 How to configure the framer to input the framing alignment bits from different sources

In E1 mode, the Frame Alignment Signal (FAS) pattern of "0011011" contained in bit 2 to 8 of every other frame (called FAS frame) are used to identify the frame boundaries. In addition, bit 2 of the non-FAS frames is fixed to "1" to prevent simulation of the FAS frames.

In the non-FAS frames, bit 1 is used to transmit the 6-bit CRC-4 multi-frame alignment signal of "001011" and two E bits. The 6-bit CRC-4 multi-frame alignment signal is used to identify the CRC-4 multi-frame boundaries.

The A bit at bit 3 of non-FAS frame is used as remote yellow alarm indication. When the A bit is "0", it denotes undistributed operation of the framer. When the A bit is "1", it denotes yellow alarm condition.

The framing alignment bits include the FAS pattern, the CRC-4 multi-frame alignment bits and the A bit. Under default condition, the XRT86L34 can generate these framing alignment bits internally.

At the same time, the users can generate the framing alignment bits externally and insert them into the framer through the Transmit Serial Data Input Interface block via the TxSer_n pin. It is the user's responsibility to maintain the accuracy and integrity of the framing alignment bits. The user also has to make sure that the framing alignment bits are inserted into the framer at right position and right timing. However, this option is only available when the XRT86L34 is configured to run at a normal back-plane rate of 2.048Mbit/s in E1 mode.

The Framing Bit Source Select bit of the Synchronization MUX Register (SMR) controls source of the framing alignment bit. The table below shows configurations of the Framing Bit Source Select bit of the Synchronization MUX Register (SMR).

SYNCHRONIZATION MUX REGISTER (SMR) (ADDRESS = 0XN109H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Framing Bit Source	R/W	This READ/WRITE bit-field permits the user to determine where the framing alignment bits should be inserted. 0 - The framing alignment bits are generated and inserted by the framer internally. 1 - If the framer is operating in normal 2.048Mbit/s mode, the framing alignment bits are passed through from the Transmit Serial Data Input Interface block via the TxSer_n pin.

4.3.7 How to configure the framer to input CRC-4 bits from different sources

Each E1 CRC-4 multi-frame is divided into two sub-multi-frames. Each sub-multi-frame consists of 8 E1 frames. If the framer is configured to operate in CRC-4 multi-frame format, bit 1 of the FAS frames are used as Cyclic Redundancy Check (CRC-4) code of the last CRC-4 sub- multi-frame. The CRC-4 bits are an indicator of the link quality and could be monitored by the user to establish error performance report.

The XRT86L34 can generate the CRC-4 bits internally by calculating the CRC check-sum of all the payload bits in each E1 sub-multi-frame.

At the same time, the users can generate the CRC-4 bits externally and insert them into the framer through the Transmit Serial Data Input Interface block via the TxSer_n pin. It is the user's responsibility to correctly compute the CRC-4 bits according to E1 algorithm. Also, the user has to make sure that the CRC-4 bits are inserted into the framer at right position and right timing. However, this option is only available when the XRT86L34 is configured to run at a normal back-plane rate of 2.048Mbit/s.

The CRC-4 Source Select bit of the Synchronization MUX Register (SMR) controls from where to input CRC-4 bits into the framer. The table below shows configurations of the CRC-4 Source Select bit of the Synchronization MUX Register (SMR).

SYNCHRONIZATION MUX REGISTER (SMR) (ADDRESS = 0XN109H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	CRC-4 Source Select	R/W	This READ/WRITE bit-field permits the user to determine where the CRC-4 bits should be inserted. 0 - The CRC-4 bits are generated and inserted by the framer internally. 1 - If the framer is operating in normal 2.048Mbit/s mode, the CRC-4 bits are generated by external equipment and passed through from the Transmit Serial Data Input Interface block via the TxSer_n pin.

4.3.8 How to configure the framer to input E bits from different sources

Each E1 CRC-4 multi-frame is divided into two sub-multi-frames. Each sub-multi-frame consists of 8 E1 frames, 4 of them are FAS frames and the other 4 are non-FAS frames. Of the second CRC-4 sub-multi-frame, bit 1 of the last 2 non-FAS frames is called E bit.

The E bits are used to indicate that the previous received sub-multi-frame is error-ed. When a sub-multi-frame is received, the framer calculated the CRC-4 bits of the received sub-multi-frame. The frame then compares the calculated CRC-4 bits with the received CRC-4 bits. If they are the same, the framer will set E bit to "1" and transmit it to the remote terminal. If the calculated CRC-4 bits and the receive CRC-4 bits are different, the framer will set E bit to "0" and transmit it out. The first E bit indicates error of the first CRC-4 sub-multi-frame while the second E bit indicates error of the second CRC-4 sub-multi-frame.

The delay between the detection of an error-ed CRC-4 sub-multi-frame and the setting of the corresponding E bit that represents the error state should not be more than one second. If the E bits are not used, they should be set to "1".

NOTE: *The E bits will always be taken into account even if the sub-multi-frame which contains them is error-ed.*

Under default condition, the XRT86L34 generate the E bits internally by calculating the CRC check-sum of all the payload bits in each received E1 sub-multi-frame and compare them against the received CRC-4 bits.

At the same time, the users can force the E bits to either "0" or "1". Source of the E bits can also be the internal HDLC controller such that the E bits can be used to transmit data link message.

The E bit Source Select bit of the Synchronization MUX Register (SMR) controls from where to input E bits into the framer. The table below shows configurations of the E bit Source Select bit of the Synchronization MUX Register (SMR).

SYNCHRONIZATION MUX REGISTER (SMR) (ADDRESS = 0XN109H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-6	E bit Source Select	R/W	These READ/WRITE bit-fields permits the user to determine where the E bits should be inserted and what the E bits should be. 00 - The E bits are generated and inserted by the framer internally. 01 - The E bits are forced to be "0" and are inserted by the framer internally. 10 - The E bits are forced to be "1" and are inserted by the framer internally. 11 - Source of the E bits is HDLC controller of the framer. The E bits are used to carry data link messages.

4.3.9 How to Configure the Framer to Apply Data and Signaling Conditioning to E1 Payload Data on a Per-Channel Basis

The XRT86L34 T1/J1/E1 Octal Framer provides individual control of each of the thirty two DS0 channels. The user can apply data and signaling conditioning to raw E1 payload data coming from the Terminal Equipment on a per-channel basis.

The XRT86L34 framer can apply the following changes to raw E1 PCM data coming from the Terminal Equipment on a per-channel basis:

- All 8 bits of the input PCM data are inverted
- The even bits of the input PCM data are inverted
- The odd bits of the input PCM data are inverted
- The MSB of the input PCM data is inverted
- All input PCM data except the MSB are inverted

Configuration of the XRT86L34 framer to apply the above-mentioned changes to raw E1 PCM data are controlled by the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of each DS0 channel.

The XRT86L34 framer can also replace the incoming raw E1 PCM data from the Terminal Equipment with predefined or user-defined codes. The XRT86L34 supports the following conditioning substitutions:

- BUSY code - an octet with hexadecimal value of 0x7F
- BUSY_TS code - an octet of pattern "111xxxxx" where "xxxxx" represents the timeslot number
- VACANT code - an octet with hexadecimal value of 0xFF
- A-law Digital Milliwatt code
- u-law Digital Milliwatt code
- IDLE code - an octet defined by the value stored in the User IDLE Code Register (UCR)
- MOOF code - MUX-Out-Of-Frame code with hexadecimal value of 0x1A
- PRBS code - an octet generated by the Pseudo-Random Bit Sequence (PRBS) Generator block of the framer

Once again, configuration of the XRT86L34 framer to replace raw E1 PCM data with the above-mentioned coding schemes are controlled by the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of each DS0 channel.

Finally, the XRT86L34 framer can configure any one or ones of the thirty two DS0 channels to be D or E channels. D channel is used primarily for data link applications. E channel is used primarily for signaling for circuit switching with multiple access configurations.

The Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of each channel determine whether that particular channel is configured as D or E channel.

The table below illustrates configurations of the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR).

TRANSMIT CHANNEL CONTROL REGISTER (TCCR) (ADDRESS = 0XN300H - 0XN31FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Transmit Conditioning Select	R/W	0000 - The input E1 PCM data of this DS0 channel is unchanged. 0001 - All 8 bits of the input E1 PCM data of this DS0 channel are inverted. 0010 - The even bits of the input E1 PCM data of this DS0 channel are inverted. 0011 - The odd bits of the input E1 PCM data of this DS0 channel are inverted. 0100 - The input E1 PCM data of this DS0 channel are replaced by the octet stored in User IDLE Code Register (UCR). 0101 - The input E1 PCM data of this DS0 channel are replaced by BUSY code (0x7F). 0110 - The input E1 PCM data of this DS0 channel are replaced by VACANT code (0xFF). 0111 - The input E1 PCM data of this DS0 channel are replaced by BUSY_TS code (111xxxxx). 1000 - The input E1 PCM data of this DS0 channel are replaced by MUX-Out-Of-Frame (MOOF) code with value 0x1A. 1001 - The input E1 PCM data of this DS0 channel are replaced by the A-law digital milliwatt pattern. 1010 - The input E1 PCM data of this DS0 channel are replaced by the u-law digital milliwatt pattern. 1011 - The MSB bit of the input E1 PCM data of this DS0 channel is inverted. 1100 - All bits of the input E1 PCM data of this DS0 channel except MSB bit are inverted. 1101 - The input E1 PCM data of this DS0 channel are replaced by PRBS pattern created by the internal PRBS Generator of XRT86L34 framer. 1110 - The input E1 PCM data of this DS0 channel is unchanged. 1111 - This channel is configured as D or E timeslot.

When the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of a particular DS0 channel are set to 0100, input E1 PCM data of this DS0 channel are replaced by the octet stored in User IDLE Code Register (UCR). The table below shows contents of the User IDLE Code Register.

USER IDLE CODE REGISTER (UCR) (ADDRESS = 0XN320H - 0XN33FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	User IDLE Code	R/W	These READ/WRITE bit-fields permits the user store any value of IDLE code into the framer. When the Transmit Data Conditioning Select [3:0] bits of TCCR register of a particular DS0 channel are set to 0100, the input E1 PCM data are replaced by contents of this register and sent to the Transmit LIU Interface.

4.3.10 How to Configure the XRT86L34 Framer to Transmit Signaling Information

Each 256-bit E1 frame is divided into 32 octets or time slots numbered 0 to 31. Each time slot is a 64kbits/s channel carrying voice or data information. The time slot 0 is used for frame and multi-frame synchronization, CRC-4 error detection, yellow alarm transmission and data link transmission. The time slot 1 to time slot 15 and time slot 17 to time slot 31 are used to carry a PCM encoded voice band signal or data. The remaining 64kbits/s channel time slot 16 may be used for signaling. The XRT86L34 T1/J1/E1 Octal Framer supports the following signaling formats to interconnect to CEPT channelized service functions:

- Common Channel Signaling (CCS)
- Channel Associated Signaling (CAS)
- Primary Rate ISDN Message Oriented Signaling (ISDN-PRI)

The XRT86L34 T1/J1/E1 Octal Framer supports insertion of various types of signaling information into the timeslot 16 of an outgoing E1 frame. It also supports extraction and substitution of signaling information from the incoming E1 frame. The following section provides a brief overview of Common Channel Signaling, Channel Associated Signaling in E1 mode.

NOTE: *The time slot 16 can also be configured to carry PCM encoded voice or data if neither CCS nor CAS signaling is used. The XRT86L34 framer allows the user to choose which one of the CCS, CAS, ISDN-PRI message or PCM data to be carries on the time slot 16.*

4.3.11 Brief Discussion of Common Channel Signaling in E1 Framing Format

As the name referred, Common Channel Signaling is signaling information common to all thirty voice or data channels of an E1 trunk. The time slot 16 may be used to carry Common Channel Signaling data of up to a rate of 64kbits/s. The national bits of time slot 0 may also be used for Common Channel Signaling. Since there are five national bits of time slot 0 per every two E1 frames, the total bandwidth of the national bits is 20kbits/s. The Common Channel Signaling is essentially data link information that provides performance monitoring and transmission quality report.

4.3.12 Brief Discussion of Channel Associated Signaling in E1 Framing Format

Signaling is required when dealing with voice and dial-up data services in E1 applications. Traditionally, signaling is provided on a dial-up telephone line, across the talk-path. Signaling is used to tell the receiver where the call or route is destined. The signal is sent through switches along the route to a distant end. Common types of signals are:

- On hook
- Off hook
- Dial tone
- Dialed digits
- Ringing cycle
- Busy tone

A signal is consists of four bits namely A, B, C and D. These bits define the state of the call for a particular time slot. The time slot 16 octet of each E1 frame can carry CAS signals for two E1 voice or data channels. Therefore, sixteen E1 frames are needed to carry CAS signals for all 32 E1 channels. The sixteen E1 frames then forms a CAS Multi-frame.

The time slot 16 of Frame number 0 of an E1 CAS Multi-frame carries the pattern of "0000 XYXX". The time slot 16 of Frame number 1 carries signals of Channel 1 and Channel 17. The time slot 16 of Frame number 2 carries signals of Channel 2 and Channel 18, and so on. The following table shows the bit allocations of Channel Associated Signaling in E1 framing format.

TIME SLOT 16 OF FRAME 0		TIME SLOT 16 OF FRAME 1		TIME SLOT 16 OF FRAME 2		TIME SLOT 16 OF FRAME 3	
0000	XYXX	ABCD of Ch. 1	ABCD of Ch. 17	ABCD of Ch. 2	ABCD of Ch. 18	ABCD of Ch. 3	ABCD of Ch. 19

TIME SLOT 16 OF FRAME 4		TIME SLOT 16 OF FRAME 5		TIME SLOT 16 OF FRAME 6		TIME SLOT 16 OF FRAME 7	
ABCD of Ch. 4	ABCD of Ch. 20	ABCD of Ch. 5	ABCD of Ch. 21	ABCD of Ch. 6	ABCD of Ch. 22	ABCD of Ch. 7	ABCD of Ch. 23

TIME SLOT 16 OF FRAME 8		TIME SLOT 16 OF FRAME 9		TIME SLOT 16 OF FRAME 10		TIME SLOT 16 OF FRAME 11	
ABCD of Ch. 8	ABCD of Ch. 24	ABCD of Ch. 9	ABCD of Ch. 25	ABCD of Ch. 10	ABCD of Ch. 26	ABCD of Ch. 11	ABCD of Ch. 27

TIME SLOT 16 OF FRAME 12		TIME SLOT 16 OF FRAME 13		TIME SLOT 16 OF FRAME 14		TIME SLOT 16 OF FRAME 15	
ABCD of Ch. 12	ABCD of Ch. 28	ABCD of Ch. 13	ABCD of Ch. 29	ABCD of Ch. 14	ABCD of Ch. 30	ABCD of Ch. 15	ABCD of Ch. 31

The four zeros pattern is the multi-frame alignment signal that indicates the beginning of an E1 CAS Multi-frame. The XRT86L34 framer, upon detection of the four zeros pattern in the time slot 16, declares CAS multi-frame synchronization and would pulse the Receive CAS Multi-frame Synchronization pulse (RxCASMSync_n) HIGH for one clock period. The user, triggering on the Receive CAS Multi-frame Synchronization pulse, would thus identify the received CAS Multi-frame boundary.

The X in XYXX pattern located in the time slot 16 of Frame number 0 should be fixed to "1" and can be used to prevent mimicking of CAS Multi-frame alignment pattern.

The Y in XYXX pattern is used for alarm indication of time slot 16 to the remote terminal. If signals of time slot 16 is transmitted and received correctly, the Y bit is set to "0". In an alarm condition, the Y bit is set to "1". Therefore, Y bit is also known as CAS Multi-frame yellow alarm.

4.3.13 Configure the framer to transmit Channel Associated Signaling

The XRT86L34 framer supports transmission of Common Channel Signaling and Channel Associated Signaling according to ITU-T Recommendation G.704. As discussed briefly before, Channel Associated Signaling includes the signaling bits, the CAS Multi-frame Alignment pattern and the X and Y bits.

Signaling bits can be inserted into the outgoing E1 frame through the following:

- Signaling data is inserted from the Transmit Signaling Control Registers (TSCR) of each timeslot.
- Signaling data is inserted from TxSig_n pin.
- Signaling data is inserted from TxOH-n pin.
- Signaling data is embedded into the input PCM data coming from the Terminal Equipment.

The CAS Multi-frame alignment pattern of four zeros can be inserted into the outgoing E1 frame by using the following method:

- CAS Multi-frame alignment pattern is inserted from theTransmit Signaling Control Registers (TSCR).
- CAS Multi-frame alignment pattern is inserted from TxSig_n pin.
- CAS Multi-frame alignment pattern is inserted from TxOH-n pin.
- CAS Multi-frame alignment pattern is embedded into the input PCM data coming from the Terminal Equipment.

The CAS Multi-frame Yellow Alarm Y bit and the X bits can be inserted into the outgoing E1 frame by using the following method:

- The X and Y bits are inserted from the Transmit Signaling Control Register (TSCR).
- The X and Y bits are inserted from TxSig_n pin.
- The X and Y bits are inserted from TxOH-n pin.
- The X and Y bits are embedded into the input PCM data coming from the Terminal Equipment.

- The X bit is inserted from the Transmit Signaling Control Register (TSCR) and Y bit is generated by the XRT86L34 framer according to operating condition of the E1 link.

4.3.13.1 Insert Signaling Bits from TSCR Register

The four most significant bits of the Transmit Signaling Control Register (TSCR) of each time slot can be used to store outgoing signaling data. The user can program these bits through microprocessor access. If the XRT86L34 framer is configure to insert signaling bits from TSCR registers, the E1 Transmit Framer block will fill up the time slot 16 octet with the signaling bits stored inside the TSCR registers. The insertion of signaling bit into PCM data is done on a per-channel basis. The most significant bit (Bit 7) of TSCR register is used to store Signaling bit A. Bit 6 is used to hold Signaling bit B. Bit 5 is used to hold Signaling bit C. Bit 4 is used to hold Signaling bit D.

The table below shows the four most significant bits of the Transmit Signaling Control Register.

TRANSMIT SIGNALING CONTROL REGISTER (TSCR) (ADDRESS = 0XN340H - 0XN35FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Signaling Bit A	R/W	This bit is used to store Signaling Bit A.
6	Signaling Bit B	R/W	This bit is used to store Signaling Bit B.
5	Signaling Bit C	R/W	This bit is used to store Signaling Bit C.
4	Signaling Bit D	R/W	This bit is used to store Signaling Bit D.

4.3.13.2 Insert Signaling Bits from TxSig_n Pin

The XRT86L34 framer can be configure to insert signaling bits provided by external equipment through the TxSig_n pins. This pin is a multiplexed I/O pin with two functions:

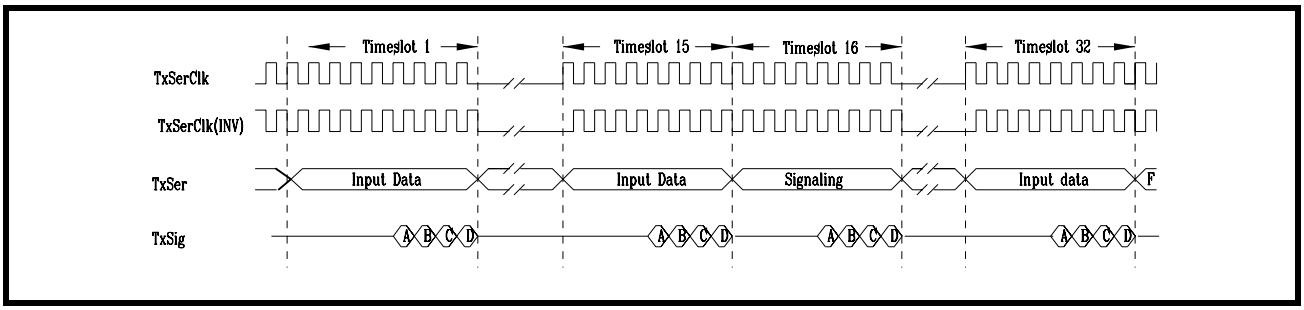
- TxTSb[0]_n - Transmit Timeslot Number Bit [0] Output pin
- TxSig_n - Transmit Signaling Input pin

When the Transmit Fractional E1 bit of the Transmit Interface Control Register (TICR) is set to 0, this pin is configured as TxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the E1 PCM data that is transmitting.

When the Transmit Fractional E1 bit of the Transmit Interface Control Register (TICR) is set to 1, this pin is configured as TxSig_n pin, it acts as an input source for the signaling bits to be transmitted in the outbound E1 frames.

Figure 40 below is a timing diagram of the TxSig_n input pin. Please note that the Signaling Bit A of a certain channel coincides with Bit 5 of the PCM data of that channel; Signaling Bit B coincides with Bit 6 of the PCM data; Signaling Bit C coincides with Bit 7 of the PCM data and Signaling Bit D coincides with Bit 8 (LSB) of the PCM data.

FIGURE 40. TIMING DIAGRAM OF THE TXSIG_N INPUT



The table below shows configurations of the Transmit Fractional E1 bit of the Transmit Interface Control Register (TICR).

TRANSMIT INTERFACE CONTROL REGISTER (TICR) (ADDRESS = 0XN120H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Transmit Fractional E1	R/W	This READ/WRITE bit-field permits the user to determine which one of the two functions the multiplexed I/O pin of TxTSb[0]_n/TxSig_n is spotting. 0 - This pin is configured as TxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the E1 PCM data that is transmitting. 1 - This pin is configured as TxSig_n pin, it acts as an input source for the signaling bits to be transmitted in the outbound E1 frames

4.3.13.3 Insert Signaling Bits from TxOH_n Pin

The XRT86L34 framer can be configure to insert signaling bits provided by external equipment through the Transmit Overhead TxOH_n input pins.

The TxOH_n pin can acts as an input source for the signaling bits to be transmitted in the outbound E1 frames. When this pin is chosen as the input source for the signaling bits, any data presents on this pin in time slot 16 would be taken into the framer directly. The time slot 16 octet of the outbound E1 frame will be replaced by data inputted from this pin in time slot 16.

Please note that the Signaling bit A of Channel 1-15 coincides with Bit 1 of the PCM data; Signaling bit B Channel 1-15 coincides with Bit 2 of the PCM data; Signaling bit C Channel 1-15 coincides with Bit 3 of the PCM; Signaling bit D Channel 1-15 coincides with Bit 4 of the PCM data.

Similarly, the Signaling bit A of Channel 17-31 coincides with Bit 5 of the PCM data; Signaling bit B Channel 17-31 coincides with Bit 6 of the PCM data; Signaling bit C Channel 17-31 coincides with Bit 7 of the PCM; Signaling bit D Channel 17-31 coincides with Bit 8 of the PCM data.

4.3.13.4 Insert Signaling Data from TxSer_n Pin

Depends on applications, the Terminal Equipment can embed signaling information into the E1 PCM data and then send the data to the XRT86L34 framer device. In this case, the user should configure the framer not to insert any signaling data. The input E1 PCM data will then be directed to the Transmit LIU Interface without any modifications.

4.3.13.5 Enable Channel Associated Signaling and Signaling Data Source Control

The Transmit Signaling Control Register (TSCR) of each channel selects source of signaling data to be inserted into the outgoing E1 frame and enables Channel Associated signaling. As we mentioned before, the signaling data can be inserted from Transmit Signaling Control Registers (TSCR) of each timeslot, from the TxSig_n input pin, from the TxOH_n input pin or from the TxSer_n input pin. The Transmit Signaling Data Source Select [1:0] bits of the Transmit Signaling Control Register (TSCR) determines from which sources the signaling data is inserted from.

The table below shows configurations of the Transmit Signaling Data Source Select [1:0] bits of the Transmit Signaling Control Register (TSCR).

TRANSMIT SIGNALING CONTROL REGISTER (TSCR) (ADDRESS = 0XN340H - 0XN357H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Signaling Source Select	R/W	00 - None of the signaling data, the CAS Multi-frame alignment pattern, the X bit or the CAS Multi-frame Yellow Alarm bit Y is inserted into the outgoing E1 PCM data by the framer. However, the user can embed the signaling data, the CAS Multi-frame alignment pattern, the X bit or the CAS Multi-frame Yellow Alarm bit Y into E1 PCM data before routing the PCM data into the framer. 01 - The signaling data, the CAS Multi-frame alignment pattern, the X bit or the CAS Multi-frame Yellow Alarm bit Y is inserted into the outgoing E1 PCM data from TSCR register of each timeslot. 10 - If the XRT86L34 framer is operating in E1 2.048Mbit/s mode and if the TxFR2048 bit of the Transmit Interface Control Register (TICR) is set to zero: The signaling data, the CAS Multi-frame alignment pattern, the X bit or the CAS Multi-frame Yellow Alarm bit Y is inserted into the outgoing E1 PCM data from the TxOH_n input pin. If the XRT86L34 framer is operating in E1 2.048Mbit/s mode and if the TxFR2048 bit of the Transmit Interface Control Register (TICR) is set to one: The signaling data, the CAS Multi-frame alignment pattern, the X bit or the CAS Multi-frame Yellow Alarm bit Y is inserted into the outgoing E1 PCM data from the TxSig_n input pin. 11 - No signaling data or the CAS Multi-frame alignment pattern is inserted into the input E1 PCM data by the framer. However, the user can embed signaling data into E1 PCM data before routing the PCM data into the framer. The X bit is inserted into the outgoing E1 PCM data from TSCR register. The CAS Multi-frame Yellow Alarm Y bit is generated by the XRT86L34 framer depends on operating condition of the E1 link.

4.3.14 How to Configure the XRT86L34 Framer to Generate and Transmit Alarms and Error Indications to Remote Terminal

The XRT86L34 T1/J1/E1 Octal Framer can be configured to monitor quality of received E1 frames. It can generate error indications if the local receive framer has received error frames from the remote terminal. If corresponding interrupt is enabled, the local microprocessor operation is interrupted by these error conditions. Upon microprocessor interruption, the user can intervene by looking into the error conditions.

At the same time, the user can configure the XRT86L34 framer to transmit alarms and error indications to remote terminal. Different alarms and error indications will be transmitted depending on the error condition. The section below gives a brief discussion of the error conditions and appropriate alarms that should be generated and transmitted by the XRT86L34 framer.

4.3.15 Brief discussion of alarms and error conditions

As defined in E1 specification, alarm conditions are created from defects. Defects are momentary impairments present on the E1 trunk. If a defect is present for a sufficient amount of time (called the integration time), then the defect becomes an alarm. Once an alarm is declared, the alarm is present until after the defect clears for a sufficient period of time. The time it takes to clear an alarm is called the de-integration time.

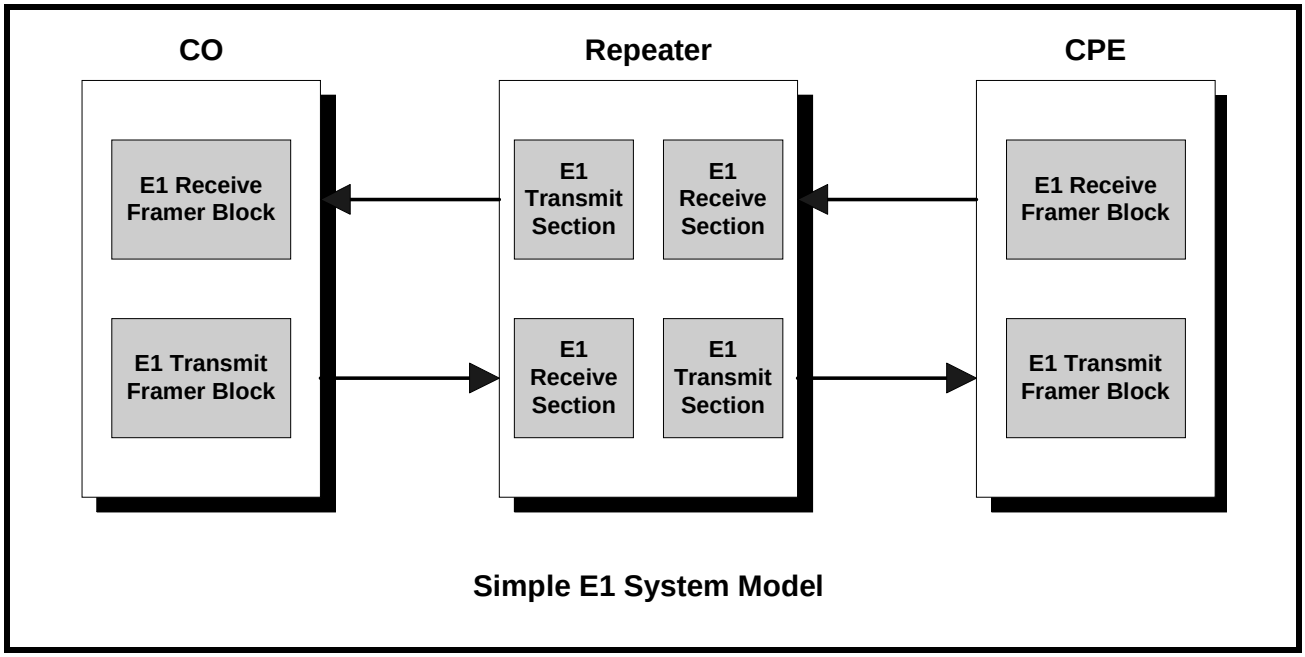
Alarms are used to detect and warn maintenance personnel of problems on the E1 trunk. There are three types of alarms:

- Red alarm or Service Alarm Indication (SAI) Signal
- Blue alarm or Alarm Indication Signal (AIS)
- Yellow alarm or Remote Alarm Indication (RAI) Signal

To explain the error conditions and generation of different alarms, let us create a simple E1 system model. In this model, an E1 signal is sourced from the Central Office (CO) through a Repeater to the Customer Premises

Equipment (CPE). At the same time, an E1 signal is routed from the CPE to the Repeater and back to the Central Office. Figure 41 below shows the simple E1 system model.

FIGURE 41. SIMPLE DIAGRAM OF E1 SYSTEM MODEL



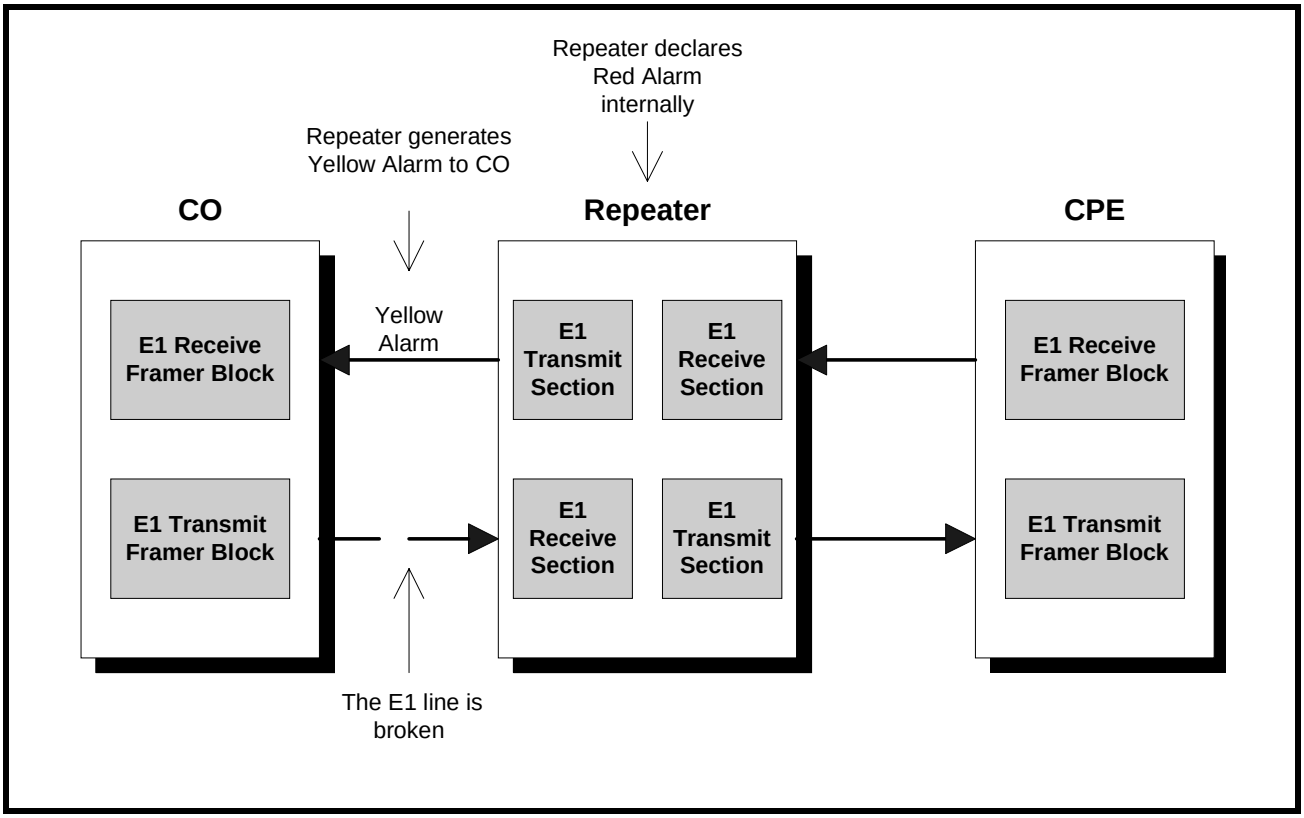
When the E1 system runs normally, that is, when there is no Loss of Signal (LOS) or Loss of Frame (LOF) detected in the line, no alarm will be generated. Sometimes, intermittent outburst of electrical noises on the line might result in Bipolar Violation or bit errors in the incoming signals, but these errors in general will not trigger the equipment to generate alarms. They will, depending on the system requirements, trigger the framer to generate interrupts that would cause the local microprocessor to create performance reports of the line.

Now, consider a case in which the E1 line from the CO to the Repeater is broken or interrupted, resulting in completely loss of incoming data or severely impaired signal quality. Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the Repeater will generate an internal Red Alarm, also known as the Service Alarm Indication. This alarm will normally trigger a microprocessor interrupt informing the user that an incoming signal failure is happening.

When the Repeater is in the Red Alarm state, it will transmit the Yellow Alarm to the CO indicating the loss of an incoming signal or loss of frame synchronization. This Yellow Alarm informs the Repeater that there is a

problem further down the line and its transmission is not being received at the Repeater. Figure 42 below illustrates the scenario in which the E1 connection from the CO to the Repeater is broken.

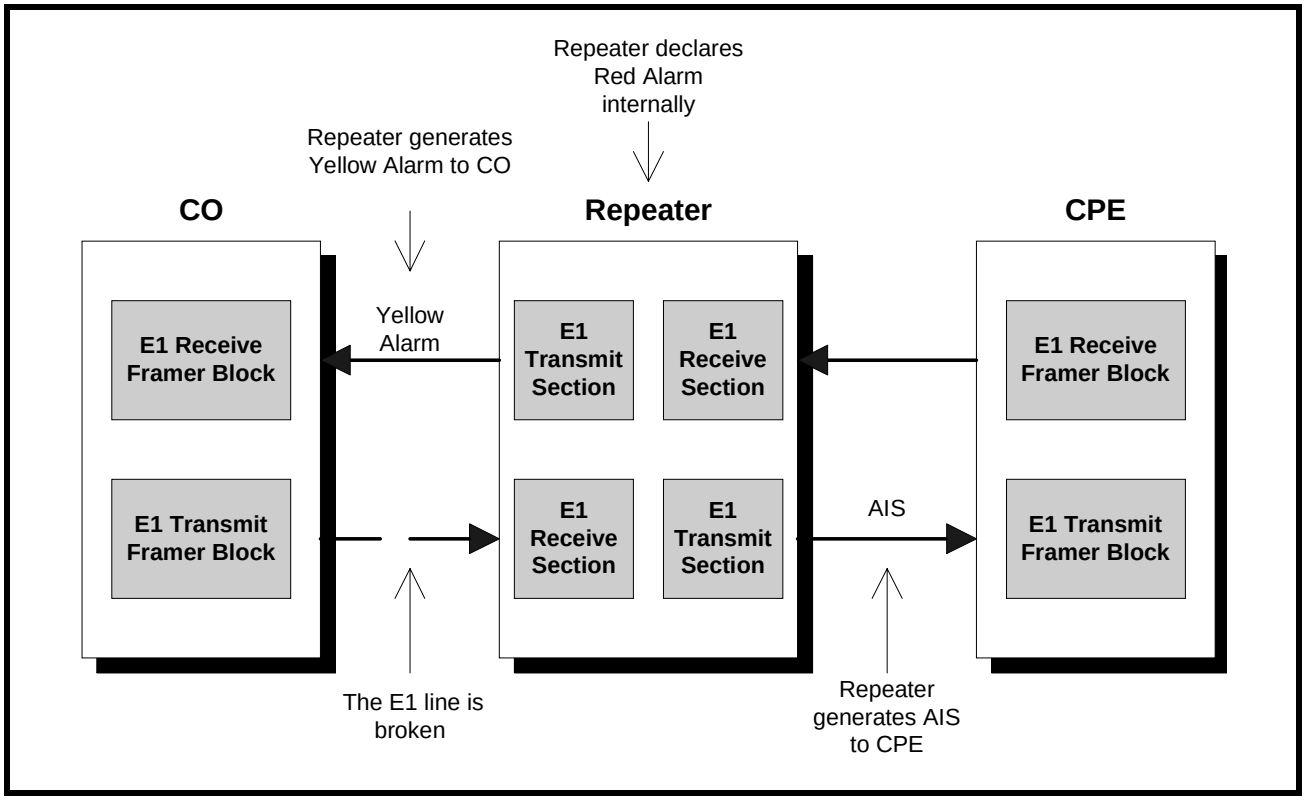
FIGURE 42. GENERATION OF YELLOW ALARM BY THE REPEATER UPON DETECTION OF LINE FAILURE



The Repeater will also transmit a Blue Alarm, also known as Alarm Indication Signal (AIS) to the CPE. Blue alarm is an all ones pattern indicating that the equipment is functioning but unable to offer service due to failures originated from remote side. It is sent such that the equipment downstream will not lose clock synchroni-

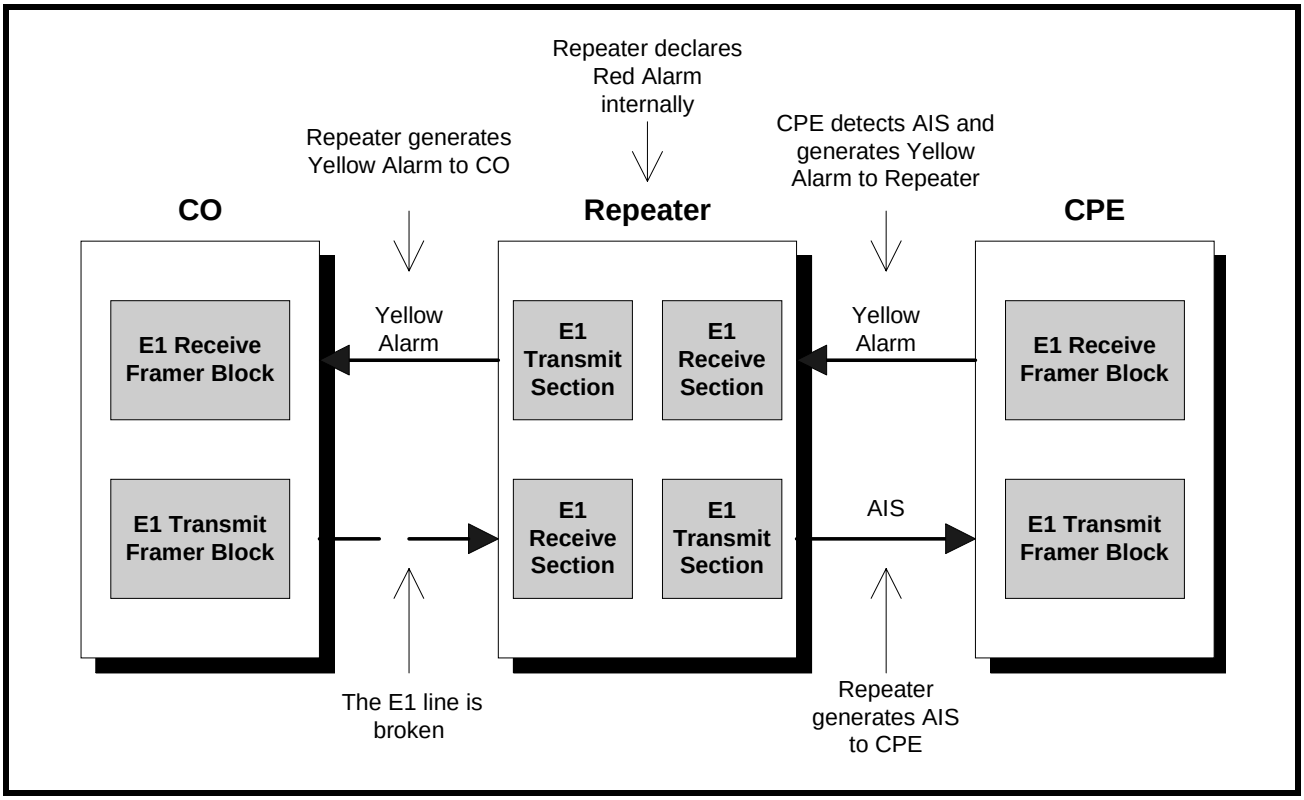
zation even though no meaningful data is received. Figure 43 below illustrates this scenario in which the Repeater is sending an AIS to the CPE upon detection of line failure from the CO.

FIGURE 43. GENERATION OF AIS BY THE REPEATER UPON DETECTION OF LINE FAILURE



Now, the CPE uses the AIS signal sent by the Repeater to recover received clock and remain in synchronization with the system. Upon detecting the incoming AIS signal, the CPE will generate a Yellow Alarm automatically to the Repeater to indicate the loss of incoming data. Figure 44 below illustrates this scenario in which the Repeater is sending an AIS to the CPE and the CPE is sending a Yellow Alarm back to the Repeater.

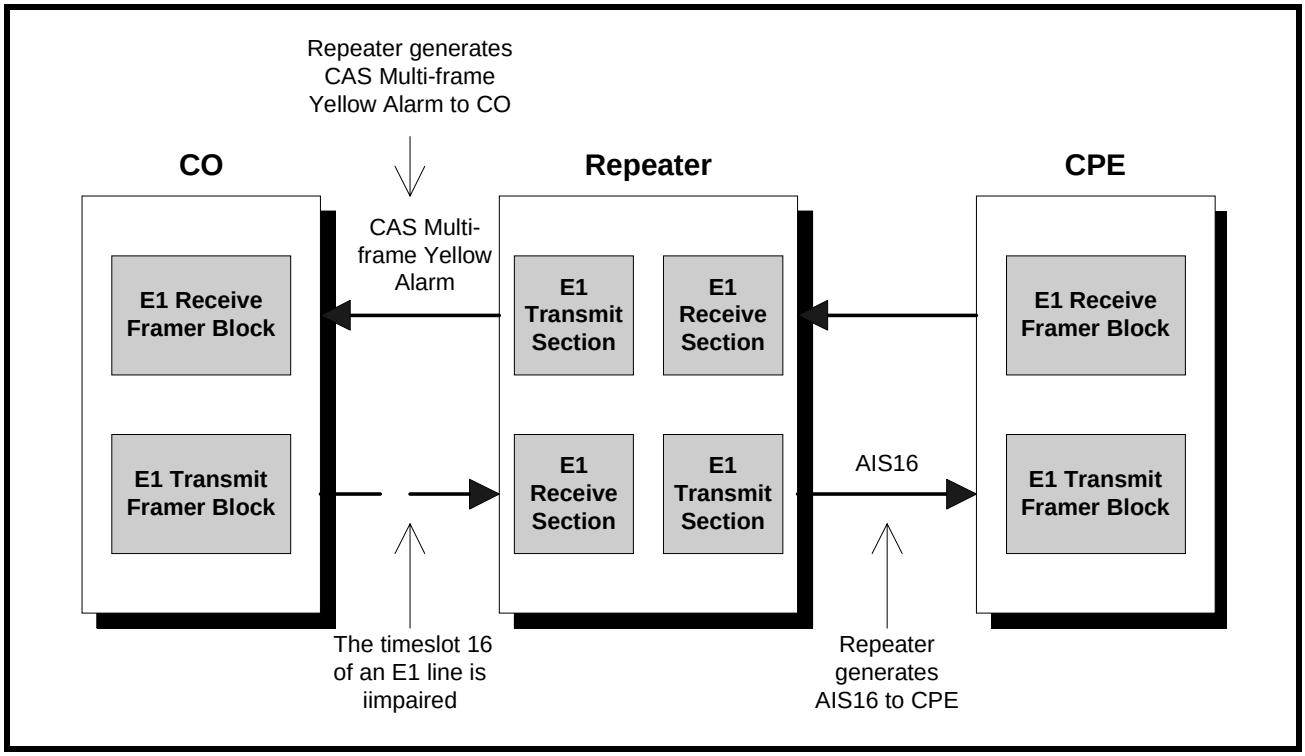
FIGURE 44. GENERATION OF YELLOW ALARM BY THE CPE UPON DETECTION OF AIS ORIGINATED BY THE REPEATER



Next, let us consider the scenario in which the signaling and data link channel (the time slot 16) of an E1 line between a far-end terminal (for example, the CO) and a near-end terminal (for example, the repeater) is impaired. In this case, the CAS signaling data received by the repeater is corrupted. The Repeater will then send an all ones pattern in time slot 16 (AIS16 pattern) downstream to the CPE. The repeater will also generate a CAS Multi-frame Yellow Alarm upstream to the CO to indicate the loss of CAS Multi-frame synchronization.

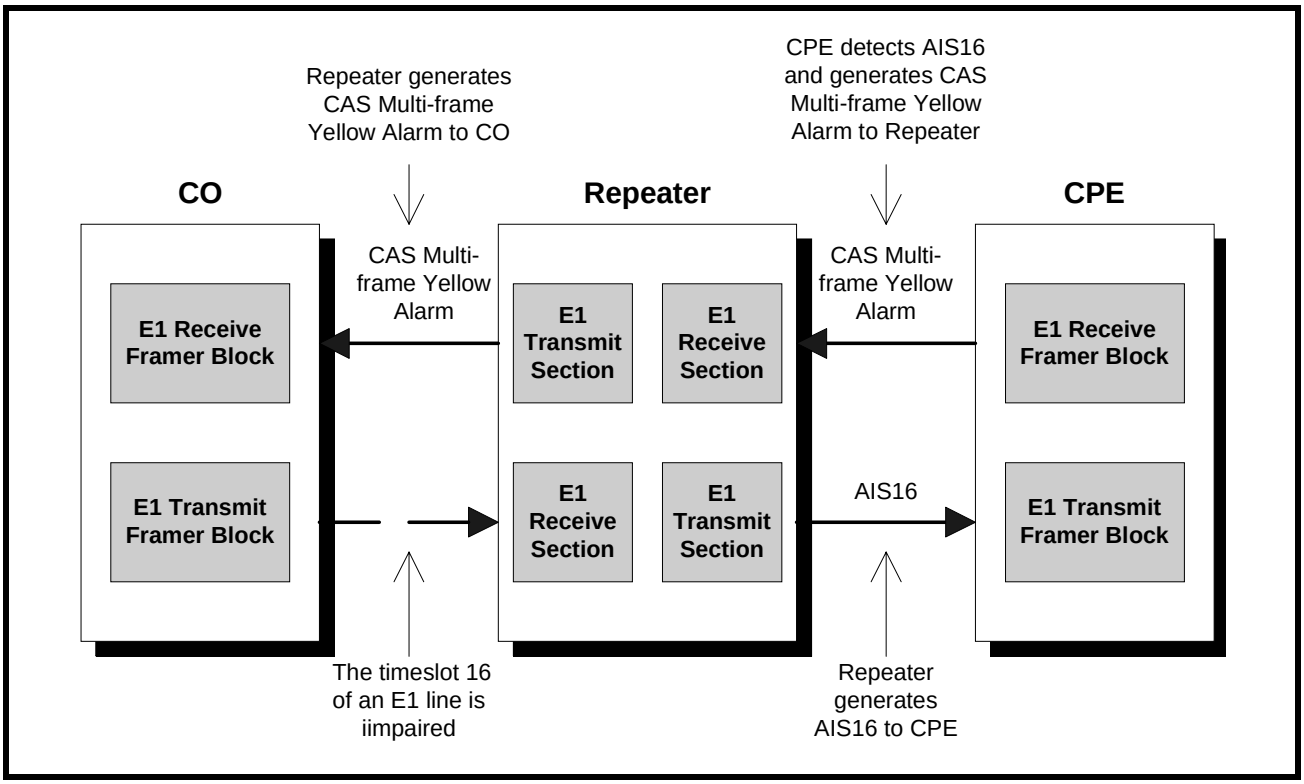
Figure 45 below illustrates this scenario in which the Repeater is sending an "AIS16" pattern to the CPE while sending a CAS Multi-frame Yellow Alarm to the CO.

FIGURE 45. GENERATION OF CAS MULTI-FRAME YELLOW ALARM AND AIS16 BY THE REPEATER



The CPE, upon detecting the incoming AIS16 signal, will generate a CAS Multi-frame Yellow Alarm to the Repeater to indicate the loss of CAS Multi-frame synchronization. Figure 46 below illustrates the CPE sending a CAS Multi-frame Yellow Alarm back to the Repeater

FIGURE 46. GENERATION OF CAS MULTI-FRAM YELLOW ALARM BY THE CPE UPON DETECTION OF "AIS16" PATTERN SENT BY THE REPEATER



In summary, AIS or Blue Alarm is sent by a piece of E1 equipment downstream indicating that the incoming signal from upstream is lost. Yellow Alarm is sent by a piece of E1 equipment upstream upon detection of Loss of Signal, Loss of Frame or when it is receiving AIS.

Similarly, an "AIS16" pattern is sent by a piece of E1 equipment downstream indicating that the incoming data link channel from upstream is damaged. The CAS Multi-frame Yellow Alarm is sent by a piece of E1 equipment upstream upon detection of Loss of CAS Multi-frame synchronization or when it is receiving an "AIS16" pattern.

4.3.16 How to configure the framer to transmit AIS

As we discussed in the previous section, Alarm Indication Signal (AIS) or Blue Alarm is transmitted by the intermediate node to indicate that the equipment is still functioning but unable to offer services. It is an all ones (except for framing bits) pattern which can be used by the equipment further down the line to maintain clock recovery and timing synchronization.

The XRT86L34 framer can generate three types of AIS when it is running in E1 format:

- Framed AIS
- Unframed AIS
- AIS16

Unframed AIS is an all ones pattern. If unframed AIS is sent, the equipment further down the line will be able to maintain timing synchronization and be able to recover clock from the received AIS signal. However, due to the lack of framing bits, the equipment farther down the line will not be able to maintain frame synchronization and will declare Loss of Frame (LOF).

On the other hand, the payload portion of a framed AIS pattern is all ones. However, a framed AIS pattern still has correct framing bits. Therefore, the equipment further down the line can still maintain frame synchronization as well as timing synchronization. In this case, no LOF or Red alarm will be declared.

"AIS16" is an AIS alarm that only supported in E1 framing format. It is an all ones pattern in time slot 16 of each E1 frame. As we mentioned before, time slot 16 is usually used for signaling and data link in E1, therefore, an "AIS16" alarm is transmitted by the intermediate node to indicate that the data link channel is having a problem. Since all the other thirty one time slots are still transmitting normal data (that is, framing information and PCM data), therefore, the equipment further down the line can still maintain frame synchronization, timing synchronization as well as receiving PCM data. In this case, no LOF or Red alarm will be declared by the equipments further down the line. However, a CAS Multi-frame Yellow Alarm will be sent by the equipment further down the line to indicate the loss of CAS Multi-frame alignment.

The Transmit Alarm Indication Signal Select [1:0] bits of the Alarm Generation Register (AGR) enable the three types of AIS transmission that are supported by the XRT86L34 framer. The table below shows configurations of the Transmit Alarm Indication Signal Select [1:0] bits of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR) (ADDRESS = 0XN108H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Transmit AIS Select	R/W	These READ/WRITE bit-fields allows the user to choose which one of the three AIS pattern supported by the XRT86L34 framer will be transmitted. 00 - No AIS alarm is generated. 01 - Enable unframed AIS alarm of all ones pattern. 11 - AIS16 pattern is generated. Only time slot 16 is carrying the all ones pattern. The other time slots still carry framing and PCM data. 11 - Enable framed AIS alarm of all ones pattern except for framing bits.

4.3.17 How to configure the framer to generate Red Alarm

Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the Repeater will generate an internal Red Alarm when enabled. This alarm will normally trigger a microprocessor interrupt informing the user that an incoming signal failure is happening.

The Loss of Frame Declaration Enable bit of the Alarm Generation Register (AGR) enable the generation of Red Alarm. The table below shows configurations of the of Frame Declaration Enable bit of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR) (ADDRESS = 0XN108H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Loss of Frame Declaration Enable	R/W	This READ/WRITE bit-field permits the framer to declare Red Alarm in case of Loss of Frame Alignment (LOF). When receiver module of the framer detects Loss of Frame Alignment in the incoming data stream, it will generate a Red Alarm. The framer will also generate an RxLOFs interrupt to notify the microprocessor that an LOF condition is occurred. A Yellow Alarm is then returned to the remote transmitter to report that the local receiver detects LOF. 0 - Red Alarm declaration is disabled. 1 - Red Alarm declaration is enabled.

4.3.18 How to configure the framer to transmit Yellow Alarm

The XRT86L34 framer supports transmission of both Yellow Alarm and CAS Multi-frame Yellow Alarm in E1 mode.

Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the receiver will transmit the Yellow Alarm back to the source indicating the loss of an incoming signal. This Yellow Alarm informs the source that there is a problem further down the line and its transmission is not being received at the destination.

On the other hand, upon detection of Loss of CAS Multi-frame alignment pattern, the receiver section of the XRT86L34 framer will transmit a CAS Multi-frame Yellow Alarm back to the source indicating the Loss of CAS Multi-frame synchronization.

The Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register (AGR) enable transmission of different types of Yellow alarm that are supported by the XRT86L34 framer.

4.3.18.1 Transmit Yellow Alarm

The Yellow Alarm bits are located at bit 3 of time slot 0 of non-FAS frames. A logic one of this bit denotes the Yellow Alarm and a logic zero of this bit denotes normal operation. The XRT86L34 supports transmission of Yellow Alarm automatically or manually.

When the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 01, the Yellow Alarm bit is transmitted by echoing the received FAS alignment pattern. If the correct FAS alignment is received, the Yellow Alarm bit is set to zero. If the FAS alignment pattern is missing or corrupted, the Yellow Alarm bit is set to one while Loss of Frame Synchronization is declared.

When the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 10, the Yellow Alarm bit is transmitted as zero.

When the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 11, the Yellow Alarm bit is transmitted as one.

4.3.18.2 Transmit CAS Multi-frame Yellow Alarm

Within the sixteen-frame CAS Multi-frame, the CAS Multi-frame Yellow Alarm bits are located at bit 6 of time slot 16 of frame number 0. A logic one of this bit denotes the CAS Multi-frame Yellow Alarm and a logic zero of this bit denotes normal operation. The XRT86L34 supports transmission of CAS Multi-frame Yellow Alarm automatically or manually.

When the CAS Multi-frame Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 01, the CAS Multi-frame Yellow Alarm bit is transmitted by echoing the received CAS Multi-frame alignment pattern (the four zeros pattern). If the correct CAS Multi-frame alignment is received, the CAS Multi-frame Yellow Alarm bit is set to zero. If the CAS Multi-frame alignment pattern is missing or corrupted, the CAS Multi-frame Yellow Alarm bit is set to one while Loss of CAS Multi-frame Synchronization is declared.

When the CAS Multi-frame Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 10, the CAS Multi-frame Yellow Alarm bit is transmitted as zero.

When the CAS Multi-frame Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 11, the CAS Multi-frame Yellow Alarm bit is transmitted as one.

The table below shows configurations of the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR) (ADDRESS = 0XN108H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	Yellow Alarm Generation Select	R/W	These READ/WRITE bit-fields allows the user to choose how the XRT86L34 would generate Yellow Alarm and CAS Multi-frame Yellow Alarm. 00 - Transmission of Yellow Alarm and CAS Multi-frame Yellow Alarm is disabled. 01 - The Yellow Alarm bit is transmitted by echoing the received FAS alignment pattern. If the correct FAS alignment is received, the Yellow Alarm bit is set to zero. If the FAS alignment pattern is missing or corrupted, the Yellow Alarm bit is set to one. The CAS Multi-frame Yellow Alarm bit is transmitted by echoing the received CAS Multi-frame alignment pattern (the four zeros pattern). If the correct CAS Multi-frame alignment is received, the CAS Multi-frame Yellow Alarm bit is set to zero. If the CAS Multi-frame alignment pattern is missing or corrupted, the CAS Multi-frame Yellow Alarm bit is set to one. 10 - The Yellow Alarm and CAS Multi-frame Yellow Alarms are transmitted as zero. 11 - The Yellow Alarm and CAS Multi-frame Yellow Alarms are transmitted as one.

5.0 THE DS1 TRANSMIT SECTION

5.1 THE DS1 TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK

5.1.1 Description of the Transmit Payload Data Input Interface Block

Each of the four framers within the XRT86L34 includes a Transmit Payload Data Input Interface block. The function of this block is to provide an interface to the local Terminal Equipment (for example, a Central Office or switching equipment) that has data to send to a Far End terminal over a DS1 or E1 transport medium.

The Payload Data Input Interface module (also known as the Back-plane Interface module) supports payload data to be taken from or presented to the system. In DS1 mode, supported data rates are 1.544Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 12.352Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s. In E1 mode, supported data rates are MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s.

The Transmit Payload Data Input Interface block supplies or accepts the following signals to the local Terminal Equipment circuitry:

- Transmit Serial Data Input (TxSER)
- Transmit Serial Clock (TxSERCLK)
- Transmit Single-frame Synchronization Signal (TxSYNC)
- Transmit Multi-frame Synchronization Signal (TxMSYNC)
- Transmit Time-slot Indicator Clock (TxCHCLK)
- Transmit Time-slot Indication Bits (TxCHN[4:0])

The Transmit Serial Data is an input pin carrying payload, signaling and sometimes Data Link data supplied by the local Terminal Equipment to the XRT86L34.

The Transmit Serial Clock is an input or output signal used by the Transmit Payload Data Input Interface block to latch in incoming serial data from the local Terminal Equipment. The Transmit Clock Inversion bit of the Transmit Interface Control Register (TICR) determines at which edge of the Transmit Serial Clock data transition on TxSER.

The table below shows configurations of the Transmit Clock Inversion bit of the Transmit Interface Control Register (TICR).

TRANSMIT INTERFACE CONTROL REGISTER (TICR) (ADDRESS = 0xn120H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Transmit Clock Inversion	R/W	0 - Serial data transition happens on rising edge of the Transmit Serial Clock. 1 - Serial data transition happens on falling edge of the Transmit Serial Clock.

Throughout the discussion of this datasheet, we assume that serial data transition happens on the rising edge of the Transmit Serial Clock unless stated otherwise.

The Transmit Single-frame Synchronization signal (TxSYNC) is either input or output. When configured as input, it indicates the beginning of a DS1 frame. When configured as output, it indicates the end of a DS1 frame.

The Transmit Multi-frame Synchronization signal is either input or output. When configured as input, it indicates the beginning of a DS1 multi-frame. When configured as output, it indicates the end of a DS1 multi-frame.

The Transmit Input Clock signal is multiplexed into the Transmit Multi-frame Synchronization pin (TxMSync_n) of XRT86L34. When the framer is running at High-speed Back-plane Interface mode, the Transmit Input Clock functions as the timing source for the High-speed Back-plane Interface.

By connecting these signals with the local Terminal Equipment, the Transmit Payload Data Input Interface accepts payload data from the Terminal Equipment and routes it to the Transmit Framer module inside the device.

5.1.2 Brief Discussion of the Transmit Payload Data Input Interface Block Operating at 1.544Mbit/s mode

If the framer is operating in normal 1.544Mbit/s Back-plane interface mode for DS1, timing source of the transmit section can be one of the three clocks:

- Transmit Serial Input Clock
- OSCCLK Driven Divided Clock
- Recovered Receive Line Clock

The Transmit Timing Source Select [1:0] bits of the Clock Select Register (CSR) determine which clock is used as the timing source. The following table shows configurations of the Transmit Timing Source Select [1:0] bits of the Clock Select Register.

CLOCK SELECT REGISTER (CSR) (ADDRESS = 0xn100H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Timing Source Select	R/W	These two READ/WRITE bit-fields permit the user to select the timing source of Transmit section of the framer. When the Transmit Back-plane interface is operating at a clock rate of 1.544MHz for T1, these two READ/WRITE bit-fields also determine the direction of Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk). When the framer is operating at other Back-plane mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all inputs. 00 - The Recovered Receive Line Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 1.544MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer. 01 - The Transmit Serial Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 1.544MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all inputs. 10 - The OSCCLK Driven Divided clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 1.544MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer. 11 - The Recovered Receive Line Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 1.544MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer.

The Transmit Serial Clock (TxSerClk_n), Transmit Single-frame Synchronization Signal (TxSync_n) and Transmit Multi-frame Synchronization Signal (TxMSync_n) can be either inputs or outputs depend on the timing source of the Transmit section of the framer.

With the OSCCLK Driven Divided Clock or the Recovered Receive Line Clock being the timing source of the transmit section, the Transmit Serial Clock (TxSerClk_n), Transmit Single-frame Synchronization Signal (TxSync_n) and Transmit Multi-frame Synchronization Signal (TxMSync_n) are all outputs.

With the timing source of the transmit section being the Transmit Serial Input Clock, the Transmit Serial Clock (TxSerClk_n), Transmit Single-frame Synchronization Signal (TxSync_n) and Transmit Multi-frame Synchronization Signal (TxMSync_n) are all inputs.

The following table illustrates the input and output nature of these signals for different Transmit timing sources.

TABLE 168: SIGNALS FOR DIFFERENT TRANSMIT TIMING SOURCES

TRANSMIT TIMING SOURCE	TXSERCLK_N	TXSYNC_N	TXMSYNC_N
Terminal Equipment Driven TxSerClk	Input	Input	Input
OSCCLK Driven Divided Clock	Output	Output	Output
Recovered Receive Line Clock	Output	Output	Output

The Transmit Time-slot Indication Bits (TxTSb[4:0]_n) are multiplexed I/O pins. The functionality of these pins is governed by the value of Transmit Fractional T1 Input Enable bit of the Transmit Interface Control Register (TICR).

The following table illustrates the configurations of the Transmit Fractional DS1 Input Enable bit.

TRANSMIT INTERFACE CONTROL REGISTER (TICR) (ADDRESS = 0xn120H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Transmit Fractional DS1 Input Enable	R/W	0 - The Transmit Time-slot Indication bits (TxTSb[4:0] are outputting five-bit binary values of Time-slot number (0-23) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. The Transmit Time-slot Indicator Clock signal (TxTSClk_n) is a 192KHz clock that pulses HIGH for one DS1 bit period whenever the Transmit Payload Data Input Interface block is accepting the LSB of each of the twenty-four time slots. 1 - The TxTSb[0]_n bit becomes the Transmit Fractional T1 Input signal (TxFrTD_n) which carries Fractional DS1 payload data into the framer. The TxTSb[1]_n bit becomes the Transmit Signaling Data Input signal (TxSig_n) which is used to insert robbed-bit signaling data into the outbound DS1 frame. The TxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-23) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. The TxTSb[3]_n bit becomes the Transmit Overhead Synchronization Pulse (TxOHSync_n) which is used to output an Overhead Synchronization Pulse that indicates the first bit of each DS1multi-frame. The TxTSClk_n will output gaped fractional DS1 clock that can be used by Terminal Equipment to clock out Fractional DS1 payload data at rising edge of the clock. Or,The TxTSClk_n pin will be a clock enable signal to Transmit Fractional DS1 Input signal (TxFrTD_n) when the un-gaped Transmit Serail Input Clock (TxSerClk_n) is used to clock in Fractional DS1 Payload Data into the framer.

When configured to operate in normal condition (that is, when the Transmit Fractional T1 Input Enable bit is equal to zero), these bits reflect the five-bit binary value of the Time Slot number (0 - 23) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. TxTSb[4] represents the MSB of the binary value and TxTSb[0] represents the LSB.

When the Transmit Fractional T1 Input Enable bit is equal to one, the TxTSb[0]_n bit becomes the Transmit Fractional T1 Input signal (TxFrTD_n). This input pin carries Fractional T1 Input data to be inserted into the outbound DS1 data stream. The Fraction T1 Input Interface allows certain time-slots of outbound DS1 data stream to have a different source other than the local Terminal Equipment. Function of the Fractional T1 Input signal will be discussed in details in later sections.

When the Transmit Fractional T1 Input Enable bit is equal to one, the TxTSb[1]_n bit becomes the Transmit Signaling Data Input signal (TxSig_n). These input pins can be used to insert robbed-bit signaling data into the outbound DS1 frame. Function of the Transmit Signaling Data Input signal will be discussed in details in later sections.

When the Transmit Fractional T1 Input Enable bit is equal to one, the TxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-23) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. MSB of the binary value is presented first and the LSB is presented last.

When the Transmit Fractional T1 Input Enable bit is equal to one, the TxTSb[3]_n bit becomes the Transmit Overhead Synchronization Pulse (TxOHSync_n). These pins can be used to output an Overhead Synchronization Pulse that indicates the first bit of each DS1multi-frame. Function of the Transmit Overhead Synchronization Output signal will be discussed in details in later sections.

The TxTSb[4]_n bit is not multiplexed.

The table below shows functionality of the TxTSb[3:0] bits when the Transmit Fractional T1 Input bit is set to different values.

TABLE 169: THE TXTSB[3:0] BITS WHEN THE TRANSMIT FRACTIONAL T1 INPUT BIT IS SET TO DIFFERENT VALUES

TRANSMIT FRACTIONAL T1 INPUT BIT = 0		TRANSMIT FRACTIONAL T1 INPUT BIT = 1	
TxTSb[0]	Output	TxFrTD	Input
TxTSb[1]	Output	TxSig	Input
TxTSb[2]	Output	TxTS	Output
TxTSb[3]	Output	TxOHSync	Output

The Transmit Time-slot Indicator Clock signal (TxTSClk_n) is a multi-function output pin. When configured to operate in normal condition (that is, when the Transmit Fractional T1 Input Enable bit is equal to zero), the TxTSClk_n is a 192KHz clock that pulses HIGH for one DS1 bit period whenever the Transmit Payload Data Input Interface block is accepting the LSB of each of the twenty-four time slots. The local Terminal Equipment should use this clock signal to sample the TxTSb[0] through TxTSb[4] bits and identify the time-slot being processed via the Transmit Section of the framer.

When the Transmit Fractional T1 Input Enable bit is equal to one, the TxTSClk_n will output gaped fractional DS1 clock at time-slots where Fractional T1 Input data is present. This clock can be used by Terminal Equipment to clock out Fractional DS1 payload data at rising edge of the clock. The framer will then input Fractional DS1 payload data using falling edge of the clock. Otherwise, this pin can be configured as a clock enable signal to Transmit Fractional DS1 Input signal (TxFrTD_n) if the framer is set accordingly. In this way, Fractional DS1 payload data is clocked into the framer using un-gaped Transmit Serail Input Clock (TxSerClk_n). A detailed discussion of the Fractional DS1 Payload Data Input Interface can be found in later sections.

Both the Transmit Time-slot Indicator Clock (TxTSClk_n) and the Transmit Time-slot Indication Bits (TxTSbb[4:0]_n) are output signals in normal 1.544Mbit/s Back-plane mode regardless of the timing source of the Transmit Section of framer.

5.1.2.1 Connect the Transmit Payload Data Input Interface block to the Local Terminal Equipment if Transmit Timing Source = TxSerClk_n

By setting the Transmit Timing Source [1:0] bits of the Clock Select Register to 01, the TxSerClk_n input signal is configured to be the timing source for the Transmit section of the framer. The Terminal Equipment should supply an external free-running clock with frequency of 1.544MHz to the TxSerClk_n input pin. The Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal are inputs to the framer.

The Transmit Single-frame Synchronization signal should pulse “High” for one DS1 bit period (648ns) at the Framing bit position of each DS1 frame. By sampling the “High” pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of a DS1 frame.

The Transmit Multi-frame Synchronization signal should pulse HIGH for one DS1 bit period (648ns) at the Framing bit position of the first frame of a DS1 multi-frame. By sampling the HIGH pulse on the Transmit Multi-frame Synchronization signal, the framer can position the beginning of a DS1 super-frame.

It is the responsibility of the Terminal Equipment to provide serial input data through the TxSer_n pin aligned with the Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal. See

Figure 47 below for how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment with the Transmit Serial clock being the timing source of transmit section.

FIGURE 47. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT WITH TXSERCLK_N AS TRANSMIT TIMING SOURCE

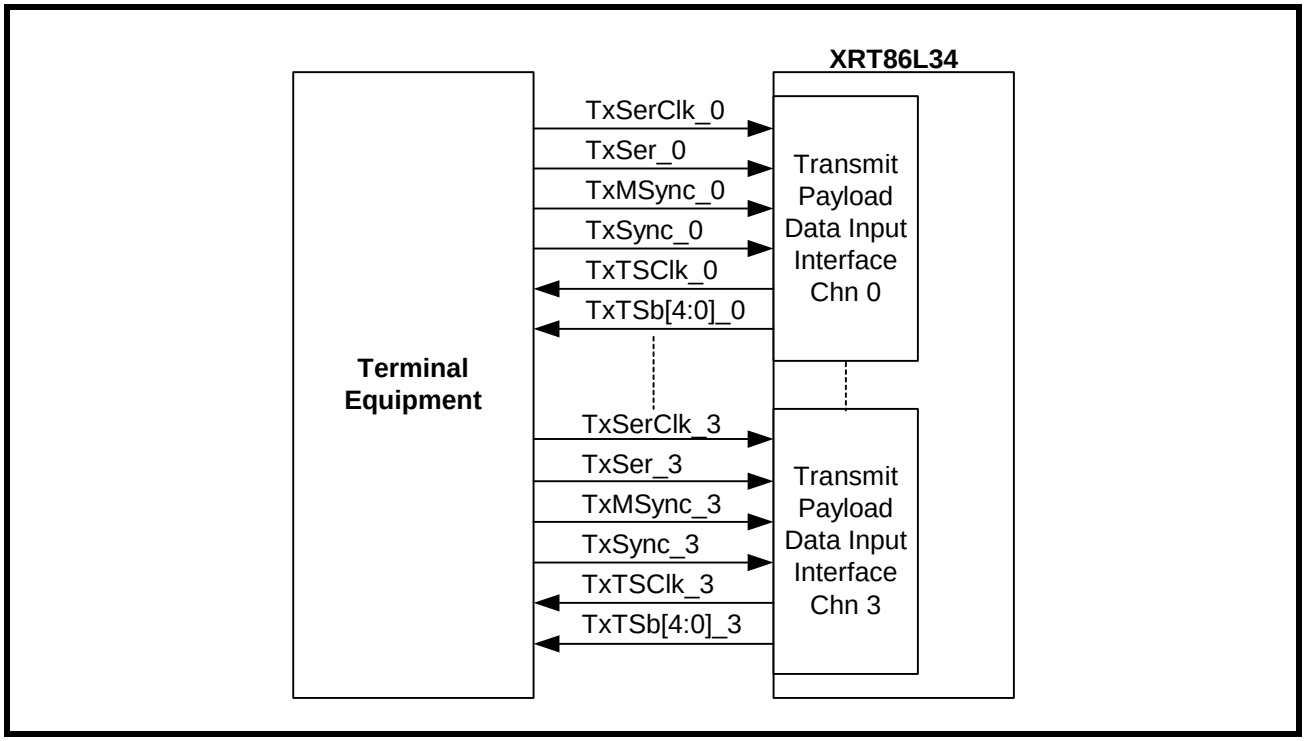
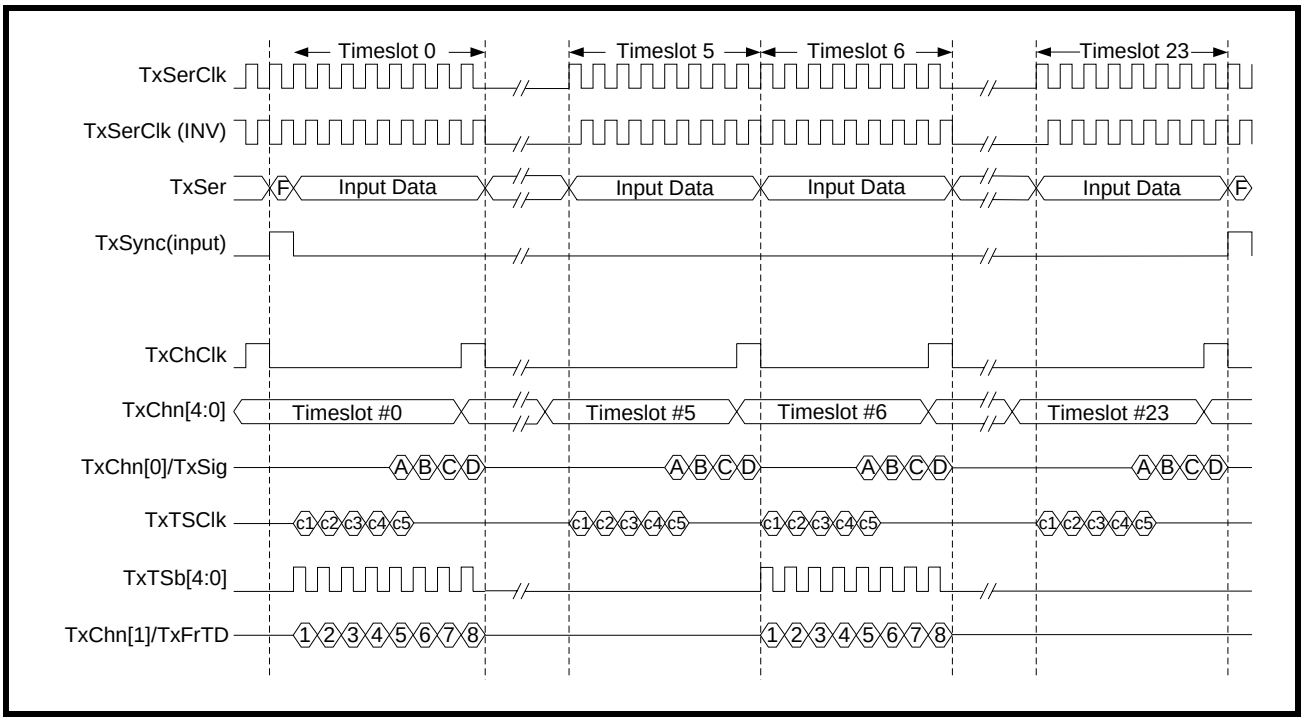


Figure 48 shows waveforms of the signals (TxSerClk_n, TxSer_n, TxSync_n, TxTSClk_n and TxTSb[4:0]_n) that connect the Transmit Payload Data Input Interface block to the local Terminal Equipment with the Transmit Serial clock being the timing source of transmit section.

FIGURE 48. WAVEFORMS OF THE SIGNALS THAT CONNECT THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WITH THE TRANSMIT SERIAL CLOCK BEING THE TIMING SOURCE OF THE TRANSMIT SECTION



5.1.2.2 Connect the Transmit Payload Data Input Interface block to the Local Terminal Equipment if the Transmit Timing Source = OSCCLK

By setting the Transmit Timing Source [1:0] bits of the Clock Select Register (CSR) to 10, the OSCCLK Driven Divided clock is configured to be the timing source for the Transmit section of the framer. A free-running clock should apply to the OSCCLK input pin with frequencies of 12.352MHz, 24.704MHz and 49.408MHz depending on the setting of OSCCLK Frequency Select [1:0] bits of the Clock Select Register (CSR).

The free-running OSCCLK is divided inside the XRT86L34 and routed to all four framers. This OSCCLK Driven Divided Clock has to be 12.352MHz in frequency. When these bits are set to 00, the framer will internally divide the incoming OSCCLK by one. Therefore, the external oscillator clock applied to the OSCCLK pin should be 12.352MHz. When these bits are set to 01, the framer will internally divide the incoming OSCCLK by two. Therefore, the external oscillator clock applied to the OSCCLK pin should be 24.704MHz. When these bits are set to 10, the framer will internally divide the incoming OSCCLK by four. Therefore, the external oscillator clock applied to the OSCCLK pin should be 49.408MHz.

The following table shows configurations of the OSCCLK Frequency Select [1:0] bits of the Clock Select Register.

CLOCK SELECT REGISTER (CSR) (ADDRESS = 0xn100H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	OSCCLK Frequency Select	R/W	**OSCCLK Frequency Select:** These two READ/WRITE bit-fields permit the user to select internal clock dividing logic of the framer depending on the frequency of incoming oscillator clock (OSCCLK). The frequency of internal clock used by the framer should be 12.352MHz. 00 - The framer will internally divide the incoming OSCCLK by one. Therefore, the external oscillator clock applied to the OSCCLK pin should be 12.352MHz. 01 - The framer will internally divide the incoming OSCCLK by two. Therefore, the external oscillator clock applied to the OSCCLK pin should be 24.704MHz. 10 - The framer will internally divide the incoming OSCCLK by four. Therefore, the external oscillator clock applied to the OSCCLK pin should be 49.408MHz.

The Transmit Serial clock signal pin (TxSerClk_n) is output from the framer. The framer outputs a 1.544MHz clock through this pin to the local Terminal Equipment. The Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal are also automatically configured to be output signals.

The Transmit Single-frame Synchronization signal should pulse HIGH for one DS1 bit period (648ns) at the last bit position of each DS1 frame. By triggering on the HIGH pulse on the Transmit Single-frame Synchronization signal, the local Terminal Equipment can identify the end of a DS1 frame and should start inserting payload data of the next DS1 frame to the framer.

The Transmit Multi-frame Synchronization signal should pulse HIGH for one DS1 bit period (648ns) at the last bit position of the last frame of a DS1 multi-frame. By triggering on the HIGH pulse on the Transmit Multi-frame Synchronization signal, the local Terminal Equipment can identify the end of a DS1 super-frame and should start inserting payload data of the next DS1 multi-frame into the framer.

See Figure 49 for how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment with the OSCCLK Driven Divided clock as the timing source of transmit section.

FIGURE 49. INTERFACING XRT86L34 TO THE LOCAL TERMINAL EQUIPMENT WITH THE OSCCLK DRIVEN DIVIDED CLOCK AS TRANSMIT TIMING SOURCE

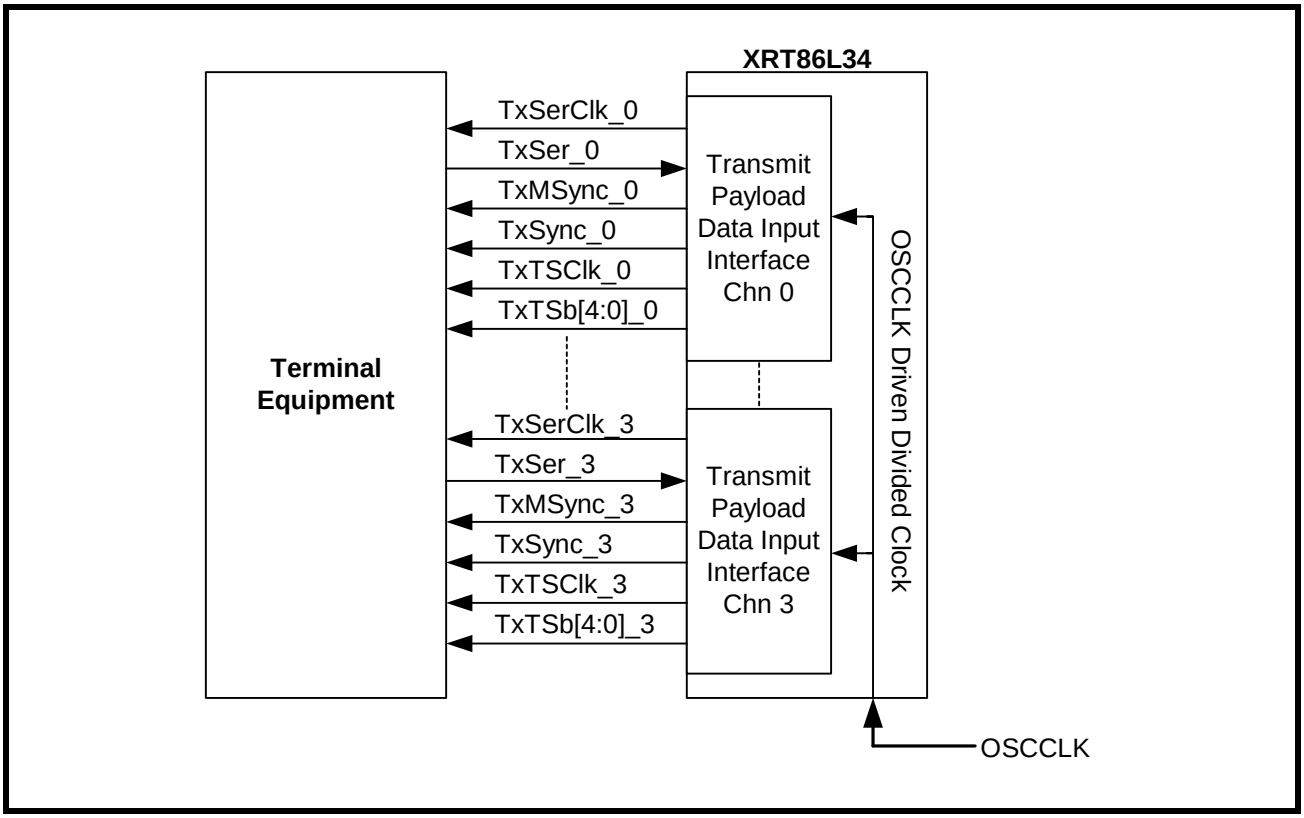
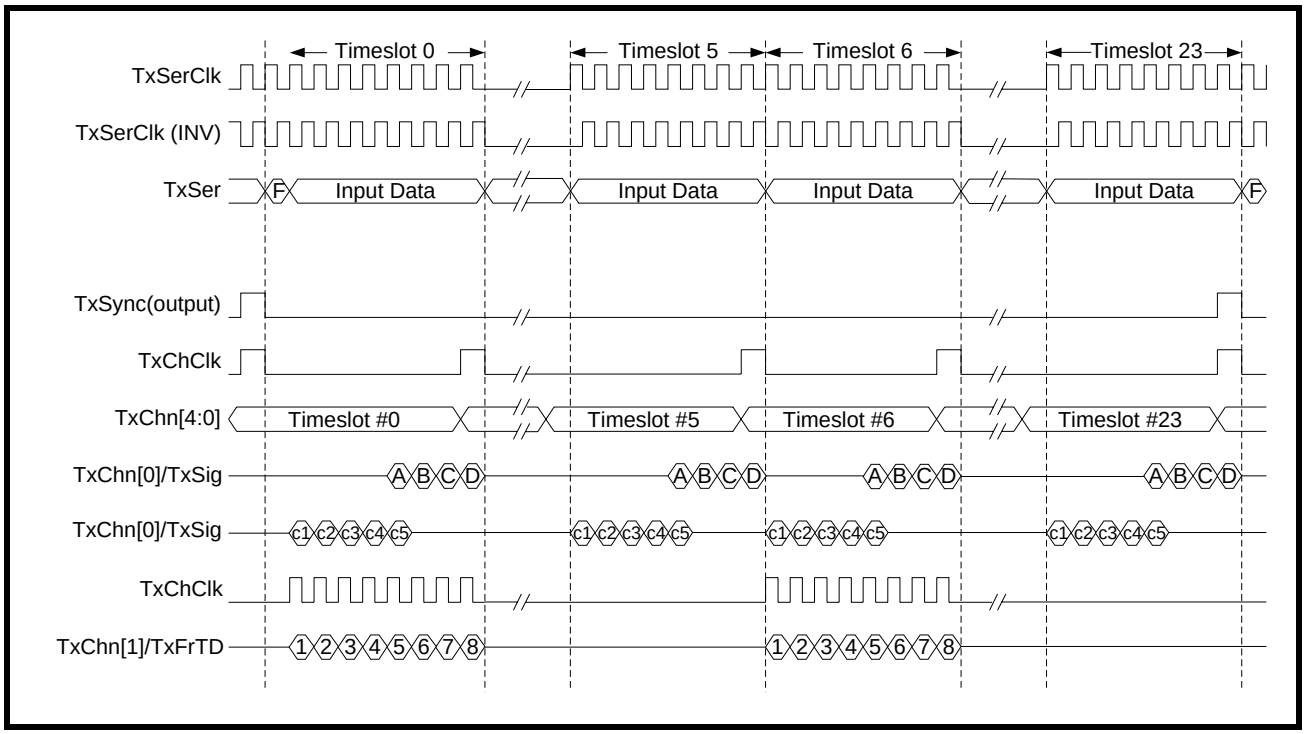


Figure 50 shows waveforms of the signals (TxSerClk_n, TxSer_n, TxSync_n, TxTSClk_n and TxTSb[4:0]_n) that connect the Transmit Payload Data Input Interface block to the local Terminal Equipment with the OSCCLK Driven Divided clock as the timing source of transmit section.

FIGURE 50. WAVEFORMS OF THE SIGNALS CONNECTING THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WITH THE OSCCLK DRIVEN DIVIDED CLOCK AS THE TIMING SOURCE OF THE TRANSMIT SECTION



5.1.2.3 Connect the Transmit Payload Data Input Interface block to the Local Terminal Equipment for Loop-timing applications

If the Transmit Timing Source [1:0] bits of the Clock Select Register are set to 00 or 11, the Recovered Receive Line Clock is configured to be the timing source for the Transmit section of the framer. This is also known as the Loop-timing mode.

If the Clock Loss Detection Enable bit of the Clock Select Register is set to one, and if the Recovered Receive Line Clock from the LIU is lost, the framer will automatically begin to use the OSCCLK Driven Divided clock as transmit timing source until the LIU is able to regain clock recovery.

The following table shows configuration of the Clock Loss Detection Enable bit of the Clock Select Register (CSR).

CLOCK SELECT REGISTER (CSR) (ADDRESS = 0xn100H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Clock Loss Detection Enable	R/W	**Clock Loss Detection Enable:** This READ/WRITE bit-field permits the user to enable the Clock Loss Detection logic for the framer when the Recovered Receive Line Clock is used as transmit timing source of the framer. 0 - The framer disables the Clock Loss Detection logic. 1 - The framer enables the Clock Loss Detection logic. If the Recovered Receive Line Clock is used as transmit timing source of the framer, and if clock recovered from the LIU is lost, the framer can detect loss of the Recovered Receive Line Clock. Upon detecting of this occurrence, the framer will automatically begin to use the OSCCLK Driven Divided clock as transmit timing source until the LIU is able to regain clock recovery. ***NOTE:*** *This bit-field is ignored if the TxSerClk or the OSCCLK Driven Divided Clock is chosen to be the timing source of Transmit Section of the framer.*

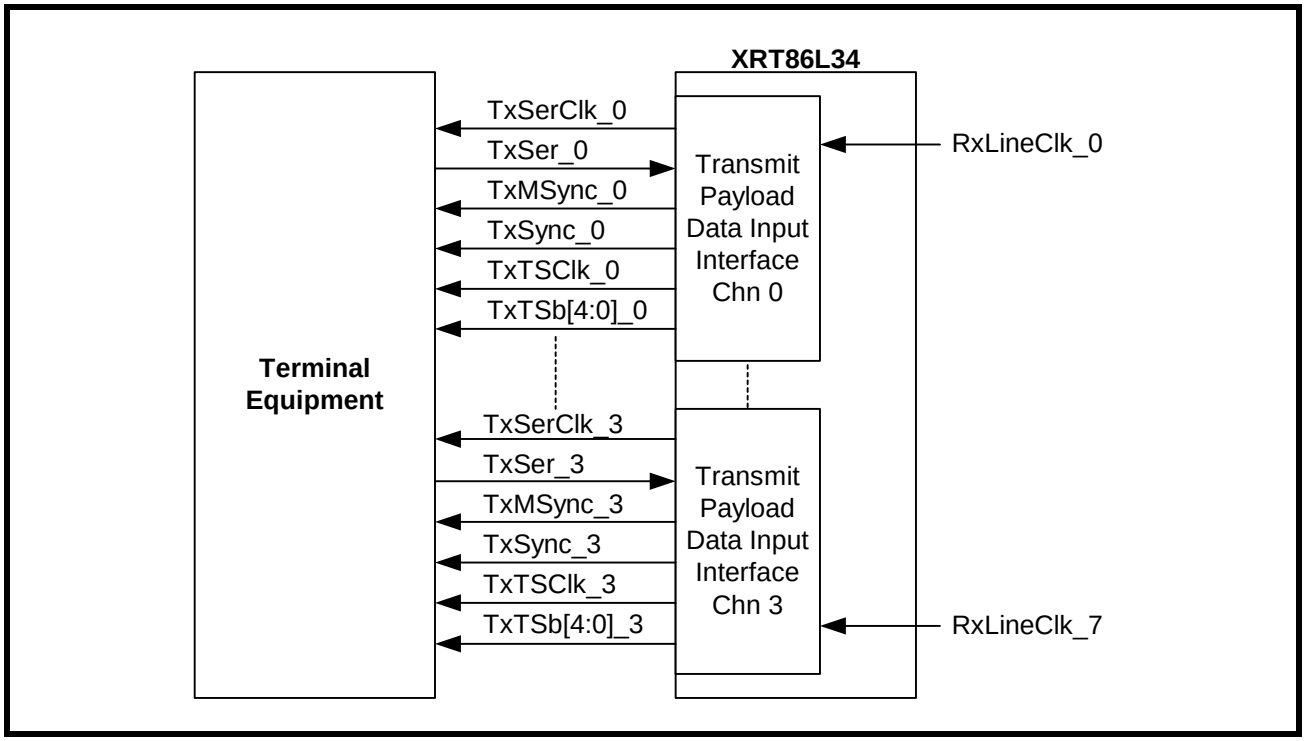
The Transmit Serial Clock signal pin (TxSerClk_n) is output from the framer. The XRT86L34 routes the Recovered Receive Line Clock internally across the framer and output through the Transmit Serial Clock signal pin to the local Terminal Equipment. The Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal are automatically configured to be output signals.

The Transmit Single-frame Synchronization signal should pulse HIGH for one DS1 bit period (648ns) at the last bit position of each DS1 frame. By triggering on the HIGH pulse on the Transmit Single-frame Synchronization signal, the local Terminal Equipment can identify the end of a DS1 frame and should start inserting payload data of the next DS1 frame to the framer.

The Transmit Multi-frame Synchronization signal should pulse HIGH for one DS1 bit period (648ns) at the last bit position of the last frame of a DS1 multi-frame. By triggering on the HIGH pulse on the Transmit Multi-frame Synchronization signal, the local Terminal Equipment can identify the end of a DS1 super-frame and should start inserting payload data of the next DS1 multi-frame into the framer.

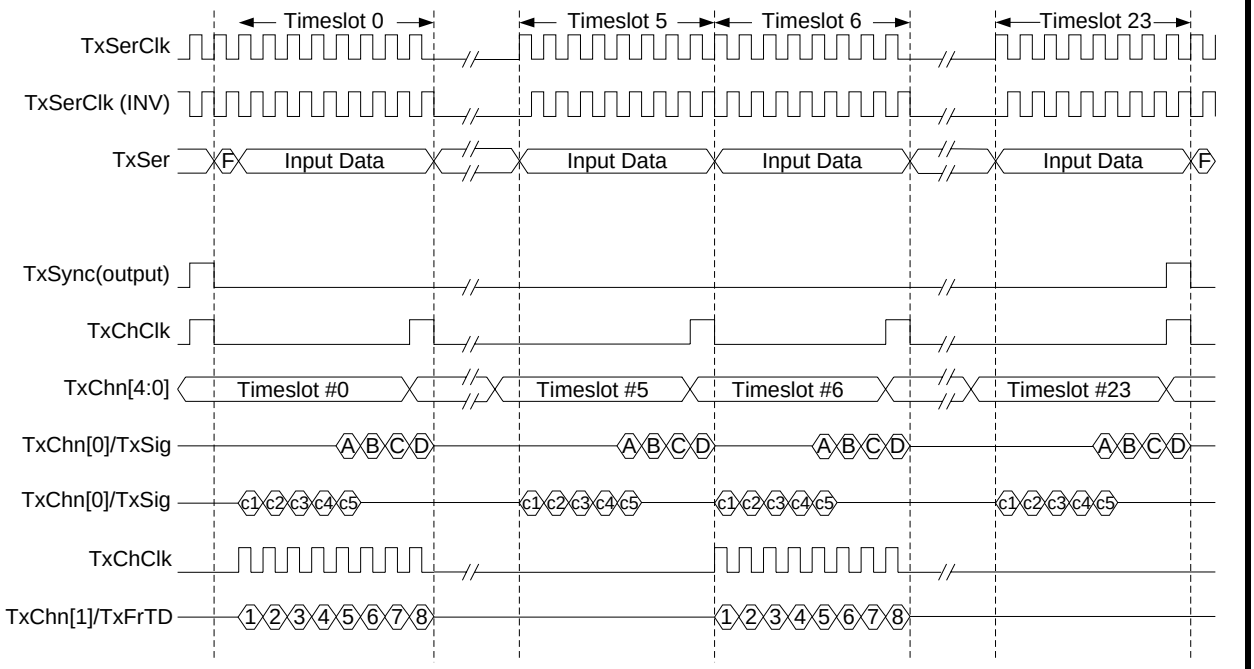
See Figure 51 for how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment with the Recovered Receive Line Clock being the timing source of transmit section.

FIGURE 51. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT WITH RECOVERED RECEIVE LINE CLOCK AS TRANSMIT TIMING SOURCE



The following Figure 52 shows waveforms of the signals (TxSerClk_n, TxSer_n, TxSync_n, TxTSClk_n and TxTSb[4:0]_n) that connecting the Transmit Payload Data Input Interface block to the local Terminal Equipment with the Recovered Receive Line Clock being the timing source of transmit section.

FIGURE 52. WAVEFORMS OF THE SIGNALS CONNECTING THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WITH THE RECOVERED RECEIVE LINE CLOCK BEING THE TIMING SOURCE OF THE TRANSMIT SECTION



5.2 TRANSMIT HIGH-SPEED BACK-PLANE INTERFACE

The High-speed Back-plane Interface supports payload data to be taken from or presented to the Terminal Equipment at a rate higher than 1.544Mbit/s. In DS1 mode, supported High-speed data rates are MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 12.352Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s. The Transmit Multiplex Enable bit and the Transmit Interface Mode Select [1:0] bits of the Transmit Interface Control Register (TICR) determine the Transmit Back-plane Interface data rate.

The following table shows configurations of the Transmit Multiplex Enable bit and the Transmit Interface Mode Select [1:0] bits of the Transmit Interface Control Register (TICR).

TRANSMIT INTERFACE CONTROL REGISTER (TICR) (ADDRESS = 0xn120H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Transmit Multiplex Enable	R/W	0 - The Transmit Back-plane Interface block is configured to non-channel-multiplexed mode. 1 - The Transmit Back-plane Interface block is configured to channel-multiplexed mode
1-0	Transmit Interface Mode Select	R/W	When combined with the Transmit Multiplex Enable bit, these bits determine the Transmit Back-plane Interface data rate.

The table below shows the combinations of Transmit Multiplex Enable bit and Transmit Interface Mode Select [1:0] bits and the resulting Transmit Back-plane Interface data rates.

TABLE 170: TRANSMIT MULTIPLEX ENABLE BIT AND TRANSMIT INTERFACE MODE SELECT [1:0] BITS WITH THE RESULTING TRANSMIT BACK-PLANE INTERFACE DATA RATES

TRANSMIT MULTIPLEX ENABLE BIT	TRANSMIT INTERFACE MODE SELECT BIT 1	TRANSMIT INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE
0	0	0	1.544Mbit/s
0	0	1	MVIP 2.048Mbit/s
0	1	0	4.096Mbit/s
0	1	1	8.192Mbit/s
1	0	0	Multiplexed 12.352Mbit/s
1	0	1	Bit Multiplexed 16.384Mbit/s
1	1	0	HMVIP 16.384Mbit/s
1	1	1	H.100 16.384Mbit/s

When the Transmit Multiplex Enable bit is set to zero, the framer is configured in non-channel-multiplexed mode. The possible data rates are 1.544Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s. In non-channel-multiplexed mode, payload data of each channel are taken from the Terminal Equipment separately. Each channel uses its own Transmit Serial Clock, Transmit Serial Data, Transmit Single-frame Synchronization signal and Transmit Multi-frame Synchronization signal as interface between the framer and the Terminal Equipment. Section 1.1.2.1, 1.1.2.2 and 1.1.2.3 provide details on how to connect the Transmit Payload Data Interface block with the Terminal Equipment when the Back-plane interface data rate is 1.544Mbit/s.

When the Back-plane interface data rate is MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s, the Transmit Serial Clock, Transmit Serial Data, Transmit Single-frame Synchronization signal and Transmit Multi-frame Synchronization signal are all configured as inputs. The Transmit Serial Clock is always an input clock with frequency of 1.544 MHz for all data rates. The TxMSync_n signal is configured as the Transmit Input Clock with frequencies of 2.048 MHz, 4.096 MHz and 8.192 MHz respectively. It serves as the primary clock source for the High-speed Back-plane Interface.

The table below summaries the clock frequencies of TxSerClk_n and TxInClk_n inputs when the framer is operating in non-multiplexed High-speed Back-plane mode.

TRANSMIT MULTIPLEX ENABLE BIT = 0

TRANSMIT INTERFACE MODE SELECT BIT 1	TRANSMIT INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE	TXSERCLK	TXMSYNC/TXINCLK
0	0	1.544Mbit/s	1.544 MHz	-
0	1	MVIP 2.048Mbit/s	1.544 MHz	2.048 MHz
1	0	4.096Mbit/s	1.544 MHz	4.096 MHz
1	1	8.192Mbit/s	1.544 MHz	8.192 MHz

When the Transmit Multiplex Enable bit is set to one, the framer is configured in channel-multiplexed mode. The possible data rates are multiplexed 12.352Mbit/s, bit-multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s and H.100 16.384Mbit/s. In channel-multiplexed mode, every four channels share the Transmit Serial Data and Transmit Single-frame Synchronization signal of one channel as interface between the framer and the local Terminal Equipment. The TxMSync_n signal of one channel is configured as the Transmit Input Clock with frequencies of 12.352 MHz or 16.384. It serves as the primary clock source for the High-speed Back-plane Interface.

Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4. The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH at the beginning of the frame with data from Channel 0-3 multiplexed together. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH at the beginning of the frame with data from Channel 4-7 multiplexed together. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse. Additionally, each channel requires the local Terminal Equipment to provide a free-running 1.544 MHz clock into the Transmit Serial Clock input.

The table below summaries the clock frequencies of TxSerClk_n and TxInClk_n inputs when the framer is operating in multiplexed High-speed Back-plane mode.

TRANSMIT MULTIPLEX ENABLE BIT = 1

TRANSMIT INTERFACE MODE SELECT BIT 1	TRANSMIT INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE	TXSERCLK	TXMSYNC/TXCLK
0	0	Multiplexed 12.352Mbit/s	1.544 MHz	12.352 MHz
0	1	Bit-multiplexed 16.384Mbit/s	1.544 MHz	16.384 MHz
1	0	HMVIP 16.384Mbit/s	1.544 MHz	16.384 MHz
1	1	H.100 16.384Mbit/s	1.544 MHz	16.384 MHz

The Transmit Serial Clock is always running at 1.544MHz for all the High-speed Back-plane Interface modes. It is automatically the timing source of the Transmit Section of the framer in High-speed Back-plane Interface mode.

The Transmit Single-frame Synchronization signal should pulse HIGH or LOW for one bit period at the Framing bit position of each DS1 frame. Length of the bit period depends on data rate of the High-speed Back-plane Interface. The Transmit Synchronization Pulse Low bit of the Transmit Interface Control Register (TICR) determines whether the Transmit Single-frame Synchronization signal is HIGH active or LOW active.

The table below shows configurations of the Transmit Synchronization Pulse LOW bit of the Transmit Interface Control Register (TICR).

TRANSMIT INTERFACE CONTROL REGISTER (TICR) (ADDRESS = 0xn120H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Transmit Synchronization Pulse LOW	R/W	0 - The Transmit Single-frame Synchronization signal will pulse HIGH indicating the beginning of a DS1 frame when the High-speed Back-plane Interface is running at a mode other than the 1.544Mbit/s. 1 - The Transmit Single-frame Synchronization signal will pulse LOW indicating the beginning of a DS1 frame when the High-speed Back-plane Interface is running at a mode other than the 1.544Mbit/s.

Throughout the discussion of this datasheet, we assume that the Transmit Single-frame Synchronization signal pulses HIGH unless stated otherwise.

The TxMSync_n signal, which is a multiplexed I/O pin, no longer functions as the Transmit Multi-frame Synchronization Signal. Indeed, it becomes the Transmit Input Clock signal (TxInClk) of the High-speed Back-plane Interface of the framer. The local Terminal Equipment should provide a free-running clock with the same frequency as the High-speed Back-plane Interface to this input pin.

The following sections discuss details of how to operate the framer in different Back-plane interface speed mode and how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment.

5.2.0.1 T1 Transmit Input Interface - MVIP 2.048 MHz

When the Transmit Multiplex Enable bit is set to zero and the Transmit Interface Mode Select [1:0] bits are set to 01, the Transmit Back-plane interface of framer is running at a data rate of 2.048Mbit/s.

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane interface is accepting data through TxSer_n at an E1 equivalent data rate of 2.048Mbit/s. The local Terminal Equipment supplies a free-running 2.048MHz clock to he Transmit Input Clock pin of the framer. The local Terminal Equipment also provides synchronized payload data at rising edge of the clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the Transmit Input Clock. The local Terminal Equipment should pump in data grouped in 256-bit frame 8000 times every second. Each frame consists of thirty-two octets as in E1. The local Terminal Equipment maps a 193-bit T1 frame into this 256-bit format as described below:

1. The Framing (F-bit) is mapped into MSB of the first E1 Time-slot. The local Terminal Equipment will stuff the rest seven bits of the first octet with "don't care" bits that would be ignored by the framer.
2. Payload data of T1 Time-slot 0, 1 and 2 are mapped into E1 Time-slot 1, 2 and 3.
3. The local Terminal Equipment will stuff E1 Time-slot 4 with eight "don't care" bits that would be ignored by the framer.
4. Following the same rules of Step 2 and 3, the local Terminal Equipment maps every three time-slots of T1 payload data into four E1 time-slots.

The mapping of T1 frame into E1 framing format is shown in the table below.

TABLE 171: THE MAPPING OF T1 FRAME INTO E1 FRAMING FORMAT

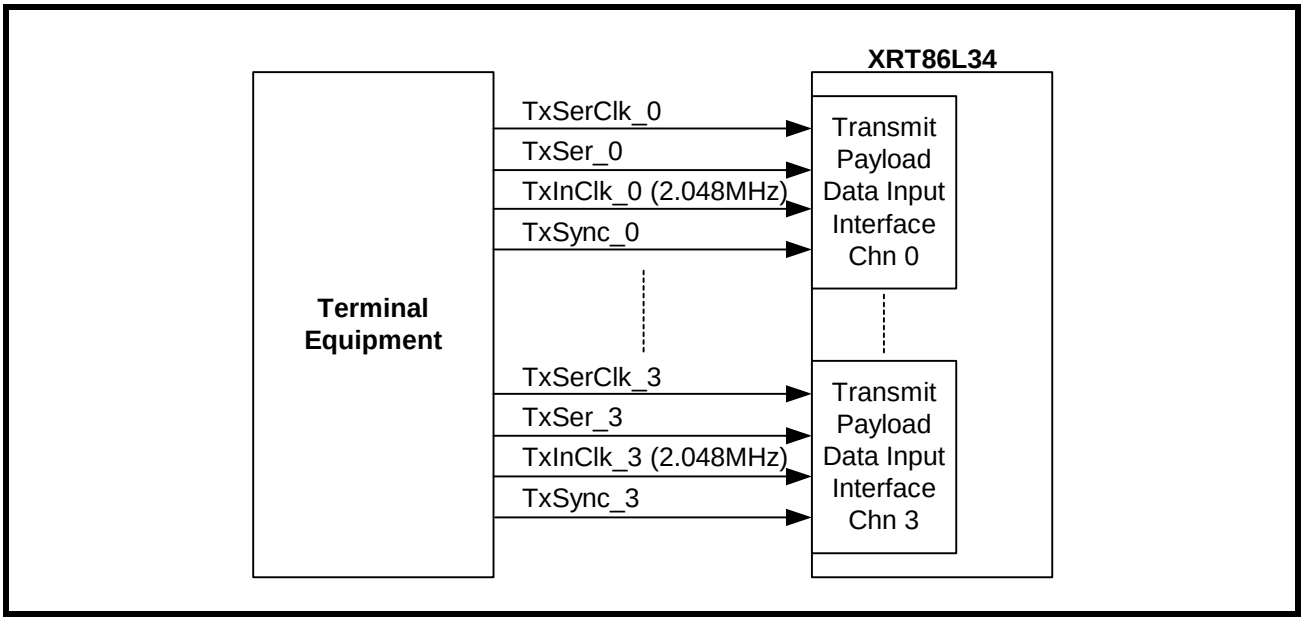
T1	F-Bit	TS0	TS1	TS2	Don't Care Bits	TS3	TS4	TS5
E1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7
T1	Don't Care Bits	TS6	TS7	TS8	Don't Care Bits	TS9	TS10	TS11
E1	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15
T1	Don't Care Bits	TS12	TS13	TS14	Don't Care Bits	TS15	TS16	TS17
E1	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23
T1	Don't Care Bits	TS18	TS19	TS20	Don't Care Bits	TS21	TS22	TS23
E1	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31

The Transmit Single-frame Synchronization input signal (TxSync_n) should pulse HIGH at the beginning (F-bit position) of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of a DS1 frame. It is responsibility of the local Terminal Equipment to align the Transmit Single-frame Synchronization signal with serial data stream going into the framer.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are then processed by the framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

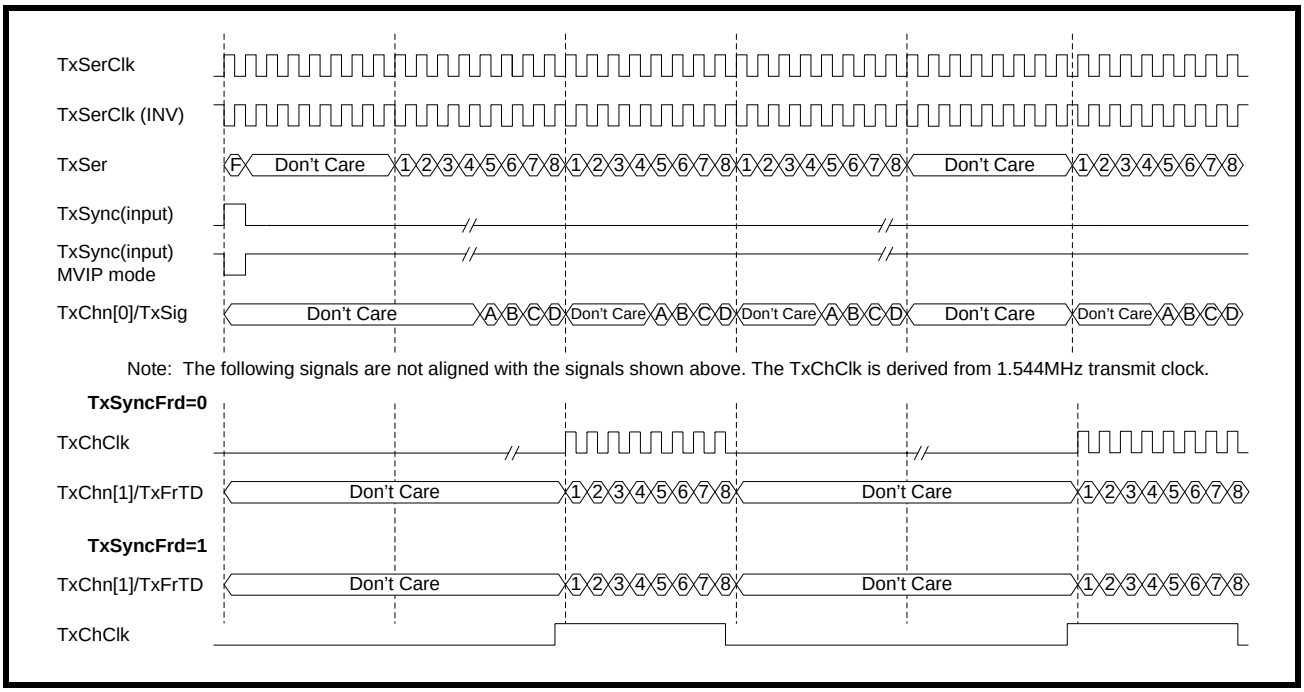
See Figure 53 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in MVIP 2.048Mbit/s mode.

FIGURE 53. INTERFACING XRT86L34 TO THE LOCAL TERMINAL EQUIPMENT USING MVIP 2.048MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at MVIP 2.048Mbit/s mode is shown in Figure 54.

FIGURE 54. TIMING DIAGRAM OF THE INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT MVIP 2.048MBIT/S MODE



5.2.0.2 T1 Transmit Input Interface - 4.096 MHz

This interface mode is the same as running at 2.048 MHz. The only difference is that the Transmit Input Clock runs two times faster at 4.096 MHz.

When the Transmit Multiplex Enable bit is set to zero and the Transmit Interface Mode Select [1:0] bits are set to 10, the Transmit Back-plane interface of framer is running at a clock rate of 4.096MHz.

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane interface is still accepting data through TxSer_n at an E1 equivalent data rate of 2.048Mbit/s. However, the local Terminal Equipment supplies a free-running 4.096MHz clock to the Transmit Input Clock pin of the framer. The local Terminal Equipment provides synchronized payload data at every other rising edge of the Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at every other falling edge of the clock. The local Terminal Equipment should pump in data grouped in 256-bit frame 8000 times every second. Each frame consists of thirty-two octets as in E1. The local Terminal Equipment maps a 193-bit T1 frame into this 256-bit format as described below:

1. The Framing (F-bit) is mapped into MSB of the first E1 Time-slot. The local Terminal Equipment will stuff the rest seven bits of the first octet with "don't care" bits that would be ignored by the framer.
2. Payload data of T1 Time-slot 0, 1 and 2 are mapped into E1 Time-slot 1, 2 and 3.
3. The local Terminal Equipment will stuff E1 Time-slot 4 with eight "don't care" bits that would be ignored by the framer.
4. Following the same rules of Step 2 and 3, the local Terminal Equipment maps every three time-slots of T1 payload data into four E1 time-slots.

The mapping of T1 frame into E1 framing format is shown in the table below.

TABLE 172: THE MAPPING OF T1 FRAME INTO E1 FRAMING FORMAT

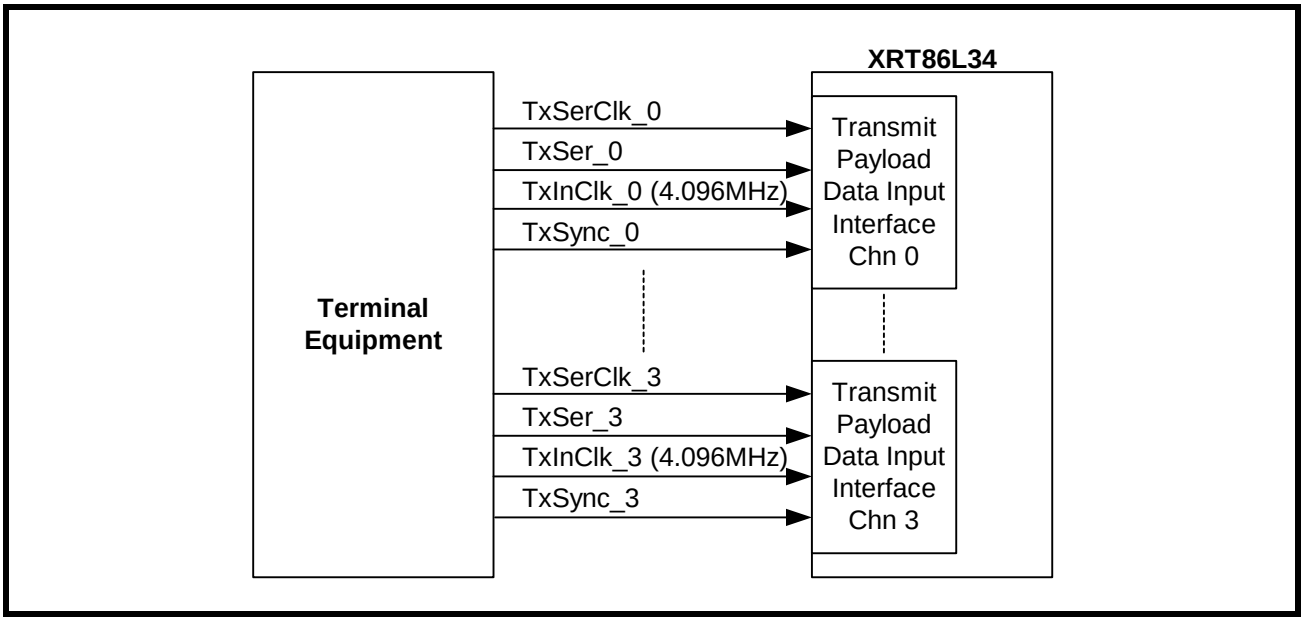
T1	F-BIT	TS0	TS1	TS2	DON'T CARE BITS	TS3	TS4	TS5
E1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7
T1	Don't Care Bits	TS6	TS7	TS8	Don't Care Bits	TS9	TS10	TS11
E1	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15
T1	Don't Care Bits	TS12	TS13	TS14	Don't Care Bits	TS15	TS16	TS17
E1	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23
T1	Don't Care Bits	TS18	TS19	TS20	Don't Care Bits	TS21	TS22	TS23
E1	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31

The Transmit Single-frame Synchronization input signal (TxSync_n) should pulse HIGH at the beginning (F-bit position) of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of a DS1 frame. It is responsibility of the local Terminal Equipment to align the Transmit Single-frame Synchronization signal with serial data stream going into the framer.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are then processed by the framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

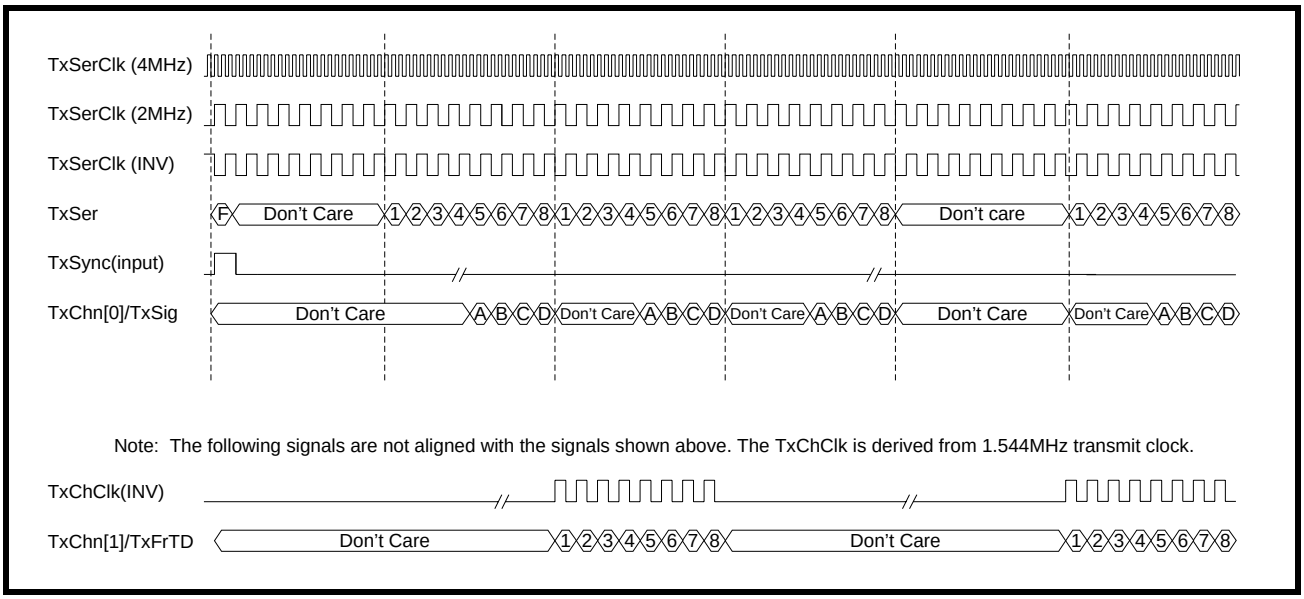
See Figure 55 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in MVIP 2.048Mbit/s mode.

FIGURE 55. INTERFACING XRT86L34 TO THE LOCAL TERMINAL EQUIPMENT USING 4.096MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at 4.096Mbit/s mode is shown in Figure 56

FIGURE 56. TIMING DIAGRAM OF THE INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 4.096MBIT/S MODE



5.2.0.3 T1 Transmit Input Interface - 8.192 MHz

This interface mode is the same as running at 2.048 MHz. The only difference is that the Transmit Input Clock runs four times faster at 8.192MHz.

When the Transmit Multiplex Enable bit is set to zero and the Transmit Interface Mode Select [1:0] bits are set to 11, the Transmit Back-plane interface of framer is running at a clock rate of 8.192MHz.

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane interface is still accepting data through TxSer_n at an E1 equivalent data rate of 2.048Mbit/s. However, the local Terminal Equipment supplies a free-running 8.192MHz clock to the Transmit Input Clock pin of the framer. The local Terminal Equipment provides synchronized payload data at every other four rising edge of the Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at every other four falling edge of the clock. The local Terminal Equipment should pump in data grouped in 256-bit frame 8000 times every second. Each frame consists of thirty-two octets as in E1. The local Terminal Equipment maps a 193-bit T1 frame into this 256-bit format as described below:

1. The Framing (F-bit) is mapped into MSB of the first E1 Time-slot. The local Terminal Equipment will stuff the rest seven bits of the first octet with "don't care" bits that would be ignored by the framer.
2. Payload data of T1 Time-slot 0, 1 and 2 are mapped into E1 Time-slot 1, 2 and 3.
3. The local Terminal Equipment will stuff E1 Time-slot 4 with eight "don't care" bits that would be ignored by the framer.
4. Following the same rules of Step 2 and 3, the local Terminal Equipment maps every three time-slots of T1 payload data into four E1 time-slots.

The mapping of T1 frame into E1 framing format is shown in the table below.

TABLE 173: THE MAPPING OF T1 FRAME INTO E1 FRAMING FORMAT

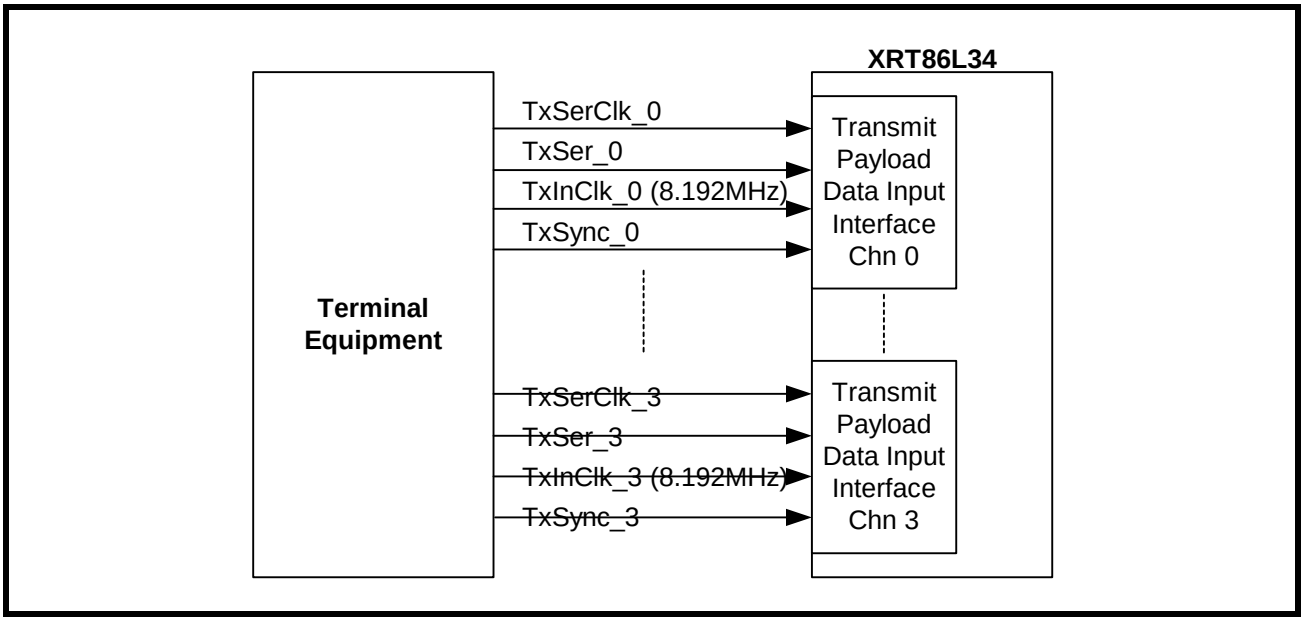
T1	F-Bit	TS0	TS1	TS2	Don't Care Bits	TS3	TS4	TS5
E1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7
T1	Don't Care Bits	TS6	TS7	TS8	Don't Care Bits	TS9	TS10	TS11
E1	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15
T1	Don't Care Bits	TS12	TS13	TS14	Don't Care Bits	TS15	TS16	TS17
E1	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23
T1	Don't Care Bits	TS18	TS19	TS20	Don't Care Bits	TS21	TS22	TS23
E1	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31

The Transmit Single-frame Synchronization input signal (TxSync_n) should pulse HIGH at the beginning (F-bit position) of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of a DS1 frame. It is responsibility of the local Terminal Equipment to align the Transmit Single-frame Synchronization signal with serial data stream going into the framer.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are then processed by the framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

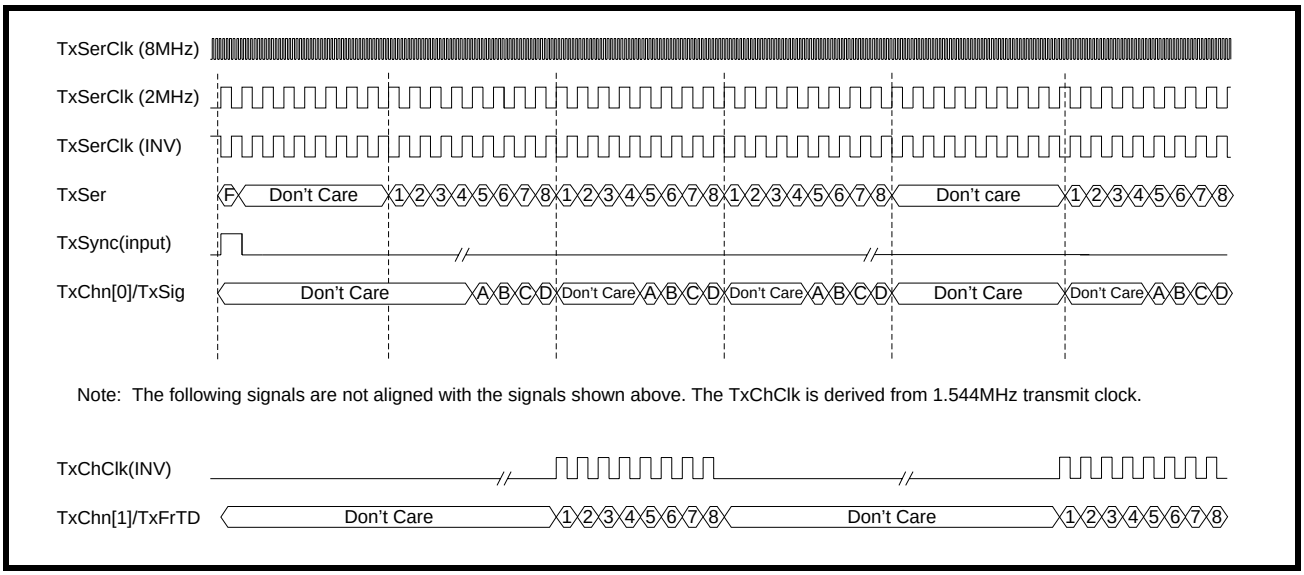
See Figure 57 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in MVIP 2.048Mbit/s mode.

FIGURE 57. INTERFACING XRT86L34 TO THE LOCAL TERMINAL EQUIPMENT USING 8.192MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at 8.192Mbit/s mode is shown in Figure 58.

FIGURE 58. TIMING DIAGRAM OF THE INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 8.192MBIT/S MODE



5.2.0.4 T1 Transmit Input Interface - Multiplexed 12.352Mbit/s

When the Transmit Multiplex Enable bit is set to one and the Transmit Interface Mode Select [1:0] bits are set to 00, the Transmit Back-plane interface of framer is running at a clock rate of 12.352MHz.

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)

- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane Interface is accepting data through TxSer_0 or TxSer_4 pins at 12.352Mbit/s. The local Terminal Equipment multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4.

Free-running clocks of 12.352MHz is supplied to the Transmit Input Clock pin of Channel 0 and Channel 4 of the framer. The local Terminal Equipment provides multiplexed payload data at rising edge of this Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the clock.

The local Terminal Equipment maps four 1.544Mbit/s DS1 data streams into this 12.352Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

FIRST OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

F_X: F-bit of Channel X

2. Payload data of four channels are repeated and grouped together in a bit-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the first payload bit of Timeslot 0 of Channel 1 and 2. The first payload bit of Timeslot 0 of Channel 3 is sent last. After the first bits of Timeslot 0 of all four channels are sent, it comes the second bit of Timeslot 0 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 12.352Mbit/s data stream.

SECOND OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	1_1	1_1	1_2	1_2	1_2	1_3

THIRD OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
2_0	2_0	2_1	2_1	2_2	2_2	2_3	2_3

X_Y: The Xth payload bit of Channel Y

3. The local Terminal Equipment also multiplexed signaling bits with payload bits and sent them together through the 12.352Mbit/s data stream. When the Terminal Equipment is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Simi-

larly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 12.352Mbit/s data stream.

SIXTH OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	5_1	A_1	5_2	A_2	5_3	A_3

SEVENTH OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
6_0	B_0	6_1	B_1	6_2	B_2	6_3	B_3

EIGHTH OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
7_0	C_0	7_1	C_1	7_2	C_2	7_3	C_3

NINETH OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
8_0	D_0	8_1	D_1	8_2	D_2	8_3	D_3

X_Y: The Xth payload bit of Channel Y

A_Y: The signaling bit A of Channel Y

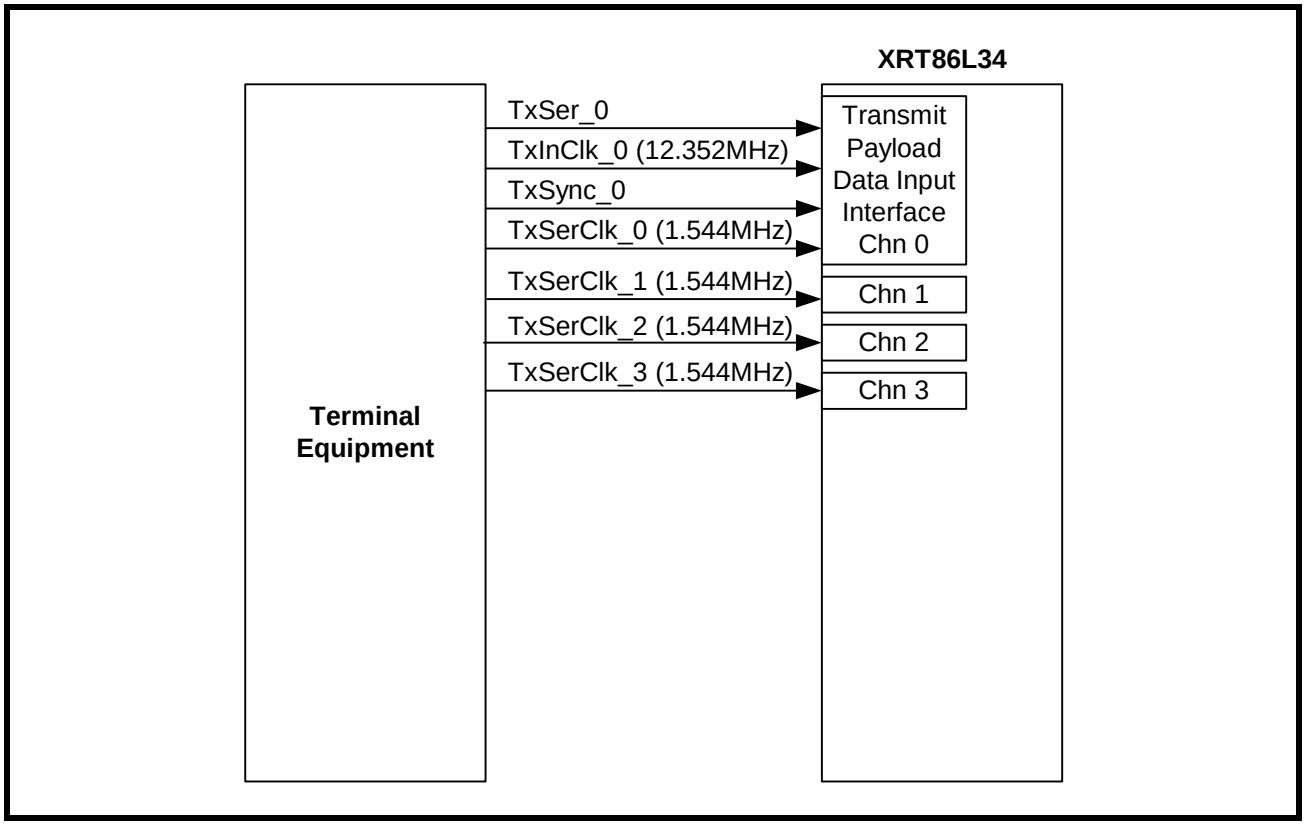
4. Following the same rules of Step 2 and 3, the local Terminal Equipment maps the payload data and signaling data of four channels into a 12.352Mbit/s data stream.

The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH for one clock cycle at the first bit position (F-bit of channel 0) of the data stream with data from Channel 0-3 multiplexed together. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH for one clock cycle at the first bit position (F-bit of Channel 4) of the data stream with data from Channel 4-7 multiplexed together. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed DS1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT86L34 and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

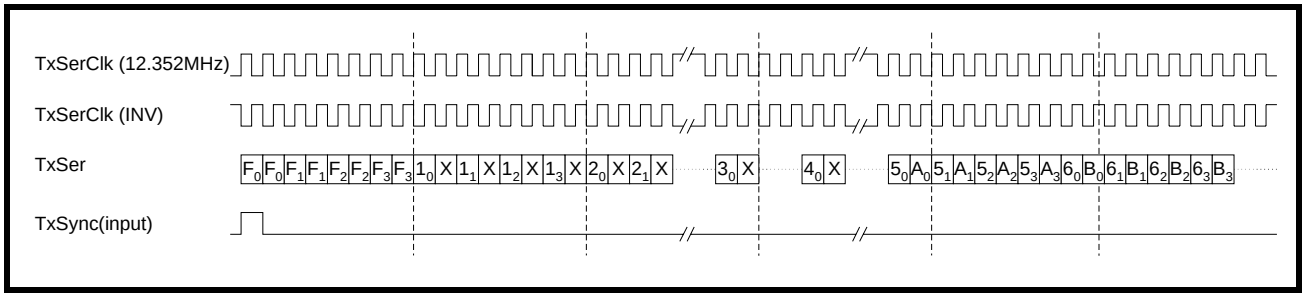
See Figure 59 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in 12.352Mbit/s mode.

FIGURE 59. INTERFACING XRT86L34 TO THE LOCAL TERMINAL EQUIPMENT USING BIT-MULTIPLEXED 12.352MBIT/S DATA BUS



The Input signal timing is shown in Figure 60 below when the framer is running at 12.352Mbit/s mode.

FIGURE 60. TIMING DIAGRAM OF THE INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 12.352MBIT/S MODE



5.2.0.5 T1 Transmit Input Interface - Bit-Multiplexed 16.384Mbit/s

When the Transmit Multiplex Enable bit is set to one and the Transmit Interface Mode Select [1:0] bits are set to 01, the Transmit Back-plane interface of framer is running at a clock rate of 16.384MHz.

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)

- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane Interface is accepting data through TxSer_0 or TxSer_4 pins at 16.384Mbit/s. The local Terminal Equipment multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz is supplied to the Transmit Input Clock pin of Channel 0 and Channel 4 of the framer. The local Terminal Equipment provides multiplexed payload data at rising edge of this Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the clock.

The local Terminal Equipment maps four 1.544Mbit/s DS1 data streams into this 16.384Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

F_X: F-bit of Channel X

2. After the first octet of data is sent, the local Terminal Equipment should insert seven octets (fifty-six bits) of "don't care" data into the outgoing data stream.
3. Payload data of four channels are repeated and grouped together in a bit-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the first payload bit of Timeslot 0 of Channel 1 and 2. The first payload bit of Timeslot 0 of Channel 3 is sent last. After the first bits of Timeslot 0 of all four channels are sent, it comes the second bit of Timeslot 0 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

NINETH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	1_1	1_1	1_2	1_2	1_2	1_3

TENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
2_0	2_0	2_1	2_1	2_2	2_2	2_3	2_3

X_Y: The Xth payload bit of Channel Y

4. The local Terminal Equipment also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream. When the Terminal Equipment is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

THIRTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	5_1	A_1	5_2	A_2	5_3	A_3

FOURTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
6_0	B_0	6_1	B_1	6_2	B_2	6_3	B_3

FIFTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
7_0	C_0	7_1	C_1	7_2	C_2	7_3	C_3

SIXTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
8_0	D_0	8_1	D_1	8_2	D_2	8_3	D_3

X_Y: The Xth payload bit of Channel Y

A_Y: The signaling bit A of Channel Y

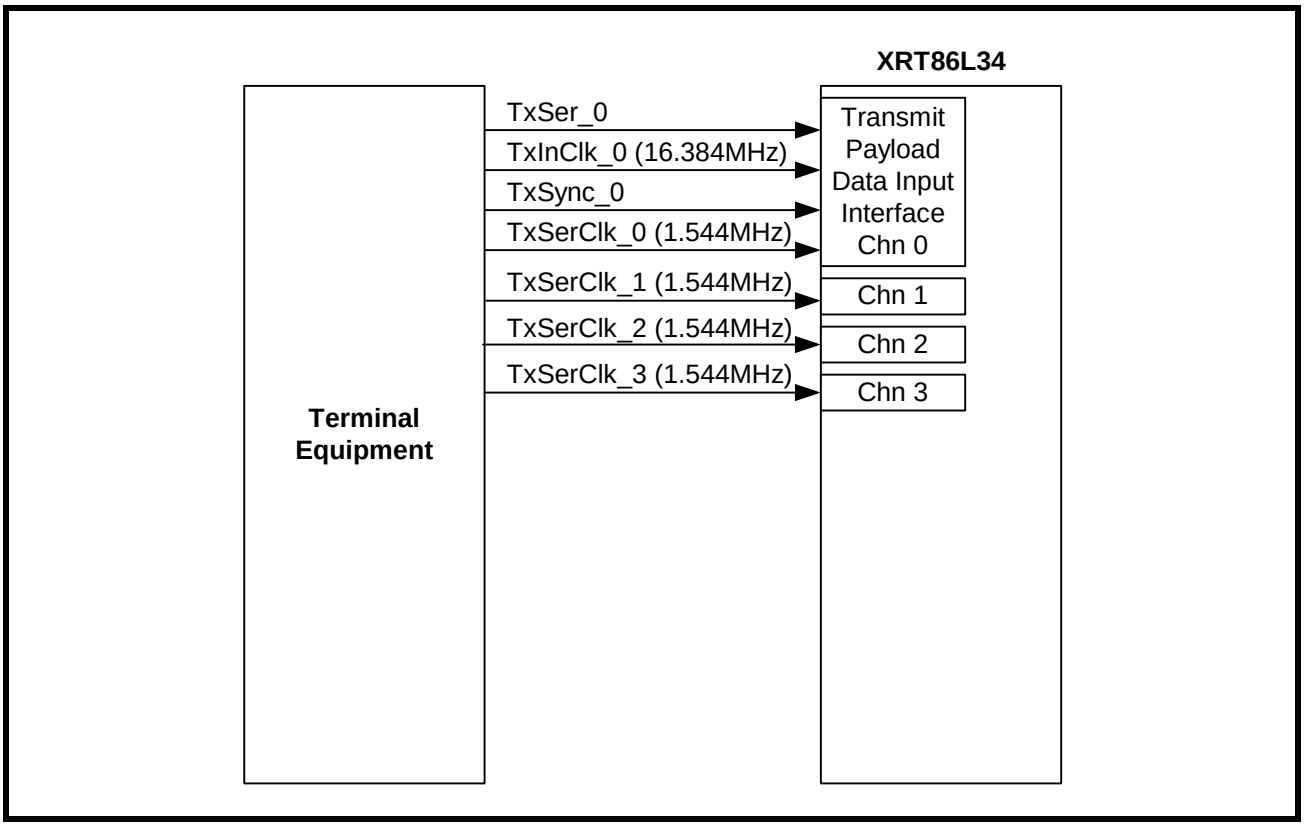
5. After payload bits of Timeslot 0, 1 and 2 of all four channels are sent, the Terminal Equipment should stuff another eight octets (sixty-four bits) of "don't care" data into the outgoing data stream.
6. Following the same rules of Step 2 to 5, the local Terminal Equipment stuffs eight octets of "don't care" data after sending twenty-four octets of multiplexed payload and signaling data. A 16.384Mbit/s data stream is thus created.

The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH for one clock cycle at the first bit position (F-bit of channel 0) of the data stream with data from Channel 0-3 multiplexed together. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH for one clock cycle at the first bit position (F-bit of Channel 4) of the data stream with data from Channel 4-7 multiplexed together. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed DS1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT86L34 and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

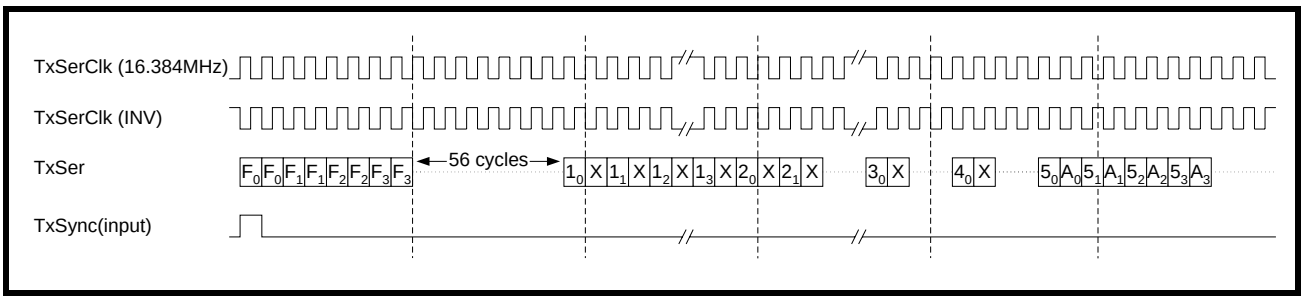
See Figure 61 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in Bit-multiplexed 16.384Mbit/s mode.

FIGURE 61. INTERFACING XRT86L34 TO THE LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 62 below when the framer is running at Bit-Multiplexed 16.384Mbit/s mode.

FIGURE 62. TIMING DIAGRAM OF THE INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT BIT-MULTIPLEXED 16.384MBIT/S MODE



5.2.0.6 T1 Transmit Input Interface - HMVIP 16.384Mbit/s

When the Transmit Multiplex Enable bit is set to one and the Transmit Interface Mode Select [1:0] bits are set to 10, the Transmit Back-plane interface of framer is running at a clock rate of 16.384MHz.

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane Interface is accepting data through TxSer_0 or TxSer_4 pins at 16.384Mbit/s. The local Terminal Equipment multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz is supplied to the Transmit Input Clock pin of Channel 0 and Channel 4 of the framer. The local Terminal Equipment provides multiplexed payload data at rising edge of this Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the clock.

The local Terminal Equipment maps four 1.544Mbit/s DS1 data streams into this 16.384Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

F_X: F-bit of Channel X

2. After the first octet of data is sent, the local Terminal Equipment should insert seven octets (fifty-six bits) of "don't care" data into the outgoing data stream.
3. 3.Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Terminal Equipment will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent the last. After the payload bits of Timeslot 0 of all four channels are sent, it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

NINTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

ELEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

THIRTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

FIFTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

X_Y: The Xth payload bit of Channel Y

4. The local Terminal Equipment also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream. When the Terminal Equipment is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

TENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	6_0	B_0	7_0	C_0	8_0	D_0

TWELFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_1	A_1	6_1	B_1	7_1	C_1	8_1	D_1

FOURTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_2	A_2	6_2	B_2	7_2	C_2	8_2	D_2

SIXTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_3	A_3	6_3	B_3	7_3	C_3	8_3	D_3

X_Y: The Xth payload bit of Channel Y

A_Y: The signaling bit A of Channel Y

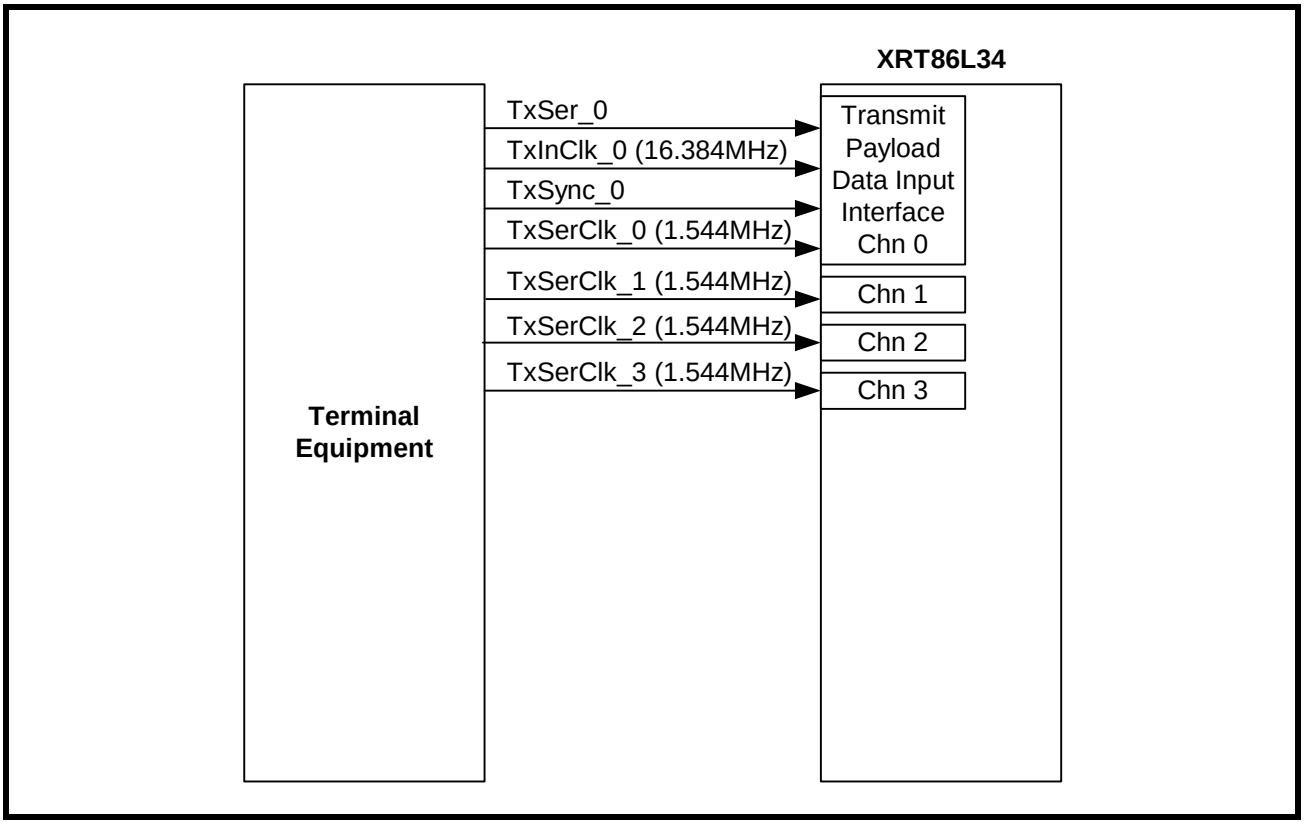
5. After payload bits of Timeslot 0, 1 and 2 of all four channels are sent, the Terminal Equipment should stuff another eight octets (sixty-four bits) of "don't care" data into the outgoing data stream.
6. Following the same rules of Step 2 to 5, the local Terminal Equipment stuffs eight octets of "don't care" data after sending twenty-four octets of multiplexed payload and signaling data. A 16.384Mbit/s data stream is thus created.

The Transmit Single-frame Synchronization signal should pulse HIGH for four clock cycles (the last two bit positions of the previous multiplexed frame and the first two bits of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH to identify the start of multiplexed data stream of Channel 4-7. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed DS1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT86L34 and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

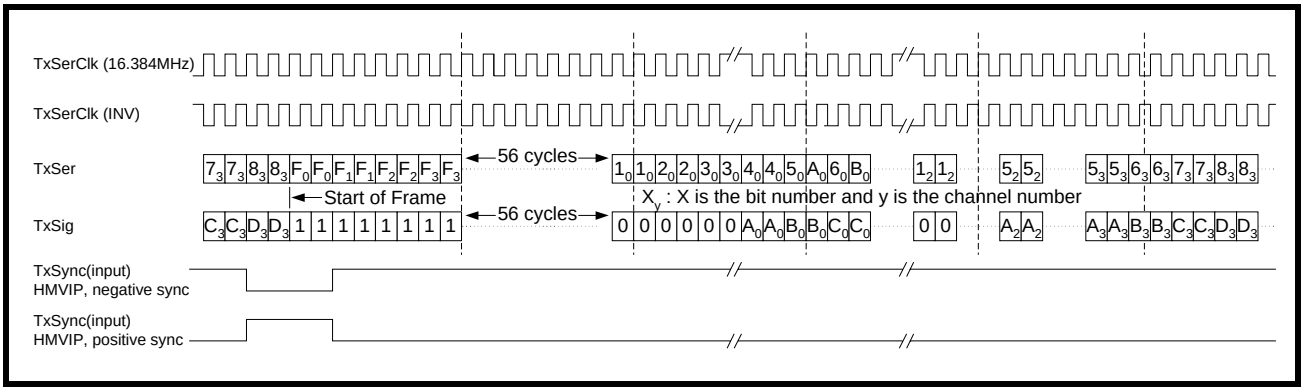
See Figure 63 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in HMVIP 16.384Mbit/s mode.

FIGURE 63. INTERFACING XRT86L34 TO THE LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 64 below when the framer is running at HMVIP 16.384Mbit/s mode.

FIGURE 64. TIMING DIAGRAM OF THE INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT HMVIP 16.384MBIT/S MODE



5.2.0.7 T1 Transmit Input Interface - H.100 16.384Mbit/s

When the Transmit Multiplex Enable bit is set to one and the Transmit Interface Mode Select [1:0] bits are set to 11, the Transmit Back-plane interface of framer is running at H.100 16.384Mbit/s mode.

(The HMVIP mode and the H.100 mode are essential the same except for the HIGH pulse position of the Transmit Single-frame Synchronization Signal)

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane Interface is accepting data through TxSer_0 or TxSer_4 pins at 16.384Mbit/s. The local Terminal Equipment multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz is supplied to the Transmit Input Clock pin of Channel 0 and Channel 4 of the framer. The local Terminal Equipment provides multiplexed payload data at rising edge of this Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the clock.

The local Terminal Equipment maps four 1.544Mbit/s DS1 data streams into this 16.384Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

FX: F-bit of Channel X

2. After the first octet of data is sent, the local Terminal Equipment should insert seven octets (fifty-six bits) of "don't care" data into the outgoing data stream.
3. 3.Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Terminal Equipment will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent the last. After the payload bits of Timeslot 0 of all four channels are sent, it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

NINTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

ELEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

THIRTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

FIFTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

X_Y: The Xth payload bit of Channel Y

4. The local Terminal Equipment also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream. When the Terminal Equipment is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

TENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	6_0	B_0	7_0	C_0	8_0	D_0

TWELFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_1	A_1	6_1	B_1	7_1	C_1	8_1	D_1

FOURTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_2	A_2	6_2	B_2	7_2	C_2	8_2	D_2

SIXTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_3	A_3	6_3	B_3	7_3	C_3	8_3	D_3

X_Y: The Xth payload bit of Channel Y

A_Y: The signaling bit A of Channel Y

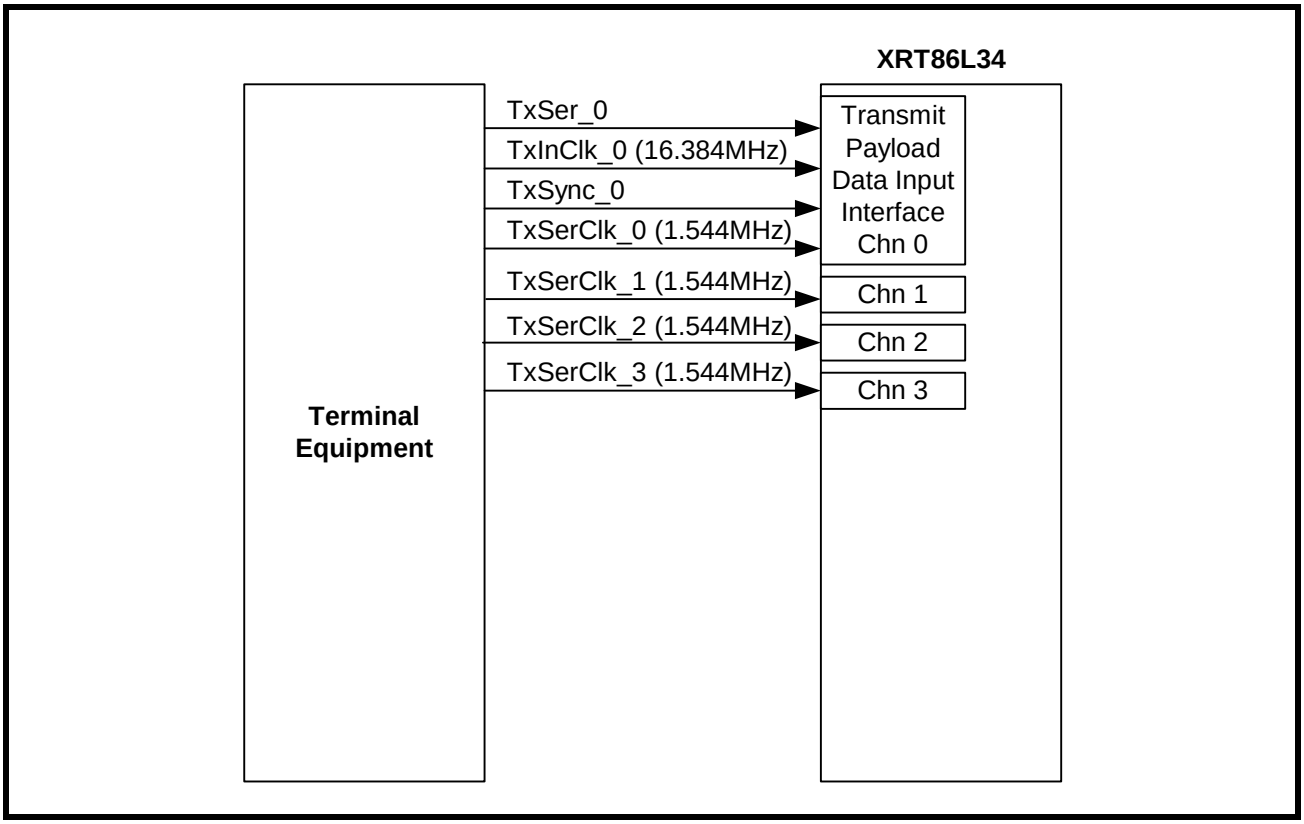
5. After payload bits of Timeslot 0, 1 and 2 of all four channels are sent, the Terminal Equipment should stuff another eight octets (sixty-four bits) of "don't care" data into the outgoing data stream.
6. Following the same rules of Step 2 to 5, the local Terminal Equipment stuffs eight octets of "don't care" data after sending twenty-four octets of multiplexed payload and signaling data. A 16.384Mbit/s data stream is thus created.

The Transmit Single-frame Synchronization signal should pulse HIGH for two clock cycles (the last bit position of the previous multiplexed frame and the first bit position of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH to identify the start of multiplexed data stream of Channel 4-7. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed DS1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT86L34 and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

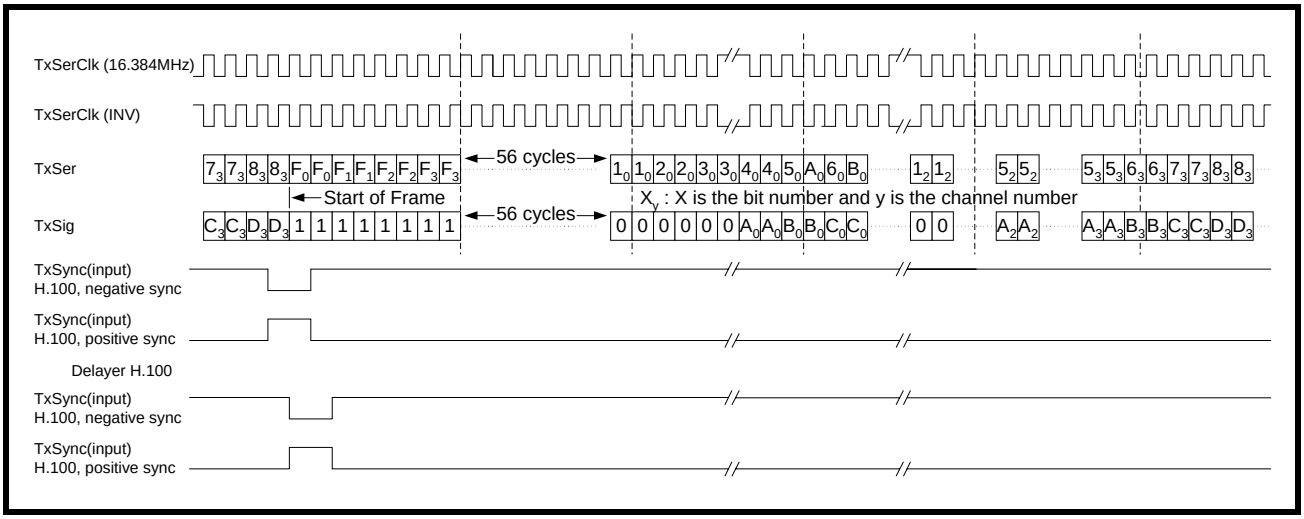
See Figure 65 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in HMVIP 16.384Mbit/s mode.

FIGURE 65. INTERFACING XRT86L34 TO THE LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 66 below when the framer is running at H.100 16.384Mbit/s mode.

FIGURE 66. TIMING DIAGRAM OF THE INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT H.100 16.384MBIT/S MODE



5.3 DS1 TRANSMIT FRAMER BLOCK

5.3.1 How to Configure XRT86L34 to Operate in DS1 Mode

The XRT86L34 Octal T1/E1/J1 Framer supports DS1, J1 or E1 framing modes. Since J1 standard is very similar to DS1 standard with a few minor changes, the J1 framing mode is included as a sub-set of the DS1 framing mode. All four framers within the XRT86L34 silicon can be individually configured to support DS1, J1 or E1 framing modes.

NOTE: *If transmitting section of one framer is configured to support either one of the framing modes, the receiving section is automatically configured to support the same framing modes.*

The T1/E1 Select bit of the Clock Select Register (CSR) controls which framing mode, that is, T1/J1 or E1, supported by the framer. The table below illustrates configurations of the T1/E1 Select bit of the Clock Select Register (CSR).

CLOCK SELECT REGISTER (CSR) (ADDRESS = 0XN100H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	T1/E1 Select	R/W	0 - The XRT86L34 framer is running in E1 mode. 1 - The XRT86L34 framer is running in T1 mode.

Since J1 and DS1 are two very similar standards, to configure the framer to run in J1 mode, the user has to select DS1 mode by setting the T1/E1 Select bit of the Clock Select Register to 1 first.

The next step is to set the J1 CRC Calculation bit of the Framing Select Register (FSR). If this bit is set to 1, the XRT86L34 will do CRC-6 calculation in J1 mode. That is, the CRC-6 calculation is based on the actual values of all 4,632 bits in DS1 multi-frame including framing bits. If this bit is set to 0, the XRT86L34 will perform CRC-6 calculation in DS1 mode. That is, the CRC-6 calculation is done based on the actual values of 4,608 payload bits of a DS1 multi-frame and assumes that all the framing bits are one.

The table below shows configurations of the J1 CRC Calculation bit of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (ADDRESS = 0XN107H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	J1 CRC Calculation	R/W	In J1 format, CRC-6 calculation is done based on the actual values of all payload bits as well as the framing bits. In DS1 format, CRC-6 calculation is done based on the payload bits only while assuming all the framing bits are one. 0 - The framer performs CRC-6 calculation in DS1 format. 1 - The framer performs CRC-6 calculation in J1 format. This feature permits the driver to comply with J1 standard.

The table below provides summary of how to select different operating modes for the XRT86L34 framer.

	T1/E1 SELECT BIT OF CSR	J1 CRC CALCULATION BIT OF FSR
T1	Set to 1	Set to 0
J1	Set to 1	Set to 1
E1	Set to 0	-

The purpose of the DS1 Transmit Framer block is to embed and encode user payload data into frames and to route this DS1 frame data to the Transmit DS1 LIU Interface block. Please note that the XRT86L34 has four (4) individual DS1 Transmit Framer blocks. Hence, the following description applies to all four of these individual Transmit DS1 Framer blocks.

The purpose of the DS1 Transmit Framer block is:

- To encode user data, inputted from the Terminal Equipment into a standard framing format.

- To provide individual data control and signaling conditioning of each DS0 channel.
- To support the transmission of HDLC messages, from the local transmitting terminal, to the remote receiving terminal.
- To transmit indications that the local receive framer has received error frames from the remote terminal.
- To transmit alarm condition indicators to the remote terminal.

The following sections discuss functionalities of the DS1 Transmit Framer block in details. We will also describe how to configure the XRT86L34 to transmit DS1 frames according to system requirement of users.

5.3.2 How to Configure the Framer to Transmit Data in Various DS1 Framing Formats

The XRT86L34 Octal T1/E1/J1 Framer supports the following DS1 framing formats:

- Super-Frame format (SF), also referred to as D4 framing
- Extended Super-Frame format (ESF)
- Non-signaling format (N)
- T1DM framing format
- SLCâ96 data link framing format, which use the Super-Frame (SF) framing structure

NOTE: *If the framer is configured to transmit DS1 frames according to one particular framing format, the receiving side of the framer is also configured to receive DS1 frames according to the same framing format. The user can set the Framing Format Select [2:0] bits of the Framing Select Register (FSR) to determine which DS1 framing format should XRT86L34 be configured to operate.*

The table below shows configurations of the Framing Format Select [2:0] bits of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (ADDRESS = 0XN107H)

<table>
<tr><th>BIT NUMBER</th><th>BIT NAME</th><th>BIT TYPE</th><th>BIT DESCRIPTION</th></tr>
<tr><td>2-0</td><td>T1 Framing Select</td><td>R/W</td><td>T1 Framing Select:
These READ/WRITE bit-fields allow the user to select one of the five T1 framing formats supported by the framer. These framing formats include ESF, SLCâ96, SF, N and T1DM mode.
<table>
<tr><th>Framing Format</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td>ESF</td><td>0</td><td>X</td><td>X</td></tr>
<tr><td>SLC®96</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>SF</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>N</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>T1DM</td><td>1</td><td>1</td><td>1</td></tr>
</table>
NOTE: Changing of framing format automatically forces the framer to perform re-synchronization.</td></tr>
</table>

5.3.3 How to configure the framer to input framing alignment bits from different sources

In DS1 mode, different framing formats are distinguished by different patterns and functions of the framing alignment bit (first bit of a DS1 frame). The XRT86L34 can generate the framing alignment bits internally according to a particular framing format.

At the same time, the users can generate the framing alignment bits externally and insert them into the framer through the Transmit Serial Data Input Interface block via the TxSer_n pin. It is the user's responsibility to maintain the accuracy and integrity of the framing alignment bits. The user also has to make sure that the fram-

ing alignment bits are inserted into the framer at right position and right timing. However, this option is only available when the XRT86L34 is configured to run at a normal back-plane rate of 1.544Mbit/s.

The Framing Bit Source Select bit of the Synchronization MUX Register (SMR) controls source of the framing alignment bit. The table below shows configurations of the Framing Bit Source Select bit of the Synchronization MUX Register (SMR).

SYNCHRONIZATION MUX REGISTER (SMR) (ADDRESS = 0XN109H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Framing Bit Source	R/W	**Framing Bit Source:** This READ/WRITE bit-field permits the user to determine where the framing alignment bits should be inserted. 0 - The framing alignment bits are generated and inserted by the framer internally. 1 - If the framer is operating in normal 1.544Mbit/s mode, the framing alignment bits are passed through from the Transmit Serial Data Input Interface block via the TxSer_n pin.

5.3.4 How to configure the framer to input CRC-6 bits from different sources

If the framer is configured to operate in Extended Super-frame Format, the framing bits of Frame number 2, 6, 10, 14, 18 and 22 of an ESF multi-frame are used as Cyclic Redundancy Check (CRC-6) code of the last ESF multi-frame. The CRC-6 bits are an indicator of the link quality and could be monitored by the user to establish error performance report.

The XRT86L34 can generate the CRC-6 bits internally by calculating the CRC check-sum of all the 4,632 bits in DS1 multi-frame while assuming the framing bits to be one.

At the same time, the users can generate the CRC-6 bits externally and insert them into the framer through the Transmit Serial Data Input Interface block via the TxSer_n pin. It is the user's responsibility to correctly compute the CRC-6 bits according to DS1 algorithm. Also, the user has to make sure that the CRC-6 bits are inserted into the framer at right position and right timing. However, this option is only available when the XRT86L34 is configured to run at a normal back-plane rate of 1.544Mbit/s.

The CRC-6 Source Select bit of the Synchronization MUX Register (SMR) controls from where to input CRC-6 bits into the framer. The table below shows configurations of the CRC-6 Source Select bit of the Synchronization MUX Register (SMR).

SYNCHRONIZATION MUX REGISTER (SMR) (ADDRESS = 0XN109H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	CRC-6 Source Select	R/W	**CRC-6 Source Select:** This READ/WRITE bit-field permits the user to determine where the CRC-6 bits should be inserted. 0 - The CRC-6 bits are generated and inserted by the framer internally. 1 - If the framer is operating in normal 1.544Mbit/s mode, the CRC-6 bits are generated by external equipment and passed through from the Transmit Serial Data Input Interface block via the TxSer_n pin.

5.3.5 How to Configure the Framer to Apply Data and Signaling Conditioning to DS1 Payload Data on a Per-Channel Basis

The XRT86L34 T1/J1/E1 Octal Framer provides individual control of each of the twenty-four DS0 channels. The user can apply data and signaling conditioning to raw DS1 payload data coming from the Terminal Equipment on a per-channel basis.

The XRT86L34 framer can apply the following changes to raw DS1 PCM data coming from the Terminal Equipment on a per-channel basis:

- All 8 bits of the input PCM data are inverted
- The even bits of the input PCM data are inverted
- The odd bits of the input PCM data are inverted
- The MSB of the input PCM data is inverted
- All input PCM data except the MSB are inverted

Configuration of the XRT86L34 framer to apply the above-mentioned changes to raw DS1 PCM data are controlled by the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of each DS0 channel.

The XRT86L34 framer can also replace the incoming raw DS1 PCM data from the Terminal Equipment with pre-defined or user-defined codes. The XRT86L34 supports the following conditioning substitutions:

- BUSY code - an octet with hexadecimal value of 0x7F
- BUSY_TS code - an octet of pattern "111xxxxx" where "xxxxx" represents the timeslot number
- VACANT code - an octet with hexadecimal value of 0xFF
- A-law Digital Milliwatt code
- u-law Digital Milliwatt code
- IDLE code - an octet defined by the value stored in the User IDLE Code Register (UCR)
- MOOF code - MUX-Out-Of-Frame code with hexadecimal value of 0x1A
- PRBS code - an octet generated by the Pseudo-Random Bit Sequence (PRBS) Generator block of the framer

Once again, configuration of the XRT86L34 framer to replace raw DS1 PCM data with the above-mentioned coding schemes are controlled by the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of each DS0 channel.

Finally, the XRT86L34 framer can configure any one or ones of the twenty-four DS0 channels to be D or E channels. D channel is used primarily for data link applications. E channel is used primarily for signaling for circuit switching with multiple access configurations.

The Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of each channel determine whether that particular channel is configured as D or E channel.

The table below illustrates configurations of the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR).

TRANSMIT CHANNEL CONTROL REGISTER (TCCR) (ADDRESS = 0XN300H - 0XN31FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Transmit Conditioning Select	R/W	0000 - The input DS1 PCM data of this DS0 channel is unchanged. 0001 - All 8 bits of the input DS1 PCM data of this DS0 channel are inverted. 0010 - The even bits of the input DS1 PCM data of this DS0 channel are inverted. 0011 - The odd bits of the input DS1 PCM data of this DS0 channel are inverted. 0100 - The input DS1 PCM data of this DS0 channel are replaced by the octet stored in User IDLE Code Register (UCR). 0101 - The input DS1 PCM data of this DS0 channel are replaced by BUSY code (0x7F). 0110 - The input DS1 PCM data of this DS0 channel are replaced by VACANT code (0xFF). 0111 - The input DS1 PCM data of this DS0 channel are replaced by BUSY_TS code (111xxxxx). 1000 - The input DS1 PCM data of this DS0 channel are replaced by MUX-Out-Of-Frame (MOOF) code with value 0x1A. 1001 - The input DS1 PCM data of this DS0 channel are replaced by the A-law digital milliwatt pattern. 1010 - The input DS1 PCM data of this DS0 channel are replaced by the u-law digital milliwatt pattern. 1011 - The MSB bit of the input DS1 PCM data of this DS0 channel is inverted. 1100 - All bits of the input DS1 PCM data of this DS0 channel except MSB bit are inverted. 1101 - The input DS1 PCM data of this DS0 channel are replaced by PRBS pattern created by the internal PRBS Generator of XRT86L34 framer. 1110 - The input DS1 PCM data of this DS0 channel is unchanged. 1111 - This channel is configured as D or E timeslot.

5.3.6 How to apply User IDLE Code to the DS1 payload data

When the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of a particular DS0 channel are set to 0100, input DS1 PCM data of this DS0 channel are replaced by the octet stored in User IDLE Code Register (UCR). The table below shows contents of the User IDLE Code Register.

USER IDLE CODE REGISTER (UCR) (ADDRESS = 0XN320H - 0X337H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	User IDLE Code	R/W	These READ/WRITE bit-fields permits the user store any value of IDLE code into the framer. When the Transmit Data Conditioning Select [3:0] bits of TCCR register of a particular DS0 channel are set to 0100, the input DS1 PCM data are replaced by contents of this register and sent to the Transmit LIU Interface.

Let us study the following example of applying the User IDLE Code.

In T1DM mode, the time slot 24 of a DS1 frame is used for synchronization and alarm. To generate the T1DM framing mode externally, the user can do the following:

- Write the T1DM synchronization word (0xBC) to the User IDLE Code Register of the time slot 24.
- Set the Transmit Data Conditioning Select [3:0] bits of the TCCR of channel 24 to "0100".

Upon doing the above, the payload data of channel 24 will be replaced by the T1DM synchronization code 0xBC.

5.3.7 How to Configure the XRT86L34 Framer to Apply Zero Code Suppression to DS1 Payload Data on a Per-Channel Basis

In order to guarantee adequate clock recovery from the received PCM data, a minimum "ones density" must be maintained. In the case of an all zero channel, that is, if all the incoming PCM data of a particular DS0 channel from the Terminal Equipment is zero, the raw PCM data is replaced by a certain pattern that no more than fifteen consecutive zeros will occur. It is known as zero code suppression.

The XRT86L34 framer supports three types of zero code suppression schemes:

- AT&T Bit 7 Stuffing - an old coding method that forces Bit 7 (the second LSB of a DS0 channel) to a 1 in an all zero channel.
- GTE Zero Code Suppression - Bit 8 (the LSB of a DS0 channel) is stuffed by 1 in non-signaling frame in an all zero channel. Otherwise, Bit 7 is stuffed by 1 in signaling frame if the signaling bit is zero.
- DDS Zero Code Suppression - an octet with hexadecimal value of 0x98 is used to replace the input data if it is all zero.

The Transmit Zero Code Suppression Select [1:0] bits of the Transmit Channel Control Register (TCCR) of a particular DS0 channel is used to select which type of zero code suppression scheme is used by the framer. The table below shows configurations of the Transmit Zero Code Suppression Select [1:0] bits of the Transmit Channel Control Register (TCCR).

TRANSMIT CHANNEL CONTROL REGISTER (TCCR) (ADDRESS = 0XN300H - 0X31FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	Transmit Zero Code Suppression Select	R/W	00 - The input DS1 PCM data of this DS0 channel is unchanged. No zero code suppression is used. 01 - AT&T Bit 7 stuffing is used. 10 - GTE zero code suppression is used. 11 - DDS zero code suppression is used.

5.3.8 How to Configure the XRT86L34 Framer to Transmit Robbed-bit Signaling Information

The XRT86L34 T1/J1/E1 Octal Framer supports insertion of Robbed-bit Signaling information into the outgoing DS1 frame. It also supports extraction and substitution of Robbed-bit Signaling information from the incoming DS1 frame. The following section provides a brief overview of Robbed-bit Signaling in DS1 mode.

5.3.9 Brief Discussion of Robbed-bit Signaling in DS1 Framing Format

Signaling is required when dealing with voice and dial-up data services in DS1 applications. Traditionally, signaling is provided on a dial-up telephone line, across the talk-path. Bit robbing, or stealing the least significant bit (8th bit) in each of the twenty-four voice channels in the signaling frames allows enough bits to signal between the transmitting and receiving end. That is how the name Robbed-bit signaling comes from. These ends can be CPE to central office (CO) for switched services, or CPE to CPE for PBX-to-PBX connections.

Signaling is used to tell the receiver where the call or route is destined. The signal is sent through switches along the route to a distant end. Common types of signals are:

- On hook
- Off hook
- Dial tone
- Dialed digits
- Ringing cycle
- Busy tone

Robbed-bit Signaling is supported in three DS1 framing formats:

- Super-Frame (SF)
- SLC®96

- Extended Super-Frame (ESF)

In Super-Frame or SLC®96 framing mode, frame number 6 and frame number 12 are signaling frames. In channelized DS1 applications, these frames are used to contain the signaling information. In frame number 6 and 12, the least significant bit of all twenty-four timeslots is 'robbed' to carry call state information. The bit in frame 6 is called the A bit and the bit in frame 12 is called the B bit. The combination of A and B defines the state of the call for the particular timeslot that these two bits are located.

FRAME NUMBER	SIGNALING BIT
6	A
12	B

In Extended Super-Frame framing mode, frame number 6, 12, 18 and 24 are signaling frames. In these frames, the least significant bit of all twenty-four timeslots is 'robbed' to carry call state information. The bit in frame 6 is called the A bit, the bit in frame 12 is called the B bit, the bit in frame 18 is called the C bit and the bit in frame 24 is called the D bit. The combination of A, B, C and D defines the state of the call for the particular timeslot that these signaling bits are located.

FRAME NUMBER	SIGNALING BIT
6	A
12	B
18	C
24	D

5.3.10 Configure the framer to transmit Robbed-bit Signaling

The XRT86L34 framer supports transmission of Robbed-bit Signaling in ESF, SF and SLC®96 framing formats. Signaling bits can be inserted into the outgoing DS1 frame through the following:

- Signaling data is inserted from Transmit Signaling Control Registers (TSCR) of each timeslot
- Signaling data is inserted from TxSig_n pin
- Signaling data is embedded into the input PCM data coming from the Terminal Equipment

5.3.10.1 Insert Signaling Bits from TSCR Register

The four most significant bits of the Transmit Signaling Control Register (TSCR) of each timeslot can be used to store outgoing signaling data. The user can program these bits through microprocessor access. If the XRT86L34 framer is configure to insert signaling bits from TSCR registers, the DS1 Transmit Framer block will strip off the least significant bits of signaling frames and replace it with the signaling bit stored inside the TSCR registers. The insertion of signaling bit into PCM data is done on a per-channel basis. The most significant bit (Bit 7) of TSCR register is used to store Signaling bit A. Bit 6 is used to hold Signaling bit B. Bit 5 is used to hold Signaling bit C. Bit 4 is used to hold Signaling bit D.

In SF or SLCâ96 mode, the user can control the XRT86L34 framer to transmit no signaling (transparent), two-code signaling, or four-code signaling. Two-code signaling is done by substituting the least significant bit (LSB) of the specific channel in frame 6 and 12 with the content of the Signaling bit A of the specific TSCR register.

NOTE: *The user should make sure that Signaling bit A and Signaling bit B of the specific TSCR register have the same value.*

Four-code signaling is done by substituting the LSB of channel data in frame 6 with the Signaling bit A and the LSB of channel data in frame 12 with the Signaling bit B of the specific channel's TSCR register. If sixteen-code signaling is selected in SF format, only the Signaling bit A and Signaling bit B information are used.

In ESF mode, the user can control the XRT86L34 framer to transmit no signaling (transparent) by disable signaling insertion, two-code signaling, four-code signaling or sixteen code signaling. Two-code signaling is done by substituting the least significant bit (LSB) of the specific channel in frame 6, 12, 18 and 24 with the content of the Signaling bit A of the specific TSCR register.

NOTE: The user should duplicate the contents of Signaling bit A of the specific TSCR register to Signaling bit B, C and D.

Four-code signaling is done by substituting the LSB of channel data in frame 6 and frame 18 with the Signaling bit A and the LSB of channel data in frame 12 and frame 24 with the Signaling bit B of the specific channel's TSCR register.

NOTE: The user should duplicate the contents of Signaling bit A of the specific TSCR register to Signaling bit C and duplicate the contents of Signaling bit B of the specific TSCR register to Signaling bit D.

Sixteen-code signaling is implemented by substituting the LSB of channel data in frames 6, 12, 18, and 24 with the content of Signaling bit A, B, C, and D of TSCR register respectively.

In N mode, no robbed-bit signaling is allowed and the transmit data stream remains intact.

The table below shows the four most significant bits of the Transmit Signaling Control Register.

TRANSMIT SIGNALING CONTROL REGISTER (TSCR) (ADDRESS = 0XN340H - 0XN357H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Signaling Bit A	R/W	This bit is used to store Signaling Bit A that is sent as the least significant bit of timeslot of frame number 6.
6	Signaling Bit B	R/W	This bit is used to store Signaling Bit B that is sent as the least significant bit of timeslot of frame number 12.
5	Signaling Bit C	R/W	This bit is used to store Signaling Bit C that is sent as the least significant bit of timeslot of frame number 18.
4	Signaling Bit D	R/W	This bit is used to store Signaling Bit D that is sent as the least significant bit of timeslot of frame number 24.

5.3.10.2 Insert Signaling Bits from TxSig_n Pin

The XRT86L34 framer can be configure to insert signaling bits provided by external equipment through the TxSig_n pins. This pin is a multiplexed I/O pin with two functions:

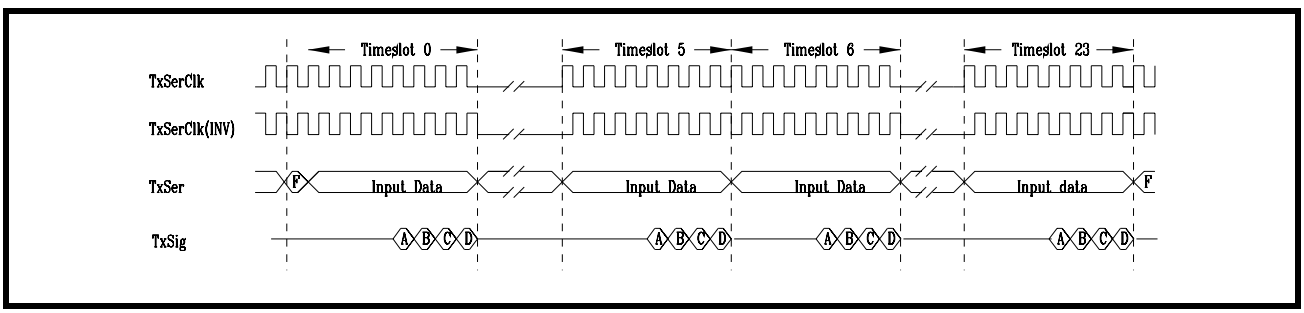
- TxTSb[0]_n - Transmit Timeslot Number Bit [0] Output pin
- TxSig_n - Transmit Signaling Input pin

When the Transmit Fractional DS1 bit of the Transmit Interface Control Register (TICR) is set to 0, this pin is configured as TxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the DS1 PCM data that is transmitting.

When the Transmit Fractional DS1 bit of the Transmit Interface Control Register (TICR) is set to 1, this pin is configured as TxSig_n pin, it acts as an input source for the signaling bits to be transmitted in the outbound DS1 frames.

Figure 67 below is a timing diagram of the TxSig_n input pin. Please note that the Signaling Bit A of a certain timeslot coincides with Bit 5 of the PCM data; Signaling Bit B coincides with Bit 6 of the PCM data; Signaling Bit C coincides with Bit 7 of the PCM data and Signaling Bit D coincides with Bit 8 (LSB) of the PCM data.

FIGURE 67. TIMING DIAGRAM OF THE TXSIG_N INPUT



The table below shows configurations of the Transmit Fractional DS1 bit of the Transmit Interface Control Register (TICR).

TRANSMIT INTERFACE CONTROL REGISTER (TICR)(ADDRESS = 0XN120H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Transmit Fractional DS1	R/W	This READ/WRITE bit-field permits the user to determine which one of the two functions the multiplexed I/O pin of TxTSb[0]_n/TxSig_n is spotting. 0 - This pin is configured as TxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the DS1 PCM data that is transmitting. 1 - This pin is configured as TxSig_n pin, it acts as an input source for the signaling bits to be transmitted in the outbound DS1 frames

5.3.10.3 Insert Signaling Data from TxSer_n Pin

Depends on applications, the Terminal Equipment can embed signaling information into the DS1 PCM data and then send the data to the XRT86L34 framer device. In this case, the user should configure the framer not to insert any signaling data. The input DS1 PCM data will then be directed to the Transmit LIU Interface without any modifications.

5.3.10.4 Enable Robbed-bit Signaling and Signaling Data Source Control

The Transmit Signaling Control Register (TSCR) of each channel selects source of signaling data to be inserted into the outgoing DS1 frame and enables robbed-bit signaling. As we mentioned before, the signaling data can be inserted from Transmit Signaling Control Registers (TSCR) of each timeslot, from the TxSig_n input pin or from the TxSer_n input pin.

The Transmit Signaling Data Source Select [1:0] bits of the Transmit Signaling Control Register (TSCR) determines from which sources the signaling data is inserted from. The table below shows configurations of the Transmit Signaling Data Source Select [1:0] bits of the Transmit Signaling Control Register (TSCR).

TRANSMIT SIGNALING CONTROL REGISTER (TSCR) (ADDRESS = 0XN340H - 0XN357H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Signaling Source Select	R/W	00 - No signaling data is inserted into the input DS1 PCM data by the framer. However, the user can embed signaling data into DS1 PCM data before routing the PCM data into the framer. 01 - Signaling data is inserted into the input DS1 PCM data from TSCR register of each timeslot. 10 - Signaling data is inserted into the input DS1 PCM data from the TxSig_n input pin. 11 - No signaling data is inserted into the input DS1 PCM data by the framer. However, the user can embed signaling data into DS1 PCM data before routing the PCM data into the framer.

The Robbed-bit Signaling Enable bit of the Transmit Signaling Control Register (TSCR) determines whether Robbed-bit Signaling is available. The table below shows configurations of the Robbed-bit Signaling Enable bit of the Transmit Signaling Control Register (TSCR).

TRANSMIT SIGNALING CONTROL REGISTER (TSCR) (ADDRESS = 0XN340H - 0XN357H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Robbed-bit Signaling Enable	R/W	0 - Robbed-bit Signaling is disabled. No signaling data will be inserted into the input PCM data no matter what the setting of the Transmit Signaling Source Select [1:0] bits is. 1 - Signaling data is enabled and inserted into the input DS1 PCM data according to setting of the Transmit Signaling Source Select [1:0] bits.

5.3.11 How to Configure the XRT86L34 Framer to Generate and Transmit Alarms and Error Indications to Remote Terminal

The XRT86L34 T1/J1/E1 Octal Framer can be configured to monitor quality of received DS1 frames. It can generate error indications if the local receive framer has received error frames from the remote terminal. If corresponding interrupt is enabled, the local microprocessor operation is interrupted by these error conditions. Upon microprocessor interruption, the user can intervene by looking into the error conditions.

At the same time, the user can configure the XRT86L34 framer to transmit alarms and error indications to remote terminal. Different alarms and error indications will be transmitted depending on the error condition. The section below gives a brief discussion of the error conditions and appropriate alarms that should be generated and transmitted by the XRT86L34 framer.

5.3.12 Brief discussion of alarms and error conditions

As defined in ANSI T1.231 specification, alarm conditions are created from defects. Defects are momentary impairments present on the DS1 trunk. If a defect is present for a sufficient amount of time (called the integration time), then the defect becomes an alarm. Once an alarm is declared, the alarm is present until after the defect clears for a sufficient period of time. The time it takes to clear an alarm is called the de-integration time.

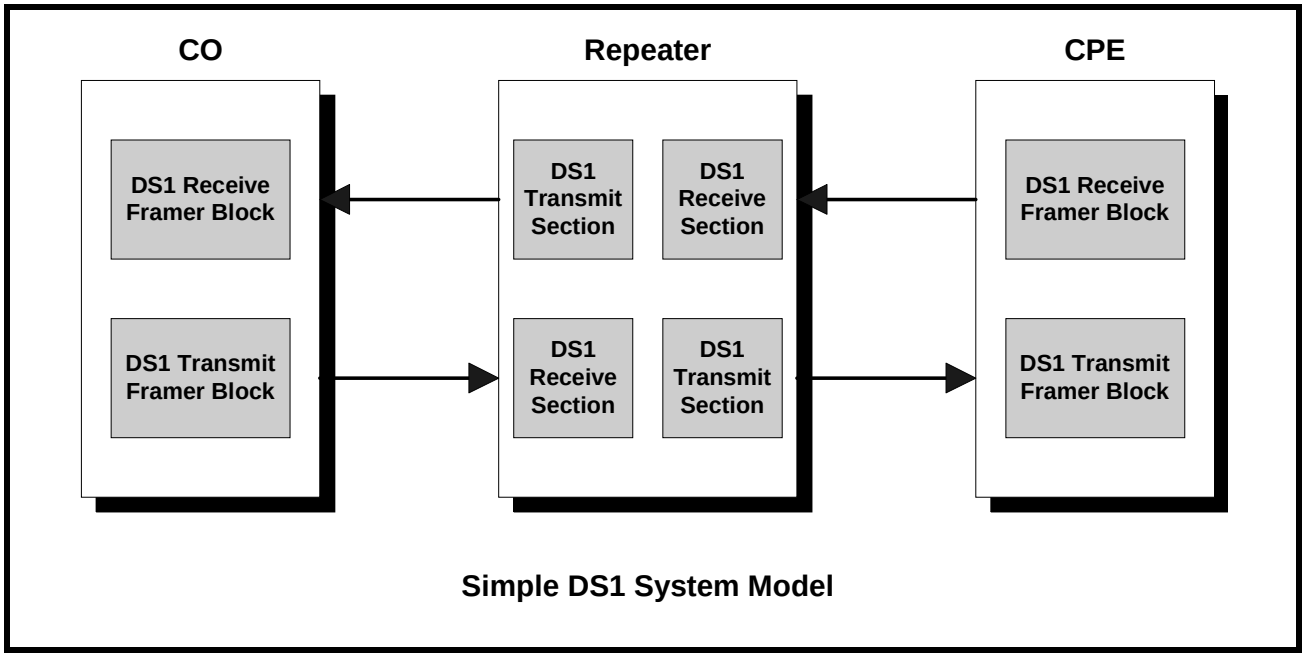
Alarms are used to detect and warn maintenance personnel of problems on the DS1 trunk. There are three types of alarms:

- Red alarm or Service Alarm Indication (SAI) Signal
- Blue alarm or Alarm Indication Signal (AIS)
- Yellow alarm or Remote Alarm Indication (RAI) Signal

To explain the error conditions and generation of different alarms, let us create a simple DS1 system model. In this model, a DS1 signal is sourced from the Central Office (CO) through a Repeater to the Customer Premises

Equipment (CPE). At the same time, a DS1 signal is routed from the CPE to the Repeater and back to the Central Office. Figure 68 below shows the simple DS1 system model.

FIGURE 68. SIMPLE DIAGRAM OF DS1 SYSTEM MODEL



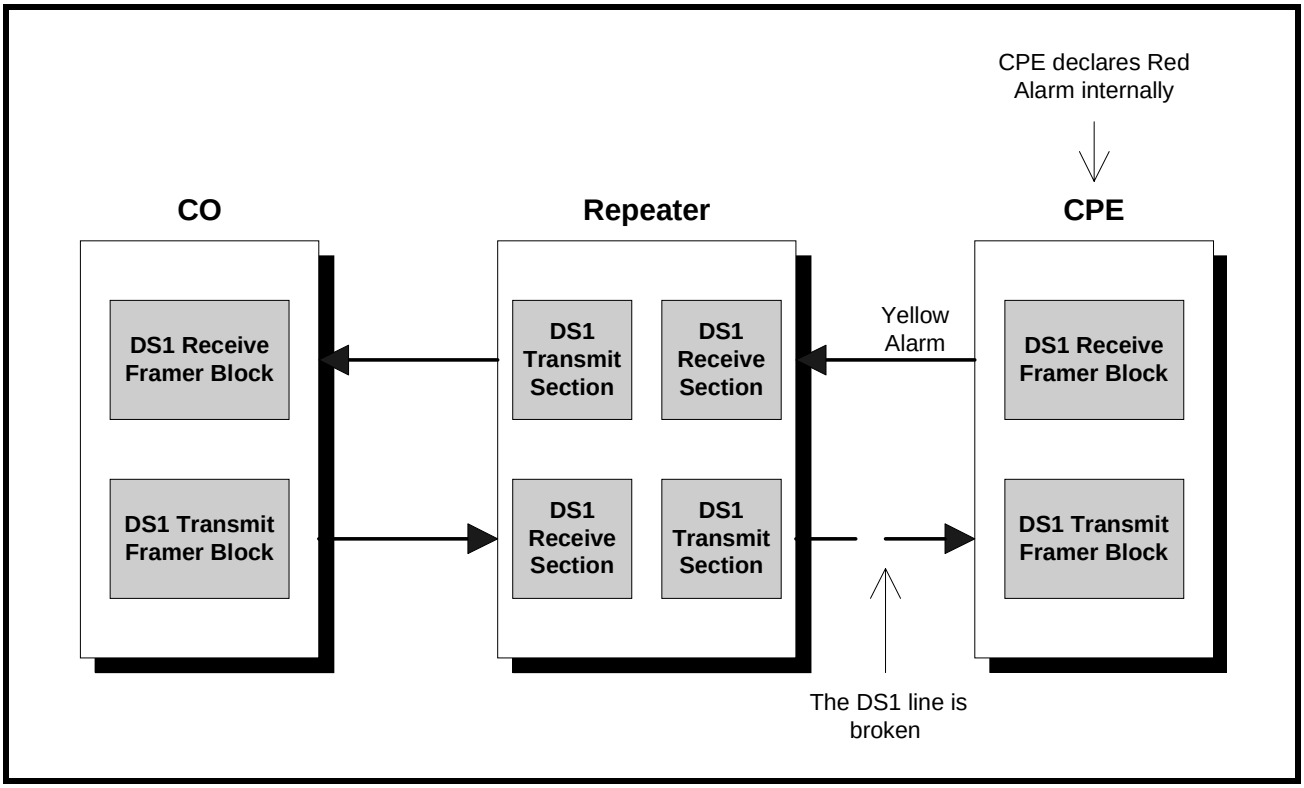
When the E1 system runs normally, that is, when there is no Loss of Signal (LOS) or Loss of Frame (LOF) detected in the line, no alarm will be generated. Sometimes, intermittent outburst of electrical noises on the line might result in Bipolar Violation or bit errors in the incoming signals, but these errors in general will not trigger the equipment to generate alarms. They will at most trigger the framer to generate interrupts which would cause the local microprocessor to create performance reports of the line.

Now, consider a case in which the E1 line from the Repeater to CPE is broken or interrupted, resulting in completely loss of incoming data or severely impaired signal quality. Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the CPE will generate an internal Red Alarm, also known as the Service Alarm Indication. This alarm will normally trigger a microprocessor interrupt informing the user that an incoming signal failure is happening.

When the CPE is in the Red Alarm state, it will transmit the Yellow Alarm to the Repeater indicating the loss of an incoming signal or loss of frame synchronization. This Yellow Alarm informs the Repeater that there is a

problem further down the line and its transmission is not being received at the CPE. The Figure below illustrates the scenario in which the E1 connection from the Repeater to CPE is broken.

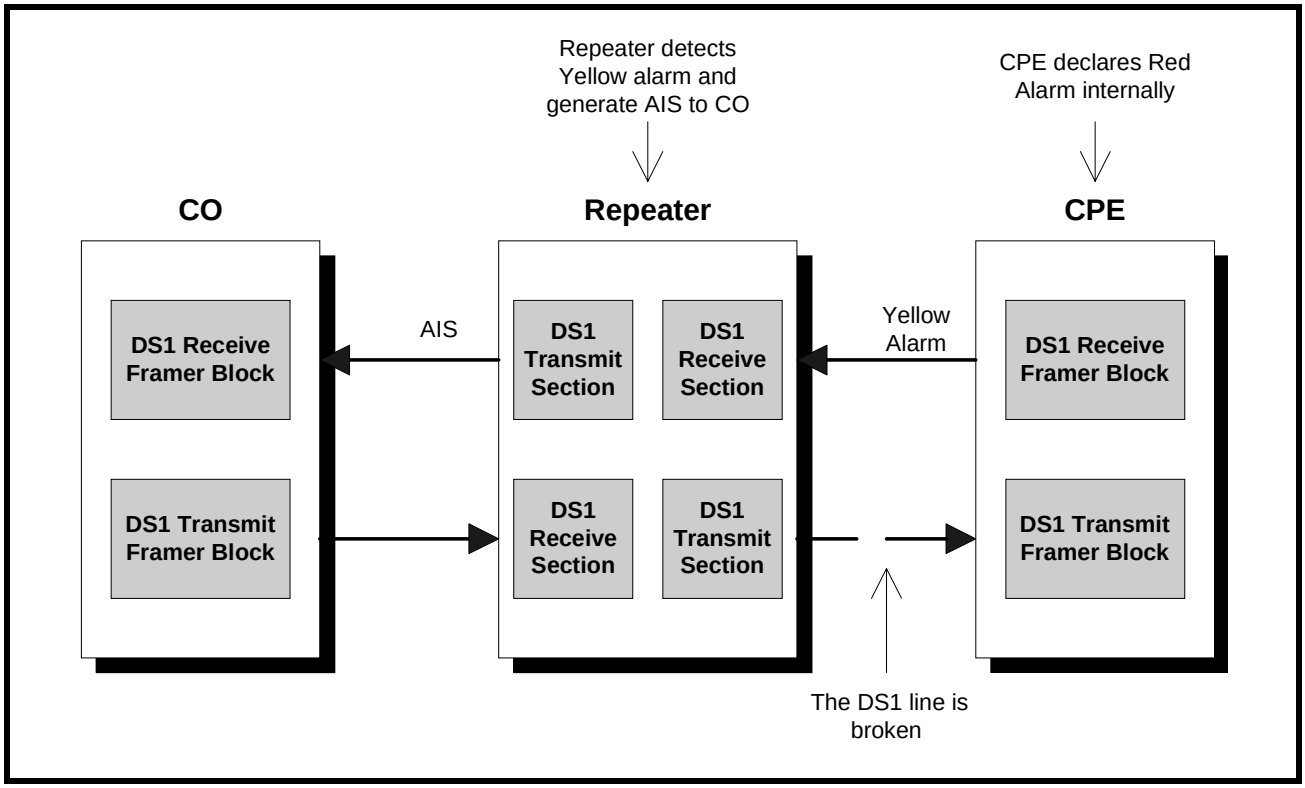
FIGURE 69. GENERATION OF YELLOW ALARM BY THE CPE UPON DETECTION OF LINE FAILURE



The Repeater, upon detection of Yellow Alarm originated from the CPE, will transmit a Blue Alarm, also known as Alarm Indication Signal (AIS) to the CO. Blue alarm is an all ones pattern indicating that the equipment is functioning but unable to offer service due to failures originated from remote side. It is sent such that the equipment downstream will not lose clock synchronization even though no meaningful data is received. The Figure

below illustrates this scenario in which the Repeater is sending an AIS to CO upon detection of Yellow alarm originated from the CPE.

FIGURE 70. GENERATION OF AIS BY THE REPEATER UPON DETECTION OF YELLOW ALARM ORIGINATED BY THE CPE

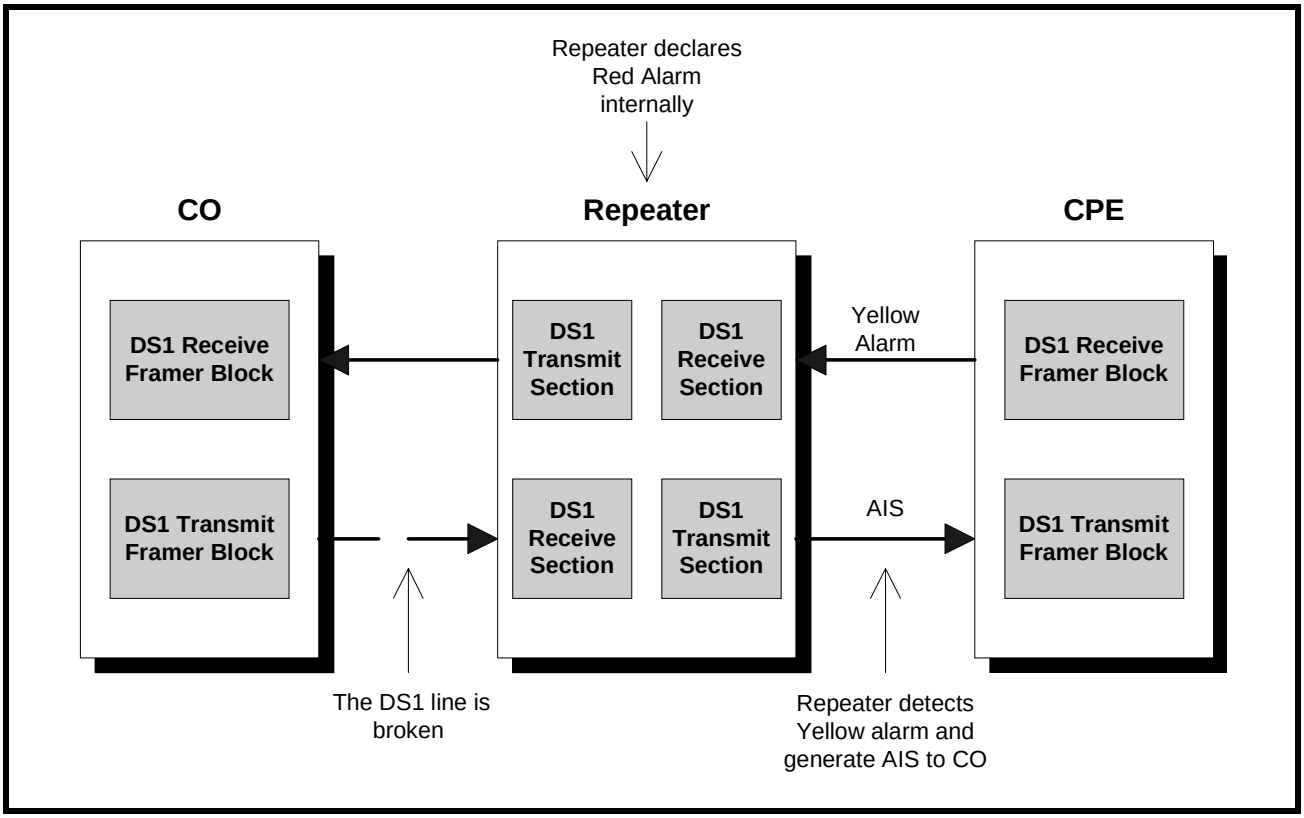


Now let us consider another scenario in which the DS1 line between CO and the Repeater is broken. Again, upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the Repeater will generate an internal Red Alarm. This alarm will normally trigger a microprocessor interrupt informing the user that an incoming signal failure is happening.

The Repeater will also send an all ones AIS pattern downstream to the CPE. The CPE uses the AIS signal to recover received clock and remain in synchronization with the system. Upon detecting the incoming AIS signal, the CPE will generate a Yellow Alarm to the Repeater to indicate the loss of incoming signal. The Figure below

illustrates this scenario in which the Repeater is sending an AIS to the CPE and the CPE is sending a Yellow Alarm back to the Repeater.

FIGURE 71. GENERATION OF YELLOW ALARM BY THE CPE UPON DETECTION OF AIS ORIGINATED BY THE REPEATER



5.3.13 How to configure the framer to transmit AIS

As we discussed in the previous section, Alarm Indication Signal (AIS) or Blue Alarm is transmitted by the intermediate node to indicate that the equipment is still functioning but unable to offer services. It is an all ones (except for framing bits) pattern which can be used by the equipment further down the line to maintain clock recovery and timing synchronization.

The XRT86L34 framer can generate two types of AIS:

- Framed AIS
- Unframed AIS

Unframed AIS is an all ones pattern. If unframed AIS is sent, the equipment further down the line will be able to maintain timing synchronization and be able to recover clock from the received AIS signal. However, due to the lack of framing bits, the equipment farther down the line will not be able to maintain frame synchronization and will declare Loss of Frame (LOF).

On the other hand, the payload portion of a framed AIS pattern is all ones. However, a framed AIS pattern still has correct framing bits. Therefore, the equipment further down the line can still maintain frame synchronization as well as timing synchronization. In this case, no LOF or Red alarm will be declared.

The Transmit Alarm Indication Signal Select [1:0] bits of the Alarm Generation Register (AGR) enable the two types of AIS transmission that are supported by the XRT86L34 framer. The table below shows configurations of the Transmit Alarm Indication Signal Select [1:0] bits of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR)(ADDRESS = 0XN108H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Transmit AIS Select	R/W	These READ/WRITE bit-fields allows the user to choose which one of the two AIS pattern supported by the XRT86L34 framer will be transmitted. 00 - No AIS alarm is generated. 01 - Enable unframed AIS alarm of all ones pattern. 10 - Enable framed AIS alarm of all ones pattern except for framing bits. 11 - No AIS alarm is generated.

5.3.14 How to configure the framer to generate Red Alarm

Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the Repeater will generate an internal Red Alarm when enabled. This alarm will normally trigger a microprocessor interrupt informing the user that an incoming signal failure is happening.

The Loss of Frame Declaration Enable bit of the Alarm Generation Register (AGR) enable the generation of Red Alarm. The table below shows configurations of the of Frame Declaration Enable bit of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR)(ADDRESS = 0XN108H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Loss of Frame Declaration Enable	R/W	This READ/WRITE bit-field permits the framer to declare Red Alarm in case of Loss of Frame Alignment (LOF). When receiver module of the framer detects Loss of Frame Alignment in the incoming data stream, it will generate a Red Alarm. The framer will also generate an RxLOFs interrupt to notify the microprocessor that an LOF condition is occurred. A Yellow Alarm is then returned to the remote transmitter to report that the local receiver detects LOF. 0 - Red Alarm declaration is disabled. 1 - Red Alarm declaration is enabled.

5.3.15 How to configure the framer to transmit Yellow Alarm

Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the receiver will transmit the Yellow Alarm back to the source indicating the loss of an incoming signal. This Yellow Alarm informs the source that there is a problem further down the line and its transmission is not being received at the destination.

The XRT86L34 framer supports transmission of Yellow Alarm when running at the following framing formats:

- SF Mode
- ESF Mode
- N Mode
- T1DM Mode

Yellow alarm is transmitted in different forms for various framing formats. The Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register (AGR) enable transmission of different types of Yellow alarm that are supported by the XRT86L34 framer.

5.3.15.1 Transmit Yellow Alarm in SF Mode

In SF mode, the XRT86L34 supports transmission of Yellow Alarm in two ways. When the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 01 or 11, the second MSB of all DS0 channels is transmitted as zero. This is Yellow Alarm for DS1 standard.

When the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 10, the Framing bit of Frame 12 is transmitted as one. This is Yellow Alarm for J1 standard.

5.3.15.2 Transmit Yellow Alarm in ESF Mode

In ESF mode, the XRT86L34 transmits Yellow Alarm on the 4Kbit/s data link channel. The Facility Data Link bits are sent in the pattern of eight ones followed by eight zeros. The number of repetitions of this pattern depends on the duration of Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register. When these select bits are set to 01 or 11, the following scenario will happen:

1. If Bit 0 of Yellow Alarm Generation Select forms a pulse width shorter or equal to the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm is transmitted for 255 patterns.
2. If Bit 0 of Yellow Alarm Generation Select forms a pulse width longer than the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm continues until Bit 0 goes LOW.
3. A second pulse on Bit 0 of Yellow Alarm Generation Select during an alarm transmission resets the pattern counter. The framer will send another 255 patterns of the Yellow Alarm.

When these select bits are set to 10, Bit 1 of the Yellow Alarm Generation Select forms a pulse that controls the duration of Yellow Alarm transmission. The alarm continues until Bit 1 goes LOW.

When these select bits are set to 01, the following scenario will happen:

1. If Bit 0 of Yellow Alarm Generation Select forms a pulse width shorter or equal to the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm is transmitted for 255 patterns.
2. If Bit 0 of Yellow Alarm Generation Select forms a pulse width longer than the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm continues until Bit 0 goes LOW.
3. A second pulse on Bit 0 of Yellow Alarm Generation Select during an alarm transmission resets the pattern counter. The framer will send another 255 patterns of the Yellow Alarm.

5.3.15.3 Transmit Yellow Alarm in N Mode

In N mode, when the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 01, 10 or 11, the second MSB of all DS0 channels is transmitted as zero.

5.3.15.4 Transmit Yellow Alarm in T1DM Mode

In T1DM mode, when the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 01, 10 or 11, the Yellow Alarm bit (the third LSB of Timeslot 23) is set to zero.The table below shows configurations of the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register (AGR).

)

ALARM GENERATION REGISTER (AGR)(ADDRESS = 0XN108H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	Yellow Alarm Generation Select	R/W	00 - Transmission of Yellow Alarm is disabled. 01 - The framer transmits Yellow Alarm by converting the second MSB of all outgoing twenty-four DS0 channel into zero. 10 - The framer transmits Yellow Alarm by sending the Super-frame Alignment Bit (Fs) of Frame 12 as one. 11 - The framer transmits Yellow Alarm by converting the second MSB of all outgoing twenty-four DS0 channel into zero. N Mode: 00 - Transmission of Yellow Alarm is disabled. 01, 10 or 11 - The framer transmits Yellow Alarm by converting the second MSB of all outgoing twenty-four DS0 channel into zero. ESF Mode: When the framer is in ESF mode, it transmits Yellow Alarm pattern of eight ones followed by eight zeros (1111_1111_0000_0000) through the 4Kbit/s data link bits. 00 - Transmission of Yellow Alarm is disabled. 01 - The following scenario will happen: **1.** If Bit 0 of Yellow Alarm Generation Select forms a pulse width shorter or equal to the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm is transmitted for 255 patterns. **2.** If Bit 0 of Yellow Alarm Generation Select forms a pulse width longer than the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm continues until Bit 0 goes LOW. **3.** A second pulse on Bit 0 of Yellow Alarm Generation Select during an alarm transmission resets the pattern counter. The framer will send another 255 patterns of the Yellow Alarm. 10 - Bit 1 of the Yellow Alarm Generation Select forms a pulse that controls the duration of Yellow Alarm transmission. The alarm continues until Bit 1 goes LOW. 11 - The following scenario will happen: **1.** If Bit 0 of Yellow Alarm Generation Select forms a pulse width shorter or equal to the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm is transmitted for 255 patterns. **2.** If Bit 0 of Yellow Alarm Generation Select forms a pulse width longer than the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm continues until Bit 0 goes LOW. **3.** A second pulse on Bit 0 of Yellow Alarm Generation Select during an alarm transmission resets the pattern counter. The framer will send another 255 patterns of the Yellow Alarm. T1DM Mode: 00 - Transmission of Yellow Alarm is disabled. 01, 10 or 11 - The framer transmits Yellow Alarm by setting the Yellow Alarm bit (Y-bit) to zero.

6.0 LIU TRANSMIT PATH

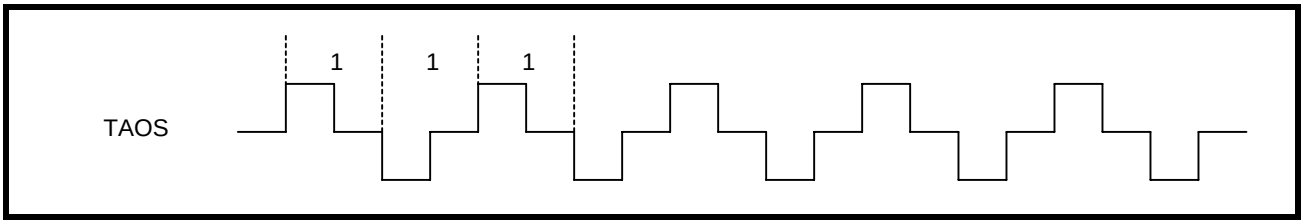
6.1 TRANSMIT DIAGNOSTIC FEATURES

In addition to TAOS, the XRT86L34 offers multiple diagnostic features for analyzing network integrity such as ATAOS, Network Loop Code generation, and QRSS on a per channel basis by programming the appropriate registers. These diagnostic features take priority over the digital data provided by the Framer block. The transmitters will send the diagnostic code to the line and will be maintained in the digital loopback if selected.

6.1.1 TAOS (Transmit All Ones)

The XRT86L34 has the ability to transmit all ones on a per channel basis by programming the appropriate channel register. This function takes priority over the digital data provided by the Framer block. For example: If a fixed "0011" pattern is provided by the Framer block and TAOS is enabled, the transmitter will output all ones. Figure 72 is a diagram showing the all ones signal at TTIP and TRING.

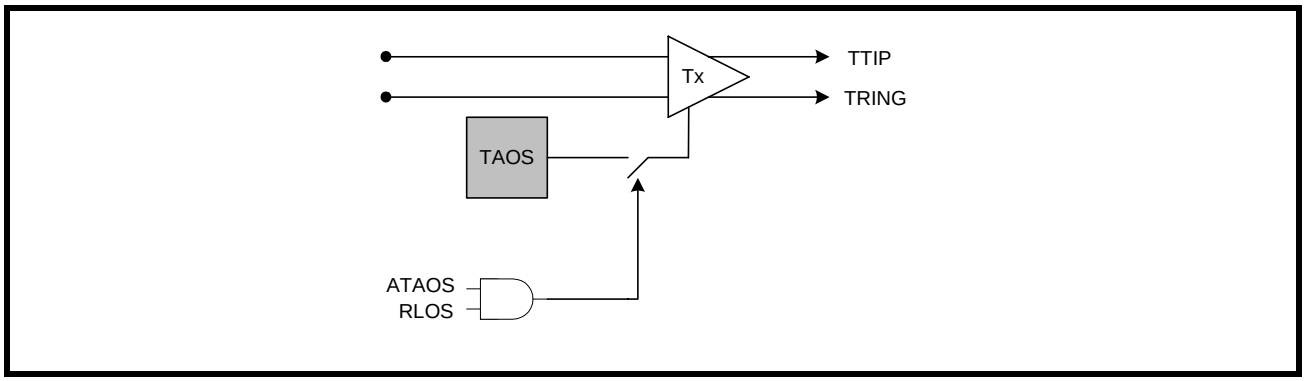
FIGURE 72. TAOS (TRANSMIT ALL ONES)



6.1.2 ATAOS (Automatic Transmit All Ones)

If ATAOS is selected by programming the appropriate global register, an AMI all ones signal will be transmitted for each channel that experiences an RLOS condition. If RLOS does not occur, the ATAOS will remain inactive until an RLOS on a given channel occurs. A simplified block diagram of the ATAOS function is shown in Figure 73.

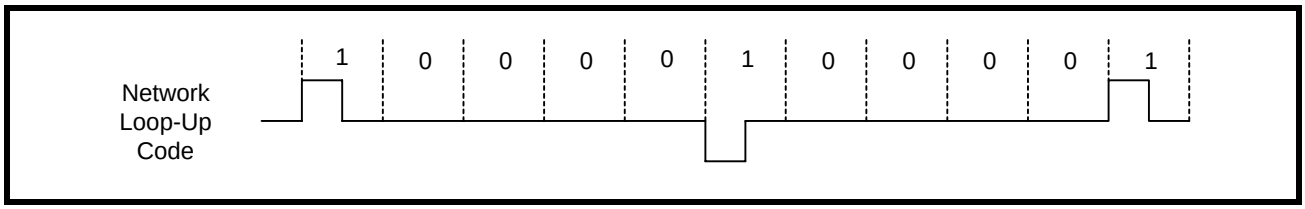
FIGURE 73. SIMPLIFIED BLOCK DIAGRAM OF THE ATAOS FUNCTION



6.1.3 Network Loop Up Code

By setting the LIU to generate a NLUC, the transmitters will send out a repeating "00001" pattern. The output waveform is shown in Figure 74.

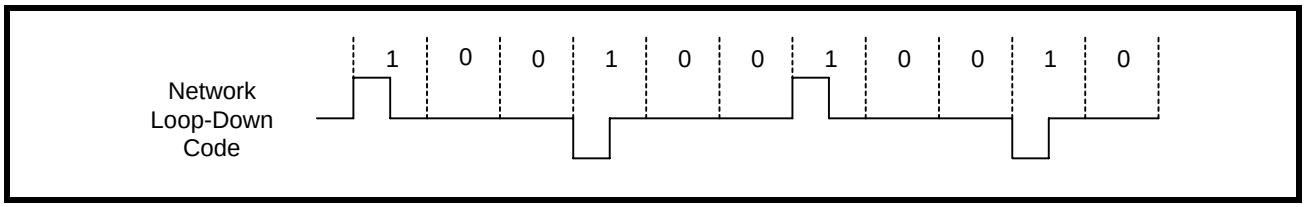
FIGURE 74. NETWORK LOOP UP CODE GENERATION



6.1.4 Network Loop Down Code

By setting the LIU to generate a NLDC, the transmitters will send out a repeating "001" pattern. The output waveform is shown in Figure 75.

FIGURE 75. NETWORK LOOP DOWN CODE GENERATION



6.1.5 QRSS Generation

The XRT86L34 can transmit a QRSS random sequence to a remote location from TTIP/TRING. The polynomial is shown in Table 174.

TABLE 174: RANDOM BIT SEQUENCE POLYNOMIALS

RANDOM PATTERN	T1	E1
QRSS/PRBS	$2^{20} - 1$	$2^{15} - 1$

6.2 T1 LONG HAUL LINE BUILD OUT (LBO)

The long haul transmitter output pulses are generated using a 7-Bit internal DAC (6-Bits plus the MSB sign bit). The line build out can be set to -7.5dB, -15dB, or -22dB cable attenuation by programming the appropriate channel register. The long haul LBO consist of 32 discrete time segments extending over four consecutive periods of TCLK. As the LBO attenuation is increased, the pulse amplitude is reduced so that the waveform complies with ANSI T1.403 specifications. A long haul pulse with -7.5dB attenuation is shown in Figure 76, a pulse with -15dB attenuation is shown in Figure 77, and a pulse with -22.5dB attenuation is shown in Figure 78.

FIGURE 76. LONG HAUL LINE BUILD OUT WITH -7.5DB ATTENUATION

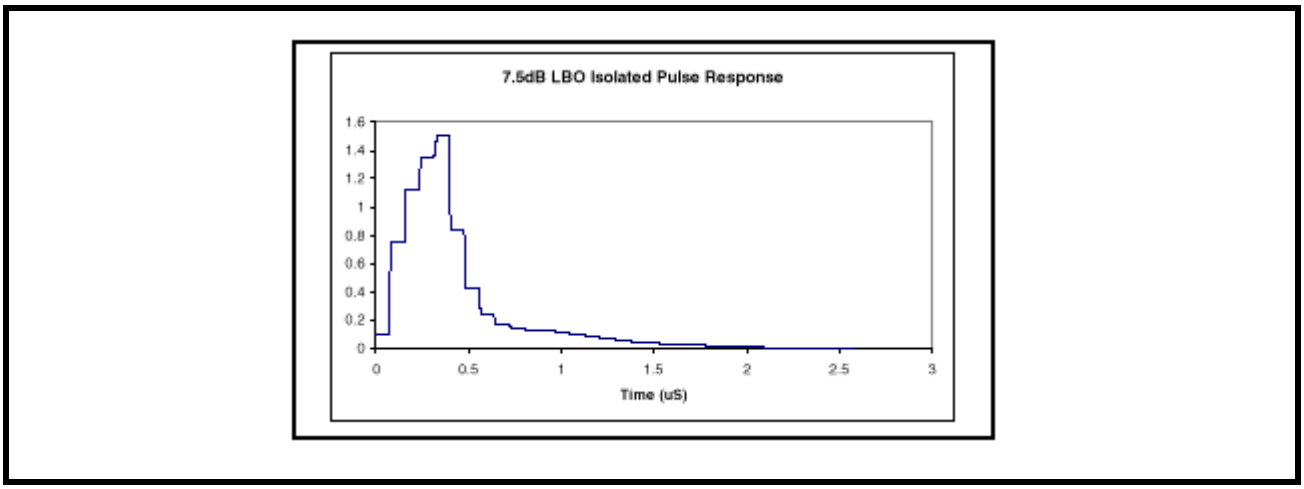


FIGURE 77. LONG HAUL LINE BUILD OUT WITH -15DB ATTENUATION

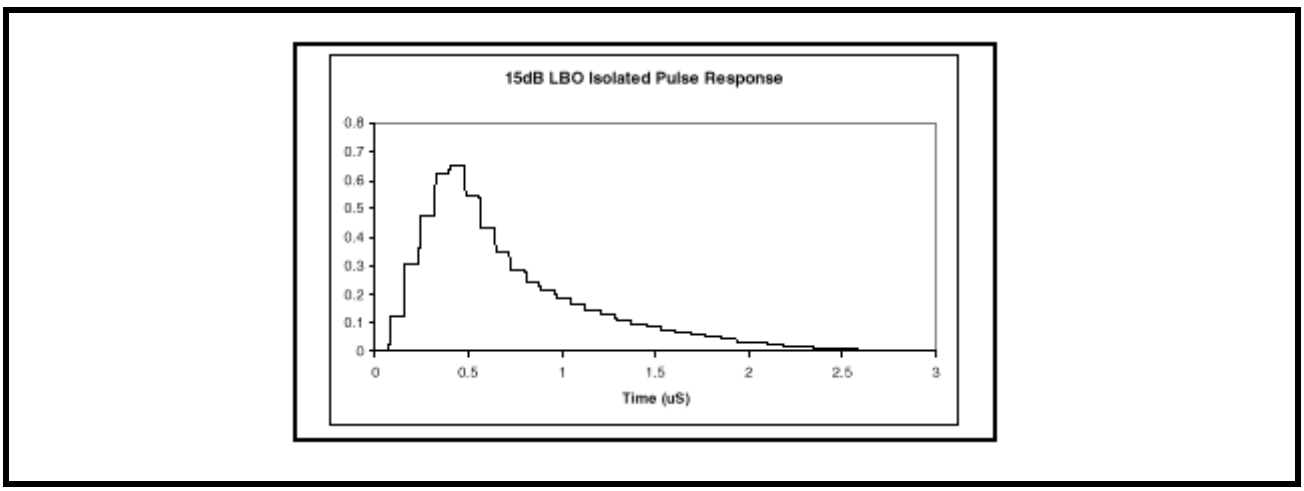
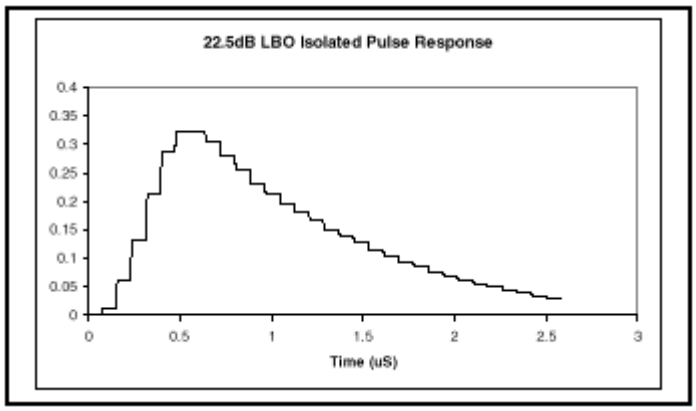


FIGURE 78. LONG HAUL LINE BUILD OUT WITH -22.5DB ATTENUATION



6.3 T1 SHORT HAUL LINE BUILD OUT (LBO)

The short haul transmitter output pulses are generated using a 7-Bit internal DAC (6-Bit plus the MSB sign bit). The line build out can be set to interface to five different ranges of cable attenuation by programming the appropriate channel register. The pulse shape is divided into eight discrete time segments which are set to fixed values to comply with the pulse template. To program the eight segments individually to optimize a special line build out, see the arbitrary pulse section of this datasheet. The short haul LBO settings are shown in Table 175

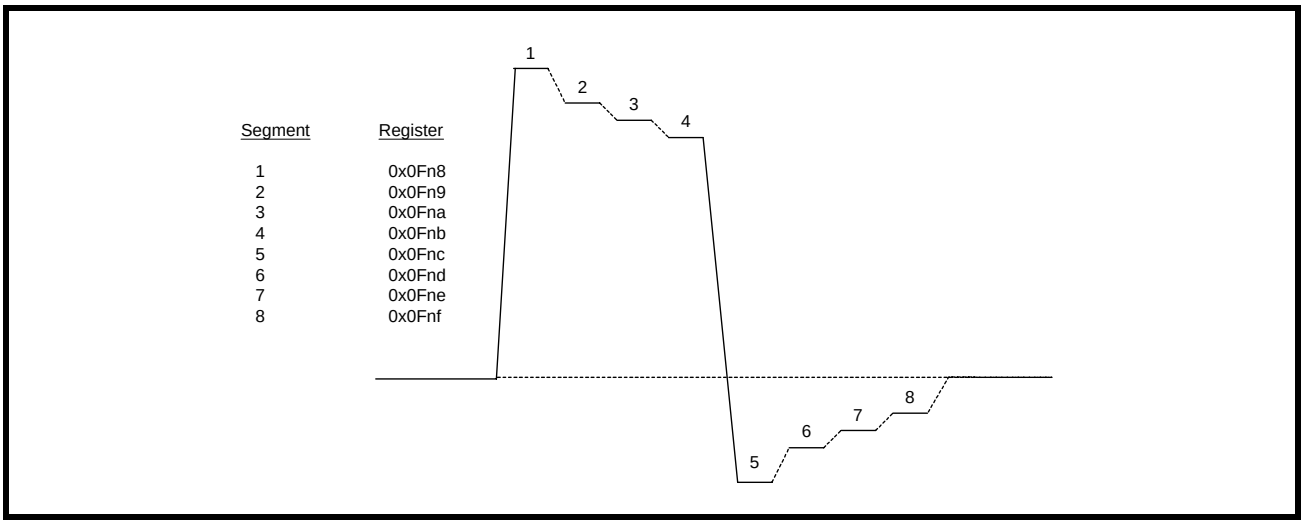
TABLE 175: SHORT HAUL LINE BUILD OUT

LBO SETTING EQC[4:0]	RANGE OF CABLE ATTENUATION
08h (01000)	0 - 133 Feet
09h (01001)	133 - 266 Feet
0Ah (01010)	266 - 399 Feet
0Bh (01011)	399 - 533 Feet
0Ch (01100)	533 - 655 Feet

6.3.1 Arbitrary Pulse Generator

In T1 mode only, the arbitrary pulse generator divides the pulse into eight individual segments. Each segment is set by a 7-Bit binary word by programming the appropriate channel register. This allows the system designer to set the overshoot, amplitude, and undershoot for a unique line build out. The MSB (bit 7) is a sign-bit. If the sign-bit is set to "0", the segment will move in a positive direction relative to a flat line (zero) condition. If this sign-bit is set to "1", the segment will move in a negative direction relative to a flat line condition. The resolution of the DAC is typically 60mV per LSB. Thus, writing 7-bit = 1111111 will clamp the output at either voltage rail corresponding to a maximum amplitude. A pulse with numbered segments is shown in Figure 79.

FIGURE 79. ARBITRARY PULSE SEGMENT ASSIGNMENT



NOTE: *By default, the arbitrary segments are programmed to 0x00h. The transmitter outputs will result in an all zero pattern to the line interface.*

6.3.2 DMO (Digital Monitor Output)

The driver monitor circuit is used to detect transmit driver failures by monitoring the activities at TTIP/TRING outputs. Driver failure may be caused by a short circuit in the primary transformer or system problems at the transmit inputs. If the transmitter of a channel has no output for more than 128 clock cycles, DMO goes "High" until a valid transmit pulse is detected. If the DMO interrupt is enabled, the change in status of DMO will cause the interrupt pin to go "Low". Once the status register is read, the interrupt pin will return "High" and the status register will be reset (RUR).

6.3.3 Transmit Jitter Attenuator

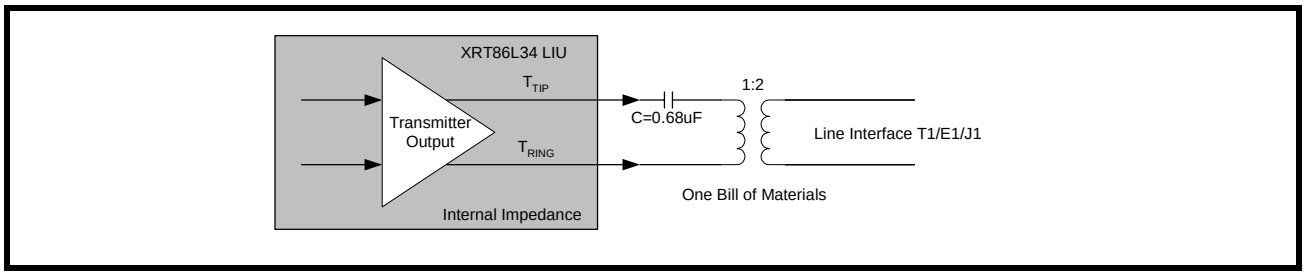
The transmit path has a dedicated jitter attenuator to reduce phase and frequency jitter in the transmit clock. The jitter attenuator uses a data FIFO (First In First Out) with a programmable depth of 32-bit or 64-bit. When the Read and Write pointers of the FIFO are within 2-Bits of over-flowing or under-flowing, the bandwidth of the jitter attenuator is widened to track the short term input jitter, thereby avoiding data corruption. When this condition occurs, the jitter attenuator will not attenuate input jitter until the Read/Write pointer's position is outside the 2-Bit window. In T1 mode, the bandwidth of the JA is always set to 3Hz. In E1 mode, the bandwidth is programmable to either 10Hz or 1.5Hz (1.5Hz automatically selects the 64-Bit FIFO depth). The JA has a clock delay equal to ½ of the FIFO bit depth.

NOTE: *The Receive Path has a dedicated jitter attenuator. See the Receive Path Line Interface Section.*

6.4 LINE TERMINATION (TTIP/TRING)

The output stage of the transmit path generates standard return-to-zero (RZ) signals to the line interface for T1/E1/J1 twisted pair or E1 coaxial cable. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The transmitter outputs only require one DC blocking capacitor of 0.68mF. For redundancy applications (or simply to tri-state the transmitters), set TxTSEL to a "1" in the appropriate channel register. A typical transmit interface is shown in Figure 80.

FIGURE 80. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION



7.0 THE E1 RECEIVE SECTION

7.1 THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK

7.1.1 Description of the Receive Payload Data Output Interface Block

Each of the four framers within the XRT86L34 device includes a Receive Payload Data Output Interface block. The function of the block is to provide an interface to the Terminal Equipment (for example, a Central Office or switching equipment) that has data to receive from a "Far End" terminal over an DS1 or E1 transport medium.

The Payload Data Output Interface module (also known as the Back-plane Interface module) supports payload data to be taken from or presented to the system. In E1 mode, supported data rates are 1.544Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 12.352Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s. In E1 mode, supported data rates are MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s.

The Receive Payload Data Output Interface block supplies or accepts the following signals to the Terminal Equipment circuitry:

- Receive Serial Data Input (RxSer_n)
- Receive Serial Clock (RxSerClk_n)
- Receive Single-frame Synchronization Signal (RxSync_n)
- Receive Multi-frame Synchronization Signal (RxMSync_n)
- Receive Time-slot Indicator Clock (RxTSClk_n)
- Receive Time-slot Indication Bits (RxTSb[4:0]_n)

The Receive Serial Data is an output pin carrying payload, signaling and sometimes Data Link data supplied by XRT86L34 device to the local Terminal Equipment.

The Receive Serial Clock is an input or output signal used by the Receive Payload Data Input Interface block to send out serial data to the local Terminal Equipment. The Receive Clock Inversion bit of the Receive Interface Control Register (TICR) determines at which edge of the Receive Serial Clock would data transition on the Receive Serial Data pin occur.

The table below shows configurations of the Receive Clock Inversion bit of the Receive Interface Control Register (RICR).

RECEIVE INTERFACE CONTROL REGISTER (RICR) (ADDRESS = 0XN122H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Clock Inversion	R/W	0 - Serial data transition happens on rising edge of the Receive Serial Clock. 1 - Serial data transition happens on falling edge of the Receive Serial Clock.

Throughout the discussion of this datasheet, we assume that serial data transition happens on rising edge of the Receive Serial Clock unless stated otherwise.

The Receive Single-frame Synchronization signal is either input or output. When configure as input, it indicates beginning of an E1 frame. When configure as output, it indicates end of an E1 frame.

The Receive Multi-frame Synchronization signal is an output pin from XRT86L34 indicating end of an E1 multi-frame.

By connecting these signals with the local Terminal Equipment, the Receive Payload Data Output Interface routes received payload data from the Receive Framer Module to the local Terminal Equipment.

7.1.2 Brief Discussion of the Receive Payload Data Output Interface Block Operating at XRT84V24 Compatible 2.048Mbit/s mode

The incoming Receive Payload Data is taken into the framer from the LIU interface using the Recovered Receive Line Clock. The payload data is then routed through the Receive Farmer Module and presented to the Receive Payload Data Output Interface through the Receive Serial Data output pin (RxSer_n). This data is then clocked out using the Receive Serial Clock (RxSerClk_n).

There is a two-frame (512 bits) elastic buffer between the Receive Framer Module and the Receive Payload Data Output Interface. This buffer can be enabled or disabled via programming the Slip Buffer Enable [1:0] bits in Slip Buffer Control Register (SBCR).

The following table shows configurations of the Slip Buffer Enable [1:0] bits in Slip Buffer Control Register.

SLIP BUFFER CONTROL REGISTER (SBCR)(ADDRESS = 0XN116H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Slip Buffer Enable	R/W	00 - Slip Buffer is bypassed. The Receive Payload Data is passing from the Receive Framer Module to the Receive Payload Data Output Interface directly without routing through the Slip Buffer. The Receive Serial Clock signal (RxSerClk_n) is an output. 01 - The Elastic Store (Slip Buffer) is enabled. The Receive Payload Data is passing from the Receive Framer Module through the Slip Buffer to the Receive Payload Data Output Interface. The Receive Serial Clock signal (RxSerClk_n) is an input. 10 - The Slip Buffer acts as a FIFO. The FIFO Latency Register (FLR) determines the data latency. The Receive Payload Data is passing from the Receive Framer Module through the FIFO to the Receive Payload Data Output Interface. The Receive Serial Clock signal (RxSerClk_n) is an input. 11 - Slip Buffer is bypassed. The Receive Payload Data is passing from the Receive Framer Module to the Receive Payload Data Output Interface directly without routing through the Slip Buffer. The Receive Serial Clock signal (RxSerClk_n) is an output.

If the Slip Buffer is not in bypass mode, then the user has the option of either providing the Receive Single-Frame Synchronization pulse or getting the Receive Single-Frame Synchronization pulse on frame boundary at the RxSync_n pin. The Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register (SBCR) determines whether the Receive Single-Frame Synchronization signal is input or output. The table below demonstrates settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register.

SLIP BUFFER CONTROL REGISTER (SBCR)(ADDRESS = 0XN116H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Slip Buffer Receive Synchronization Direction	R/W	0 - The Receive Single-Frame Synchronization signal (RxSync_n) is an output if the Slip Buffer is not in bypass mode. 1 - The Receive Single-Frame Synchronization signal (RxSync_n) is an input if the Slip Buffer is not in bypass mode.

If the Slip Buffer is in bypass mode, the Receive Payload Data is routed to the Receive Payload Data Output Interface from the Receive Framer Module directly. The Recovered Line Clock is used to carry the Receive Payload Data all the way from the LIU interface, to the Receive Framer Module and eventually output through the Receive Serial Data output pin. The Receive Serial Clock signal is therefore an output using the Recovered Receive Line Clock as timing source. The Receive Single-Frame Synchronization signal is also output in Slip Buffer bypass mode.

If the Slip Buffer is enabled, the Receive Payload Data is latched into the Elastic Store using the Recovered Receive Line Clock. The local Terminal Equipment supplies a free-running 2.048MHz clock to the Receive Serial Clock pin to latch the Receive Payload Data out from the Elastic Store. Since the Recovered Receive Line Clock and the Receive Serial Clock are coming from different timing sources, the Slip Buffer will gradually fill or empty. If the elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties and a read occurs, then a full frame of data will be repeated and a status bit will be updated. If the buffer fills and a write comes, then a full frame of data will be deleted and another status bit will be set. A detailed description of the Elastic Buffer can be found in later sections. In this mode, the Receive Single-Frame Synchronization signal can be either input or output depending on the settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register.

If the Slip Buffer is put into a FIFO mode, it is acting like a standard First-In-First-Out storage. A fixed READ and WRITE latency is maintained in a programmable fashion controlled by the FIFO Latency Register (FIFOLR). The local Terminal Equipment supplies a 2.048MHz clock to the Receive Serial Clock pin to latch the Receive Payload Data out from the FIFO. However, it is the responsibility of the user to phase lock the input Receive Serial Clock to the Recovered Receive Line Clock to avoid either over-run or under-run of the FIFO. In this mode, the Receive Single-Frame Synchronization signal can be either input or output depending on the settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register.

The following table summaries the input or output nature of the Receive Serial Clock and Receive Single-Frame Synchronization signals for different Slip Buffer settings.

RECEIVE TIMING SOURCE	RXSERCLK_N	RXSYNC_N	
		Slip Buffer Synchronization Direction Bit = 0	Slip Buffer Synchronization Direction Bit = 1
Slip Buffer Bypassed	Output	Output	Output
Slip Buffer Enabled	Input	Output	Input
Slip Buffer Acts as FIFO	Input	Output	Input

The Receive Time-slot Indication Bits (RxTSb[4:0]_n) are multiplexed I/O pins. The functionality of these pins is governed by the value of Receive Fractional E1 Output Enable bit of the Receive Interface Control Register (RICR). The following table illustrates the configurations of the Receive Fractional E1 Input Enable bit.

RECEIVE INTERFACE CONTROL REGISTER (RICR) (ADDRESS = 0XN122H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Fractional E1 Output Enable	R/W	0 - The Receive Time-slot Indication bits (RxTSb[4:0] are outputting five-bit binary values of Time-slot number (0-31) being accepted and processed by the Receive Payload Data Output Interface block of the framer. The Receive Time-slot Indicator Clock signal (RxTSClk_n) is a 256KHz clock that pulses HIGH for one E1 bit period whenever the Receive Payload Data Output Interface block is accepting the LSB of each of the twenty-four time slots. 1 - The RxTSb[0]_n bit becomes the Receive Fractional E1 Output signal (RxFrTD_n) which carries Fractional E1 payload data from the framer. The RxTSb[1]_n bit becomes the Receive Signaling Data Output signal (RxSig_n) which is used to carry robbed-bit signaling data extracted from the inbound E1 frame. The RxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-31) being accepted and processed by the Receive Payload Data Output Interface block of the framer. The RxTSClk_n will output gaped fractional E1 clock that can be used by Terminal Equipment to latch in Fractional E1 payload data at rising edge of the clock. Or, The RxTSClk_n pin will be a clock enable signal to Receive Fractional E1 Output signal (RxFrTD_n) when the un-gaped Receive Serail Output Clock (RxSerClk_n) is used to latch in Fractional E1 Payload Data into the Terminal Equipment.

When configured to operate in normal condition (that is, when the Receive Fractional E1 Input Enable bit is equal to zero), these bits reflect the five-bit binary value of the Time Slot number (0-31) being outputted and processed by the Receive Payload Data Output Interface block of the framer. RxTSb[4] represents the MSB of the binary value and RxTSb[0] represents the LSB.

When the Receive Fractional E1 Output Enable bit is equal to one, the RxTSb[0]_n bit becomes the Receive Fractional E1 Output signal (RxFrTD_n). This output pin carries Fractional E1 Output data extracted by the framer from the incoming E1 data stream. The Fractional E1 Output Interface allows certain time-slots of E1 data to be routed to destinations other than the local Terminal Equipment. Function of the Fractional E1 Output signal will be discussed in details in later sections.

When the Receive Fractional E1 Output Enable bit is equal to one, the RxTSb[1]_n bit becomes the Receive Signaling Data Output signal (RxSig_n). These output pins can be used to carry robbed-bit signaling data extracted from the inbound E1 frame. Function of the Receive Signaling Data Output signal will be discussed in details in later sections.

When the Receive Fractional E1 Output Enable bit is equal to one, the RxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-31) being outputted and processed by the Receive Payload Data Output Interface block of the framer. MSB of the binary value is presented first and the LSB is presented last.

The RxTSb[3]_n and RxTSb[4}_n pins are not multiplexed.

The table below shows functionality of the RxTSb[2:0] bits when the Receive Fractional E1 Output bit is set to different values.

Receive Fractional E1 Output Bit = 0		Receive Fractional E1 Output Bit = 1	
RxTSb[0]	Output	RxFrTD	Output
RxTSb[1]	Output	RxSig	Output
RxTSb[2]	Output	RxTS	Output

The Receive Time-slot Indicator Clock signal (RxTSClk_n) is a multi-function output pin. When configured to operate in normal condition (that is, when the Receive Fractional E1 Input Enable bit is equal to zero), the RxTSClk_n is a 256KHz clock that pulses HIGH for one E1 bit period whenever the Receive Payload Data Output Interface block is outputting the LSB of each of the twenty-four time slots. The local Terminal Equipment should use this clock signal to sample the RxTSb[0] through RxTSb[4] bits and identify the time-slot being processed via the Receive Section of the framer.

When the Receive Fractional E1 Output Enable bit is equal to one, the RxTSClk_n will output gaped fractional E1 clock whenever Fractional E1 payload data is present at the RxFrTD_n pin. The local Terminal Equipment can latch in Fractional E1 payload data at falling edge of the clock. Otherwise, this pin will be a clock enable signal to Receive Fractional E1 output signal (RxFrTD_n) if the framer is configured accordingly. In this way, Fractional E1 payload data is clocked into the Terminal Equipment using un-gaped Receive Serial Output Clock (RxSerClk_n). A detailed discussion of the Fractional E1 Payload Data Output Interface can be found in later sections.

A detailed discussion of how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment with Slip Buffer enabled or disabled can be found in the later sections.

7.1.2.1 Connect the Receive Payload Data Output Interface block to the Local Terminal Equipment if the Slip Buffer is bypassed

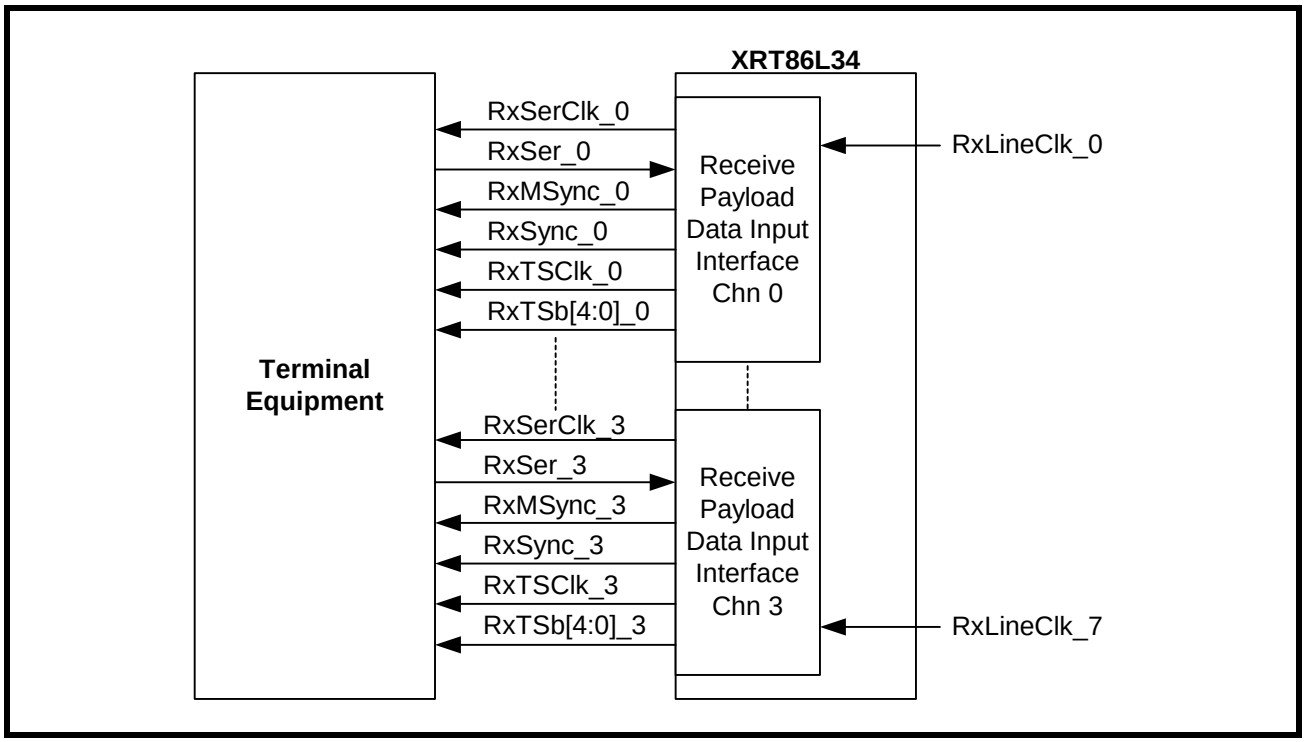
By setting the Slip Buffer Enable [1:0] bits of the Slip Buffer Control Register to 00 or 11, the Receive Framer Module routes the Receive Payload Data directly to the Receive Payload Data Output Interface without passing through the Elastic Buffer. The XRT86L34 device uses the Recovered Receive Line Clock internally to carry the Receive Payload Data directly across the whole chip. The Recovered Receive Line Clock is essentially become timing source of the Receive Serial Clock output.

If the Slip Buffer is bypassed, the Receive Single-frame Synchronization signal is automatically configured to be output signals. It should pulse HIGH for one E1 bit period (488ns) at the last bit position of each E1 frame. By triggering on the HIGH pulse on the Receive Single-frame Synchronization signal, the Terminal Equipment can identify the end of an E1 frame and should prepare to accept payload data of the next E1 frame from the framer.

The Receive Multi-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the last bit position of an E1 multi-frame. By triggering on the HIGH pulse on the Receive Multi-frame Synchronization signal, the framer can identify the end of an E1 super-frame and should prepare to accept payload data of the next E1 super-frame from the framer.

See Figure 81 for how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is bypassed and the Recovered Receive Line Clock is timing source of the Receive section.

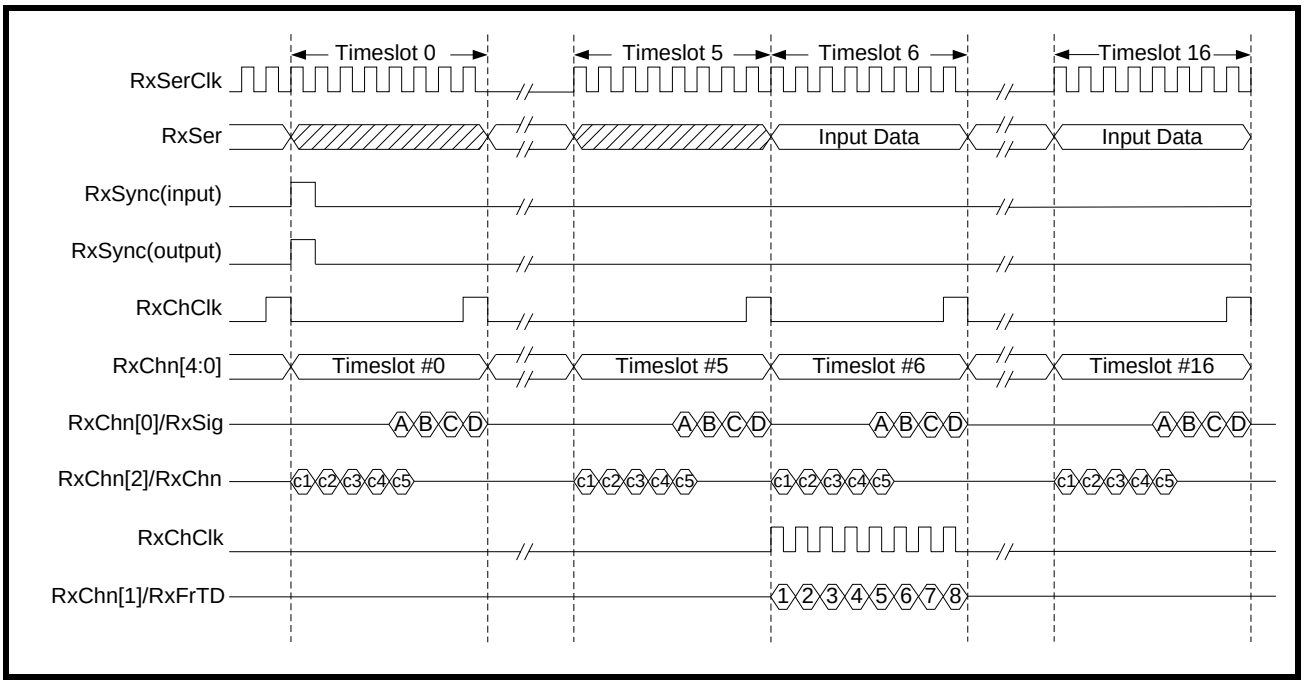
FIGURE 81. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT WITH SLIP BUFFER BYPASSED AND RECOVERED RECEIVE LINE CLOCK AS RECEIVE TIMING SOURCE



The following Figure 82 shows waveforms of the signals (RxSerClk_n, RxSer_n, RxSync_n, RxTSClk_n and RxTSb[4:0]_n) which connecting the Receive Payload Data Output Interface block to the local Terminal Equip-

ment when the Slip Buffer is bypassed and the Recovered Receive Line Clock is timing source of the Receive section.

FIGURE 82. WAVEFORMS OF THE SIGNALS CONNECTING THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WHEN THE SLIP BUFFER IS BYPASSED AND THE RECOVERED LINE CLOCK IS THE TIMING SOURCE OF THE RECEIVE SECTION



7.1.2.2 Connect the Receive Payload Data Output Interface block to the Local Terminal Equipment if the Slip Buffer is enabled

By setting the Slip Buffer Enable [1:0] bits of the Slip Buffer Control Register to 01, the framer includes the two-frame Elastic Buffer into its data path. The Receive Framer Module routes the Receive Payload Data to the Elastic Buffer first. The Receive Payload Data is then presented to the Receive Payload Data Output Interface. The XRT86L34 device uses the Recovered Receive Line Clock internally to clock in the Receive Payload Data into the Elastic Buffer. The Terminal Equipment should provide a 2.048MHz clock to the Receive Serial Clock input pin to latch data out from the Elastic Buffer.

The Recovered Receive Line Clock and the Receive Serial Clock are generated from two different timing sources. That is, the Recovered Receive Line Clock is originating from a remote site while Receive Serial Clock generating by a local oscillator. Any mismatch in frequencies of these two clocks will result in the Slip Buffer to gradually fill or deplete.

Overtime, the Elastic Buffer either fills or empties completely. Once that happened, a controlled slip by the XRT86L34 device will occur. The Receive Slip Buffer Slip bit of the Slip Buffer Status Register (SBSR) is set to 1.

If the buffer empties and a read occurs, then a full frame of data will be repeated and the Receive Slip Buffer Empty bit of the Slip Buffer Status Register (SBSR) will be forced HIGH. If the buffer fills and a write comes, then a full frame of data will be deleted and the Receive Slip Buffer Full bit of the Slip Buffer Status Register (SBSR) will be forced HIGH.

The following table demonstrates settings of the Receive Slip Buffer Slip bit, Receive Slip Buffer Empty bit and Receive Slip Buffer Full bit of the Slip Buffer Status Register.

SLIP BUFFER STATUS REGISTER (SBSR)(ADDRESS = 0XNB08H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Slip Buffer Full	R/W	0 - The Receive Slip Buffer is not full. 1 - The Receive Slip Buffer is full and one frame of data is discarded.
1	Receive Slip Buffer Empty	R/W	0 - The Receive Slip Buffer is not empty. 1 - The Receive Slip Buffer is empty and one frame of data is repeated.
1	Receive Slip Buffer Slip	R/W	0 - The Receive Slip Buffer does not slip. 1 - The Receive Slip Buffer slips since either full or emptied.

In this mode, the Receive Single-Frame Synchronization signal can be either input or output depending on the settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register. When the Slip Buffer Receive Synchronization Direction bit is set to 0, the Receive Single-Frame Synchronization signal (RxSync_n) is an. When the Slip Buffer Receive Synchronization Direction bit is set to 1,the Receive Single-Frame Synchronization signal (RxSync_n) is an input.

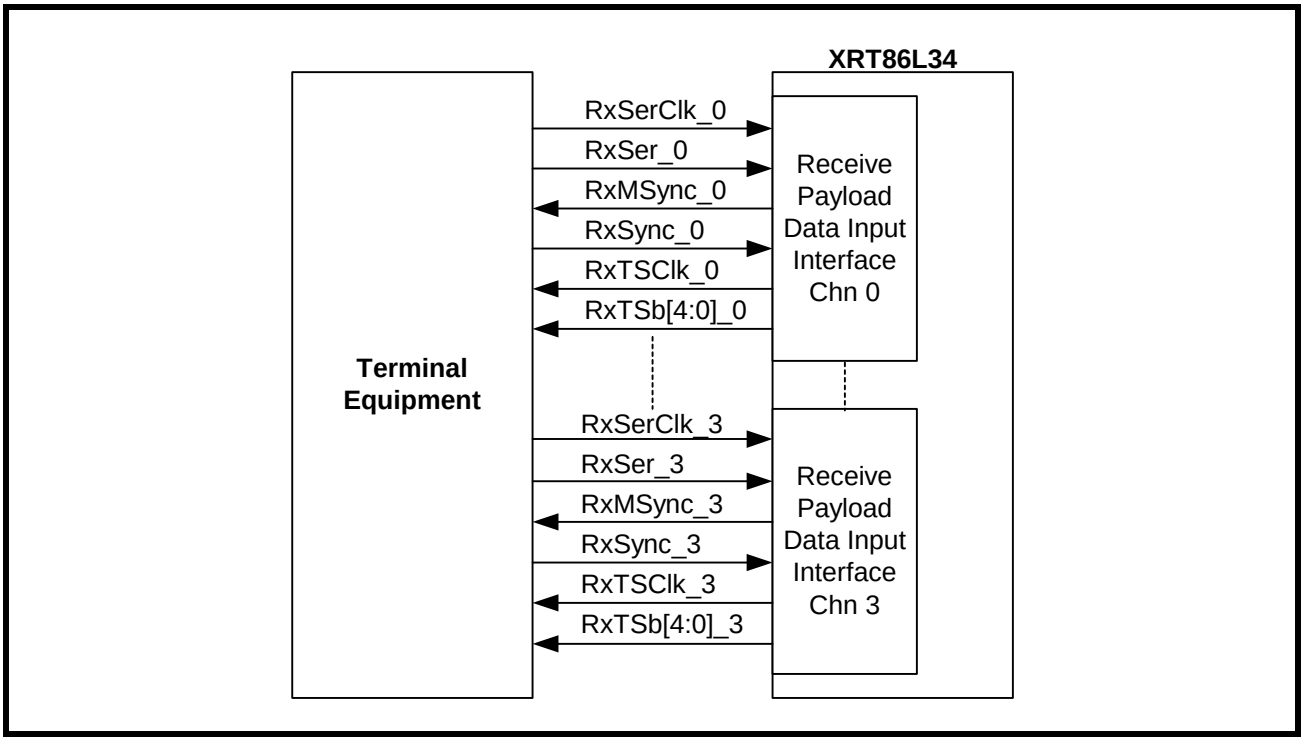
If the Receive Single-Frame Synchronization signal is an output, it should pulse HIGH for one E1 bit period (488ns) at the last bit position of each E1 frame. By triggering on the HIGH pulse on the Receive Single-frame Synchronization signal, the Terminal Equipment can identify the end of an E1 frame and should prepare to accept payload data of the next E1 frame from the framer.

If the Receive Single-Frame Synchronization signal is an input, it should pulse HIGH for one E1 bit period (488ns) at the first bit position (F-bit) of each E1 frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer should identity the beginning of an E1 frame and can send out data in a synchronized way. It is the responsibility of the local Terminal Equipment to align the start of an E1 frame with the Receive Single-Frame Synchronization pulse.

The Receive Multi-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the last bit position of Frame number one of an E1 multi-frame. By triggering on the HIGH pulse on the Receive Multi-frame Synchronization signal, the framer can identify the end of an E1 super-frame and should prepare to accept payload data of the next E1 super-frame from the framer.

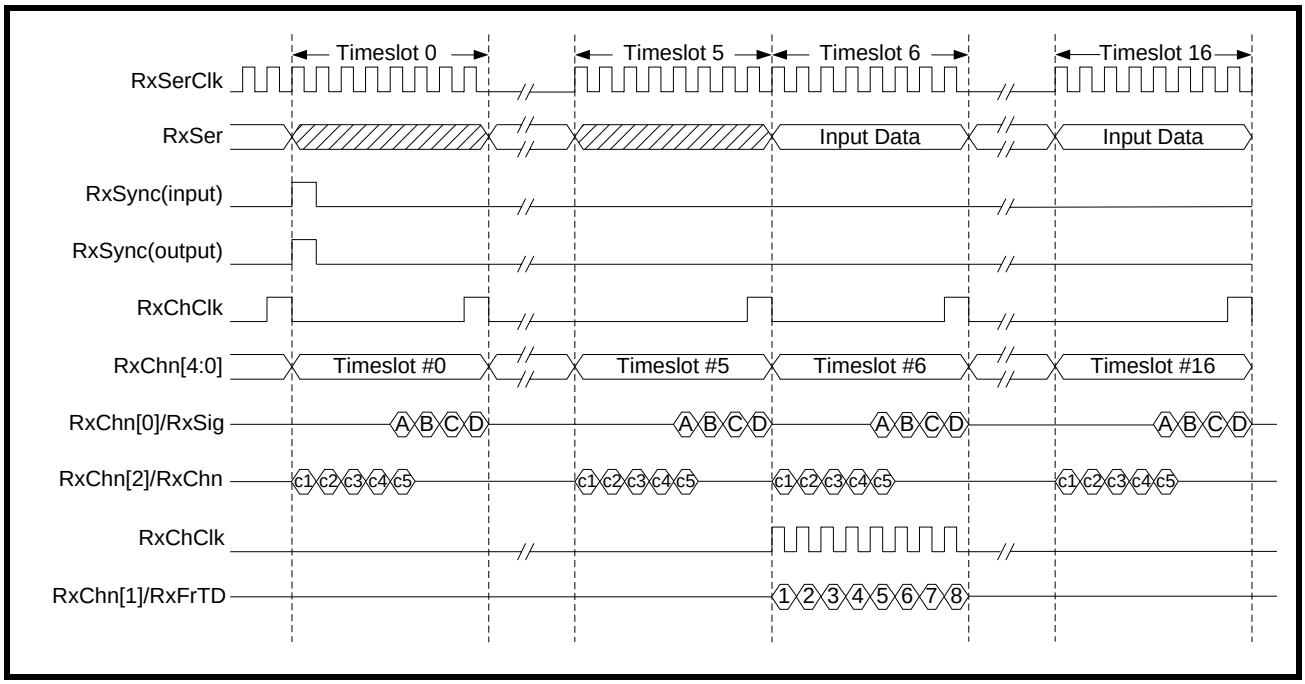
See Figure 83 for how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is enabled.

FIGURE 83. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT WITH SLIP BUFFER ENABLED OR ACTS AS FIFO



The following Figure 84 shows waveforms of the signals (RxSerClk_n, RxSer_n, RxSync_n, RxTSClk_n and RxTSb[4:0]_n) which connecting the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is enabled.

FIGURE 84. WAVEFORMS OF THE SIGNALS THAT CONNECT THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WHEN THE SLIP BUFFER IS ENABLED



7.1.2.3 Connect the Receive Payload Data Output Interface block to the Local Terminal Equipment if the Slip Buffer is configured as FIFO

By setting the Slip Buffer Enable [1:0] bits of the Slip Buffer Control Register to 10, the framer puts the Elastic Buffer into FIFO mode. Receive Framer Module routes the Receive Payload Data through the First-In-First-Out storage to the Receive Payload Data Output Interface. The XRT86L34 device uses the Recovered Receive Line Clock internally to clock in the Receive Payload Data into the FIFO. The Terminal Equipment should provide an external 2.048MHz clock to the Receive Serial Clock input pin to latch data out from the FIFO.

It is the responsibility of the user to phase lock the input Receive Serial Clock to the Recovered Receive Line Clock to avoid either over-run or under-run of the FIFO. The latency between writing a bit into the FIFO and reading the same bit from it (READ and WRITE latency) is actually depth of the FIFO, which is maintained in a programmable fashion controlled by the FIFO Latency Register (FIFOLR). The largest possible depth of the FIFO is thirty-two bytes or one E1 frame. The default depth of the FIFO when XRT86L34 first powered up is four bytes. The table below shows the FIFO Latency Register.

FIFO LATENCY REGISTER (FIFOL) (ADDRESS = 0XN117H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4-0	FIFO Latency	R/W	These bits determine depth of the FIFO in terms of bytes. The largest possible value is thirty-two bytes or one E1 frame.

In this mode, the Receive Single-Frame Synchronization signal can be either input or output depending on the settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register. When the Slip Buffer Receive Synchronization Direction bit is set to 0, the Receive Single-Frame Synchronization signal (RxSync_n) is an. When the Slip Buffer Receive Synchronization Direction bit is set to 1,the Receive Single-Frame Synchronization signal (RxSync_n) is an input.

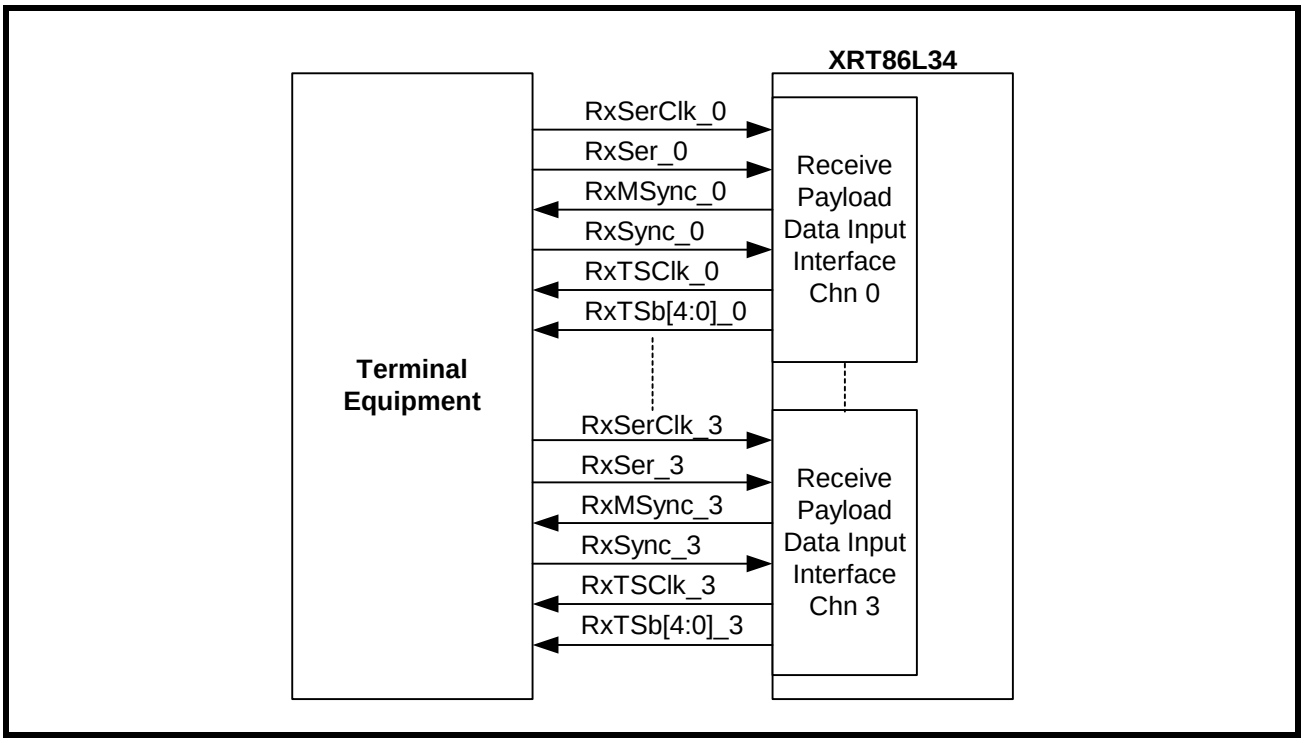
If the Receive Single-Frame Synchronization signal is an output, it should pulse HIGH for one E1 bit period (488ns) at the last bit position of each E1 frame. By triggering on the HIGH pulse on the Receive Single-frame Synchronization signal, the Terminal Equipment can identify the end of an E1 frame and should prepare to accept payload data of the next E1 frame from the framer.

If the Receive Single-Frame Synchronization signal is an input, it should pulse HIGH for one E1 bit period (488ns) at the first bit position (F-bit) of each E1 frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer should identity the beginning of an E1 frame and can send out data in a synchronized way. It is the responsibility of the local Terminal Equipment to align the start of an E1 frame with the Receive Single-Frame Synchronization pulse.

The Receive Multi-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the last bit position of Frame number one of an E1 multi-frame. By triggering on the HIGH pulse on the Receive Multi-frame Synchronization signal, the framer can identify the end of an E1 super-frame and should prepare to accept payload data of the next E1 super-frame from the framer.

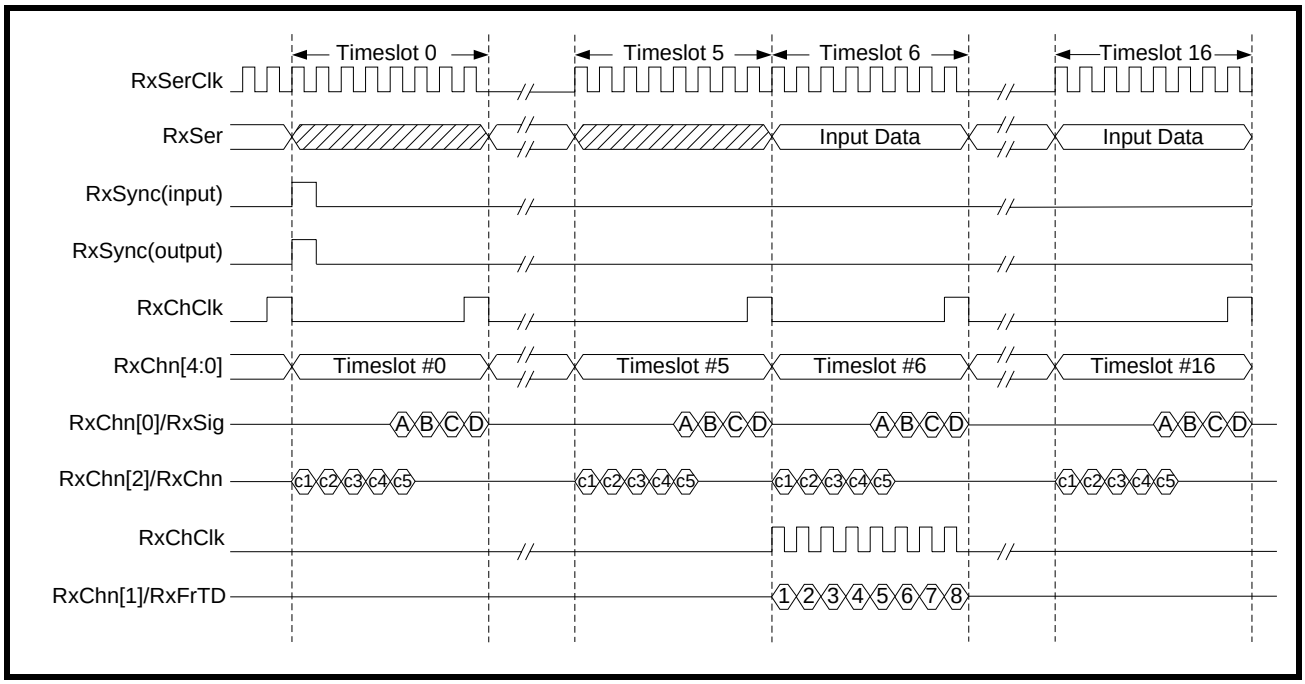
See Figure 85 for how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is acted as FIFO.

FIGURE 85. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT WITH SLIP BUFFER ENABLED OR ACTS AS FIFO



The following Figure 86 shows waveforms of the signals (RxSerClk_n, RxSer_n, RxSync_n, RxTSClk_n and RxTSb[4:0]_n) which connecting the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is acted as FIFO.

FIGURE 86. WAVEFORMS OF THE SIGNALS THAT CONNECT THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WHEN THE SLIP BUFFER IS ACTED AS FIFO



7.1.3 High Speed Receive Back-plane Interface

The High-speed Back-plane Interface supports payload data to be taken from or presented to the local Terminal Equipment at different data rates. In E1 mode, supported High-speed data rates are MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s. The Receive Multiplex Enable bit and the Receive Interface Mode Select [1:0] bits of the Receive Interface Control Register (RICR) determine the Receive Back-plane Interface data rate.

The following table shows configurations of the Receive Multiplex Enable bit and the Receive Interface Mode Select [1:0] bits of the Receive Interface Control Register (RICR).

RECEIVE INTERFACE CONTROL REGISTER (RICR) (ADDRESS = 0XN122H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Multiplex Enable	R/W	0 - The Receive Back-plane Interface block is configured to non-channel-multiplexed mode 1 - The Receive Back-plane Interface block is configured to channel-multiplexed mode
1-0	Receive Interface Mode Select	R/W	When combined with the Receive Multiplex Enable bit, these bits determine the Receive Back-plane Interface data rate.

The table below shows the combinations of Receive Multiplex Enable bit and Receive Interface Mode Select [1:0] bits and the resulting Receive Back-plane Interface data rates.

RECEIVE MULTIPLEX ENABLE BIT	RECEIVE INTERFACE MODE SELECT BIT 1	RECEIVE INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE
0	0	0	XRT84V24 Compatible 2.048Mbit/s
0	0	1	MVIP 2.048Mbit/s
0	1	0	4.096Mbit/s
0	1	1	8.192Mbit/s
1	0	0	-
1	0	1	Bit Multiplexed 16.384Mbit/s
1	1	0	HMVIP 16.384Mbit/s
1	1	1	H.100 16.384Mbit/s

When the Receive Multiplex Enable bit is set to zero, the framer is configured in non-channel-multiplexed mode. The possible data rates are XRT84V24 Compatible 2.048Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s. In non-channel-multiplexed mode, payload data of each channel are sending out from the Receive High-speed Back-plane Interface separately. Each channel uses its own Receive Serial Clock, Receive Serial Data, Receive Single-frame Synchronization signal and Receive Multi-frame Synchronization signal as interface between the framer and the Terminal Equipment. Section 2.1.1.1, 2.1.1.2 and 2.1.1.3 provide details on how to connect the Receive Payload Data Interface block with the local Terminal Equipment when the Back-plane interface data rate is 2.048Mbit/s.

When the Back-plane interface data rate is MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s, the Receive Serial Clock, Receive Serial Data and Receive Single-frame Synchronization are all configured as inputs. The Receive Multi-frame Synchronization signal is still output. The Receive Serial Clock is configured as an input timing source for the High-speed Back-plane Interface with frequencies of 2.048 MHz, 4.096 MHz and 8.192 MHz respectively.

The table below summaries the clock frequencies of RxSerClk_n input when the framer is operating in non-multiplexed High-speed Back-plane mode.

RECEIVE MULTIPLEX ENABLE BIT = 0

RECEIVE INTERFACE MODE SELECT BIT 1	RECEIVE INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE	RXSERCLK
0	0	XRT84V24 Compatible 2.048Mbit/s	2.048MHz
0	1	MVIP 2.048Mbit/s	2.048 MHz
1	0	4.096Mbit/s	4.096 MHz
1	1	8.192Mbit/s	8.192 MHz

When the Receive Multiplex Enable bit is set to one, the framer is configured in channel-multiplexed mode. The possible data rates are bit-multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s and H.100 16.384Mbit/s. In channel-multiplexed mode, four channels share the Receive Serial Data, Receive Single-frame Synchronization signal and Receive Serial Clock of one channel as interface between the framer and the Terminal Equipment. The Receive Serial Clock runs at frequencies of 12.352 MHz or 16.384 MHz. It serves as the primary clock source for the High-speed Back-plane Interface.

Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4. The Re-

ceive Single-frame Synchronization signal of Channel 0 pulses HIGH at the beginning of the frame with data from Channel 0-3 multiplexed together. The Receive Single-frame Synchronization signal of Channel 4 pulses HIGH at the beginning of the frame with data from Channel 4-7 multiplexed together.

The table below summaries the clock frequencies of RxSerClk_n input when the framer is operating in multiplexed High-speed Back-plane mode.

RECEIVE MULTIPLEX ENABLE BIT = 1

RECEIVE INTERFACE MODE SELECT BIT 1	RECEIVE INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE	RXSERCLK
0	0	-	-
0	1	Bit-multiplexed 16.384Mbit/s	16.384 MHz
1	0	HMVIP 16.384Mbit/s	16.384 MHz
1	1	H.100 16.384Mbit/s	16.384 MHz

When the frame is running at High-speed Back-plane Interface mode other than the 2.048Mbit/s data rate, the Receive Single-frame Synchronization signal could pulse HIGH or LOW indicating boundaries of E1 frames. The Receive Synchronization Pulse Low bit of the Receive Interface Control Register (TICR) determines whether the Receive Single-frame Synchronization signal is HIGH active or LOW active.

The table below shows configurations of the Receive Synchronization Pulse LOW bit of the Receive Interface Control Register (RICR).

RECEIVE INTERFACE CONTROL REGISTER (RICR)(ADDRESS = 0XN122H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Synchronization Pulse LOW	R/W	0 - The Receive Single-frame Synchronization signal will pulse HIGH indicating the beginning of an E1 frame when the High-speed Back-plane Interface is running at a mode other than the 2.048Mbit/s. 1 - The Receive Single-frame Synchronization signal will pulse LOW indicating the beginning of an E1 frame when the High-speed Back-plane Interface is running at a mode other than the 2.048Mbit/s.

Throughout the discussion of this datasheet, we assume that the Receive Single-frame Synchronization signal pulses HIGH unless stated otherwise.

The following sections discuss details of how to operate the framer in different Back-plane interface speed mode and how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment.

7.1.3.1 E1 Receive Input Interface - MVIP 2.048 MHz

When the Receive Multiplex Enable bit is set to zero and the Receive Interface Mode Select [1:0] bits are set to 01, the Receive Back-plane interface of framer is running at a data rate of 2.048Mbit/s.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

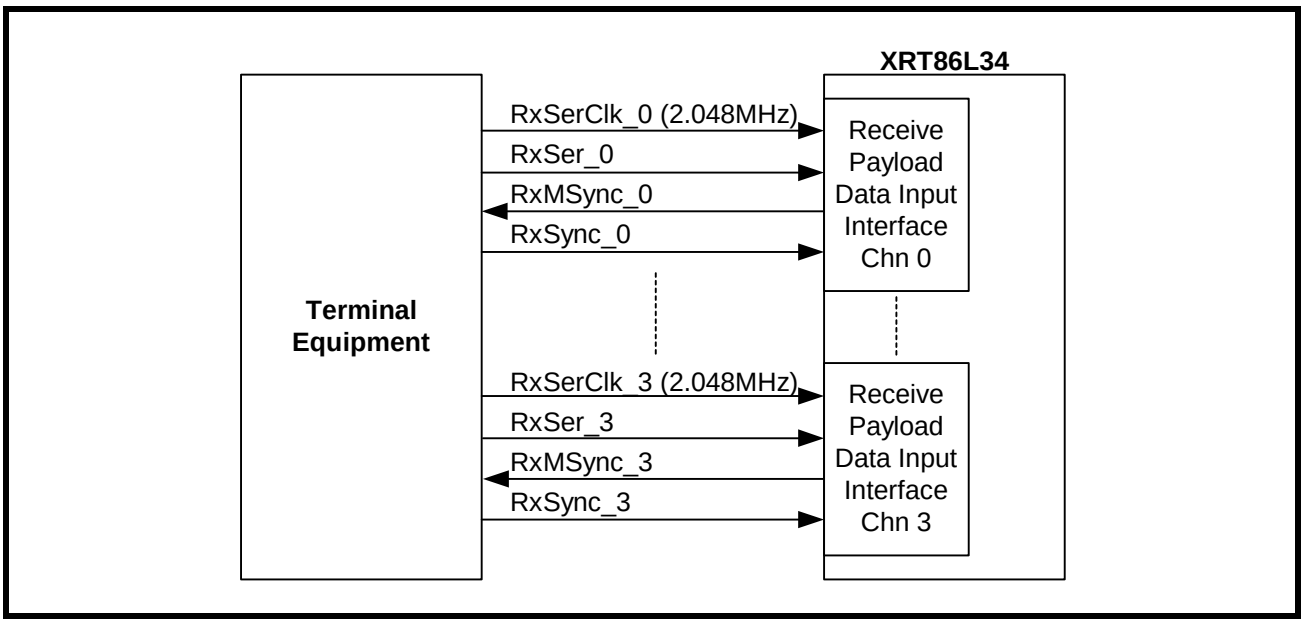
The Receive Back-plane interface is pumping out data through RxSer_n at an E1 equivalent data rate of 2.048Mbit/s. The local Terminal Equipment supplies a free-running 2.048MHz clock to the Receive Serial Clock input. The Receive High-speed Back-plane Interface of the framer then sends out serial data at rising

edge of the Receive Serial Clock. The local Terminal Equipment samples the serial data at falling edge of the clock.

The Receive Single-frame Synchronization input signal (RxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer can identity the beginning of an E1 frame and start pumping payload data out.

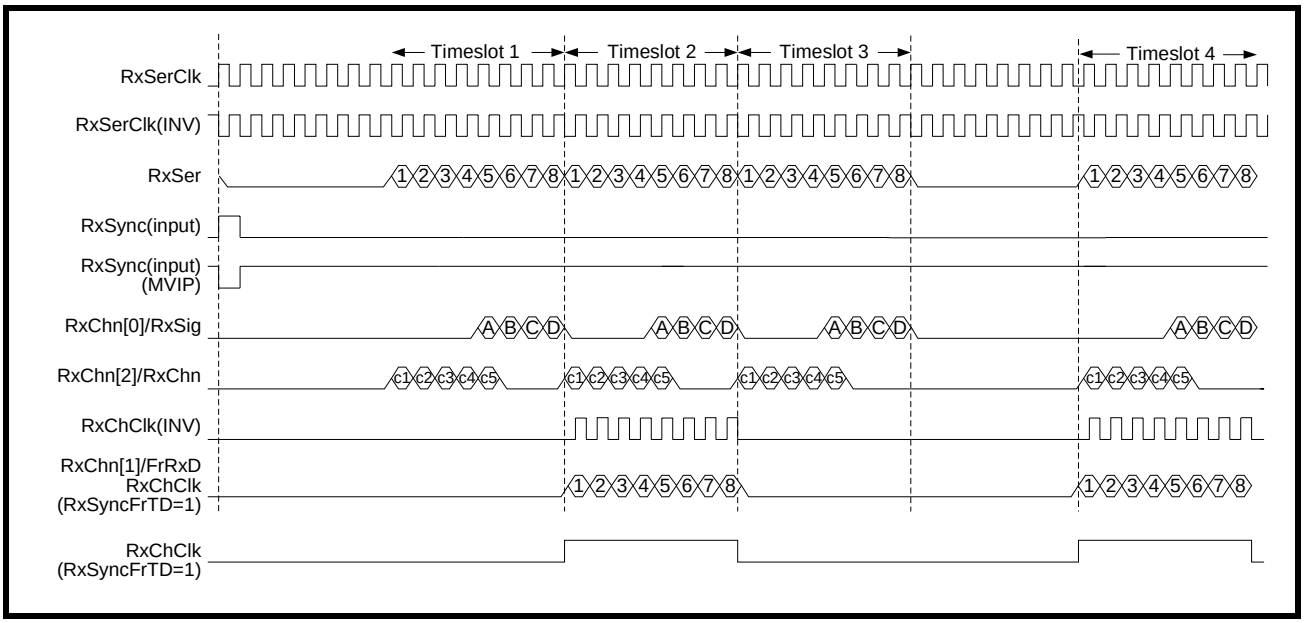
See Figure 87 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in MVIP 2.048Mbit/s mode.

FIGURE 87. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING MVIP 2.048MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at MVIP 2.048Mbit/s mode is shown in Figure 88.

FIGURE 88. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT MVIP 2.048MBIT/S



7.1.3.2 E1 Receive Input Interface - 4.096 MHz

(This interface mode is the same as running at 2.048 MHz. The only difference is that the Receive Serial Clock runs two times faster at 4.096 MHz)

When the Receive Multiplex Enable bit is set to zero and the Receive Interface Mode Select [1:0] bits are set to 10, the Receive Back-plane interface of framer is running at a clock rate of 4.096MHz.

The interface consists of the following pins:

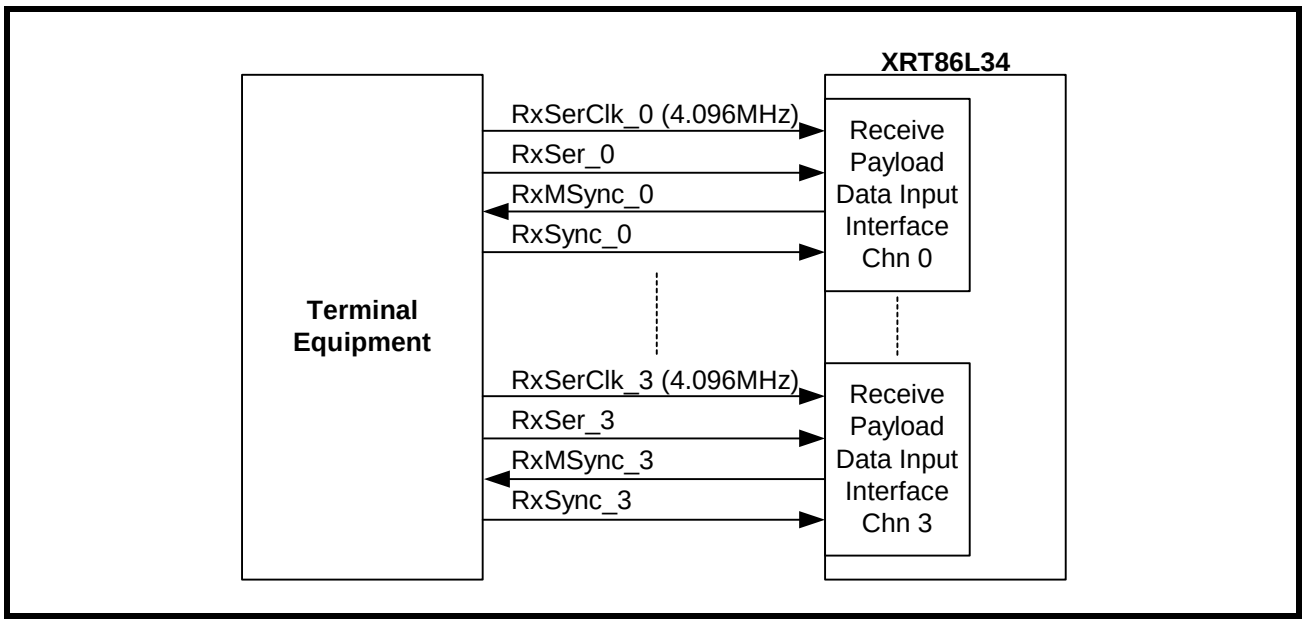
- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane interface is pumping out data through RxSer_n at an E1 equivalent data rate of 2.048Mbit/s. The local Terminal Equipment supplies a free-running 4.096MHz clock to the Receive Serial Clock input. The Receive High-speed Back-plane Interface of the framer then sends out serial data at every other rising edge of the Receive Serial Clock. The local Terminal Equipment samples the serial data at every other falling edge of the clock.

The Receive Single-frame Synchronization input signal (RxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer can identity the beginning of an E1 frame and start pumping payload data out.

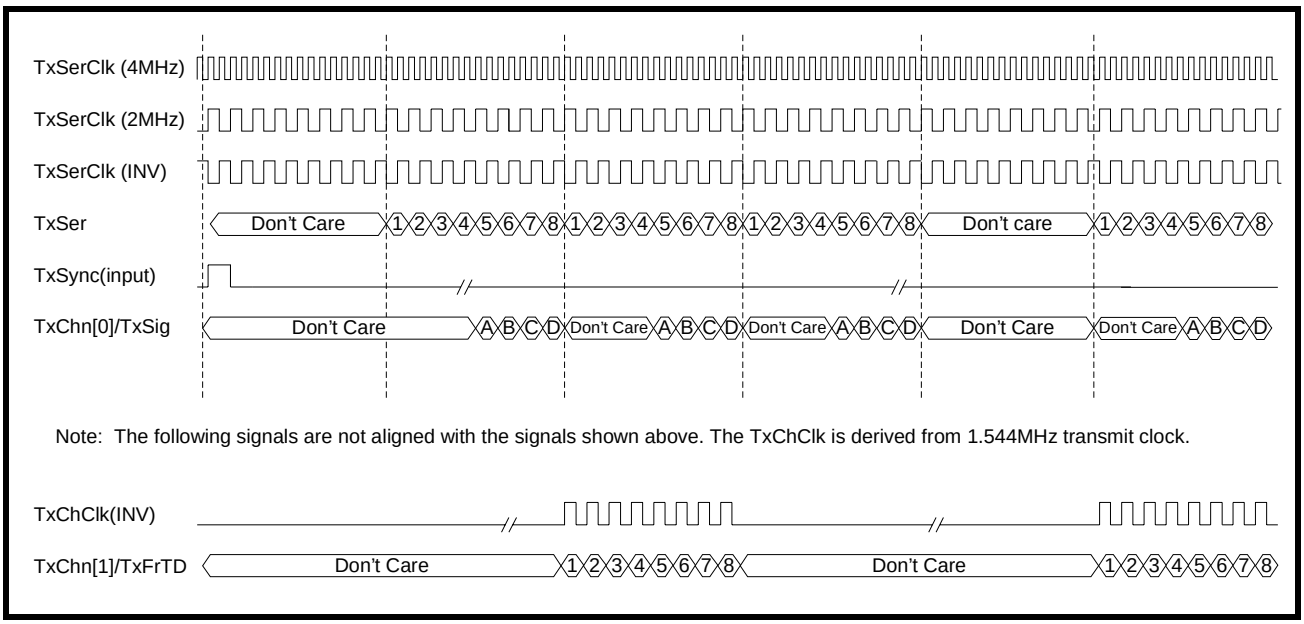
See Figure 89 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in 4.096Mbit/s mode.

FIGURE 89. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING 4.096MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at 4.096Mbit/s mode is shown in Figure 90.

FIGURE 90. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 4.096MBIT/S MODE



7.1.3.3 E1 Receive Input Interface - 8.192 MHz

(This interface mode is the same as running at 2.048 MHz. The only difference is that the Receive Serial Clock runs four times faster at 8.192MHz)

When the Receive Multiplex Enable bit is set to zero and the Receive Interface Mode Select [1:0] bits are set to 11, the Receive Back-plane interface of framer is running at a clock rate of 8.192MHz.

The interface consists of the following pins:

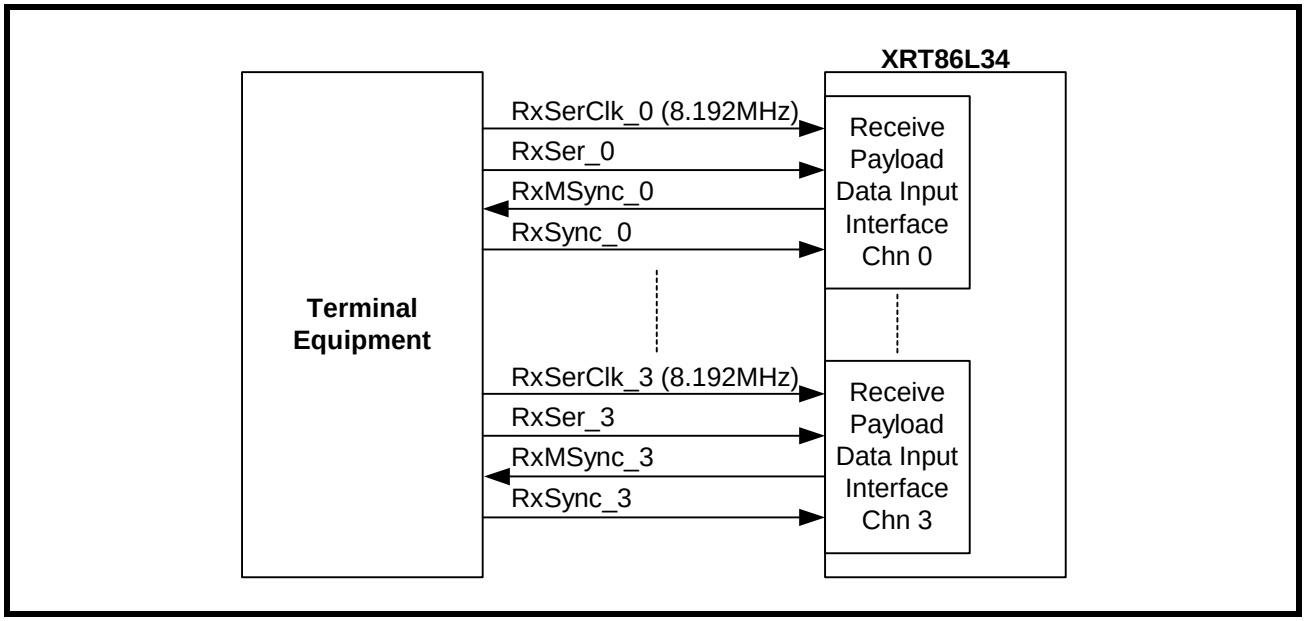
- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane interface is pumping out data through RxSer_n at an E1 equivalent data rate of 2.048Mbit/s. The local Terminal Equipment supplies a free-running 8.192MHz clock to the Receive Serial Clock input. The Receive High-speed Back-plane Interface of the framer then sends out serial data at every other four rising edge of the Receive Serial Clock. The local Terminal Equipment samples the serial data at every other four falling edge of the clock.

The Receive Single-frame Synchronization input signal (RxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer can identity the beginning of an E1 frame and start pumping payload data out.

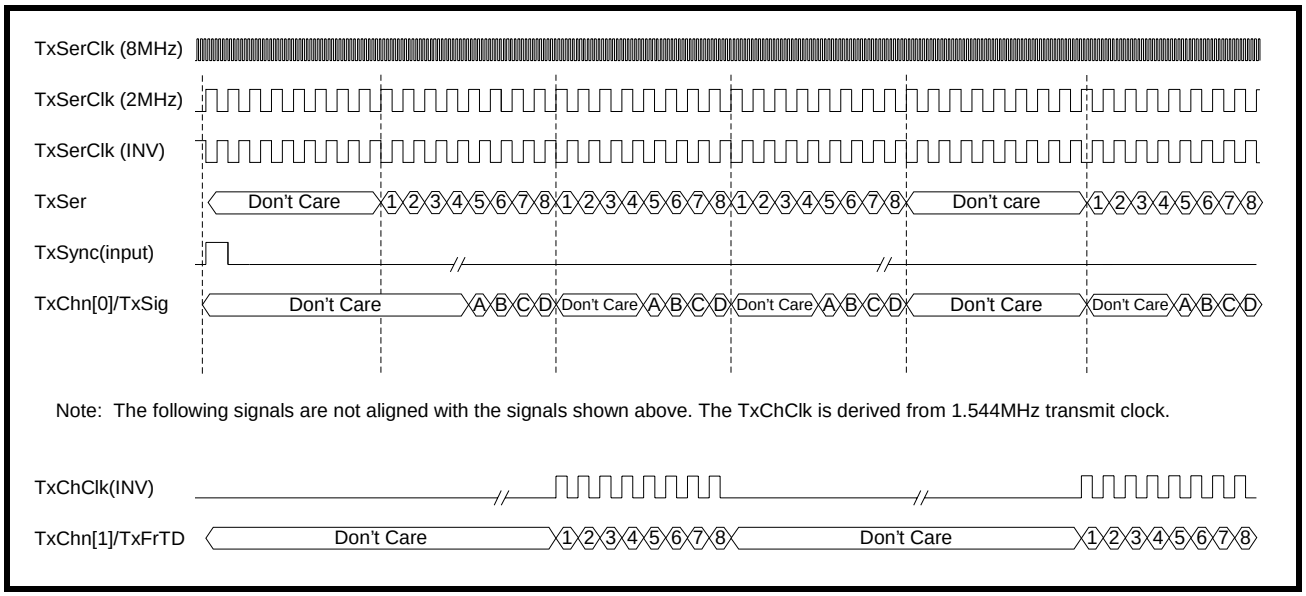
See Figure 91 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in 8.192Mbit/s mode.

FIGURE 91. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING 8.192MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at 8.192Mbit/s mode is shown in Figure 92.

FIGURE 92. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 8.192MBIT/S MODE



7.1.3.4 E1 Receive Input Interface - Bit-Multiplexed 16.384Mbit/s

When the Receive Multiplex Enable bit is set to one and the Receive Interface Mode Select [1:0] bits are set to 01, the Receive Back-plane interface of framer is running at a clock rate of 16.384MHz.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)

- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane Interface is pumping out data through RxSer_0 or RxSer_4 pins at 16.384Mbit/s. It multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz are supplied to the Receive Serial Clock pin of Channel 0 and Channel 4 of the framer. The Receive High-speed Back-plane Interface of the farmer provides data at rising edge of this Receive Serial Clock. The local Terminal Equipment then latches incoming serial data at falling edge of the clock.

The Receive High-speed Back-plane Interface maps four 2.048Mbit/s E1 data streams into this 16.384Mbit/s data stream as described below:

1. Payload data of four channels are repeated and grouped together in a bit-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the first payload bit of Timeslot 0 of Channel 1 and 2. The first payload bit of Timeslot 0 of Channel 3 is sent last.

After the first bits of Timeslot 0 of all four channels are sent, it comes the second bit of Timeslot 0 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	1_1	1_1	1_2	1_2	1_3	1_3

SECOND OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
2_0	2_0	2_1	2_1	2_2	2_2	2_3	2_3

X_Y: The Xth payload bit of Channel Y

2. The Receive High-speed Back-plane Interface also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream.

When the Receive High-speed Back-plane Interface is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

FIFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	5_1	A_1	5_2	A_2	5_3	A_3

SIXTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
6_0	B_0	6_1	B_1	6_2	B_2	6_3	B_3

SEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
7_0	C_0	7_1	C_1	7_2	C_2	7_3	C_3

EIGHTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
8_0	D_0	8_1	D_1	8_2	D_2	8_3	D_3

X_Y: The Xth payload bit of Channel Y

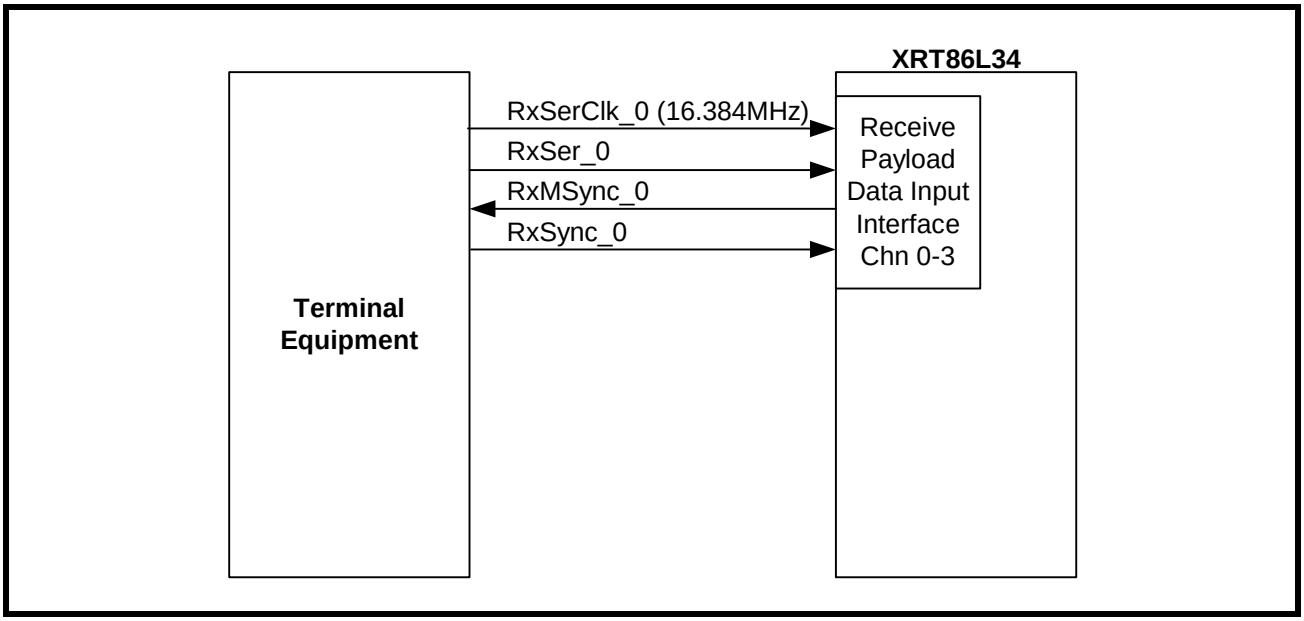
A_Y: The signaling bit A of Channel Y

3. After the first octets of all four channels are sent, the Receive High-speed Back-plane Interface will start sending the second octets following the same rules of Step 1 and 2.

The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH for one clock cycle at the first bit position of the data stream with data from Channel 0-3 multiplexed together. The Receive Single-frame Synchronization signal of Channel 4 pulses HIGH for one clock cycle at the first bit position of the data stream with data from Channel 4-7 multiplexed together. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the Receive High-speed Back-plane Interface of the framer can identify the beginning of a multiplexed frame and can start sending payload data of that frame.

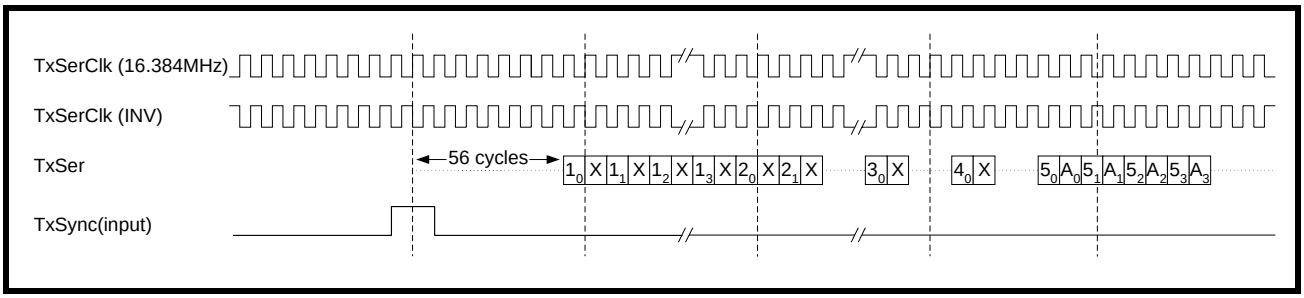
See Figure 93 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in Bit-multiplexed 16.384Mbit/s mode.

FIGURE 93. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING 16.384 MBIT/S DATA BUS



The Input signal timing is shown in Figure 94 below when the framer is running at Bit-Multiplexed 16.384Mbit/s mode.

FIGURE 94. IMING SIGNAL WHEN THE FRAMER IS RUNNING AT BIT-MULTIPLEXED 16.384MBIT/S MODE



7.1.3.5 E1 Receive Input Interface - HMVIP 16.384Mbit/s

When the Receive Multiplex Enable bit is set to one and the Receive Interface Mode Select [1:0] bits are set to 10, the Receive Back-plane interface of framer is running at a clock rate of 16.384MHz.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane Interface is pumping out data through RxSer_0 or RxSer_4 pins at 16.384Mbit/s. The Receive High-speed Back-plane Interface multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin

of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz are supplied to the Receive Serial Clock pin of Channel 0 and Channel 4 of the framer. The Receive High-speed Back-plane Interface of the farmer provides data at rising edge of this Receive Serial Clock. The local Terminal Equipment then latches incoming serial data at falling edge of the clock.

The Receive High-speed Back-plane Interface maps four 2.048Mbit/s E1 data streams into this 16.384Mbit/s data stream as described below:

1. Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Terminal Equipment will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent the last.

After the payload bits of Timeslot 0 of all four channels are sent, it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

THIRD OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

FIFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

SEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

X_Y: The Xth payload bit of Channel Y

2. The Receive High-speed Back-plane Interface also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream.

When the Receive High-speed Back-plane Interface is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

SECOND OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	6_0	B_0	7_0	C_0	8_0	D_0

FOURTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_1	A_1	6_1	B_1	7_1	C_1	8_1	D_1

SIXTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_2	A_2	6_2	B_2	7_2	C_2	8_2	D_2

EIGHTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_3	A_3	6_3	B_3	7_3	C_3	8_3	D_3

X_Y: The Xth payload bit of Channel Y

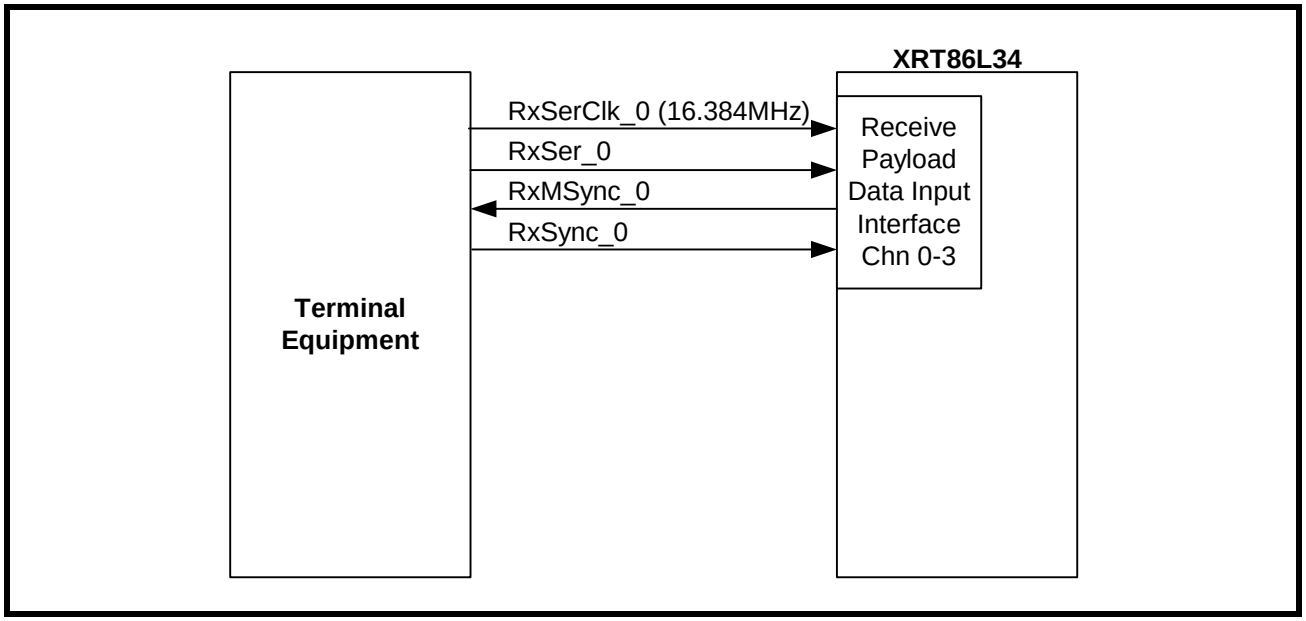
A_Y: The signaling bit A of Channel Y

3. After the first octets of all four channels are sent, the Receive High-speed Back-plane Interface will start sending the second octets following the same rules of Step 1 and 2.

The Receive Single-frame Synchronization signal should pulse HIGH for four clock cycles (the last two bit positions of the previous multiplexed frame and the first two bits of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the Receive High-speed Back-plane Interface of the framer can identify the beginning of a multiplexed frame and can start sending payload data of that frame.

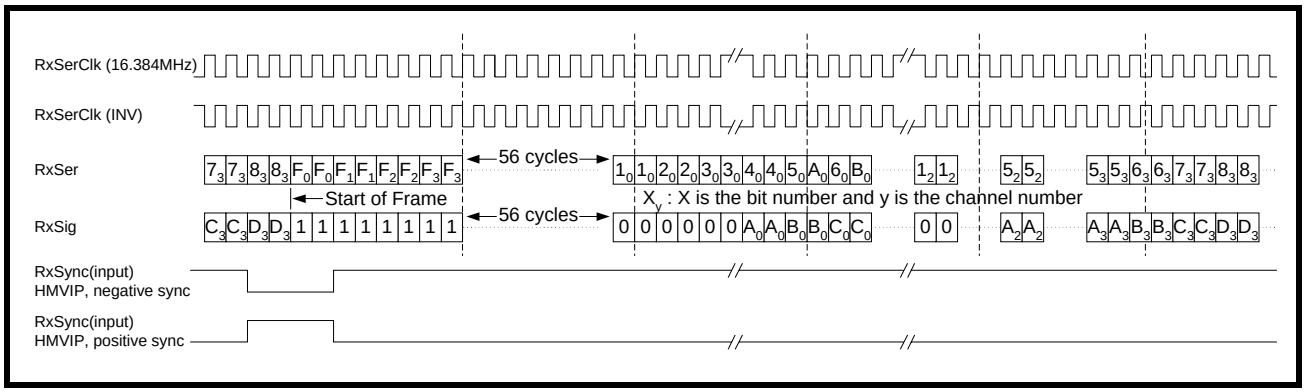
See Figure 95 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in HMVIP 16.384Mbit/s mode.

FIGURE 95. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 96 below when the framer is running at HMVIP 16.384Mbit/s mode.

FIGURE 96. TIMING SIGNAL WHEN THE FRAMER IS RUNNING AT HMVIP 16.384MBIT/S MODE



7.1.3.6 E1 Receive Input Interface - H.100 16.384Mbit/s

When the Receive Multiplex Enable bit is set to one and the Receive Interface Mode Select [1:0] bits are set to 11, the Receive Back-plane interface of framer is running at H.100 16.384Mbit/s mode.

(The HMVIP mode and the H.100 mode are essential the same except for the HIGH pulse position of the Receive Single-frame Synchronization Signal)

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane Interface is pumping out data through RxSer_0 or RxSer_4 pins at 16.384Mbit/s. The Receive High-speed Back-plane Interface multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz are supplied to the Receive Serial Clock pin of Channel 0 and Channel 4 of the framer. The Receive High-speed Back-plane Interface of the farmer provides data at rising edge of this Receive Serial Clock. The local Terminal Equipment then latches incoming serial data at falling edge of the clock.

The Receive High-speed Back-plane Interface maps four 2.048Mbit/s E1 data streams into this 16.384Mbit/s data stream as described below:

1. Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Receive High-speed Back-plane Interface will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent the last.

After the payload bits of Timeslot 0 of all four channels are sent, it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

THIRD OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

FIFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

SEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

X_Y: The Xth payload bit of Channel Y

2. The Receive High-speed Back-plane Interface also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream.

When the Receive High-speed Back-plane Interface is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

SECOND OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	6_0	B_0	7_0	C_0	8_0	D_0

FOURTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_1	A_1	6_1	B_1	7_1	C_1	8_1	D_1

SIXTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_2	A_2	6_2	B_2	7_2	C_2	8_2	D_2

EIGHTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_3	A_3	6_3	B_3	7_3	C_3	8_3	D_3

X_Y: The Xth payload bit of Channel Y

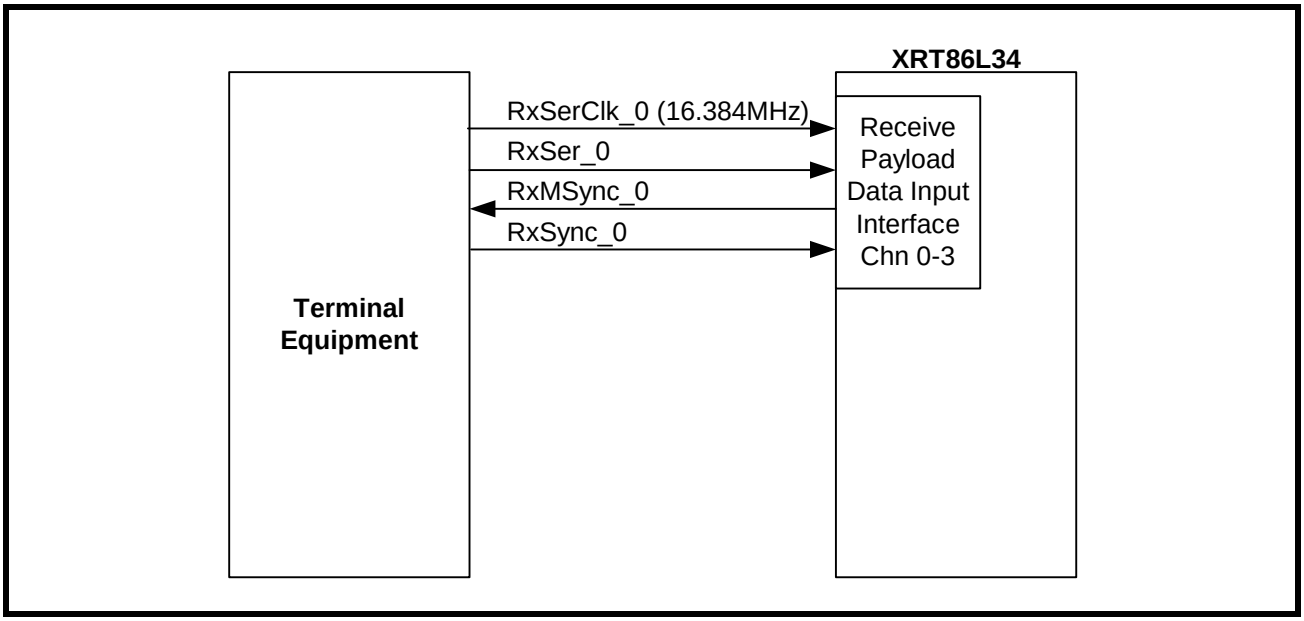
A_Y: The signaling bit A of Channel Y

3. After the first octets of all four channels are sent, the Receive High-speed Back-plane Interface will start sending the second octets following the same rules of Step 1 and 2.

The Receive Single-frame Synchronization signal should pulse HIGH for two clock cycles (the last bit position of the previous multiplexed frame and the first bit position of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the Receive High-speed Back-plane Interface of the framer can identify the beginning of a multiplexed frame and can start sending payload data of that frame.

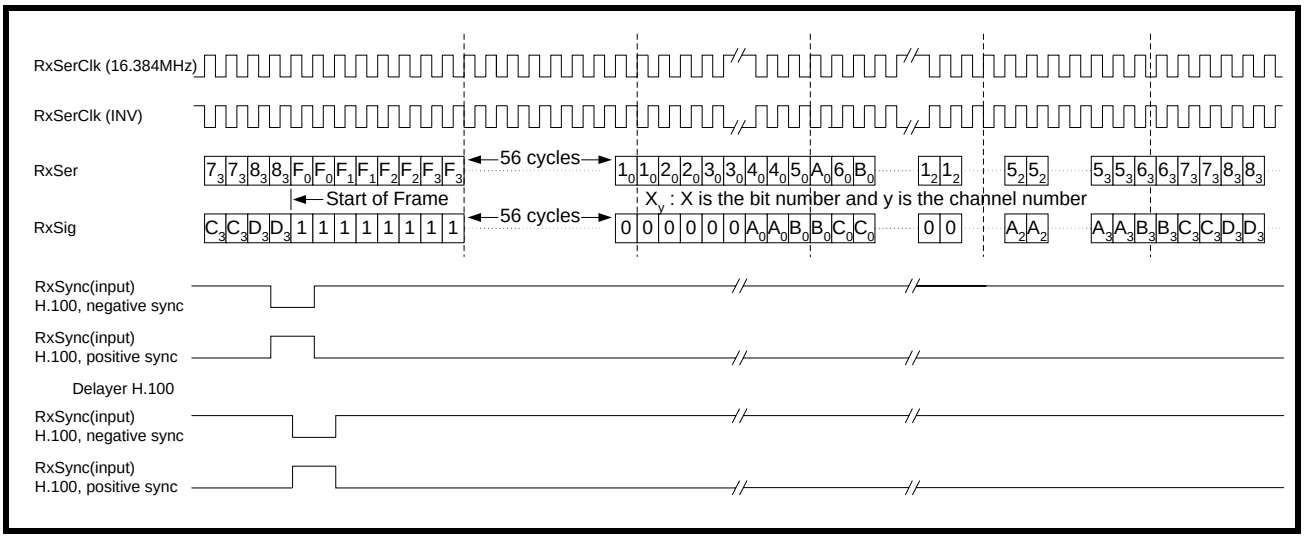
See Figure 97 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in HMVIP 16.384Mbit/s mode.

FIGURE 97. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 98 below when the framer is running at H.100 16.384Mbit/s mode.

FIGURE 98. TIMING SIGNAL WHEN THE FRAMER IS RUNNING AT H.100 16.384MBIT/S MODE



7.2 E1 RECEIVE FRAMER BLOCK

7.2.1 How to Configure XRT86L34 to Operate in E1 Mode

The XRT86L34 Octal T1/E1/J1 Framer supports DS1, J1 or E1 framing modes. Since J1 standard is very similar to DS1 standard with a few minor changes, the J1 framing mode is included as a sub-set of the DS1 framing mode. All four framers within the XRT86L34 silicon can be individually configured to support DS1, J1 or E1 framing modes.

NOTE: *If transmitting section of one framer is configured to support either one of the framing modes, the receiving section is automatically configured to support the same framing modes.*

The T1/E1 Select bit of the Clock Select Register (CSR) controls which framing mode, that is, T1/J1 or E1, supported by the framer. The table below illustrates configurations of the T1/E1 Select bit of the Clock Select Register (CSR).

CLOCK SELECT REGISTER (CSR)(ADDRESS = 0XN100H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	T1/E1 Select	R/W	0 - The XRT86L34 framer is running in E1 mode. 1 - The XRT86L34 framer is running in T1 mode.

The purpose of the E1 Transmit Framer block is to embed and encode user payload data into frames and to route this E1 frame data to the Transmit E1 LIU Interface block. Please note that the XRT86L34 has four (4) individual E1 Transmit Framer blocks. Hence, the following description applies to all four of these individual Transmit E1 Framer blocks.

The purpose of the E1 Transmit Framer block is:

- To encode user data, inputted from the Terminal Equipment into a standard framing format.
- To provide individual data control and signaling conditioning of each DS0 channel.
- To support the transmission of HDLC messages, from the local transmitting terminal, to the remote receiving terminal.
- To transmit indications that the local receive framer has received error frames from the remote terminal.
- To transmit alarm condition indicators to the remote terminal.

The following sections discuss the functionalities of E1 Transmit Framer block in details. We will also describe how to configure the XRT86L34 to transmit E1 frames according to system requirement of users.

7.2.2 How to Configure the Framer to Receive Data in Various E1 Framing Formats

The XRT86L34 Octal T1/E1/J1 Framer is designed to meet the requirement of ITU-T Recommendation G.704. The E1 framer supports the following:

- Frame Alignment Signal (FAS)
- CRC-4 Multi-frame

The ITU-T Recommendation G.704 also specifies two forms of signaling that can be supported by the E1 Transport medium:

- Channel Associated Signaling (CAS)
- Common Channel Signaling (CCS)

The XRT86L34 framer supports both CAS, CCS signaling format together with Clear Channel without signaling.

7.2.3 How to configure the framer to choose FAS searching algorithm

The XRT86L34 framer can use two algorithms to search for FAS pattern and thus declare FAS alignment synchronization. The FAS Selection bit of the Framing Select Register (FSR) allows the user to choose which one of the two algorithms for searching FAS frame alignment.

The table below shows configurations of the FAS Selection bit of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (ADDRESS = 0XN107H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	FAS Selection bit	R/W	This Read/Write bit field allows the user to determine which algorithm is used for searching FAS frame alignment pattern. When an FAS alignment pattern is found and locked, the XRT86L34 will generate Receive Synchronization (RxSync_n) pulse. 0 - Algorithm 1 is selected for searching FAS frame alignment pattern. 1 - Algorithm 2 is selected for searching FAS frame alignment pattern.

7.2.4 How to configure the framer to enable CRC-4 Multi-frame alignment and select the locking criteria

The CRC-4 Selection [1:0] bits of the Framing Select Register (FSR) enable the framer to search for CRC-4 Multi-frame alignment and select the criteria for locking the CRC-4 Multi-frame alignment.

The table below shows configurations of the CRC-4 Selection [1:0] bit of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (ADDRESS = 0XN107H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	CRC-4 Selection bit	R/W	Theses Read/Write bit fields allow the user to enable searching of CRC-4 Multi-frame alignment and determine what criteria are used for locking the CRC-4 Multi-frame alignment pattern. 00 - Searching of CRC-4 Multi-frame alignment is disabled. The XRT86L34 framer will not search for CRC-4 Multi-frame alignment and thus will not declare CRC-4 Multi-frame synchronization. No Receive CRC-4 Multi-frame Synchronization (RxCRCMsync_n) pulse will be generated by the framer. 01 - Searching of CRC-4 Multi-frame alignment is enabled. The XRT86L34 will search for and declare CRC-4 Multi-frame synchronization if: At least one valid CRC-4 Multi-frame alignment signal is observed within 8 ms. 10 - Searching of CRC-4 Multi-frame alignment is enabled. The XRT86L34 will search for and declare CRC-4 Multi-frame synchronization if: At least two valid CRC-4 Multi-frame alignment signals are observed within 8 ms. The time separating two CRC-4 Multi-frame alignment signals is multiple of 2 ms. 11 - Searching of CRC-4 Multi-frame alignment is enabled. The XRT86L34 will search for and declare CRC-4 Multi-frame synchronization if: At least three valid CRC-4 Multi-frame alignment signals are observed within 8 ms. The time separating two CRC-4 Multi-frame alignment signals is multiple of 2 ms.

7.2.5 How to configure the framer to enable CAS Multi-frame alignment

The XRT86L34 framer can use two algorithms to search for CAS Multi-frame alignment pattern. Upon detecting of CAS Multi-frame alignment pattern, the framer will declare CAS Multi-frame alignment synchronization and generate the Receive CAS Multi-frame synchronization pulse (RxCASMsync_n). The CAS Selection [1:0] bits of the Framing Select Register (FSR) enable the framer to search for CAS Multi-frame alignment.

The table below shows configurations of the CAS Selection [1:0] bit of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (ADDRESS = 0XN107H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	CAS Selection bit	R/W	These Read/Write bit fields allow the user to enable searching of CAS Multi-frame alignment and determine which algorithm of the two are used for locking the CAS Multi-frame alignment pattern. 00 - Searching of CAS Multi-frame alignment is disabled. The XRT86L34 framer will not search for CAS Multi-frame alignment and thus will not declare CAS Multi-frame synchronization. No Receive CAS Multi-frame Synchronization (RxCRCMsync_n) pulse will be generated by the framer. 01 - Searching of CAS Multi-frame alignment is enabled. The XRT86L34 will search for and declare CAS Multi-frame synchronization using Algorithm 1. 10 - Searching of CAS Multi-frame alignment is enabled. The XRT86L34 will search for and declare CAS Multi-frame synchronization using Algorithm 2 (G.732). 11 - Searching of CAS Multi-frame alignment is disabled. The XRT86L34 framer will not search for CAS Multi-frame alignment and thus will not declare CAS Multi-frame synchronization. No Receive CAS Multi-frame Synchronization (RxCRCMsync_n) pulse will be generated by the framer.

7.2.6 How to Configure the Framer to Apply Data and Signaling Conditioning to Received E1 Payload Data on a Per-Channel Basis

The XRT86L34 T1/J1/E1 Octal Framer provides individual control of each of the thirty two DS0 channels. The user can apply data and signaling conditioning to the received E1 payload data coming from the E1 LIU Receive Block on a per-channel basis.

The XRT86L34 framer can apply the following changes to the received E1 payload data coming from the Terminal Equipment on a per-channel basis:

- All 8 bits of the received payload data are inverted
- The even bits of the received payload data are inverted
- The odd bits of the received payload data are inverted
- The MSB of the received payload data is inverted
- All received payload data except the MSB are inverted

Configurations of the XRT86L34 framer to apply the above-mentioned changes to the received E1 PAYLOAD data are controlled by the Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of each DS0 channel.

The XRT86L34 framer can also replace the incoming E1 payload data from the E1 LIU Receive Block with predefined or user-defined codes. The XRT86L34 supports the following conditioning substitutions:

- BUSY code - an octet with hexadecimal value of 0x7F
- BUSY_TS code - an octet of pattern "111xxxxx" where "xxxxx" represents the timeslot number
- VACANT code - an octet with hexadecimal value of 0xFF
- A-law Digital Milliwatt code
- u-law Digital Milliwatt code
- IDLE code - an octet defined by the value stored in the User IDLE Code Register (UCR)
- MOOF code - MUX-Out-Of-Frame code with hexadecimal value of 0x1A
- PRBS code - an octet generated by the Pseudo-Random Bit Sequence (PRBS) Generator block of the framer

Once again, configuration of the XRT86L34 framer to replace the received E1 payload data with the above-mentioned coding schemes are controlled by the Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of each DS0 channel.

Finally, the XRT86L34 framer can configure any one or ones of the thirty two DS0 channels to be D or E channels. D channel is used primarily for data link applications. E channel is used primarily for signaling for circuit switching with multiple access configurations.

The Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of each channel determine whether that particular channel is configured as D or E channel.

The table below illustrates configurations of the Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR).

RECEIVE CHANNEL CONTROL REGISTER (RCCR) (ADDRESS = 0XN360H - 0XN37FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Receive Conditioning Select	R/W	0000 - The received E1 payload data of this DS0 channel is unchanged. 0001 - All 8 bits of the input E1 payload data of this DS0 channel are inverted. 0010 - The even bits of the input E1 payload data of this DS0 channel are inverted. 0011 - The odd bits of the input E1 payload data of this DS0 channel are inverted. 0100 - The input E1 payload data of this DS0 channel are replaced by the octet stored in User IDLE Code Register (UCR). 0101 - The input E1 payload data of this DS0 channel are replaced by BUSY code (0x7F). 0110 - The input E1 payload data of this DS0 channel are replaced by VACANT code (0xFF). 0111 - The input E1 payload data of this DS0 channel are replaced by BUSY_TS code (111xxxxx). 1000 - The input E1 payload data of this DS0 channel are replaced by MUX-Out-Of-Frame (MOOF) code with value 0x1A. 1001 - The input E1 payload data of this DS0 channel are replaced by the A-law digital milliwatt pattern. 1010 - The input E1 payload data of this DS0 channel are replaced by the u-law digital milliwatt pattern. 1011 - The MSB bit of the input E1 payload data of this DS0 channel is inverted. 1100 - All bits of the input E1 payload data of this DS0 channel except MSB bit are inverted. 1101 - The input E1 payload data of this DS0 channel are replaced by PRBS pattern created by the internal PRBS Generator of XRT86L34 framer. 1110 - The input E1 payload data of this DS0 channel is unchanged. 1111 - This channel is configured as D or E timeslot.

When the Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of a particular DS0 channel are set to 0100, the received E1 payload data of this DS0 channel are replaced by the octet stored in the Receive User IDLE Code Register (RUCR). The table below shows contents of the Receive User IDLE Code Register.

RECEIVE USER IDLE CODE REGISTER (UCR) (ADDRESS = 0XN380H - 0XN397H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	User IDLE Code	R/W	These READ/WRITE bit-fields permits the user store any value of IDLE code into the framer. When the Receive Data Conditioning Select [3:0] bits of RCCR register of a particular DS0 channel are set to 0100, the received E1 payload data are replaced by contents of this register and sent to the Terminal Equipment.

7.2.7 How to Configure the XRT86L34 Framer to Extract Robbed-bit Signaling Information

The XRT86L34 T1/J1/E1 Octal Framer supports insertion of Robbed-bit Signaling information into the outgoing E1 frame. It also supports extraction and substitution of Robbed-bit Signaling information from the incoming E1 frame. The following section describes how does the XRT86L34 framer extract and substitute Robbed-bit Signaling in E1 mode.

7.2.8 Configure the framer to receive and extract Robbed-bit Signaling

The XRT86L34 framer supports receiving and extraction of CAS signaling. The Receive Signaling Extraction Control [1:0] bits of the Receive Signaling Control Register (RSCR) of each channel select either:

- No signaling extraction
- Two-code signaling
- Four-code signaling or
- Sixteen-code signaling

The table below shows configurations of the Receive Signaling Extraction Control [1:0] bits of the Receive Signaling Control Register.

RECEIVE SIGNALING CONTROL REGISTER (RSCR) (ADDRESS = 0XN3A0H - 0XN3B7H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Signaling Extraction Control	R/W	00 - The XRT86L34 framer does not extract signaling information from incoming E1 payload data. 01 - The XRT86L34 framer extracts sixteen-code signaling information from incoming E1 payload data. 10 - The XRT86L34 framer extracts four-code signaling information from incoming E1 payload data. 11 - The XRT86L34 framer extracts two-code signaling information from incoming E1 payload data.

Upon receiving and extraction of signaling bits from the incoming E1 frames, the XRT86L34 framer compares the signaling bits with the previously received ones. If there is a change of signaling data, a Signaling Update (SIG) interrupt request may be generated at the end of an E1 multi-frame. The user can thus be notified of a Change of Signaling Data event.

To enable the Signaling Update interrupt, the Signaling Change Interrupt Enable bit of the Framer Interrupt Enable Register (FIER) has to be set. In addition, the T1/E1 Framer Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Signaling Change Interrupt Enable bit of the Framer Interrupt Enable Register.

FRAMER INTERRUPT ENABLE REGISTER (FIER) (ADDRESS = 0XNB05H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Signaling Change Interrupt Enable	R/W	0 - The Signaling Update interrupt is disabled. 1 - The Signaling Update interrupt is enabled.

The table below shows configurations of the T1/E1 Framer Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	T1/E1 Framer Interrupt Enable	R/W	0 - Every interrupt generated by the Framer Interrupt Status Register (FISR) is disabled. 1 - Every interrupt generated by the Framer Interrupt Status Register (FISR) is enabled.

When these interrupt enable bits are set and the signaling information received is changed, the E1 Receive Framer block will set the Signaling Updated status bit of the Framer Interrupt Status Register (FISR) to one. This status indicator is valid until the Framer Interrupt Status Register is read. Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Signaling Update status bits of the Framer Interrupt Status Register.

FRAMER INTERRUPT STATUS REGISTER (FISR) (ADDRESS = 0XNB04H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Signaling Updated	RUR / WC	0 - There is no change of signaling information in the incoming E1 payload data. 1 - There is change of signaling information in the incoming E1 payload data.

Now, there is only one problem remains. Since there are thirty two DS0 channels in E1, how do we know signaling information of which channel is changed?

To solve this problem, the XRT86L34 provides three 8-bit Signaling Change Registers to indicate the channel(s) which signaling data change had occurred over the last E1 multi-frame period. Each bit of the Signaling Change Registers represents one timeslot of the E1 frame. If any particular bit is zero, it means there is no change of signaling data occurred in that particular timeslot over the last E1 multi-frame period. If any particular bit is one, it means there is change of signaling data occurred over the last E1 multi-frame period.

The table below shows configurations of the Signaling Change Registers.

SIGNALING CHANGE REGISTERS (SCR) (ADDRESS = 0XN10DH - 0XN10FH)

LOCATION \ BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0xn10DH	Ch 0	Ch 1	Ch 2	Ch 3	Ch 4	Ch 5	Ch 6	Ch 7
0xn10EH	Ch 8	Ch 9	Ch 10	Ch 11	Ch 12	Ch 13	Ch 14	Ch 15
0xn10FH	Ch 16	Ch 17	Ch 18	Ch 19	Ch 20	Ch 21	Ch 22	Ch 23
0xn10FH	Ch 24	Ch 25	Ch 26	Ch 27	Ch 28	Ch 29	Ch 30	Ch 31

By reading contents of the Signaling Update status bits of the Framer Interrupt Status Register and the Signaling Change Registers, the user can clearly identify which one(s) of the thirty-two DS0 channels has changed signaling information over the last multi-frame period.

Depending on configurations of the XRT86L34 framer, the signaling bits can be extracted from the incoming E1 frame and direct to all or any one of the following destinations:

- Signaling data is stored to Receive Signaling Register Array (RSRA) of each channel
- Signaling data is sent to the Terminal Equipment through the Receive Signaling Output pin (RxSig_n)

- Signaling data is sent to the Terminal Equipment through the Receive Overhead Output pin (RxOH_n)
- Signaling data is embedded into the output PCM data sending towards the Terminal Equipment through the Receive Serial Output pin (RxSer_n)

The follow sections discuss how to configure the XRT86L34 framer to extract signaling information bits and send them to different destinations.

7.2.8.1 Store Signaling Bits into RSRA Register Array

The four least significant bits of the Receive Signaling Register Array (RSRA) of each timeslot can be used to store received signaling data. The user can read these bits through microprocessor access. If the XRT86L34 framer is configure to extract signaling bits from incoming E1 payload data, the E1 Receive Framer block will strip off the CAS signaling bits from time slot 16 of the incoming E1 frames and store them into appropriate locations of the RSRA. The extraction of signaling bit from E1 PCM data is done on a per-channel basis. The Bit 3 of RSRA register is used to hole Signaling bit A. Bit 2 is used to hold Signaling bit B. Bit 1 is used to hold Signaling bit C. Bit 0 is used to hold Signaling bit D.

The table below shows the four least significant bits of the Receive Signaling Register Array.

RECEIVE SIGNALING REGISTER ARRAY (RSRA) (ADDRESS = 0XN500H - 0XN51FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Signaling Bit A	R/W	This bit is used to store Signaling Bit A that is received and extracted.
2	Signaling Bit B	R/W	This bit is used to store Signaling Bit B that is received and extracted.
1	Signaling Bit C	R/W	This bit is used to store Signaling Bit C that is received and extracted.
0	Signaling Bit D	R/W	This bit is used to store Signaling Bit D that is received and extracted.

7.2.8.2 Outputting Signaling Bits through RxSig_n Pin

The XRT86L34 framer can be configure to output extracted signaling bits to external equipment through the RxSig_n pins. This pin is a multiplexed I/O pin with two functions:

- RxTSb[0]_n - Receive Timeslot Number Bit [0] Output pin
- RxSig_n - Receive Signaling Output pin

When the Receive Fractional E1 bit of the Receive Interface Control Register (RICR) is set to 0, this pin is configured as RxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the E1 PCM data that is receiving.

When the Receive Fractional E1 bit of the Receive Interface Control Register (RICR) is set to 1, this pin is configured as RxSig_n pin, it acts as an output source for the signaling bits to be received in the inbound E1 frames.

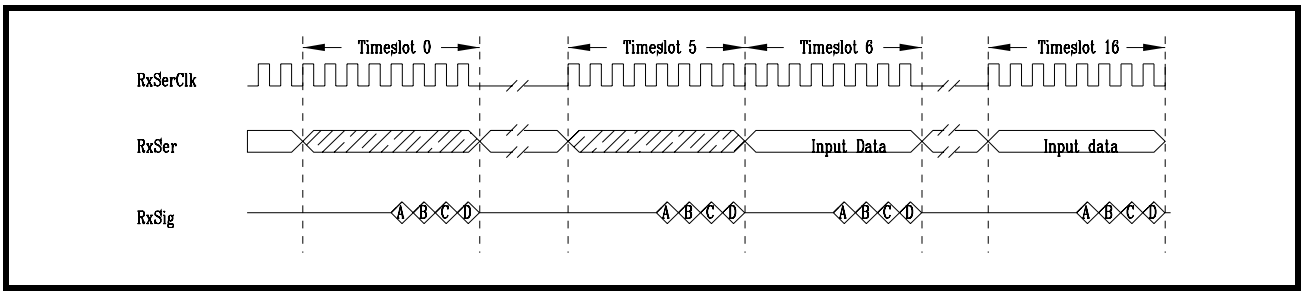
The table below shows configurations of the Receive Fractional E1 bit of the Receive Interface Control Register (RICR).

RECEIVE INTERFACE CONTROL REGISTER (RICR) (ADDRESS = 0XN120H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Fractional E1	R/W	This READ/WRITE bit-field permits the user to determine which one of the two functions the multiplexed I/O pin of RxTSb[0]_n/RxSig_n is spotting. 0 - This pin is configured as RxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the E1 PCM data that is receiving. 1 - This pin is configured as RxSig_n pin, it acts as an output source for the signaling bits to be received in the inbound E1 frames

Figure 99 below is a timing diagram of the RxSig_n output pin. Please note that the Signaling Bit A of a certain timeslot coincides with Bit 3 of the Received serial output data; Signaling Bit B coincides with Bit 2 of the Received serial output data; Signaling Bit C coincides with Bit 1 of the Received serial output data and Signaling Bit D coincides with Bit 0 of the Received serial output data.

FIGURE 99. TIMING DIAGRAM OF RXSIG_N OUTPUT PIN



7.2.8.3 Outputting Signaling Bits from RxOH_n Pin

The XRT86L34 framer can be configure to output extracted signaling bits to external equipment through the Receive Overhead RxOH_n output pins.

The RxOH_n pin can acts as an output source for the signaling bits to be received in the inbound E1 frames. When this pin is chosen as the output source for the signaling bits, any data presents in time slot 16 of the incoming E1 frames would be presented onto the pin directly.

Please note that the Signaling bit A of Channel 1-15 coincides with Bit 1 of the PCM data; Signaling bit B Channel 1-15 coincides with Bit 2 of the PCM data; Signaling bit C Channel 1-15 coincides with Bit 3 of the PCM; Signaling bit D Channel 1-15 coincides with Bit 4 of the PCM data.

Similarly, the Signaling bit A of Channel 17-31 coincides with Bit 5 of the PCM data; Signaling bit B Channel 17-31 coincides with Bit 6 of the PCM data; Signaling bit C Channel 17-31 coincides with Bit 7 of the PCM; Signaling bit D Channel 17-31 coincides with Bit 8 of the PCM data.

The Receive Signaling Output Enable bit of the Receive Signaling Control Register (RSCR) determines whether the extracted signaling bits will be sent through the Receive Overhead Output pin (RxOH_n) to external equipments. The table below shows configurations of the Receive Overhead Output Enable bit of the Receive Signaling Control Register.

RECEIVE SIGNALING CONTROL REGISTER (RSCR) (ADDRESS = 0XN3A0H - 0XN3BFH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Signaling Output Enable	R/W	0 - The XRT86L34 framer will not send extracted signaling bits from the incoming E1 payload data to external equipment through the Receive Overhead Output pin (RxOH_n). 1 - The XRT86L34 framer will send extracted signaling bits from the incoming E1 payload data to external equipment through the Receive Overhead Output pin (RxOH_n).

7.2.8.4 Send Signaling Data through RxSer_n Pin

As mentioned in the above sections, signaling information embedded in the incoming E1 PCM data can be sent to either the RSRA register array and/or sent through the Receive Signaling Output pin, at the same time, the signaling data will be directed to the Receive Serial Data Output pin together with other incoming E1 payload data. The external equipment can thus still extract signaling data from the received E1 payload data separately.

7.2.8.5 Signaling Data Substitution

After channel conditioning, the signaling conditioning can be optionally enabled by the RSCR registers. The actual signaling bits in each channel can be replaced either with all ones or with signaling bits stored in the Receive Substitution Signaling Register (RSSR). To enable signaling substitution, the Receive Signaling Substitution Enable bit of the Receive Signaling Control Register (RSCR) has to be set to one. The table below shows configuration of the Receive Signaling Substitution Enable bit of the Receive Signaling Control Register.

RECEIVE SIGNALING CONTROL REGISTER (RSCR) (ADDRESS = 0XN3A0H - 0XN3BFH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Receive Signaling Substitution Enable	R/W	0 - Signaling Substitution is disabled. The XRT86L34 framer will not replace extracted signaling bits from the incoming E1 payload data with all ones or with signaling bits stored in RSSR registers. 1 - Signaling Substitution is enabled. The XRT86L34 framer will replace extracted signaling bits from the incoming E1 payload data with all ones or with signaling bits stored in RSSR registers.

As mentioned before, the actual signaling bits in each channel can be replaced either with all ones or with signaling bits stored in the Receive Substitution Signaling Register (RSSR). The table below shows configurations of the Receive Substitution Signaling Register.

RECEIVE SUBSTITUTION SIGNALING REGISTER (RSSR) (ADDRESS = 0XN380H - 0XN39FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-4	Reserved	R/W	
3	SIG16-A SIG4-A SIG2-A		Sixteen-Code Signaling bit A Four-Code Signaling bit A Two-Code Signaling bit A
2	SIG16-B SIG4-B SIG2-A		Sixteen-Code Signaling bit B Four-Code Signaling bit B Two-Code Signaling bit A
1	SIG16-C SIG4-A SIG2-A		Sixteen-Code Signaling bit C Four-Code Signaling bit A Two-Code Signaling bit A
0	SIG16-D SIG4-B SIG2-A		Sixteen-Code Signaling bit D Four-Code Signaling bit B Two-Code Signaling bit A

The Receive Signaling Substitution Control [1:0] bits can select all ones substitution, two-code signaling substitution, four-code signaling substitution, or sixteen-code signaling.

The XRT86L34 framer can substitute received signaling bits with all ones. Two-code signaling substitution is done by substituting all the four signaling bits with the content of the SIG2-A bit of the register. Four-code signaling substitution is done by substituting the first two signaling bits of the four with the SIG4-A bit and the last two signaling bits of the four with the SIG4-B bit of the RSSR register. Sixteen-code signaling substitution is implemented by substituting the four signaling bits with the content of SIG16-A, SIG16-B, SIG16-C, and SIG16-D bits of RSSR register respectively.

The table below shows configurations of the Receive Signaling Substitution Control [1:0] bits of the Receive Signaling Control Register.

RECEIVE SIGNALING CONTROL REGISTER (RSCR) (ADDRESS = 0XN340H - 0XN35FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Receive Signaling Substitution Control	R/W	00 - The received signaling bits are replaced by all ones and send to the external equipment. 01 - Two-code signaling substitution is applied to the received signaling bits. The replaced signaling information is sent to the external equipment. 10 - Four-code signaling substitution is applied to the received signaling bits. The replaced signaling information is sent to the external equipment. 11 - Sixteen-code signaling substitution is applied to the received signaling bits. The replaced signaling information is sent to the external equipment.

7.2.9 How to Configure the Framer to Detect Alarms and Error Conditions

The XRT86L34 T1/J1/E1 Octal Framer can be configured to monitor quality of received E1 frames. It can generate error indicators if the local receive framer has received error frames from the remote terminal. If corresponding interrupt is enabled, the local microprocessor operation is interrupted by these error conditions. Upon microprocessor interruption, the user can intervene by looking into the error conditions.

At the same time, the user can configure the XRT86L34 framer to receive alarms and error indications to remote terminal. Different alarms and error indications will be received depending on the error condition.

The section below gives a brief discussion of the error conditions that can be detected by the XRT86L34 framer and error indications that will be generated.

7.2.10 How to configure the framer to detect AIS Alarm

Transmission of Alarm Indication Signal (AIS) or Blue Alarm by the intermediate node indicates that the equipment is still functioning but unable to offer services. It is an all ones (except for framing bits) pattern which can be used by the equipment further down the line to maintain clock recovery and timing synchronization.

The XRT86L34 framer can detect three types of AIS in E1 mode:

- Framed AIS
- Unframed AIS
- AIS16

Unframed AIS is an all ones pattern. If unframed AIS is sent, the equipment further down the line will be able to maintain timing synchronization and be able to recover clock from the received AIS signal. However, due to the lack of framing bits, the equipment farther down the line will not be able to maintain frame synchronization and will declare Loss of Frame (LOF).

On the other hand, the payload portion of a framed AIS pattern is all ones. However, a framed AIS pattern still has correct framing bits. Therefore, the equipment further down the line can still maintain frame synchronization as well as timing synchronization. In this case, no LOF or Red alarm will be declared.

"AIS16" is an AIS alarm that only supported in E1 framing format. It is an all ones pattern in time slot 16 of each E1 frame. As we mentioned before, time slot 16 is usually used for signaling and data link in E1, therefore, an "AIS16" alarm is transmitted by the intermediate node to indicate that the data link channel is having a problem. Since all the other thirty one time slots are still transmitting normal data (that is, framing information and PCM data), therefore, the equipment further down the line can still maintain frame synchronization, timing synchronization as well as receiving PCM data. In this case, no LOF or Red alarm will be declared by the equipments further down the line. However, a CAS Multi-frame Yellow Alarm will be sent by the equipment further down the line to indicate the loss of CAS Multi-frame alignment.

The Alarm indication logic within the Receive Framer block of the XRT86L34 framer monitors the incoming E1 frames for AIS (both framed and unframed) and AIS16 errors.

AIS alarm condition are detected and declared according to the following procedure:

1. The incoming E1 frames are monitored for AIS detection. AIS detection is defined as an unframed or framed pattern with less than three zeros in two consecutive frames. In the case of framed AIS, time slot 0 is excluded.
2. An AIS detection counter within the Receive Framer block of the XRT86L34 counts the occurrences of AIS detection over a 4 ms interval. It will indicate a valid AIS flag when thirteen or more of a possible sixteen AIS are detected.
3. Each 4 ms interval with a valid AIS flag increments a flag counter which declares AIS alarm when 25 valid flags have been collected.

Therefore, AIS condition has to be persisted for 104 ms before AIS alarm condition is declared by the XRT86L34 framer.

If there is no valid AIS flag over a 4ms interval, the Alarm indication logic will decrement the flag counter. The AIS alarm is removed when the counter reaches 0. That is, AIS alarm will be removed if in over 104 ms, there is no valid AIS flag.

AIS16 alarm condition are detected and declared according to the following procedure:

1. The incoming E1 frames are monitored for AIS16 detection. AIS16 detection is defined as two consecutive all ones time slot 16 bytes while CAS Multi-frame alignment pattern is missing or CAS Multi-frame is out of synchronization.
2. An AIS16 detection counter within the Receive Framer block of the XRT86L34 counts the occurrences of AIS16 detection.
3. Each valid AIS flag increments a flag counter which declares AIS alarm when 22 valid flags have been collected.

If there is no valid AIS16 flag, the Alarm indication logic will decrement the flag counter. The AIS16 alarm is removed when the counter reaches 0.

The Alarm Indication Signal Detection Select [1:0] bits of the Alarm Generation Register (AGR) enable the three types of AIS detection that are supported by the XRT86L34 framer. The table below shows configurations of the Alarm Indication Signal Detection Select [1:0] bits of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR) (ADDRESS = 0XN108H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	AIS Detection Select	R/W	00 - AIS alarm detection is disabled. 01 - Detection of unframed AIS alarm of all ones pattern is enabled. 10 - Detection of AIS16 alarm is enabled. 11 - Detection of framed AIS alarm of all ones pattern except for framing bits is enabled.

If detection of unframed or framed AIS alarm is enabled by the user and if AIS is present in the incoming E1 frame, the XRT86L34 framer can generate a Receive AIS State Change interrupt associated with the setting of Receive AIS State Change bit of the Alarm and Error Status Register to one.

To enable the Receive AIS State Change interrupt, the Receive AIS State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) have to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive AIS State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (ADDRESS = 0XNB03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive AIS State Change Interrupt Enable	R/W	0 - The Receive AIS State Change interrupt is disabled. 1 - The Receive AIS State Change interrupt is enabled.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and AIS is present in the incoming E1 frame, the XRT86L34 framer will declare AIS by doing the following:

- Set the read-only Receive AIS State bit of the Alarm and Error Status Register (AESR) to one indicating there is AIS alarm detected in the incoming E1 frame.
- Set the Receive AIS State Change bit of the Alarm and Error Status Register to one indicating there is a change in state of AIS. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive AIS State Change status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive AIS State Change	RUR / WC	0 - There is no change of AIS state in the incoming E1 payload data. 1 - There is change of AIS state in the incoming E1 payload data.

The Receive AIS State bit of the Alarm and Error Status Register (AESR), on the other hand, is a read-only bit indicating there is AIS alarm detected in the incoming E1 frame.

The table below shows the Receive AIS State status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Receive AIS State	R	0 - There is no AIS alarm condition detected in the incoming E1 payload data. 1 - There is AIS alarm condition detected in the incoming E1 payload data.

7.2.11 How to configure the framer to detect Red Alarm

The Alarm indication logic within the Receive Framer block of the XRT86L34 framer monitors the incoming E1 frames for red alarm or Loss of Frame (LOF) condition. Red alarm condition are detected and declared according to the following procedure:

1. The red alarm is detected by monitoring the occurrence of Loss of Frame (LOF) over a 4 ms interval.
2. An LOF valid flag will be posted on the interval when one or more LOF occurred during the interval.
3. Each interval with a valid LOF flag increments a flag counter which declares RED alarm when 25 valid intervals have been accumulated.
4. An interval without valid LOF flag decrements the flag counter. The Red alarm is removed when the counter reaches zero.

If LOF condition is present in the incoming E1 frame, the XRT86L34 framer can generate a Receive Red Alarm State Change interrupt associated with the setting of Receive Red Alarm State Change bit of the Alarm and Error Status Register to one.

To enable the Receive Red Alarm State Change interrupt, the Receive Red Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Red Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (ADDRESS = 0XNB03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Red Alarm State Change Interrupt Enable	R/W	0 - The Receive Red Alarm State Change interrupt is disabled. No Receive Loss of Frame (RxLOF) interrupt will be generated upon detection of LOF condition. 1 - The Receive Red Alarm State Change interrupt is enabled. Receive Loss of Frame (RxLOF) interrupt will be generated upon detection of LOF condition.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and Red Alarm is present in the incoming E1 frame, the XRT86L34 framer will declare Red Alarm by doing the following:

- Set the read-only Receive Red Alarm State bit of the Alarm and Error Status Register (AESR) to one indicating there is Red Alarm detected in the incoming E1 frame.
- Set the Receive Red Alarm State Change bit of the Alarm and Error Status Register to one indicating there is a change in state of Red Alarm. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Red Alarm State Change status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Red Alarm State Change	RUR / WC	0 - There is no change of Red Alarm state in the incoming E1 payload data. 1 - There is change of Red Alarm state in the incoming E1 payload data.

The Receive Red Alarm State bit of the Alarm and Error Status Register (AESR), on the other hand, is a read-only bit indicating there is Red Alarm detected in the incoming E1 frame.

The table below shows the Receive Red Alarm State status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Red Alarm State	R	0 - There is no Red Alarm condition detected in the incoming E1 payload data. 1 - There is Red Alarm condition detected in the incoming E1 payload data.

7.2.12 How to configure the framer to detect Yellow Alarm

The Alarm indication logic within the Receive Framer block of the XRT86L34 framer monitors the incoming E1 frames for Yellow Alarm condition. The yellow alarm is detected and declared according to the following procedure:

1. Monitor the occurrence of Yellow Alarm pattern over a 4 ms interval. A YEL valid flag will be posted on the interval when Yellow Alarm pattern occurred during the interval.
2. Each interval with a valid YEL flag increments a flag counter which declares YEL alarm when 80 valid intervals have been accumulated.
3. An interval without valid YEL flag decrements the flag counter. The YEL alarm is removed when the counter reaches zero.

If Yellow Alarm condition is present in the incoming E1 frame, the XRT86L34 framer can generate a Receive Yellow Alarm State Change interrupt associated with the setting of Receive Yellow Alarm State Change bit of the Alarm and Error Status Register to one.

To enable the Receive Yellow Alarm State Change interrupt, the Receive Yellow Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Yellow Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (ADDRESS = 0XNB03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Receive Yellow Alarm State Change Interrupt Enable	R/W	0 - The Receive Yellow Alarm State Change interrupt is disabled. Any state change of Receive Yellow Alarm will not generate an interrupt. 1 - The Receive Yellow Alarm State Change interrupt is enabled. Any state change of Receive Yellow Alarm will generate an interrupt.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and Yellow Alarm is present in the incoming E1 frame, the XRT86L34 framer will declare Yellow Alarm by doing the following:

- Set the Receive Yellow Alarm State Change bit of the Alarm and Error Status Register to one indicating there is a change in state of Yellow Alarm. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Yellow Alarm State Change status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Receive Yellow Alarm State Change	RUR / WC	0 - There is no change of Yellow Alarm state in the incoming E1 payload data. 1 - There is change of Yellow Alarm state in the incoming E1 payload data.

7.2.13 How to configure the framer to detect CAS Multi-frame Yellow Alarm

The Alarm indication logic within the Receive Framer block of the XRT86L34 framer monitors the incoming E1 frames for CAS Multi-frame Yellow Alarm condition. The CAS Multi-frame Yellow Alarm is detected and declared according to the following procedure:

1. Monitor the occurrence of CAS Multi-frame Yellow Alarm pattern over a 4 ms interval. An MYEL valid flag will be posted on the interval when CAS Multi-frame Yellow Alarm pattern occurred during the interval.
2. Each interval with a valid MYEL flag increments a flag counter which declares MYEL alarm when 80 valid intervals have been accumulated.
3. An interval without valid MYEL flag decrements the flag counter. The MYEL alarm is removed when the counter reaches zero.

If CAS Multi-frame Yellow Alarm condition is present in the incoming E1 frame, the XRT86L34 framer can generate a Receive CAS Multi-frame Yellow Alarm State Change interrupt associated with the setting of Receive CAS Multi-frame Yellow Alarm State Change bit of the Alarm and Error Status Register to one.

To enable the Receive CAS Multi-frame Yellow Alarm State Change interrupt, the Receive CAS Multi-frame Yellow Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive CAS Multi-frame Yellow Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (ADDRESS = 0XNB03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive CAS Multi-frame Yellow Alarm State Change Interrupt Enable	R/W	0 - The Receive CAS Multi-frame Yellow Alarm State Change interrupt is disabled. Any state change of Receive CAS Multi-frame Yellow Alarm will not generate an interrupt. 1 - The Receive CAS Multi-frame Yellow Alarm State Change interrupt is enabled. Any state change of Receive CAS Multi-frame Yellow Alarm will generate an interrupt.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and CAS Multi-frame Yellow Alarm is present in the incoming E1 frame, the XRT86L34 framer will declare CAS Multi-frame Yellow Alarm by doing the following:

- Set the Receive CAS Multi-frame Yellow Alarm State Change bit of the Alarm and Error Status Register to one indicating there is a change in state of CAS Multi-frame Yellow Alarm. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive CAS Multi-frame Yellow Alarm State Change status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive CAS Multi-frame Yellow Alarm State Change	RUR / WC	0 - There is no change of CAS Multi-frame Yellow Alarm state in the incoming E1 payload data. 1 - There is change of CAS Multi-frame Yellow Alarm state in the incoming E1 payload data.

7.2.14 How to configure the framer to detect Bipolar Violation

The line coding for the E1 signal should be bipolar. That is, a binary "0" is received as zero volts while a binary "1" is received as either a positive or negative pulse, opposite in polarity to the previous pulse. A Bipolar Violation or BPV occurs when the alternate polarity rule is violated. The Alarm indication logic within the Receive Framer block of the XRT86L34 framer monitors the incoming E1 frames for Bipolar Violations.

If a Bipolar Violation is present in the incoming E1 frame, the XRT86L34 framer can generate a Receive Bipolar Violation interrupt associated with the setting of Receive Bipolar Violation bit of the Alarm and Error Status Register to one.

To enable the Receive Bipolar Violation interrupt, the Receive Bipolar Violation Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Bipolar Violation Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (ADDRESS = 0XNB03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Bipolar Violation Interrupt Enable	R/W	0 - The Receive Bipolar Violation interrupt is disabled. Occurrence of one or more bipolar violations will not generate an interrupt. 1 - The Receive Bipolar Violation interrupt is enabled. Occurrence of one or more bipolar violations will generate an interrupt.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and one or more Bipolar Violations are present in the incoming E1 frame, the XRT86L34 framer will declare Receive Bipolar Violation by doing the following:

- Set the Receive Bipolar Violation bit of the Alarm and Error Status Register to one indicating there are one or more Bipolar Violations. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Bipolar Violation status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Bipolar Violation State Change	RUR / WC	0 - There is no change of Bipolar Violation state in the incoming E1 payload data. 1 - There is change of Bipolar Violation state in the incoming E1 payload data.

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (ADDRESS = 0XNB03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Loss of Signal Interrupt Enable	R/W	0 - The Receive Loss of Signal interrupt is disabled. Occurrence of Loss of Signals will not generate an interrupt. 1 - The Receive Loss of Signal interrupt is enabled. Occurrence of Loss of Signals will generate an interrupt.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and one or more Loss of Signals are present in the incoming E1 frame, the XRT86L34 framer will declare Receive Loss of Signal by doing the following:

- ·Set the Receive Loss of Signal bit of the Alarm and Error Status Register to one indicating there is one or more Loss of Signals. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Loss of Signal status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Loss of Signal State	RUR / WC	0 - There is no change of Loss of Signal state in the incoming E1 payload data. 1 - There is change of Loss of Signal state in the incoming E1 payload data.

8.0 THE DS1 RECEIVE SECTION

8.1 THE DS1 RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK

8.1.1 Description of the Receive Payload Data Output Interface Block

Each of the four framers within the XRT86L34 includes a Receive Payload Data Output Interface block. The function of the block is to provide an interface to the Terminal Equipment (for example, a Central Office or switching equipment) that has data to receive from a "Far End" terminal over a DS1 or E1 transport medium.

The Payload Data Output Interface module (also known as the Back-plane Interface module) supports payload data to be taken from or presented to the system. In DS1 mode, supported data rates are 1.544Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 12.352Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s. In E1 mode, supported data rates are MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s.

The Receive Payload Data Output Interface block supplies or accepts the following signals to the Terminal Equipment circuitry:

- Receive Serial Data Input (RxSer_n)
- Receive Serial Clock (RxSerClk_n)
- Receive Single-frame Synchronization Signal (RxSync_n)
- Receive Multi-frame Synchronization Signal (RxMSync_n)
- Receive Time-slot Indicator Clock (RxTSClk_n)
- Receive Time-slot Indication Bits (RxTSb[4:0]_n)

The Receive Serial Data is an output pin carrying payload, signaling and sometimes Data Link data supplied by XRT86L34 to the local Terminal Equipment.

The Receive Serial Clock is an input or output signal used by the Receive Payload Data Input Interface block to send out serial data to the local Terminal Equipment. The Receive Clock Inversion bit of the Receive Interface Control Register (TICR) determines at which edge of the Receive Serial Clock would data transition on the Receive Serial Data pin occur.

The table below shows configurations of the Receive Clock Inversion bit of the Receive Interface Control Register (RICR).

RECEIVE INTERFACE CONTROL REGISTER (RICR) (ADDRESS = 0xn122H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Clock Inversion	R/W	0 - Serial data transition happens on rising edge of the Receive Serial Clock. 1 - Serial data transition happens on falling edge of the Receive Serial Clock.

Throughout the discussion of this datasheet, we assume that serial data transition happens on rising edge of the Receive Serial Clock unless stated otherwise.

The Receive Single-frame Synchronization signal is either input or output. When configure as input, it indicates beginning of a DS1 frame. When configure as output, it indicates end of a DS1 frame.

The Receive Multi-frame Synchronization signal is an output pin from XRT86L34 indicating end of a DS1 multi-frame.

By connecting these signals with the local Terminal Equipment, the Receive Payload Data Output Interface routes received payload data from the Receive Framer Module to the local Terminal Equipment.

8.1.2 Brief Discussion of the Receive Payload Data Output Interface Block Operating at 1.544Mbit/s mode

The incoming Receive Payload Data is taken into the framer from the LIU interface using the Recovered Receive Line Clock. The payload data is then routed through the Receive Farmer Module and presented to the Receive Payload Data Output Interface through the Receive Serial Data output pin (RxSer_n). This data is then clocked out using the Receive Serial Clock (RxSerClk_n).

There is a two-frame (512 bits) elastic buffer between the Receive Framer Module and the Receive Payload Data Output Interface. This buffer can be enabled or disabled via programming the Slip Buffer Enable [1:0] bits in Slip Buffer Control Register (SBCR).

The following table shows configurations of the Slip Buffer Enable [1:0] bits in Slip Buffer Control Register.

SLIP BUFFER CONTROL REGISTER (SBCR) (ADDRESS = 0xn116H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Slip Buffer Enable	R/W	00 - Slip Buffer is bypassed. The Receive Payload Data is passing from the Receive Framer Module to the Receive Payload Data Output Interface directly without routing through the Slip Buffer. The Receive Serial Clock signal (RxSerClk_n) is an output. 01 - The Elastic Store (Slip Buffer) is enabled. The Receive Payload Data is passing from the Receive Framer Module through the Slip Buffer to the Receive Payload Data Output Interface. The Receive Serial Clock signal (RxSerClk_n) is an input. 10 - The Slip Buffer acts as a FIFO. The FIFO Latency Register (FLR) determines the data latency. The Receive Payload Data is passing from the Receive Framer Module through the FIFO to the Receive Payload Data Output Interface. The Receive Serial Clock signal (RxSerClk_n) is an input. 11 - Slip Buffer is bypassed. The Receive Payload Data is passing from the Receive Framer Module to the Receive Payload Data Output Interface directly without routing through the Slip Buffer. The Receive Serial Clock signal (RxSerClk_n) is an output.

If the Slip Buffer is not in bypass mode, then the user has the option of either providing the Receive Single-Frame Synchronization pulse or getting the Receive Single-Frame Synchronization pulse on frame boundary at the RxSync_n pin. The Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register (SBCR) determines whether the Receive Single-Frame Synchronization signal is input or output.

The table below demonstrates settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register.

SLIP BUFFER CONTROL REGISTER (SBCR) (ADDRESS = 0xn116H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Slip Buffer Receive Synchronization Direction	R/W	0 - The Receive Single-Frame Synchronization signal (RxSync_n) is an output if the Slip Buffer is not in bypass mode. 1 - The Receive Single-Frame Synchronization signal (RxSync_n) is an input if the Slip Buffer is not in bypass mode.

If the Slip Buffer is in bypass mode, the Receive Payload Data is routed to the Receive Payload Data Output Interface from the Receive Framer Module directly. The Recovered Line Clock is used to carry the Receive Payload Data all the way from the LIU interface, to the Receive Framer Module and eventually output through the Receive Serial Data output pin. The Receive Serial Clock signal is therefore an output using the Recovered Receive Line Clock as timing source. The Receive Single-Frame Synchronization signal is also output in Slip Buffer bypass mode.

If the Slip Buffer is enabled, the Receive Payload Data is latched into the Elastic Store using the Recovered Receive Line Clock. The local Terminal Equipment supplies a free-running 1.544MHz clock to the Receive Serial Clock pin to latch the Receive Payload Data out from the Elastic Store. Since the Recovered Receive Line Clock and the Receive Serial Clock are coming from different timing sources, the Slip Buffer will gradually fill or empty. If the elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties and a read occurs, then a full frame of data will be repeated and a status bit will be updated. If the buffer fills and a write comes, then a full frame of data will be deleted and another status bit will be set. A detailed description of the Elastic Buffer can be found in later sections. In this mode, the Receive Single-Frame Synchronization signal can be either input or output depending on the settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register.

If the Slip Buffer is put into a FIFO mode, it is acting like a standard First-In-First-Out storage. A fixed READ and WRITE latency is maintained in a programmable fashion controlled by the FIFO Latency Register (FIFOLR). The local Terminal Equipment supplies a 1.544MHz clock to the Receive Serial Clock pin to latch the Receive Payload Data out from the FIFO. However, it is the responsibility of the user to phase lock the input Receive Serial Clock to the Recovered Receive Line Clock to avoid either over-run or under-run of the FIFO. In this mode, the Receive Single-Frame Synchronization signal can be either input or output depending on the settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register.

The following table summaries the input or output nature of the Receive Serial Clock and Receive Single-Frame Synchronization signals for different Slip Buffer settings.

TABLE 176: THE RECEIVE SERIAL CLOCK AND RECEIVE SINGLE-FRAME SYNCHRONIZATION SIGNALS FOR DIFFERENT SLIP BUFFER SETTINGS

RECEIVE TIMING SOURCE	RXSERCLK_N	RXSYNC_N	
		SLIP BUFFER SYNCHRONIZATION DIRECTION BIT = 0	SLIP BUFFER SYNCHRONIZATION DIRECTION BIT = 1
Slip Buffer Bypassed	Output	Output	Output
Slip Buffer Enabled	Input	Output	Input
Slip Buffer Acts as FIFO	Input	Output	Input

The Receive Time-slot Indication Bits (RxTSb[4:0]_n) are multiplexed I/O pins. The functionality of these pins is governed by the value of Receive Fractional T1 Output Enable bit of the Receive Interface Control Register (RICR). The following table illustrates the configurations of the Receive Fractional DS1 Input Enable bit.

RECEIVE INTERFACE CONTROL REGISTER (RICR) (ADDRESS = 0xn122H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Fractional DS1 Output Enable	R/W	0 - The Receive Time-slot Indication bits (RxTSb[4:0] are outputting five-bit binary values of Time-slot number (0-23) being accepted and processed by the Receive Payload Data Output Interface block of the framer. The Receive Time-slot Indicator Clock signal (RxTSClk_n) is a 192KHz clock that pulses HIGH for one DS1 bit period whenever the Receive Payload Data Output Interface block is accepting the LSB of each of the twenty-four time slots. 1 - The RxTSb[0]_n bit becomes the Receive Fractional T1 Output signal (RxFrTD_n) which carries Fractional DS1 payload data from the framer. The RxTSb[1]_n bit becomes the Receive Signaling Data Output signal (RxSig_n) which is used to carry robbed-bit signaling data extracted from the inbound DS1 frame. The RxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-23) being accepted and processed by the Receive Payload Data Output Interface block of the framer. The RxTSClk_n will output gaped fractional DS1 clock that can be used by Terminal Equipment to latch in Fractional DS1 payload data at rising edge of the clock. Or, The RxTSClk_n pin will be a clock enable signal to Receive Fractional DS1 Output signal (RxFrTD_n) when the un-gaped Receive Serial Output Clock (RxSerClk_n) is used to latch in Fractional DS1 Payload Data into the Terminal Equipment.

When configured to operate in normal condition (that is, when the Receive Fractional T1 Input Enable bit is equal to zero), these bits reflect the five-bit binary value of the Time Slot number (0 - 23) being outputted and processed by the Receive Payload Data Output Interface block of the framer. RxTSb[4] represents the MSB of the binary value and RxTSb[0] represents the LSB.

When the Receive Fractional T1 Output Enable bit is equal to one, the RxTSb[0]_n bit becomes the Receive Fractional T1 Output signal (RxFrTD_n). This output pin carries Fractional T1 Output data extracted by the framer from the incoming DS1 data stream. The Fractional T1 Output Interface allows certain time-slots of DS1

data to be routed to destinations other than the local Terminal Equipment. Function of the Fractional T1 Output signal will be discussed in details in later sections.

When the Receive Fractional T1 Output Enable bit is equal to one, the RxTSb[1]_n bit becomes the Receive Signaling Data Output signal (RxSig_n). These output pins can be used to carry robbed-bit signaling data extracted from the inbound DS1 frame. Function of the Receive Signaling Data Output signal will be discussed in details in later sections.

When the Receive Fractional T1 Output Enable bit is equal to one, the RxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-23) being outputted and processed by the Receive Payload Data Output Interface block of the framer. MSB of the binary value is presented first and the LSB is presented last.

The RxTSb[3]_n and RxTSb[4}_n pins are not multiplexed.

The table below shows functionality of the RxTSb[2:0] bits when the Receive Fractional T1 Output bit is set to different values.

TABLE 177: THE RXTSB[2:0] BITS WHEN THE RECEIVE FRACTIONAL T1 OUTPUT BIT IS SET TO DIFFERENT VALUES

RECEIVE FRACTIONAL T1 OUTPUT BIT = 0		RECEIVE FRACTIONAL T1 OUTPUT BIT = 1	
RxTSb[0]	Output	RxFrTD	Output
RxTSb[1]	Output	RxSig	Output
RxTSb[2]	Output	RxTS	Output

The Receive Time-slot Indicator Clock signal (RxTSClk_n) is a multi-function output pin. When configured to operate in normal condition (that is, when the Receive Fractional T1 Input Enable bit is equal to zero), the RxTSClk_n is a 192KHz clock that pulses HIGH for one DS1 bit period whenever the Receive Payload Data Output Interface block is outputting the LSB of each of the twenty-four time slots. The local Terminal Equipment should use this clock signal to sample the RxTSb[0] through RxTSb[4] bits and identify the time-slot being processed via the Receive Section of the framer.

When the Receive Fractional T1 Output Enable bit is equal to one, the RxTSClk_n will output gaped fractional DS1 clock whenever Fractional DS1 payload data is present at the RxFrTD_n pin. The local Terminal Equipment can latch in Fractional DS1 payload data at falling edge of the clock. Otherwise, this pin will be a clock enable signal to Receive Fractional DS1 output signal (RxFrTD_n) if the framer is configured accordingly. In this way, Fractional DS1 payload data is clocked into the Terminal Equipment using un-gaped Receive Serial Output Clock (RxSerClk_n). A detailed discussion of the Fractional DS1 Payload Data Output Interface can be found in later sections.

A detailed discussion of how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment with Slip Buffer enabled or disabled can be found in the later sections.

8.1.2.1 Connect the Receive Payload Data Output Interface block to the Local Terminal Equipment if the Slip Buffer is bypassed

By setting the Slip Buffer Enable [1:0] bits of the Slip Buffer Control Register to 00 or 11, the Receive Framer Module routes the Receive Payload Data directly to the Receive Payload Data Output Interface without passing through the Elastic Buffer. The XRT86L34 uses the Recovered Receive Line Clock internally to carry the Receive Payload Data directly across the whole chip. The Recovered Receive Line Clock is essentially become timing source of the Receive Serial Clock output.

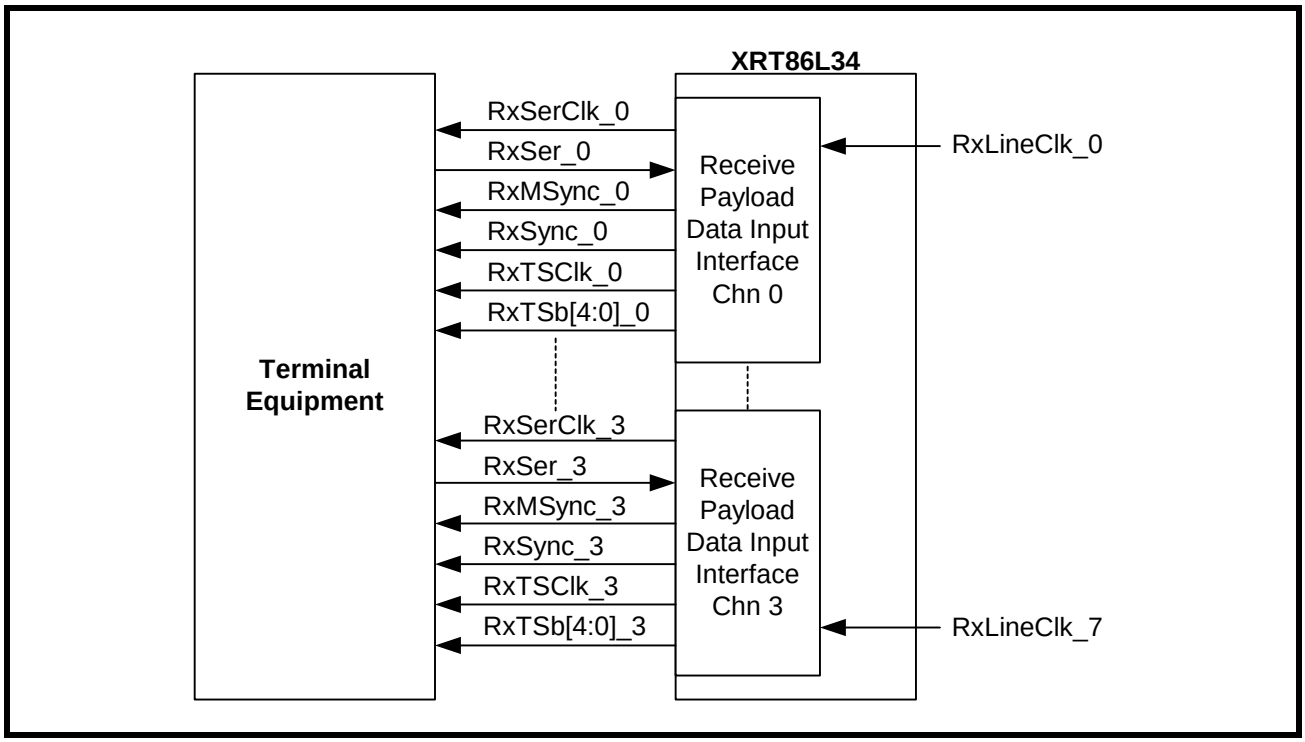
If the Slip Buffer is bypassed, the Receive Single-frame Synchronization signal is automatically configured to be output signals. It should pulse HIGH for one DS1 bit period (648ns) at the last bit position of each DS1 frame. By triggering on the HIGH pulse on the Receive Single-frame Synchronization signal, the Terminal Equipment can identify the end of a DS1 frame and should prepare to accept payload data of the next DS1 frame from the framer.

The Receive Multi-frame Synchronization signal should pulse HIGH for one DS1 bit period (648ns) at the last bit position of a DS1 multi-frame. By triggering on the HIGH pulse on the Receive Multi-frame Synchronization

signal, the framer can identify the end of a DS1 super-frame and should prepare to accept payload data of the next DS1 super-frame from the framer.

See Figure 100 for how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is bypassed and the Recovered Receive Line Clock is timing source of the Receive section.

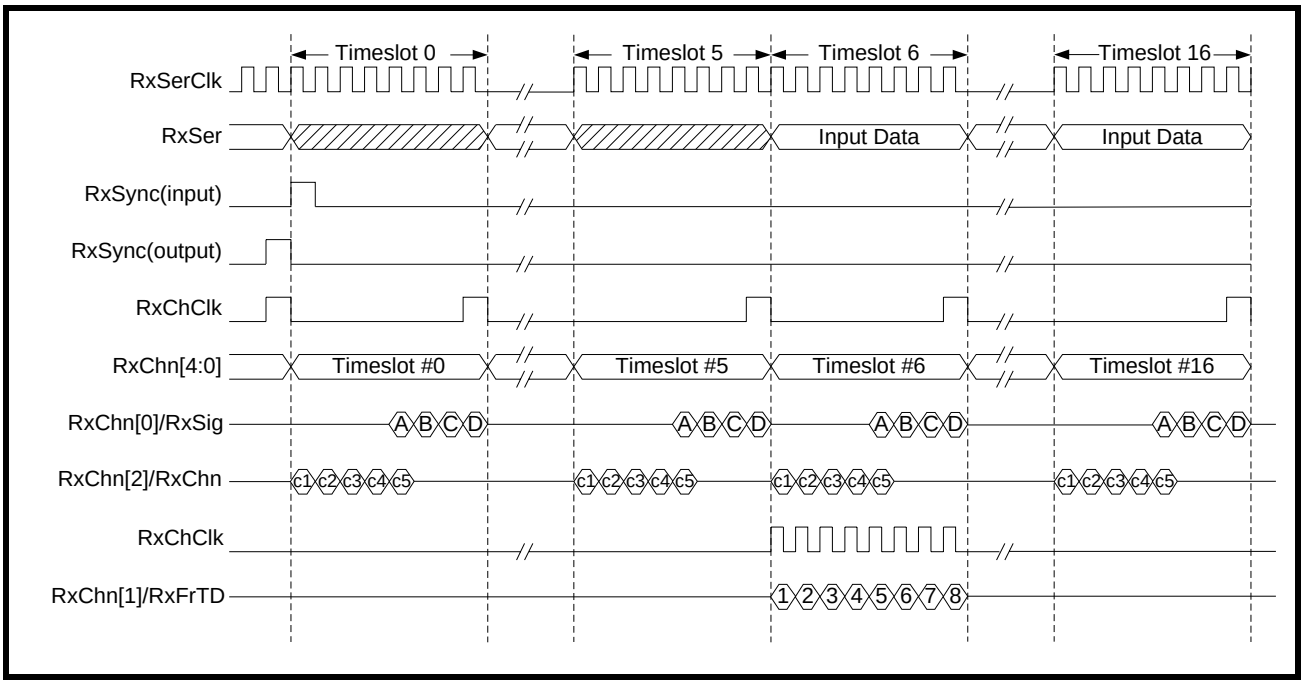
FIGURE 100. INTERFACING XRT86L34 LOCAL TERMINAL EQUIPMENT WITH SLIFF BUFFER BYPASSED AND RECOVERED RECEIVE LINE CLOCK AS RECEIVE TIMING SOURCE



The following Figure 101 shows waveforms of the signals (RxSerClk_n, RxSer_n, RxSync_n, RxTSClk_n and RxTSb[4:0]_n) which connecting the Receive Payload Data Output Interface block to the local Terminal Equip-

ment when the Slip Buffer is bypassed and the Recovered Receive Line Clock is timing source of the Receive section.

FIGURE 101. WAVEFORMS OF THE SIGNALS CONNECTING THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WHEN THE SLIP BUFFER IS BYPASSED AND THE RECOVERED LINE CLOCK IS THE TIMING SOURCE OF THE RECEIVE SECTION



8.1.2.2 Connect the Receive Payload Data Output Interface block to the Local Terminal Equipment if the Slip Buffer is enabled

By setting the Slip Buffer Enable [1:0] bits of the Slip Buffer Control Register to 01, the framer includes the two-frame Elastic Buffer into its data path. The Receive Framer Module routes the Receive Payload Data to the Elastic Buffer first. The Receive Payload Data is then presented to the Receive Payload Data Output Interface. The XRT86L34 uses the Recovered Receive Line Clock internally to clock in the Receive Payload Data into the Elastic Buffer. The Terminal Equipment should provide a 1.544MHz clock to the Receive Serial Clock input pin to latch data out from the Elastic Buffer.

The Recovered Receive Line Clock and the Receive Serial Clock are generated from two different timing sources. That is, the Recovered Receive Line Clock is originating from a remote site while Receive Serial Clock generating by a local oscillator. Any mismatch in frequencies of these two clocks will result in the Slip Buffer to gradually fill or deplete.

Overtime, the Elastic Buffer either fills or empties completely. Once that happened, a controlled slip by the XRT86L34 will occur. The Receive Slip Buffer Slip bit of the Slip Buffer Status Register (SBSR) is set to 1.

If the buffer empties and a read occurs, then a full frame of data will be repeated and the Receive Slip Buffer Empty bit of the Slip Buffer Status Register (SBSR) will be forced HIGH. If the buffer fills and a write comes, then a full frame of data will be deleted and the Receive Slip Buffer Full bit of the Slip Buffer Status Register (SBSR) will be forced HIGH.

The following table demonstrates settings of the Receive Slip Buffer Slip bit, Receive Slip Buffer Empty bit and Receive Slip Buffer Full bit of the Slip Buffer Status Register.

SLIP BUFFER STATUS REGISTER (SBSR) (ADDRESS = 0xnB08H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Slip Buffer Full	R/W	0 - The Receive Slip Buffer is not full. 1 - The Receive Slip Buffer is full and one frame of data is discarded.
1	Receive Slip Buffer Empty	R/W	0 - The Receive Slip Buffer is not empty. 1 - The Receive Slip Buffer is empty and one frame of data is repeated.
1	Receive Slip Buffer Slip	R/W	0 - The Receive Slip Buffer does not slip. 1 - The Receive Slip Buffer slips since either full or emptied.

In this mode, the Receive Single-Frame Synchronization signal can be either input or output depending on the settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register. When the Slip Buffer Receive Synchronization Direction bit is set to 0, the Receive Single-Frame Synchronization signal (RxSync_n) is an. When the Slip Buffer Receive Synchronization Direction bit is set to 1,the Receive Single-Frame Synchronization signal (RxSync_n) is an input.

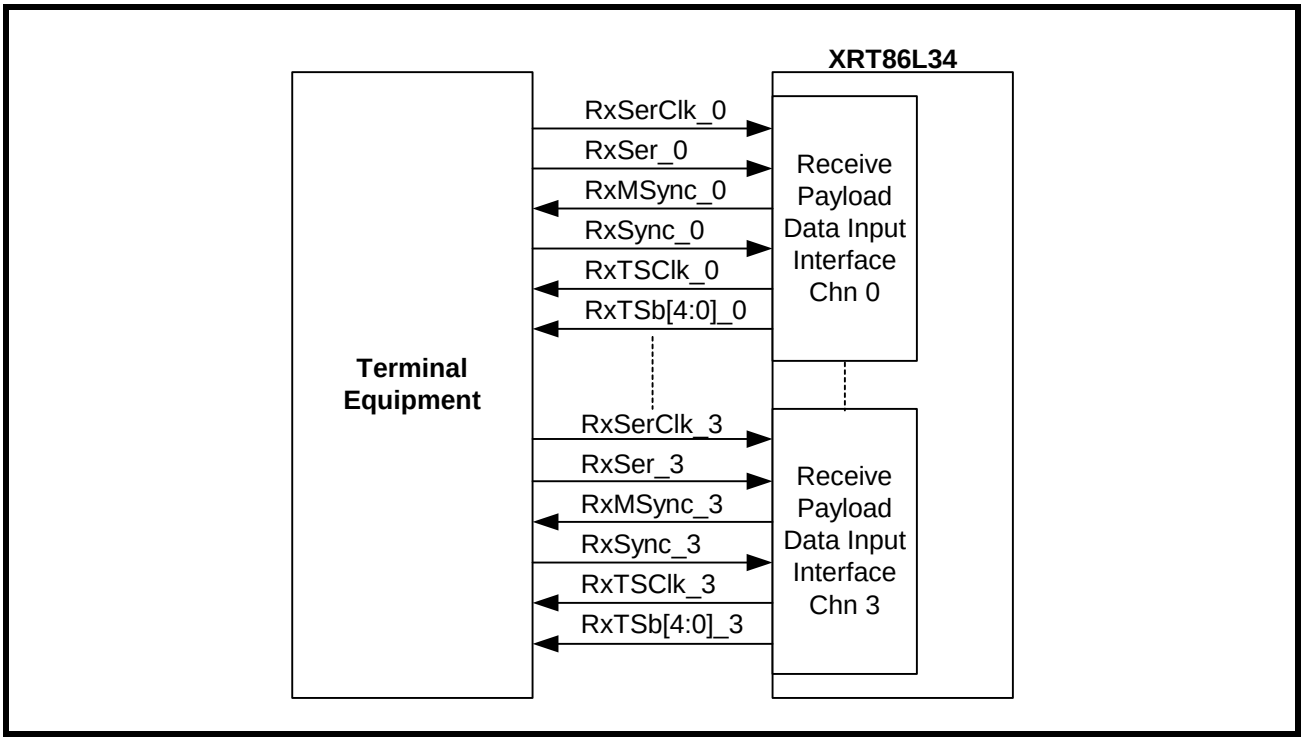
If the Receive Single-Frame Synchronization signal is an output, it should pulse HIGH for one DS1 bit period (648ns) at the last bit position of each DS1 frame. By triggering on the HIGH pulse on the Receive Single-frame Synchronization signal, the Terminal Equipment can identify the end of a DS1 frame and should prepare to accept payload data of the next DS1 frame from the framer.

If the Receive Single-Frame Synchronization signal is an input, it should pulse HIGH for one DS1 bit period (648ns) at the first bit position (F-bit) of each DS1 frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer should identity the beginning of a DS1 frame and can send out data in a synchronized way. It is the responsibility of the local Terminal Equipment to align the start of a DS1 frame with the Receive Single-Frame Synchronization pulse.

The Receive Multi-frame Synchronization signal should pulse HIGH for one DS1 bit period (648ns) at the last bit position of Frame number one of a DS1 multi-frame. By triggering on the HIGH pulse on the Receive Multi-frame Synchronization signal, the framer can identify the end of a DS1 super-frame and should prepare to accept payload data of the next DS1 super-frame from the framer.

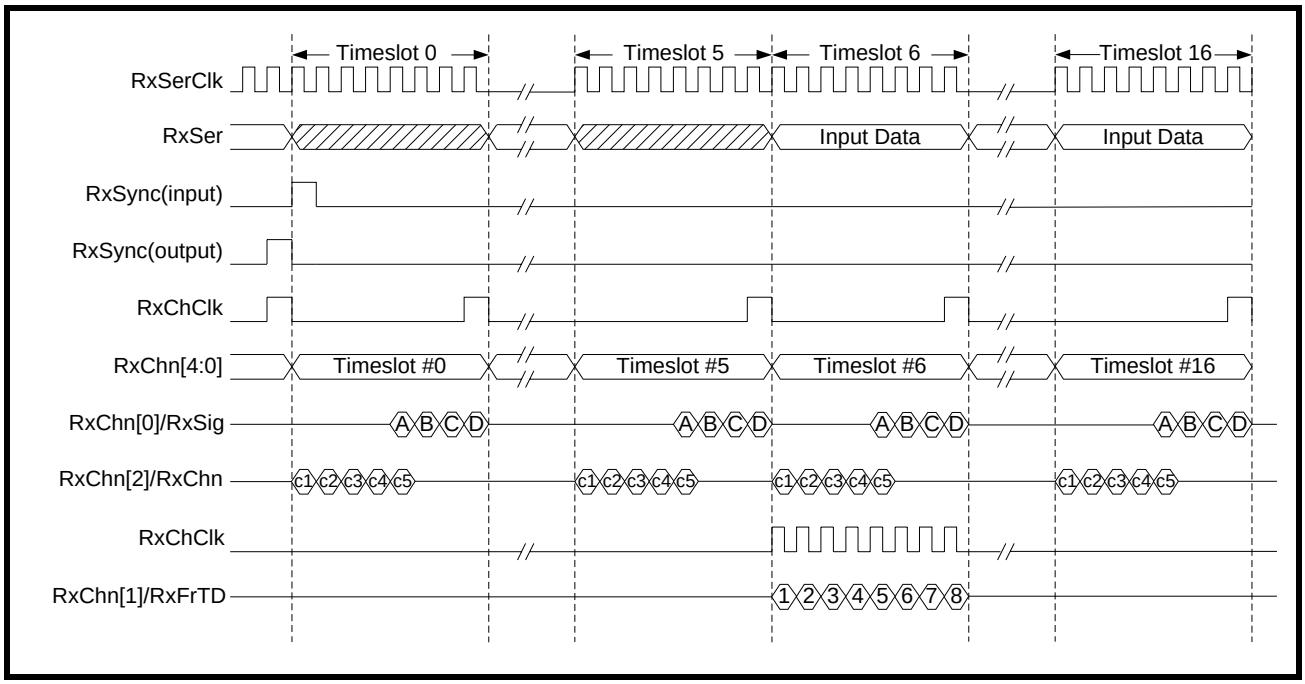
See Figure 102 for how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is enabled.

FIGURE 102. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT WITH SLIP BUFFER ENABLED OR ACTS AS FIFO



The following Figure 103 shows waveforms of the signals (RxSerClk_n, RxSer_n, RxSync_n, RxTSClk_n and RxTSb[4:0]_n) which connecting the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is enabled.

FIGURE 103. WAVEFORMS OF THE SIGNALS THAT CONNECT THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WHEN THE SLIP BUFFER IS ENABLED



8.1.2.3 Connect the Receive Payload Data Output Interface block to the Local Terminal Equipment if the Slip Buffer is configured as FIFO

By setting the Slip Buffer Enable [1:0] bits of the Slip Buffer Control Register to 10, the framer puts the Elastic Buffer into FIFO mode. Receive Framer Module routes the Receive Payload Data through the First-In-First-Out storage to the Receive Payload Data Output Interface. The XRT86L34 uses the Recovered Receive Line Clock internally to clock in the Receive Payload Data into the FIFO. The Terminal Equipment should provide an external 1.544MHz clock to the Receive Serial Clock input pin to latch data out from the FIFO.

It is the responsibility of the user to phase lock the input Receive Serial Clock to the Recovered Receive Line Clock to avoid either over-run or under-run of the FIFO. The latency between writing a bit into the FIFO and reading the same bit from it (READ and WRITE latency) is actually depth of the FIFO, which is maintained in a programmable fashion controlled by the FIFO Latency Register (FIFOLR). The largest possible depth of the FIFO is thirty-two bytes or one E1 frame. The default depth of the FIFO when XRT86L34 first powered up is four bytes. The table below shows the FIFO Latency Register.

FIFO LATENCY REGISTER (FIFOLR) (ADDRESS = 0x117H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4-0	FIFO Latency	R/W	These bits determine depth of the FIFO in terms of bytes. The largest possible value is thirty-two bytes or one E1 frame.

In this mode, the Receive Single-Frame Synchronization signal can be either input or output depending on the settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register. When the Slip Buffer Receive Synchronization Direction bit is set to 0, the Receive Single-Frame Synchronization signal

(RxSync_n) is an. When the Slip Buffer Receive Synchronization Direction bit is set to 1,the Receive Single-Frame Synchronization signal (RxSync_n) is an input.

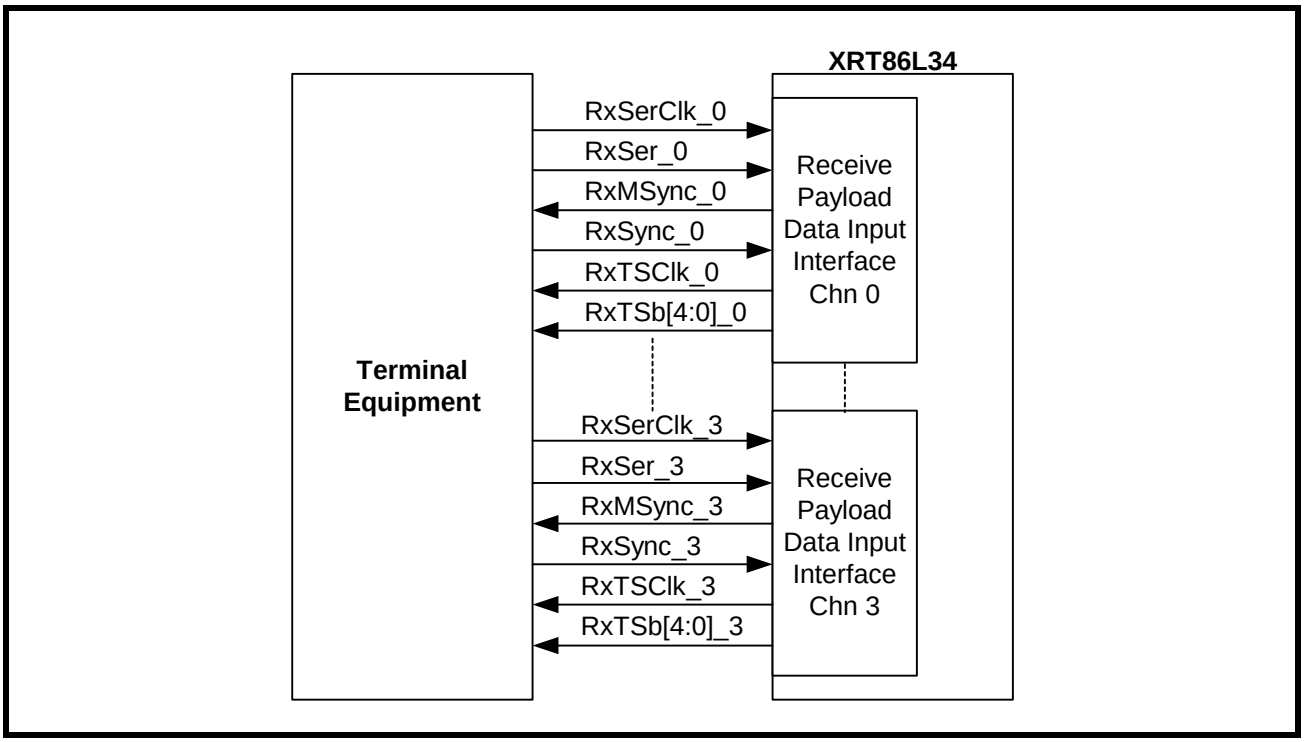
If the Receive Single-Frame Synchronization signal is an output, it should pulse HIGH for one DS1 bit period (648ns) at the last bit position of each DS1 frame. By triggering on the HIGH pulse on the Receive Single-frame Synchronization signal, the Terminal Equipment can identify the end of a DS1 frame and should prepare to accept payload data of the next DS1 frame from the framer.

If the Receive Single-Frame Synchronization signal is an input, it should pulse HIGH for one DS1 bit period (648ns) at the first bit position (F-bit) of each DS1 frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer should identity the beginning of a DS1 frame and can send out data in a synchronized way. It is the responsibility of the local Terminal Equipment to align the start of a DS1 frame with the Receive Single-Frame Synchronization pulse.

The Receive Multi-frame Synchronization signal should pulse HIGH for one DS1 bit period (648ns) at the last bit position of Frame number one of a DS1 multi-frame. By triggering on the HIGH pulse on the Receive Multi-frame Synchronization signal, the framer can identify the end of a DS1 super-frame and should prepare to accept payload data of the next DS1 super-frame from the framer.

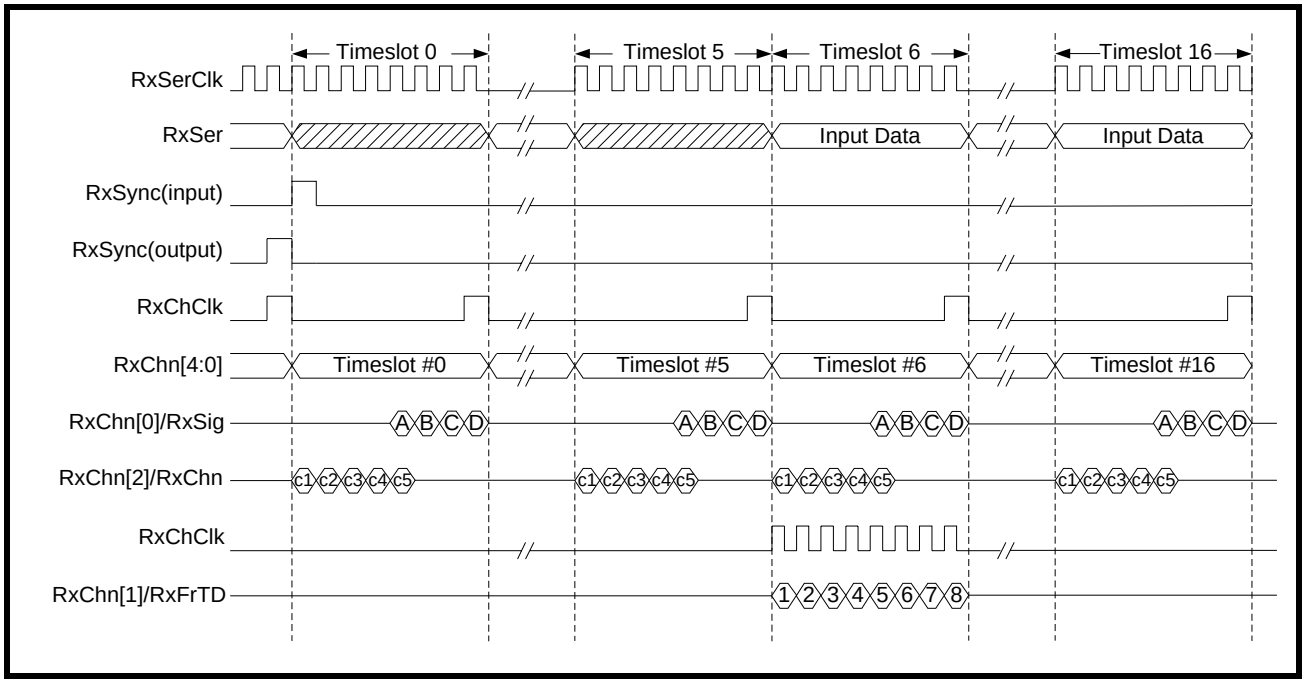
See Figure 104 for how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is acted as FIFO.

FIGURE 104. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT WITH SLIP BUFFER ENABLED OR ACTS AS FIFO



The following Figure 105 shows waveforms of the signals (RxSerClk_n, RxSer_n, RxSync_n, RxTSClk_n and RxTSb[4:0]_n) which connecting the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is acted as FIFO.

FIGURE 105. WAVEFORMS OF THE SIGNALS THAT CONNECT THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WHEN THE SLIP BUFFER IS ACTED AS FIFO



8.1.3 High Speed Receive Back-plane Interface

The High-speed Back-plane Interface supports payload data to be taken from or presented to the local Terminal Equipment at a rate higher than 1.544Mbit/s. In DS1 mode, supported High-speed data rates are MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 12.352Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s. The Receive Multiplex Enable bit and the Receive Interface Mode Select [1:0] bits of the Receive Interface Control Register (RICR) determine the Receive Back-plane Interface data rate.

The following table shows configurations of the Receive Multiplex Enable bit and the Receive Interface Mode Select [1:0] bits of the Receive Interface Control Register (RICR).

RECEIVE INTERFACE CONTROL REGISTER (RICR) (ADDRESS = 0xn122H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Multiplex Enable	R/W	0 - The Receive Back-plane Interface block is configured to non-channel-multiplexed mode. 1 - The Receive Back-plane Interface block is configured to channel-multiplexed mode
1-0	Receive Interface Mode Select	R/W	When combined with the Receive Multiplex Enable bit, these bits determine the Receive Back-plane Interface data rate.

The table below shows the combinations of Receive Multiplex Enable bit and Receive Interface Mode Select [1:0] bits and the resulting Receive Back-plane Interface data rates.

TABLE 178: RECEIVE MULTIPLEX ENABLE BIT AND RECEIVE INTERFACE MODE SELECT [1:0] BITS WITH THE RESULTING RECEIVE BACK-PLANE INTERFACE DATA RATES

RECEIVE MULTIPLEX ENABLE BIT	RECEIVE INTERFACE MODE SELECT BIT 1	RECEIVE INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE
0	0	0	1.544Mbit/s
0	0	1	MVIP 2.048Mbit/s
0	1	0	4.096Mbit/s
0	1	1	8.192Mbit/s
1	0	0	Multiplexed 12.352Mbit/s
1	0	1	Bit Multiplexed 16.384Mbit/s
1	1	0	HMVIP 16.384Mbit/s
1	1	1	H.100 16.384Mbit/s

When the Receive Multiplex Enable bit is set to zero, the framer is configured in non-channel-multiplexed mode. The possible data rates are 1.544Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s. In non-channel-multiplexed mode, payload data of each channel are sending out from the Receive High-speed Back-plane Interface separately. Each channel uses its own Receive Serial Clock, Receive Serial Data, Receive Single-frame Synchronization signal and Receive Multi-frame Synchronization signal as interface between the framer and the Terminal Equipment. Section 2.1.1.1, 2.1.1.2 and 2.1.1.3 provide details on how to connect the Receive Payload Data Interface block with the local Terminal Equipment when the Back-plane interface data rate is 1.544Mbit/s.

When the Back-plane interface data rate is MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s, the Receive Serial Clock, Receive Serial Data and Receive Single-frame Synchronization are all configured as inputs. The Receive Multi-frame Synchronization signal is still output. The Receive Serial Clock is configured as an input timing source for the High-speed Back-plane Interface with frequencies of 2.048 MHz, 4.096 MHz and 8.192 MHz respectively.

The table below summaries the clock frequencies of RxSerClk_n input when the framer is operating in non-multiplexed High-speed Back-plane mode.

RECEIVE MULTIPLEX ENABLE BIT = 0

RECEIVE INTERFACE MODE SELECT BIT 1	RECEIVE INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE	RXSERCLK
0	0	1.544Mbit/s	1.544MHz
0	1	MVIP 2.048Mbit/s	2.048 MHz
1	0	4.096Mbit/s	4.096 MHz
1	1	8.192Mbit/s	8.192 MHz

When the Receive Multiplex Enable bit is set to one, the framer is configured in channel-multiplexed mode. The possible data rates are multiplexed 12.352Mbit/s, bit-multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s and H.100 16.384Mbit/s. In channel-multiplexed mode, four channels share the Receive Serial Data, Receive Single-frame Synchronization signal and Receive Serial Clock of one channel as interface between the framer and the Terminal Equipment. The Receive Serial Clock runs at frequencies of 12.352 MHz or 16.384 MHz. It serves as the primary clock source for the High-speed Back-plane Interface.

Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH at the beginning of the frame with data from Channel 0-3 multiplexed together. The Receive Single-frame Synchronization signal of Channel 4 pulses HIGH at the beginning of the frame with data from Channel 4-7 multiplexed together.

The table below summaries the clock frequencies of RxSerClk_n input when the framer is operating in multiplexed High-speed Back-plane mode.

RECEIVE MULTIPLEX ENABLE BIT = 1

RECEIVE INTERFACE MODE SELECT BIT 1	RECEIVE INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE	RXSERCLK
0	0	Multiplexed 12.352Mbit/s	12.352 MHz
0	1	Bit-multiplexed 16.384Mbit/s	16.384 MHz
1	0	HMVIP 16.384Mbit/s	16.384 MHz
1	1	H.100 16.384Mbit/s	16.384 MHz

When the frame is running at High-speed Back-plane Interface mode other than the 1.544Mbit/s data rate, the Receive Single-frame Synchronization signal could pulse HIGH or LOW indicating boundaries of DS1 frames. The Receive Synchronization Pulse Low bit of the Receive Interface Control Register (TICR) determines whether the Receive Single-frame Synchronization signal is HIGH active or LOW active.

The table below shows configurations of the Receive Synchronization Pulse LOW bit of the Receive Interface Control Register (RICR).

RECEIVE INTERFACE CONTROL REGISTER (RICR) (ADDRESS = 0xn122H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Synchronization Pulse LOW	R/W	0 - The Receive Single-frame Synchronization signal will pulse HIGH indicating the beginning of a DS1 frame when the High-speed Back-plane Interface is running at a mode other than the 1.544Mbit/s. 1 - The Receive Single-frame Synchronization signal will pulse LOW indicating the beginning of a DS1 frame when the High-speed Back-plane Interface is running at a mode other than the 1.544Mbit/s.

Throughout the discussion of this datasheet, we assume that the Receive Single-frame Synchronization signal pulses HIGH unless stated otherwise.

The following sections discuss details of how to operate the framer in different Back-plane interface speed mode and how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment.

8.1.3.1 T1 Receive Input Interface - MVIP 2.048 MHz

When the Receive Multiplex Enable bit is set to zero and the Receive Interface Mode Select [1:0] bits are set to 01, the Receive Back-plane interface of framer is running at a data rate of 2.048Mbit/s.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane interface is pumping out data through RxSer_n at an E1 equivalent data rate of 2.048Mbit/s. The local Terminal Equipment supplies a free-running 2.048MHz clock to the Receive Serial Clock input. The Receive High-speed Back-plane Interface of the framer then sends out serial data at rising edge of the Receive Serial Clock. The local Terminal Equipment samples the serial data at falling edge of the clock.

The Terminal Equipment take in data grouped in 256-bit frame 8000 times every second. Each frame consists of thirty-two octets as in E1. The Receive High-speed Back-plane Interface maps a 193-bit T1 frame into this 256-bit format as described below:

1. The F-bit is mapped into MSB of the first E1 Time-slot. The framer will insert seven "don't care" bits to the rest of the first octet that would be ignored by the local Terminal Equipment.
2. Payload data of T1 Time-slot 0, 1 and 2 are mapped into E1 Time-slot 1, 2 and 3.
3. The Receive High-speed Back-plane Interface will stuff E1 Time-slot 4 with eight "don't care" bits that would be ignored by the local Terminal Equipment.
4. Following the same rules of Step 2 and 3, the Receive High-speed Back-plane Interface maps every three time-slots of T1 payload data into four E1 time-slots.

The mapping of T1 frame into E1 framing format is shown in the table below.

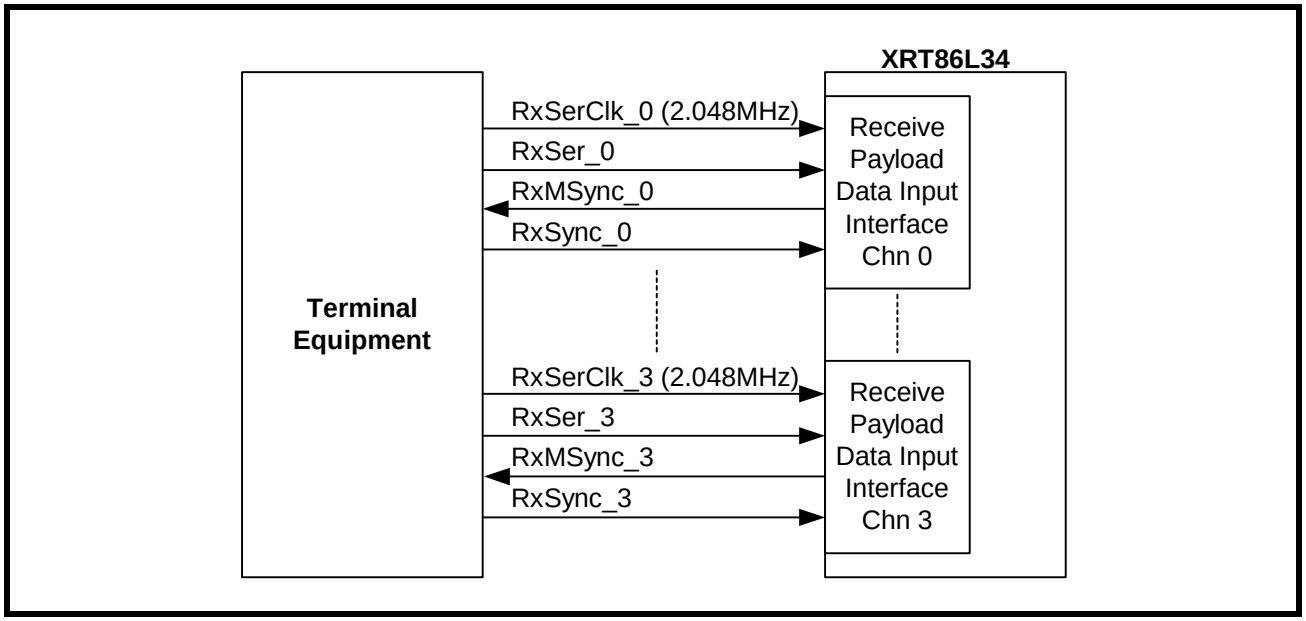
TABLE 179: THE MAPPING OF T1 FRAME INTO E1 FRAMING FORMAT

T1	F-Bit	TS0	TS1	TS2	Don't Care Bits	TS3	TS4	TS5
E1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7
T1	Don't Care Bits	TS6	TS7	TS8	Don't Care Bits	TS9	TS10	TS11
E1	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15
T1	Don't Care Bits	TS12	TS13	TS14	Don't Care Bits	TS15	TS16	TS17
E1	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23
T1	Don't Care Bits	TS18	TS19	TS20	Don't Care Bits	TS21	TS22	TS23
E1	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31

The Receive Single-frame Synchronization input signal (RxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer can identity the beginning of a DS1 frame and start pumping payload data out.

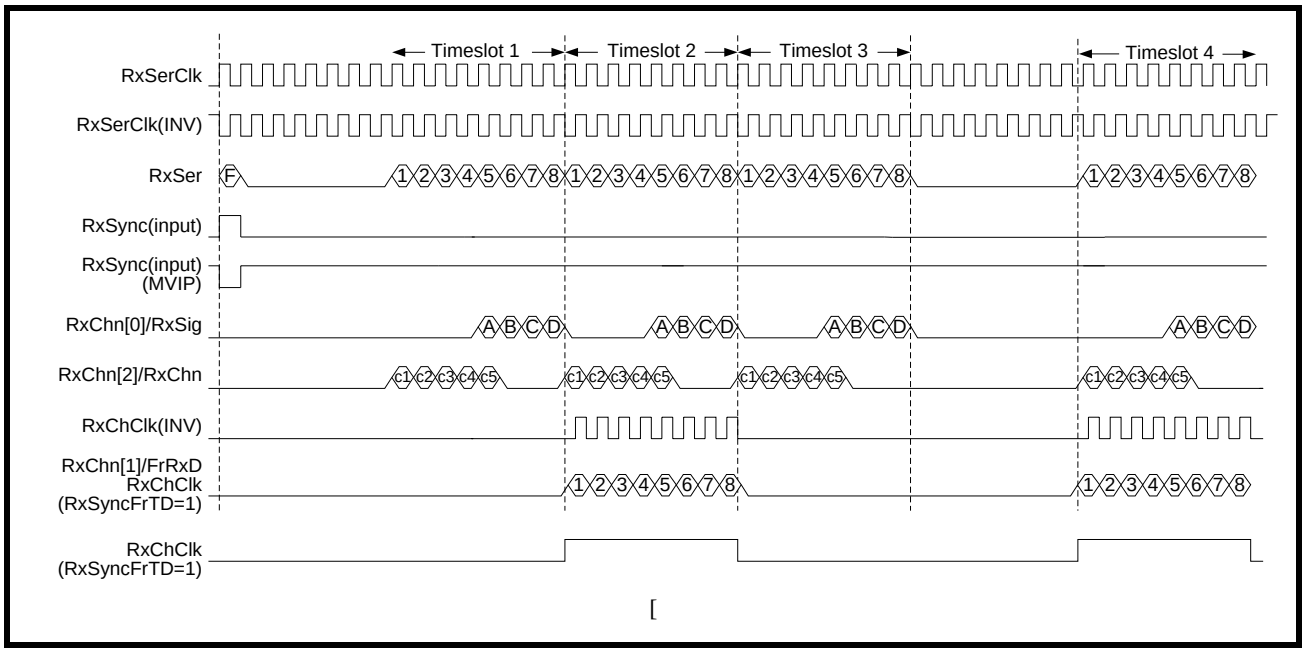
See Figure 106 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in MVIP 2.048Mbit/s mode.

FIGURE 106. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING MVIP 2.048MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at MVIP 2.048Mbit/s mode is shown in Figure 107.

FIGURE 107. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT MVIP 2.048MBIT/S



8.1.3.2 T1 Receive Input Interface - 4.096 MHz

This interface mode is the same as running at 2.048 MHz. The only difference is that the Receive Serial Clock runs two times faster at 4.096 MHz.

When the Receive Multiplex Enable bit is set to zero and the Receive Interface Mode Select [1:0] bits are set to 10, the Receive Back-plane interface of framer is running at a clock rate of 4.096MHz.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane interface is pumping out data through RxSer_n at an E1 equivalent data rate of 2.048Mbit/s. The local Terminal Equipment supplies a free-running 4.096MHz clock to the Receive Serial Clock input. The Receive High-speed Back-plane Interface of the framer then sends out serial data at every other rising edge of the Receive Serial Clock. The local Terminal Equipment samples the serial data at every other falling edge of the clock.

The Terminal Equipment take in data grouped in 256-bit frame 8000 times every second. Each frame consists of thirty-two octets as in E1. The Receive High-speed Back-plane Interface maps a 193-bit T1 frame into this 256-bit format as described below:

1. The F-bit is mapped into MSB of the first E1 Time-slot. The framer will insert seven "don't care" bits to the rest of the first octet that would be ignored by the local Terminal Equipment.
2. Payload data of T1 Time-slot 0, 1 and 2 are mapped into E1 Time-slot 1, 2 and 3.
3. The Receive High-speed Back-plane Interface will stuff E1 Time-slot 4 with eight "don't care" bits that would be ignored by the local Terminal Equipment.
4. Following the same rules of Step 2 and 3, the Receive High-speed Back-plane Interface maps every three time-slots of T1 payload data into four E1 time-slots.

The mapping of T1 frame into E1 framing format is shown in the table below.

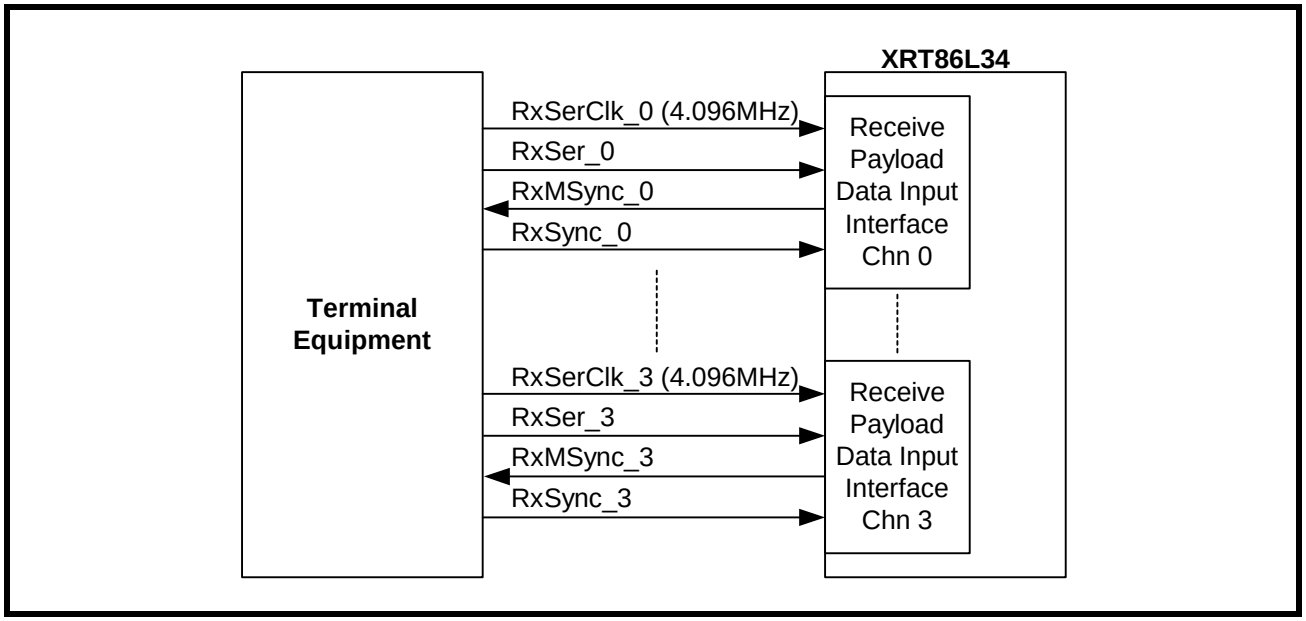
TABLE 180: THE MAPPING OF T1 FRAME INTO E1 FRAMING FORMAT

T1	F-Bit	TS0	TS1	TS2	Don't Care Bits	TS3	TS4	TS5
E1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7
T1	Don't Care Bits	TS6	TS7	TS8	Don't Care Bits	TS9	TS10	TS11
E1	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15
T1	Don't Care Bits	TS12	TS13	TS14	Don't Care Bits	TS15	TS16	TS17
E1	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23
T1	Don't Care Bits	TS18	TS19	TS20	Don't Care Bits	TS21	TS22	TS23
E1	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31

The Receive Single-frame Synchronization input signal (RxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer can identity the beginning of a DS1 frame and start pumping payload data out.

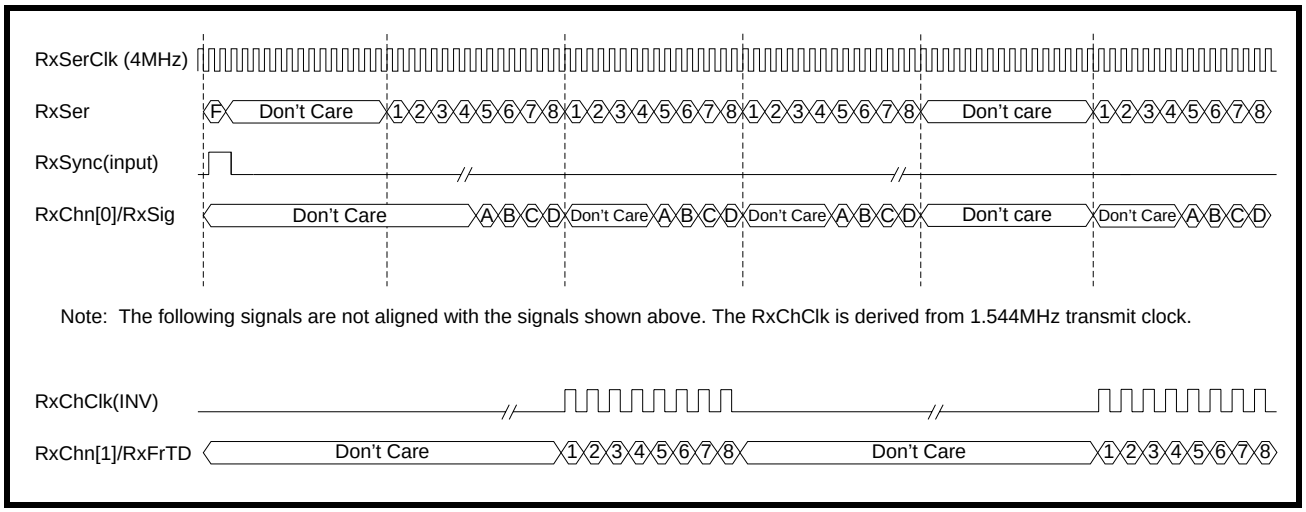
See Figure 108 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in 4.096Mbit/s mode.

FIGURE 108. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING 4.096MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at 4.096Mbit/s mode is shown in Figure 109.

FIGURE 109. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 4.096MBIT/S



8.1.3.3 T1 Receive Input Interface - 8.192 MHz

This interface mode is the same as running at 2.048 MHz. The only difference is that the Receive Serial Clock runs four times faster at 8.192MHz.

When the Receive Multiplex Enable bit is set to zero and the Receive Interface Mode Select [1:0] bits are set to 11, the Receive Back-plane interface of framer is running at a clock rate of 8.192MHz.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)

- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane interface is pumping out data through RxSer_n at an E1 equivalent data rate of 2.048Mbit/s. The local Terminal Equipment supplies a free-running 8.192MHz clock to the Receive Serial Clock input. The Receive High-speed Back-plane Interface of the framer then sends out serial data at every other four rising edge of the Receive Serial Clock. The local Terminal Equipment samples the serial data at every other four falling edge of the clock.

The Terminal Equipment take in data grouped in 256-bit frame 8000 times every second. Each frame consists of thirty-two octets as in E1. The Receive High-speed Back-plane Interface maps a 193-bit T1 frame into this 256-bit format as described below:

1. The F-bit is mapped into MSB of the first E1 Time-slot. The framer will insert seven "don't care" bits to the rest of the first octet that would be ignored by the local Terminal Equipment.
2. Payload data of T1 Time-slot 0, 1 and 2 are mapped into E1 Time-slot 1, 2 and 3.
3. The Receive High-speed Back-plane Interface will stuff E1 Time-slot 4 with eight "don't care" bits that would be ignored by the local Terminal Equipment.
4. Following the same rules of Step 2 and 3, the Receive High-speed Back-plane Interface maps every three time-slots of T1 payload data into four E1 time-slots.

The mapping of T1 frame into E1 framing format is shown in the table below.

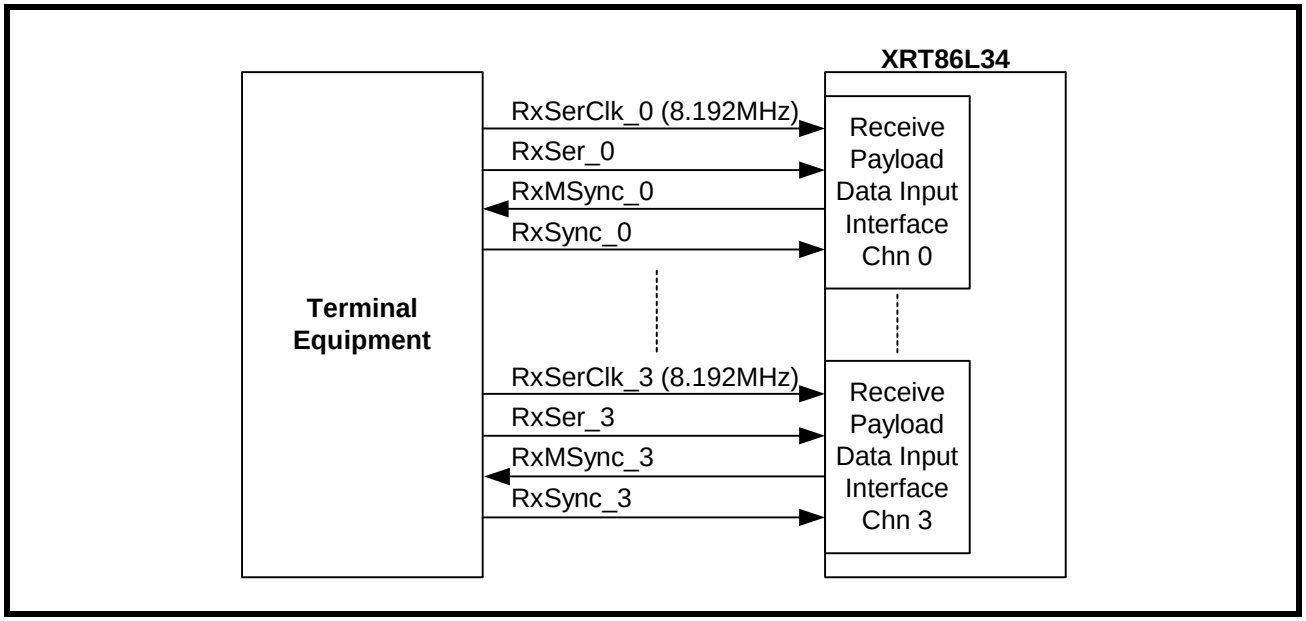
TABLE 181: THE MAPPING OF T1 FRAME INTO E1 FRAMING FORMAT

T1	F-Bit	TS0	TS1	TS2	Don't Care Bits	TS3	TS4	TS5
E1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7
T1	Don't Care Bits	TS6	TS7	TS8	Don't Care Bits	TS9	TS10	TS11
E1	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15
T1	Don't Care Bits	TS12	TS13	TS14	Don't Care Bits	TS15	TS16	TS17
E1	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23
T1	Don't Care Bits	TS18	TS19	TS20	Don't Care Bits	TS21	TS22	TS23
E1	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31

The Receive Single-frame Synchronization input signal (RxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer can identity the beginning of a DS1 frame and start pumping payload data out.

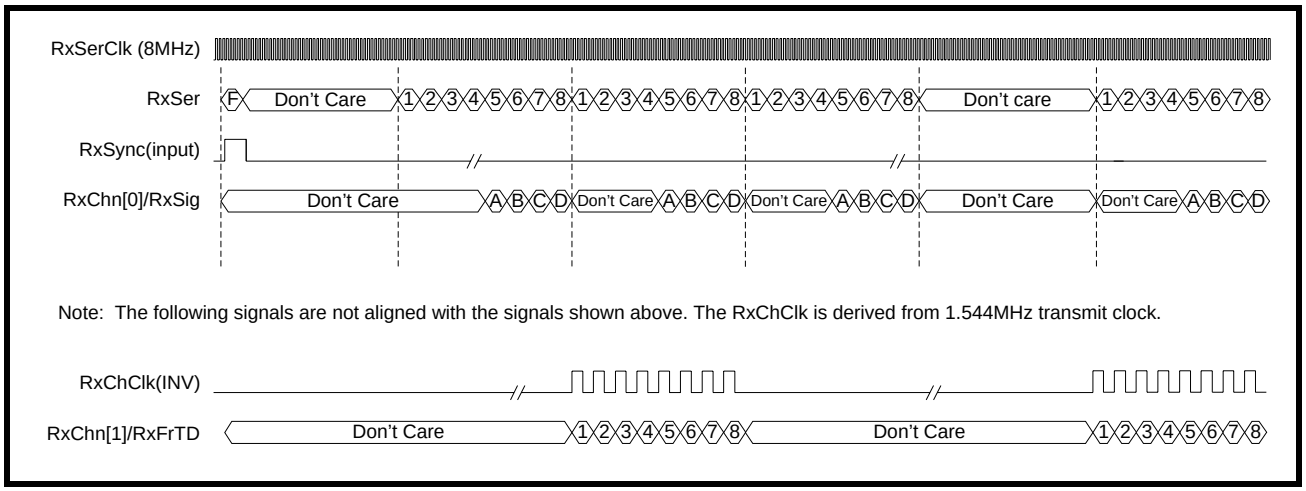
See Figure 110 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in 8.192Mbit/s mode.

FIGURE 110. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING 8.192MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at 8.192Mbit/s mode is shown in Figure 111.

FIGURE 111. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 8.192MBIT/S



8.1.3.4 T1 Receive Input Interface - Multiplexed 12.352Mbit/s

When the Receive Multiplex Enable bit is set to one and the Receive Interface Mode Select [1:0] bits are set to 00, the Receive Back-plane interface of framer is running at a clock rate of 12.352MHz.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)

- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane Interface is pumping data through RxSer_0 or RxSer_4 pins at 12.352Mbit/s. It multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4.

Free-running clocks of 12.352MHz are supplied to the Receive Serial Clock pin of Channel 0 and Channel 4 of the framer. The Receive High-speed Back-plane Interface of the farmer provides data at rising edge of this Receive Serial Clock. The local Terminal Equipment then latches incoming serial data at falling edge of the clock.

The Receive High-speed Back-plane Interface multiplexes four 1.544Mbit/s DS1 data streams into this 12.352Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

FIRST OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

F_X: F-bit of Channel X

2. Payload data of four channels are repeated and grouped together in a bit-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the first payload bit of Timeslot 0 of Channel 1 and 2. The first payload bit of Timeslot 0 of Channel 3 is sent last. After the first bits of Timeslot 0 of all four channels are sent, it comes the second bit of Timeslot 0 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 12.352Mbit/s data stream.

SECOND OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	1_1	1_1	1_2	1_2	1_3	1_3

THIRD OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
2_0	2_0	2_1	2_1	2_2	2_2	2_3	2_3

X_Y: The Xth payload bit of Channel Y

3. The Receive High-speed Back-plane Interface also multiplexed signaling bits with payload bits and sent them together through the 12.352Mbit/s data stream. When Receive High-speed Back-plane Interface is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 12.352Mbit/s data stream.

SIXTH OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	5_1	A_1	5_2	A_2	5_3	A_3

SEVENTH OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
6_0	B_0	6_1	B_1	6_2	B_2	6_3	B_3

EIGHTH OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
7_0	C_0	7_1	C_1	7_2	C_2	7_3	C_3

NINETH OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
8_0	D_0	8_1	D_1	8_2	D_2	8_3	D_3

X_Y: The Xth payload bit of Channel Y

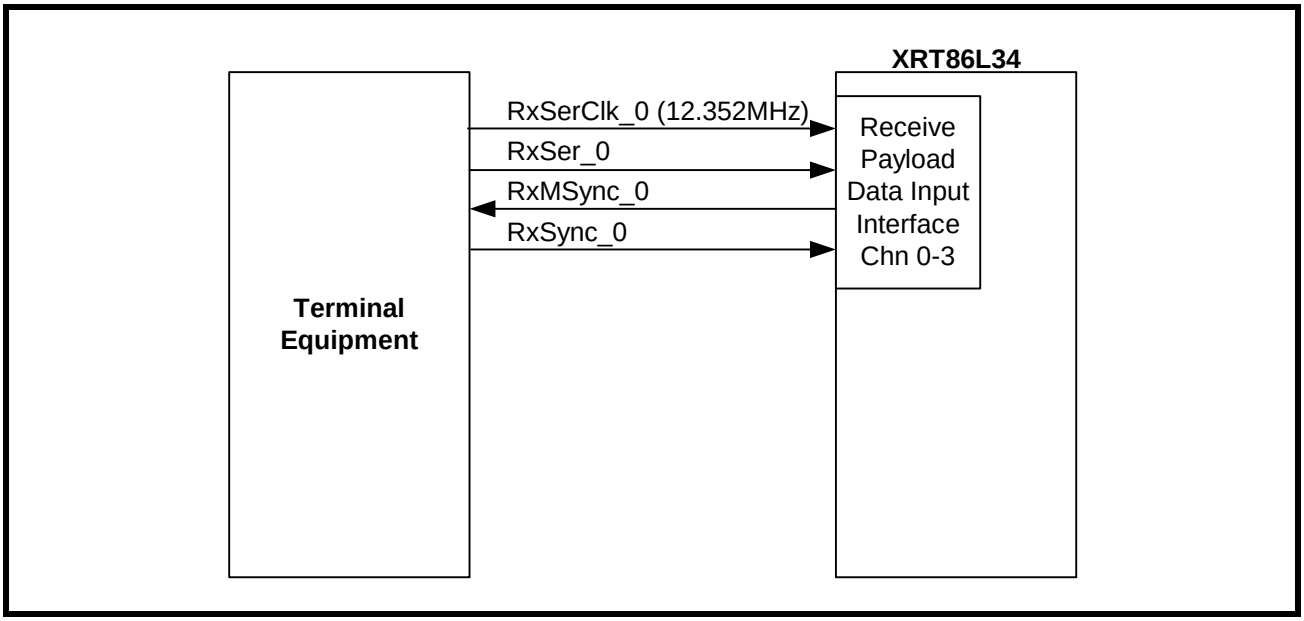
A_Y: The signaling bit A of Channel Y

4. Following the same rules of Step 2 and 3, the Receive High-speed Back-plane Interface maps the payload data and signaling data of four channels into a 12.352Mbit/s data stream.

The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH for one clock cycle at the first bit position (F-bit of channel 0) of the data stream with data from Channel 0-3 multiplexed together. The Receive Single-frame Synchronization signal of Channel 4 pulses HIGH for one clock cycle at the first bit position (F-bit of Channel 4) of the data stream with data from Channel 4-7 multiplexed together. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the Receive High-speed Back-plane Interface of the framer can identify the beginning of a multiplexed frame and can start sending payload data of that frame.

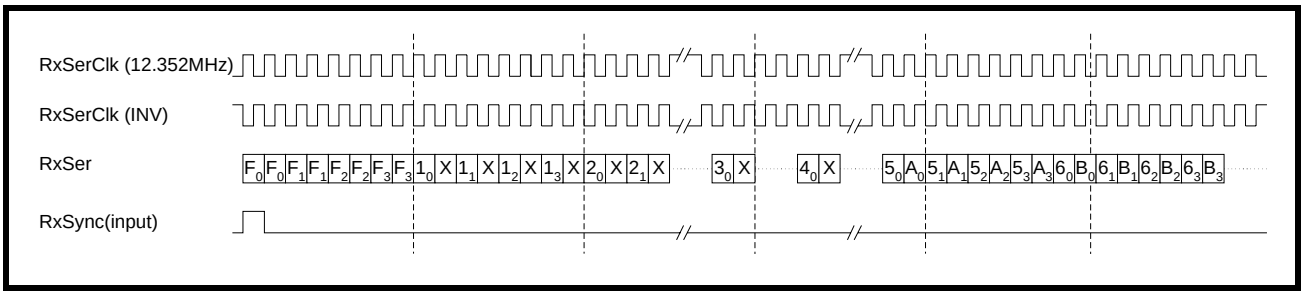
See Figure 112 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in 12.352Mbit/s mode.

FIGURE 112. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING 12.352MBIT/S DATA BUS



The Input signal timing is shown in Figure 113 below when the framer is running at 12.352Mbit/s mode.

FIGURE 113. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 12.352MBIT/S



8.1.3.5 T1 Receive Input Interface - Bit-Multiplexed 16.384Mbit/s

When the Receive Multiplex Enable bit is set to one and the Receive Interface Mode Select [1:0] bits are set to 01, the Receive Back-plane interface of framer is running at a clock rate of 16.384MHz.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane Interface is pumping out data through RxSer_0 or RxSer_4 pins at 16.384Mbit/s. It multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz are supplied to the Receive Serial Clock pin of Channel 0 and Channel 4 of the framer. The Receive High-speed Back-plane Interface of the farmer provides data at rising edge of this Receive Serial Clock. The local Terminal Equipment then latches incoming serial data at falling edge of the clock.

The Receive High-speed Back-plane Interface maps four 1.544Mbit/s DS1 data streams into this 16.384Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

F_X: F-bit of Channel X

2. After the first octet of data is sent, the Receive High-speed Back-plane Interface should insert seven octets (fifty-six bits) of "don't care" data into the outgoing data stream.
3. Payload data of four channels are repeated and grouped together in a bit-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the first payload bit of Timeslot 0 of Channel 1 and 2. The first payload bit of Timeslot 0 of Channel 3 is sent last. After the first bits of Timeslot 0 of all four channels are sent, it comes the second bit of Timeslot 0 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

NINTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	1_1	1_1	1_2	1_2	1_3	1_3

TENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
2_0	2_0	2_1	2_1	2_2	2_2	2_3	2_3

XY: The Xth payload bit of Channel Y

4. The Receive High-speed Back-plane Interface also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream. When the Receive High-speed Back-plane Interface is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

THIRTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	5_1	A_1	5_2	A_2	5_3	A_3

FOURTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
6_0	B_0	6_1	B_1	6_2	B_2	6_3	B_3

FIFTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
7_0	C_0	7_1	C_1	7_2	C_2	7_3	C_3

SIXTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
8_0	D_0	8_1	D_1	8_2	D_2	8_3	D_3

X_Y: The Xth payload bit of Channel Y

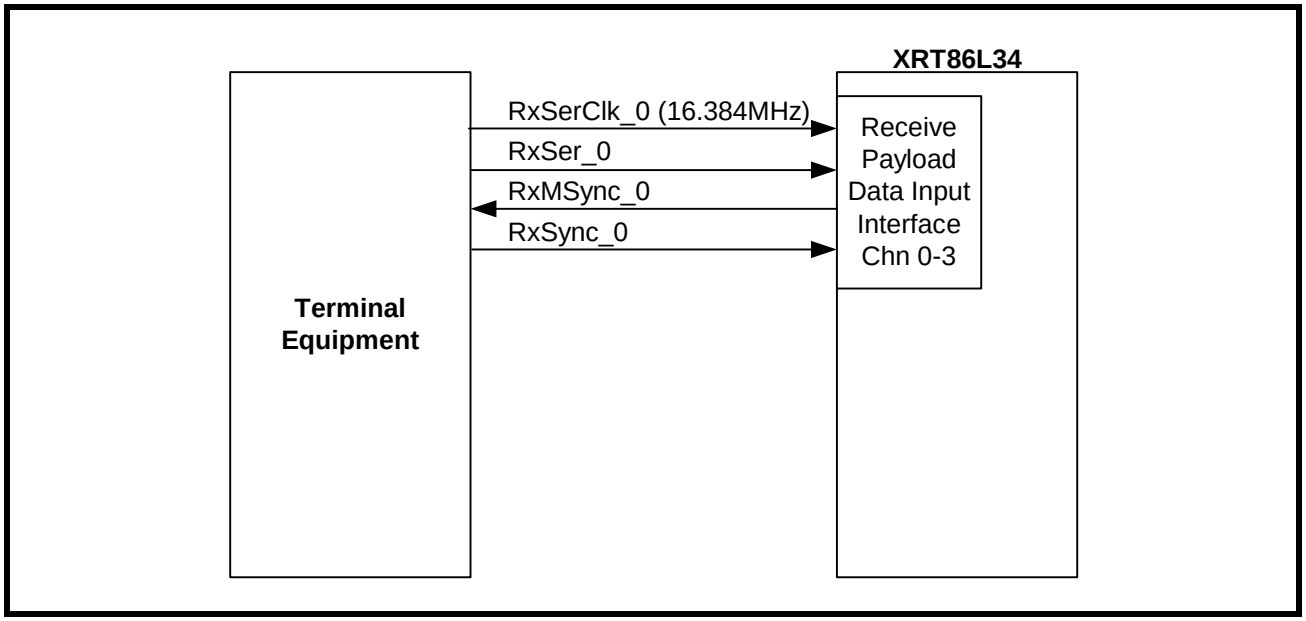
A_Y: The signaling bit A of Channel Y

5. After payload bits of Timeslot 0, 1 and 2 of all four channels are sent, the Receive High-speed Back-plane Interface should stuff another eight octets (sixty-four bits) of "don't care" data into the outgoing data stream.
6. Following the same rules of Step 2 to 5, the Receive High-speed Back-plane Interface stuffs eight octets of "don't care" data after sending twenty-four octets of multiplexed payload and signaling data. A 16.384Mbit/s data stream is thus created.

The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH for one clock cycle at the first bit position (F-bit of channel 0) of the data stream with data from Channel 0-3 multiplexed together. The Receive Single-frame Synchronization signal of Channel 4 pulses HIGH for one clock cycle at the first bit position (F-bit of Channel 4) of the data stream with data from Channel 4-7 multiplexed together. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the Receive High-speed Back-plane Interface of the framer can identify the beginning of a multiplexed frame and can start sending payload data of that frame.

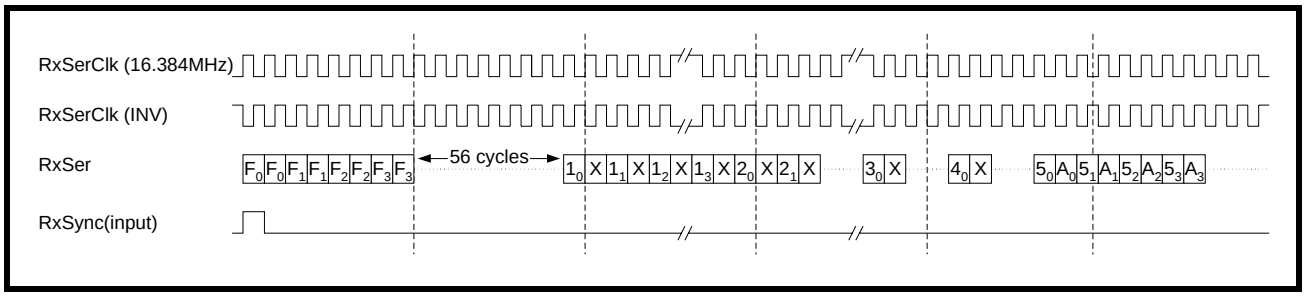
See Figure 114 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in Bit-multiplexed 16.384Mbit/s mode.

FIGURE 114. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 115 below when the framer is running at Bit-Multiplexed 16.384Mbit/s mode.

FIGURE 115. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT BIT-MULTIPLEXED 16.384MBIT/S



8.1.3.6 T1 Receive Input Interface - HMVIP 16.384Mbit/s

When the Receive Multiplex Enable bit is set to one and the Receive Interface Mode Select [1:0] bits are set to 10, the Receive Back-plane interface of framer is running at a clock rate of 16.384MHz.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane Interface is pumping out data through RxSer_0 or RxSer_4 pins at 16.384Mbit/s. The Receive High-speed Back-plane Interface multiplexes payload and signaling data of every four channels into

one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz are supplied to the Receive Serial Clock pin of Channel 0 and Channel 4 of the framer. The Receive High-speed Back-plane Interface of the farmer provides data at rising edge of this Receive Serial Clock. The local Terminal Equipment then latches incoming serial data at falling edge of the clock.

The Receive High-speed Back-plane Interface maps four 1.544Mbit/s DS1 data streams into this 16.384Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

FX: F-bit of Channel X

2. After the first octet of data is sent, the Receive High-speed Back-plane Interface insert seven octets (fifty-six bits) of "don't care" data into the outgoing data stream.
3. Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Terminal Equipment will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent the last. After the payload bits of Timeslot 0 of all four channels are sent, it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

NINTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

ELEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

THIRTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

FIFTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

XY: The Xth payload bit of Channel Y

4. The Receive High-speed Back-plane Interface also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream. When the Receive High-speed Back-plane Interface is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

TENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	6_0	B_0	7_0	C_0	8_0	D_0

TWELFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_1	A_1	6_1	B_1	7_1	C_1	8_1	D_1

FOURTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_2	A_2	6_2	B_2	7_2	C_2	8_2	D_2

SIXTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_3	A_3	6_3	B_3	7_3	C_3	8_3	D_3

X_Y: The Xth payload bit of Channel Y

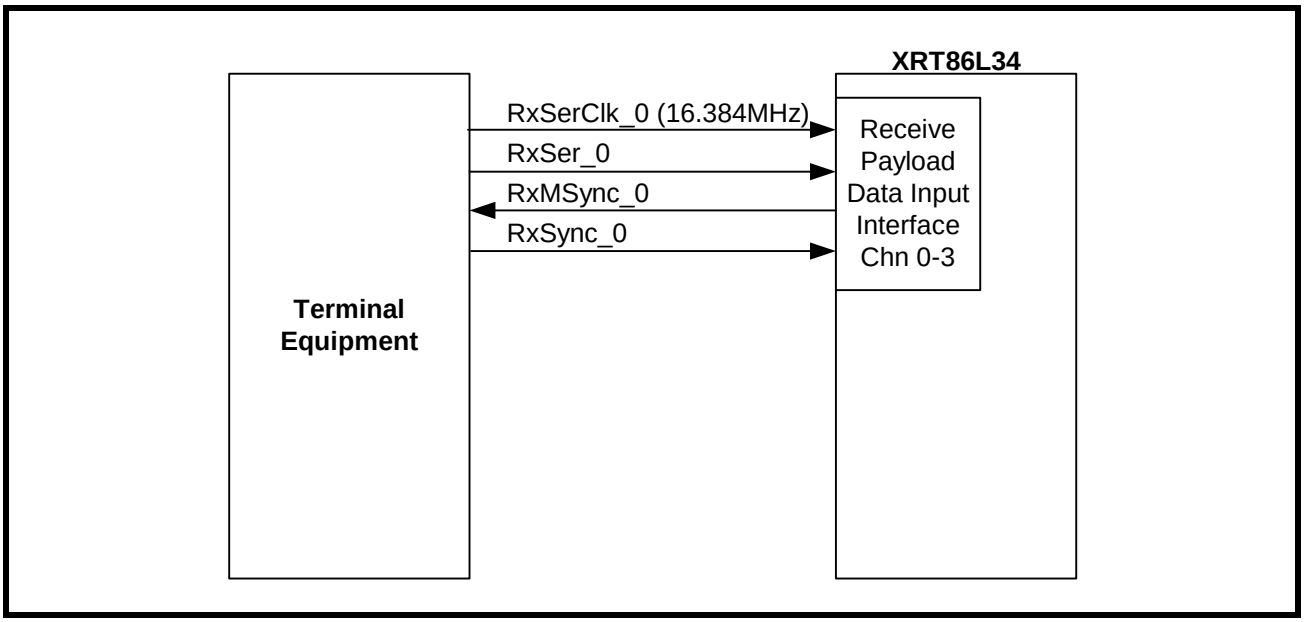
A_Y: The signaling bit A of Channel Y

5. After payload bits of Timeslot 0, 1 and 2 of all four channels are sent, the Receive High-speed Back-plane Interface should stuff another eight octets (sixty-four bits) of "don't care" data into the outgoing data stream.
6. Following the same rules of Step 2 to 5, Receive High-speed Back-plane Interface stuffs eight octets of "don't care" data after sending twenty-four octets of multiplexed payload and signaling data. A 16.384Mbit/s data stream is thus created.

The Receive Single-frame Synchronization signal should pulse HIGH for four clock cycles (the last two bit positions of the previous multiplexed frame and the first two bits of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the Receive High-speed Back-plane Interface of the framer can identify the beginning of a multiplexed frame and can start sending payload data of that frame.

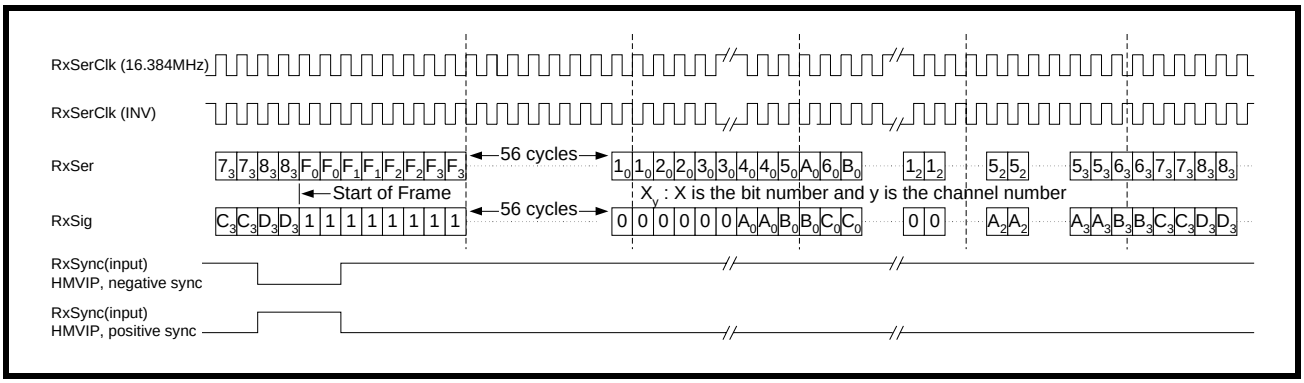
See Figure 116 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in HMVIP 16.384Mbit/s mode.

FIGURE 116. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 117 below when the framer is running at HMVIP 16.384Mbit/s mode.

FIGURE 117. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT HMVIP 16.384MBIT/S



8.1.3.7 T1 Receive Input Interface - H.100 16.384Mbit/s

When the Receive Multiplex Enable bit is set to one and the Receive Interface Mode Select [1:0] bits are set to 11, the Receive Back-plane interface of framer is running at H.100 16.384Mbit/s mode.

The HMVIP mode and the H.100 mode are essential the same except for the HIGH pulse position of the Receive Single-frame Synchronization Signal.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane Interface is pumping out data through RxSer_0 or RxSer_4 pins at 16.384Mbit/s. The Receive High-speed Back-plane Interface multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz are supplied to the Receive Serial Clock pin of Channel 0 and Channel 4 of the framer. The Receive High-speed Back-plane Interface of the farmer provides data at rising edge of this Receive Serial Clock. The local Terminal Equipment then latches incoming serial data at falling edge of the clock.

The Receive High-speed Back-plane Interface maps four 1.544Mbit/s DS1 data streams into this 16.384Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

F_X: F-bit of Channel X

2. After the first octet of data is sent, the Receive High-speed Back-plane Interface insert seven octets (fifty-six bits) of "don't care" data into the outgoing data stream.
3. Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Receive High-speed Back-plane Interface will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent the last. After the payload bits of Timeslot 0 of all four channels are sent,

it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

NINTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

ELEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

THIRTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

FIFTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

X_Y: The Xth payload bit of Channel Y

4. The Receive High-speed Back-plane Interface also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream. When the Receive High-speed Back-plane Interface is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

TENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	6_0	B_0	7_0	C_0	8_0	D_0

TWELFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_1	A_1	6_1	B_1	7_1	C_1	8_1	D_1

FOURTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_2	A_2	6_2	B_2	7_2	C_2	8_2	D_2

SIXTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_3	A_3	6_3	B_3	7_3	C_3	8_3	D_3

X_Y: The Xth payload bit of Channel Y

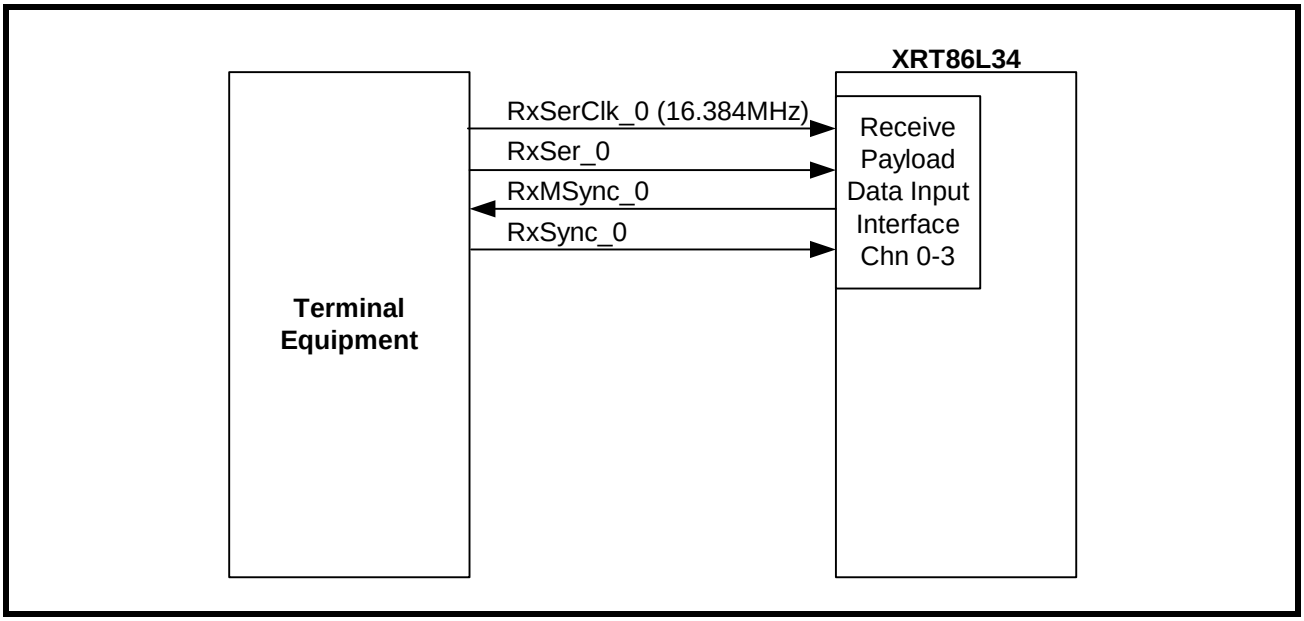
A_Y: The signaling bit A of Channel Y

5. After payload bits of Timeslot 0, 1 and 2 of all four channels are sent, the Terminal Equipment should stuff another eight octets (sixty-four bits) of "don't care" data into the outgoing data stream.
6. Following the same rules of Step 2 to 5, the Receive High-speed Back-plane Interface stuffs eight octets of "don't care" data after sending twenty-four octets of multiplexed payload and signaling data. A 16.384Mbit/s data stream is thus created.

The Receive Single-frame Synchronization signal should pulse HIGH for two clock cycles (the last bit position of the previous multiplexed frame and the first bit position of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the Receive High-speed Back-plane Interface of the framer can identify the beginning of a multiplexed frame and can start sending payload data of that frame.

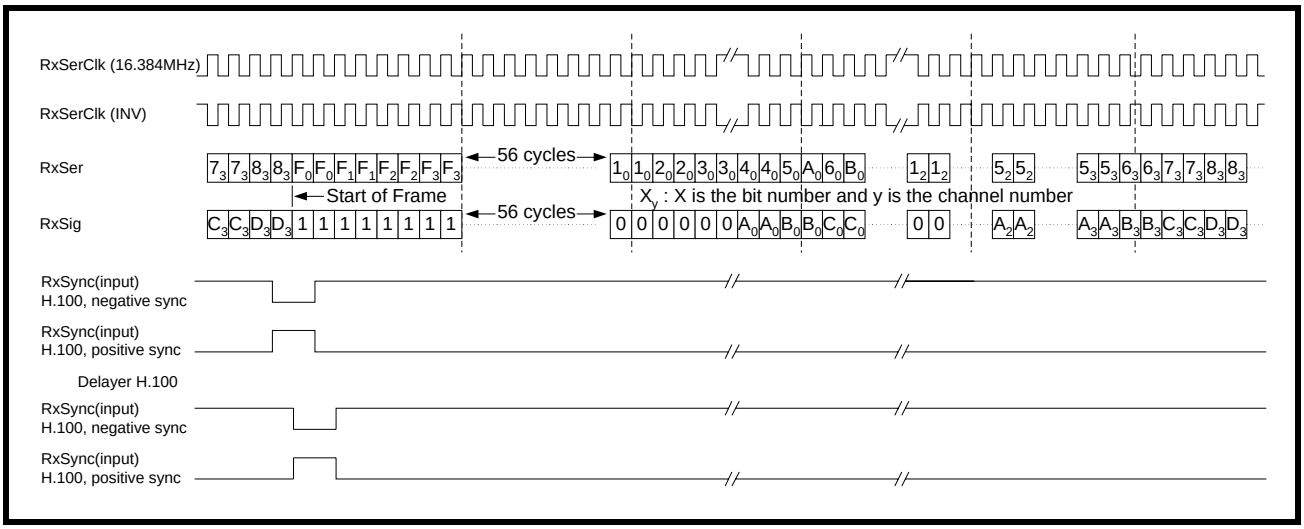
See Figure 118 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in HMVIP 16.384Mbit/s mode.

FIGURE 118. INTERFACING XRT86L34 TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 119 below when the framer is running at H.100 16.384Mbit/s mode.

FIGURE 119. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT H.100 16.384MBIT/S



8.2 DS1 RECEIVE FRAMER BLOCK

8.2.1 How to Configure XRT86L34 to Operate in DS1 Mode

The XRT86L34 Octal T1/E1/J1 Framer supports DS1, J1 or E1 framing modes. Since J1 standard is very similar to DS1 standard with a few minor changes, the J1 framing mode is included as a sub-set of the DS1 framing mode. All four framers within the XRT86L34 silicon can be individually configured to support DS1, J1 or E1 framing modes.

NOTE: *If transmitting section of one framer is configured to support either one of the framing modes, the receiving section is automatically configured to support the same framing modes.*

The T1/E1 Select bit of the Clock Select Register (CSR) controls which framing mode supported by the framer. The table below illustrates configurations of the T1/E1 Select bit of the Clock Select Register (CSR).

CLOCK SELECT REGISTER (CSR) (ADDRESS = 0XN100H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	T1/E1 Select	R/W	0 - The XRT86L34 framer is running in E1 mode. 1 - The XRT86L34 framer is running in T1 mode.

Since J1 and DS1 are two very similar standards, to configure the framer to run in J1 mode, the user has to select DS1 mode by setting the T1/E1 Select bit of the Clock Select Register to 1 first.

The next step is to set the J1 CRC Calculation bit of the Framing Select Register (FSR). If this bit is set to 1, the XRT86L34 will do CRC-6 calculation in J1 mode. That is, the CRC-6 calculation is based on the actual values of all 4,632 bits in DS1 multi-frame including framing bits. If this bit is set to 0, the XRT86L34 will perform CRC-6 calculation in DS1 mode. That is, the CRC-6 calculation is done based on the actual values of 4,608 payload bits of a DS1 multi-frame and assumes that all the framing bits are one.

The table below shows configurations of the J1 CRC Calculation bit of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (ADDRESS = 0XN107H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	J1 CRC Calculation	R/W	In J1 format, CRC-6 calculation is done based on the actual values of all payload bits as well as the framing bits. In DS1 format, CRC-6 calculation is done based on the payload bits only while assuming all the framing bits are one. 0 - The framer will perform CRC-6 calculation in DS1 format. 1 - The framer will perform CRC-6 calculation in J1 format. This feature permits the driver to comply with J1 standard.

The table below provides summary of how to select different operating modes for the XRT86L34 framer.

	T1/E1 SELECT BIT OF CSR	J1 CRC CALCULATION BIT OF FSR
T1	Set to 1	Set to 0
J1	Set to 1	Set to 1
E1	Set to 0	-

The purpose of the DS1 Receive Framer block is to accept framed DS1 data from the Receive DS1 LIU Interface block. The Receive Framer block will identify frame boundary and establish framing alignment synchronization of the incoming DS1 frame. The Receive Framer Block will then decode and extract user payload data from received frames Please note that the XRT86L34 has four (4) individual DS1 Transmit Framer blocks. Hence, the following description applies to all four of these individual Transmit DS1 Framer blocks.

The purpose of the DS1 Receive Framer block is:

- To identify frame boundary and establish framing alignment synchronization.
- To decode user data, inputted from the Receive DS1 LIU Interface block to the Terminal Equipment.
- To provide individual data control and signaling conditioning of each DS0 channel.
- To support the receiving and extraction of HDLC messages, from the remote receiving terminal.
- To detect error conditions and generate indications and interrupts to notify the user that the local receive framer has received error frames from the remote terminal.

- To receive and decode alarm condition indicators from the remote terminal.

The following sections discuss functionalities of the DS1 Receive Framer block in details.

8.2.2 How to Configure the Framer to Receive Data in Various DS1 Framing Formats

The XRT86L34 Octal T1/E1/J1 Framer supports the following DS1 framing formats:

- Super-Frame format (SF), also referred to as D4 framing
- Extended Super-Frame format (ESF)
- Non-signaling format (N)
- T1DM framing format
- SLC®96 data link framing format, which use the Super-Frame (SF) framing structure

NOTE: *If the framer is configured to receive DS1 frames according to one particular framing format, the transmitting side of the framer is also configured to transmit DS1 frames according to the same framing format.*

The user can set the Framing Format Select [2:0] bits of the Framing Select Register (FSR) to determine which DS1 framing format should XRT86L34 be configured to operate.

The table below shows configurations of the Framing Format Select [2:0] bits of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (ADDRESS = 0XN107H)

<table>
<tr><th>BIT NUMBER</th><th>BIT NAME</th><th>BIT TYPE</th><th>BIT DESCRIPTION</th></tr>
<tr><td>2-0</td><td>T1 Framing Select</td><td>R/W</td><td>These READ/WRITE bit-fields allow the user to select one of the five T1 framing formats supported by the framer. These framing formats include ESF, SLC®96, SF, N and T1DM mode.
<table>
<tr><th>Framing Format</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td>ESF</td><td>0</td><td>X</td><td>X</td></tr>
<tr><td>SLC®96</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>SF</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>N</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>T1DM</td><td>1</td><td>1</td><td>1</td></tr>
</table>
NOTE: Changing of framing format will automatically force the framer to perform re-synchronization.</td></tr>
</table>

8.2.3 How to Configure the Framer to Apply Data and Signaling Conditioning to Received DS1 Payload Data on a Per-Channel Basis

The XRT86L34 T1/J1/E1 Octal Framer provides individual control of each of the twenty-four DS0 channels. The user can apply data and signaling conditioning to the received DS1 payload data coming from the DS1 LIU Receive Block on a per-channel basis.

The XRT86L34 framer can apply the following changes to the received DS1 payload data coming from the Terminal Equipment on a per-channel basis:

- All 8 bits of the received payload data are inverted
- The even bits of the received payload data are inverted
- The odd bits of the received payload data are inverted
- The MSB of the received payload data is inverted
- All received payload data except the MSB are inverted

Configurations of the XRT86L34 framer to apply the above-mentioned changes to the received DS1 PAYLOAD data are controlled by the Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of each DS0 channel.

The XRT86L34 framer can also replace the incoming DS1 payload data from the DS1 LIU Receive Block with pre-defined or user-defined codes. The XRT86L34 supports the following conditioning substitutions:

- BUSY code - an octet with hexadecimal value of 0x7F
- BUSY_TS code - an octet of pattern "111xxxxx" where "xxxxx" represents the timeslot number
- VACANT code - an octet with hexadecimal value of 0xFF
- A-law Digital Milliwatt code
- u-law Digital Milliwatt code
- IDLE code - an octet defined by the value stored in the User IDLE Code Register (UCR)
- MOOF code - MUX-Out-Of-Frame code with hexadecimal value of 0x1A
- PRBS code - an octet generated by the Pseudo-Random Bit Sequence (PRBS) Generator block of the framer

Once again, configuration of the XRT86L34 framer to replace the received DS1 payload data with the above-mentioned coding schemes are controlled by the Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of each DS0 channel.

Finally, the XRT86L34 framer can configure any one or ones of the twenty-four DS0 channels to be D or E channels. D channel is used primarily for data link applications. E channel is used primarily for signaling for circuit switching with multiple access configurations.

The Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of each channel determine whether that particular channel is configured as D or E channel.

The table below illustrates configurations of the Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR).

RECEIVE CHANNEL CONTROL REGISTER (RCCR) (ADDRESS = 0XN360H - 0XN37FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Receive Conditioning Select	R/W	0000 - The received DS1 payload data of this DS0 channel is unchanged. 0001 - All 8 bits of the input DS1 payload data of this DS0 channel are inverted. 0010 - The even bits of the input DS1 payload data of this DS0 channel are inverted. 0011 - The odd bits of the input DS1 payload data of this DS0 channel are inverted. 0100 - The input DS1 payload data of this DS0 channel are replaced by the octet stored in User IDLE Code Register (UCR). 0101 - The input DS1 payload data of this DS0 channel are replaced by BUSY code (0x7F). 0110 - The input DS1 payload data of this DS0 channel are replaced by VACANT code (0xFF). 0111 - The input DS1 payload data of this DS0 channel are replaced by BUSY_TS code (111xxxxx). 1000 - The input DS1 payload data of this DS0 channel are replaced by MUX-Out-Of-Frame (MOOF) code with value 0x1A. 1001 - The input DS1 payload data of this DS0 channel are replaced by the A-law digital milliwatt pattern. 1010 - The input DS1 payload data of this DS0 channel are replaced by the u-law digital milliwatt pattern. 1011 - The MSB bit of the input DS1 payload data of this DS0 channel is inverted. 1100 - All bits of the input DS1 payload data of this DS0 channel except MSB bit are inverted. 1101 - The input DS1 payload data of this DS0 channel are replaced by PRBS pattern created by the internal PRBS Generator of XRT86L34 framer. 1110 - The input DS1 payload data of this DS0 channel is unchanged. 1111 - This channel is configured as D or E timeslot.

When the Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of a particular DS0 channel are set to 0100, the received DS1 payload data of this DS0 channel are replaced by the octet stored in the Receive User IDLE Code Register (RUCR). The table below shows contents of the Receive User IDLE Code Register.

RECEIVE USER IDLE CODE REGISTER (UCR) (ADDRESS = 0XN380H - 0XN397H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	User IDLE Code	R/W	These READ/WRITE bit-fields permits the user store any value of IDLE code into the framer. When the Receive Data Conditioning Select [3:0] bits of RCCR register of a particular DS0 channel are set to 0100, the received DS1 payload data are replaced by contents of this register and sent to the Terminal Equipment.

8.2.4 How to Configure the XRT86L34 Framer to Apply Zero Code Suppression to Received DS1 Payload Data on a Per-Channel Basis

In order to guarantee adequate clock recovery from the received PCM data, a minimum "ones density" must be maintained. In the case of an all zero channel, that is, if all the incoming PCM data of a particular DS0 channel from the Terminal Equipment is zero, the raw PCM data is replaced by a certain pattern that no more than fifteen consecutive zeros will occur. It is known as zero code suppression.

In the receive end, the user needs to know what type of zero code suppression scheme is applied on the receiving data. In this way, a correct decoding method or the reverse of zero code suppression can be done to extract the payload data from the DS1 LIU Receive Block.

The XRT86L34 framer supports three types of zero code suppression schemes:

- AT&T Bit 7 Stuffing - an old coding method that forces Bit 7 (the second LSB of a DS0 channel) to a 1 in an all zero channel.
- GTE Zero Code Suppression - Bit 8 (the LSB of a DS0 channel) is stuffed by 1 in non-signaling frame in an all zero channel. Otherwise, Bit 7 is stuffed by 1 in signaling frame if the signaling bit is zero.
- DDS Zero Code Suppression - an octet with hexadecimal value of 0x98 is used to replace the input data if it is all zero.

The Receive Zero Code Suppression Select [1:0] bits of the Receive Channel Control Register (RCCR) of a particular DS0 channel is used to select which type of zero code suppression scheme is applied to the received DS1 payload data. The table below shows configurations of the Receive Zero Code Suppression Select [1:0] bits of the Receive Channel Control Register (RCCR).

RECEIVE CHANNEL CONTROL REGISTER (RCCR) (ADDRESS = 0XN360H - 0XN37FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	Receive Zero Code Suppression Select	R/W	00 - The received DS1 PAYLOAD data of this DS0 channel is unchanged. No zero code suppression is used. 01 - AT&T Bit 7 stuffing is used. 10 - GTE zero code suppression is used. 11 - DDS zero code suppression is used.

8.2.5 How to Configure the XRT86L34 Framer to Extract Robbed-bit Signaling Information

The XRT86L34 T1/J1/E1 Octal Framer supports insertion of Robbed-bit Signaling information into the outgoing DS1 frame. It also supports extraction and substitution of Robbed-bit Signaling information from the incoming DS1 frame. The following section describes how does the XRT86L34 framer extract and substitute Robbed-bit Signaling in DS1 mode.

8.2.6 Configure the framer to receive and extract Robbed-bit Signaling

The XRT86L34 framer supports receiving and extraction of Robbed-bit Signaling in ESF, SF and SLC®96 framing formats. The Receive Signaling Extraction Control [1:0] bits of the Receive Signaling Control Register (RSCR) of each channel select either:

- No signaling extraction
- Two-code signaling
- Four-code signaling or
- Sixteen-code signaling

In SF or SLCâ96 mode, the Receive Signaling Extraction Control [1:0] bits can select no signaling (transparent), two-code signaling, or four-code signaling. Two-code signaling decoding is done by stripping the least significant bit (LSB) of the specific channel in frame 6 and 12 and stores it into the Signaling Bit A position of RSRA register array. Four-code signaling is done by stripping the LSB of channel data in frame 6 and the LSB of channel data in frame 12, and store them into Signaling Bit A and Signaling Bit B position of RSRA register array respectively. If 16-code signaling is selected in SF format, only the Signaling bit A and Signaling Bit B positions are filled.

In ESF mode, the Receive Signaling Extraction Control [1:0] bits can select no signaling (transparent), two-code signaling, four-code, or sixteen-code signaling. Two-code signaling decoding is done by stripping the least significant bit (LSB) of the specific channel in frame 6, 12, 18 and 24 and stores it into the Signaling Bit A position of RSRA register array. Four-code signaling is done by stripping the LSB of channel data in frame 6 and frame 18 and the LSB of channel data in frame 12 and 24, and store them into Signaling Bit A and Signaling Bit B position of RSRA register array respectively. Sixteen-code signaling is implemented by stripping the

LSB of channel data in frames 6, 12, 18, and 24 and stores them into the Signaling Bit A, Signaling Bit B, Signaling Bit C and Signaling Bit D position of RSRA register array respectively.

The table below shows configurations of the Receive Signaling Extraction Control [1:0] bits of the Receive Signaling Control Register.

RECEIVE SIGNALING CONTROL REGISTER (RSCR) (ADDRESS = 0XN3A0H - 0XN3B7H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Signaling Extraction Control	R/W	00 - The XRT86L34 framer does not extract signaling information from incoming DS1 payload data. 01 - The XRT86L34 framer extracts sixteen-code signaling information from incoming DS1 payload data. 10 - The XRT86L34 framer extracts four-code signaling information from incoming DS1 payload data. 11 - The XRT86L34 framer extracts two-code signaling information from incoming DS1 payload data.

Upon receiving and extraction of signaling bits from the incoming DS1 frames, the XRT86L34 framer compares the signaling bits with the previously received ones. If there is a change of signaling data, a Signaling Update (SIG) interrupt request may be generated at the end of a DS1 multi-frame. The user can thus be notified of a Change of Signaling Data event.

To enable the Signaling Update interrupt, the Signaling Change Interrupt Enable bit of the Framer Interrupt Enable Register (FIER) has to be set. In addition, the T1/E1 Framer Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Signaling Change Interrupt Enable bit of the Framer Interrupt Enable Register.

FRAMER INTERRUPT ENABLE REGISTER (FIER) (ADDRESS = 0XNB05H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Signaling Change Interrupt Enable	R/W	0 - The Signaling Update interrupt is disabled. 1 - The Signaling Update interrupt is enabled.

The table below shows configurations of the T1/E1 Framer Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	T1/E1 Framer Interrupt Enable	R/W	0 - Every interrupt generated by the Framer Interrupt Status Register (FISR) is disabled. 1 - Every interrupt generated by the Framer Interrupt Status Register (FISR) is enabled.

When these interrupt enable bits are set and the signaling information received is changed, the DS1 Receive Framer block will set the Signaling Updated status bit of the Framer Interrupt Status Register (FISR) to one. This status indicator is valid until the Framer Interrupt Status Register is read. Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Signaling Update status bits of the Framer Interrupt Status Register.

FRAMER INTERRUPT STATUS REGISTER (FISR) (ADDRESS = 0XNB04H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Signaling Updated	RUR / WC	0 - There is no change of signaling information in the incoming DS1 payload data. 1 - There is change of signaling information in the incoming DS1 payload data.

Now, there is only one problem remains. Since there are twenty-four DS0 channels in DS1, how do we know signaling information of which channel is changed?

To solve this problem, the XRT86L34 provides three 8-bit Signaling Change Registers to indicate the channel(s) which signaling data change had occurred over the last DS1 multi-frame period. Each bit of the Signaling Change Registers represents one timeslot of the DS1 frame. If any particular bit is zero, it means there is no change of signaling data occurred in that particular timeslot over the last DS1 multi-frame period. If any particular bit is one, it means there is change of signaling data occurred over the last DS1 multi-frame period.

The table below shows configurations of the Signaling Change Registers.

SIGNALING CHANGE REGISTERS (SCR) (ADDRESS = 0XN10DH - 0XN10FH)

LOCATION \ BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0XN10DH	CH 0	CH 1	CH 2	CH 3	CH 4	CH 5	CH 6	CH 7
0xn10EH	Ch 8	Ch 9	Ch 10	Ch 11	Ch 12	Ch 13	Ch 14	Ch 15
0xn10FH	Ch 16	Ch 17	Ch 18	Ch 19	Ch 20	Ch 21	Ch 22	Ch 23

By reading contents of the Signaling Update status bits of the Framer Interrupt Status Register and the Signaling Change Registers, the user can clearly identify which one(s) of the twenty-four DS0 channels has changed signaling information over the last multi-frame period.

Depending on configurations of the XRT86L34 framer, the signaling bits can be extracted from the incoming DS1 frame and direct to all or any one of the following destinations:

- Signaling data is stored to Receive Signaling Register Array (RSRA) of each channel
- Signaling data is sent to the Terminal Equipment through the Receive Signaling Output pin (RxSig_n)
- Signaling data is embedded into the output PCM data sending towards the Terminal Equipment through the Receive Serial Output pin (RxSer_n)

The follow sections discuss how to configure the XRT86L34 framer to extract signaling information bits and send them to different destinations.

8.2.6.1 Store Signaling Bits into RSRA Register Array

The four least significant bits of the Receive Signaling Register Array (RSRA) of each timeslot can be used to store received signaling data. The user can read these bits through microprocessor access. If the XRT86L34 framer is configure to extract signaling bits from incoming DS1 payload data, the DS1 Receive Framer block will strip off the least significant bits of signaling frames and store them into appropriate locations of the RSRA. The extraction of signaling bit from DS1 PCM data is done on a per-channel basis. The Bit 3 of RSRA register is used to hole Signaling bit A. Bit 2 is used to hold Signaling bit B. Bit 1 is used to hold Signaling bit C. Bit 0 is used to hold Signaling bit D.

The table below shows the four least significant bits of the Receive Signaling Register Array.

RECEIVE SIGNALING REGISTER ARRAY (RSRA) (ADDRESS = 0XN500H - 0XN517H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Signaling Bit A	R/W	This bit is used to store Signaling Bit A that is received and extracted as the least significant bit of timeslot of frame number 6.
2	Signaling Bit B	R/W	This bit is used to store Signaling Bit B that is received and extracted as the least significant bit of timeslot of frame number 12.
1	Signaling Bit C	R/W	This bit is used to store Signaling Bit C that is received and extracted as the least significant bit of timeslot of frame number 18.
0	Signaling Bit D	R/W	This bit is used to store Signaling Bit D that is received and extracted as the least significant bit of timeslot of frame number 24.

8.2.6.2 Outputting Signaling Bits through RxSig_n Pin

The XRT86L34 framer can be configure to output extracted signaling bits to external equipment through the RxSig_n pins. This pin is a multiplexed I/O pin with two functions:

- RxTSb[0]_n - Receive Timeslot Number Bit [0] Output pin
- RxSig_n - Receive Signaling Output pin

When the Receive Fractional DS1 bit of the Receive Interface Control Register (TICR) is set to 0, this pin is configured as RxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the DS1 PCM data that is receiving.

When the Receive Fractional DS1 bit of the Receive Interface Control Register (TICR) is set to 1, this pin is configured as RxSig_n pin, it acts as an output source for the signaling bits to be received in the inbound DS1 frames.

The table below shows configurations of the Receive Fractional DS1 bit of the Receive Interface Control Register (TICR).

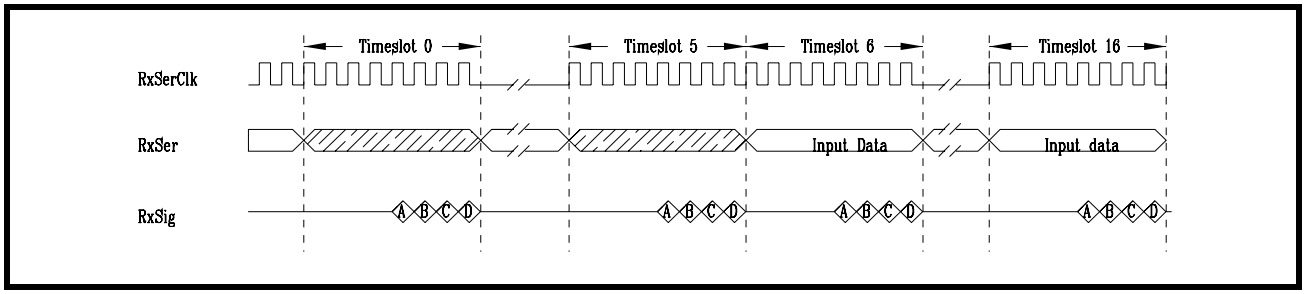
RECEIVE INTERFACE CONTROL REGISTER (TICR) (ADDRESS = 0XN120H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Fractional DS1	R/W	This READ/WRITE bit-field permits the user to determine which one of the two functions the multiplexed I/O pin of RxTSb[0]_n/RxSig_n is spotting. 0 - This pin is configured as RxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the DS1 PCM data that is receiving. 1 - This pin is configured as RxSig_n pin, it acts as an output source for the signaling bits to be received in the inbound DS1 frames

Figure 120 below is a timing diagram of the RxSig_n output pin. Please note that the Signaling Bit A of a certain timeslot coincides with Bit 3 of the Received serial output data; Signaling Bit B coincides with Bit 2 of the

Received serial output data; Signaling Bit C coincides with Bit 1 of the Received serial output data and Signaling Bit D coincides with Bit 0 of the Received serial output data.

FIGURE 120. TIMING DIAGRAM OF THE RXSIG_N OUTPUT PIN



The Receive Signaling Output Enable bit of the Receive Signaling Control Register (RSCR) determines whether the extracted signaling bits will be sent through the Receive Signaling Output pin (RxSig_n) to external equipments. The table below shows configurations of the Receive Signaling Output Enable bit of the Receive Signaling Control Register.

RECEIVE SIGNALING CONTROL REGISTER (RSCR) (ADDRESS = 0XN3A0H - 0XN3B7H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Signaling Output Enable	R/W	0 - The XRT86L34 framer will not send extracted signaling bits from the incoming DS1 payload data to external equipment through the Receive Signaling Output pin (RxSig_n). 1 - The XRT86L34 framer will send extracted signaling bits from the incoming DS1 payload data to external equipment through the Receive Signaling Output pin (RxSig_n).

8.2.6.3 Send Signaling Data through RxSer_n Pin

As mentioned in the above sections, signaling information embedded in the incoming DS1 PCM data can be sent to either the RSRA register array and/or sent through the Receive Signaling Output pin, at the same time, the signaling data will be directed to the Receive Serial Data Output pin together with other incoming DS1 payload data. The external equipment can thus still extract signaling data from the received DS1 payload data separately.

8.2.6.4 Signaling Data Substitution

After channel conditioning, the signaling conditioning can be optionally enabled by the RSCR registers. The actual signaling bits in each channel can be replaced either with all ones or with signaling bits stored in the Receive Substitution Signaling Register (RSSR). To enable signaling substitution, the Receive Signaling Substitution Enable bit of the Receive Signaling Control Register (RSCR) has to be set to one. The table below shows configuration of the Receive Signaling Substitution Enable bit of the Receive Signaling Control Register.

RECEIVE SIGNALING CONTROL REGISTER (RSCR) (ADDRESS = 0XN3A0H - 0XN3B7H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Receive Signaling Substitution Enable	R/W	0 - Signaling Substitution is disabled. The XRT86L34 framer will not replace extracted signaling bits from the incoming DS1 payload data with all ones or with signaling bits stored in RSSR registers. 1 - Signaling Substitution is enabled. The XRT86L34 framer will replace extracted signaling bits from the incoming DS1 payload data with all ones or with signaling bits stored in RSSR registers.

As mentioned before, the actual signaling bits in each channel can be replaced either with all ones or with signaling bits stored in the Receive Substitution Signaling Register (RSSR). The table below shows configurations of the Receive Substitution Signaling Register.

RECEIVE SUBSTITUTION SIGNALING REGISTER (RSSR) (ADDRESS = 0XN380H - 0XN397H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-4	Reserved	R/W	
3	SIG16-A SIG4-A SIG2-A		Sixteen-Code Signaling bit A Four-Code Signaling bit A Two-Code Signaling bit A
2	SIG16-B SIG4-B SIG2-A		Sixteen-Code Signaling bit B Four-Code Signaling bit B Two-Code Signaling bit A
1	SIG16-C SIG4-A SIG2-A		Sixteen-Code Signaling bit C Four-Code Signaling bit A Two-Code Signaling bit A
0	SIG16-D SIG4-B SIG2-A		Sixteen-Code Signaling bit D Four-Code Signaling bit B Two-Code Signaling bit A

In SF or SLC®96 mode, the Receive Signaling Substitution Control [1:0] bits can select all ones substitution, two-code signaling substitution, or four-code signaling substitution. The XRT86L34 framer can substitute received signaling bits with all ones. Two-code signaling substitution is done by substituting the least significant bit (LSB) of the specific channel in frame 6 and 12 with the content of the SIG2-A bit of the Receive Substitution Signaling Register (RSSR). Four-code signaling substitution is done by substituting the LSB of channel data in frame 6 with the SIG4-A bit and the LSB of channel data in frame 12 with the SIG4-B bit of the RSSR register. If 16-code signaling substitution is selected in SF format, only the SIG16-A bit and SIG16-B bit are used.

In ESF mode, the Receive Signaling Substitution Control [1:0] bits can select all ones substitution, two-code signaling substitution, four-code signaling substitution, or sixteen-code signaling. The XRT86L34 framer can substitute received signaling bits with all ones. Two-code signaling substitution is done by substituting the LSB of the specific channel in frame 6, 12, 18, and 24 with the content of the SIG2-A bit of the register. Four-code signaling substitution is done by substituting the LSB of channel data in frames 6 and 18 with the SIG4-A bit and the LSB of channel data in frames 12 and 24 with the SIG4-B bit of the RSSR register. Sixteen-code signaling substitution is implemented by substituting the LSB of channel data in frames 6, 12, 18, and 24 with the content of SIG16-A, SIG16-B, SIG16-C, and SIG16-D bits of RSSR register respectively.

The table below shows configurations of the Receive Signaling Substitution Control [1:0] bits of the Receive Signaling Control Register.

RECEIVE SIGNALING CONTROL REGISTER (RSCR) (ADDRESS = 0XN340H - 0XN357H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Receive Signaling Substitution Control	R/W	00 - The received signaling bits are replaced by all ones and send to the external equipment. 01 - Two-code signaling substitution is applied to the received signaling bits. The replaced signaling information is sent to the external equipment. 10 - Four-code signaling substitution is applied to the received signaling bits. The replaced signaling information is sent to the external equipment. 11 - Sixteen-code signaling substitution is applied to the received signaling bits. The replaced signaling information is sent to the external equipment. ***NOTE:*** *In SF mode, this option is disabled.*

9.0 LIU RECEIVE PATH

9.1 LINE TERMINATION (RTIP/RRING)

9.1.1 CASE 1: Internal Termination

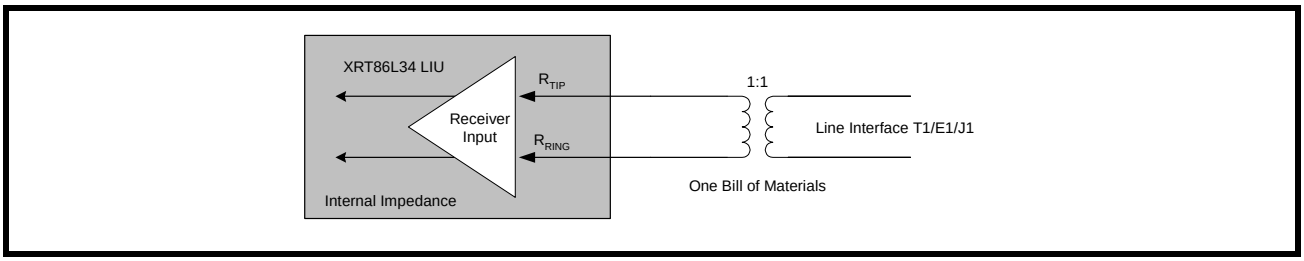
The input stage of the receive path accepts standard T1/E1/J1 twisted pair or E1 coaxial cable inputs through RTIP and RRING. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The receive termination impedance is selected by programming TERSEL[1:0] to match the line impedance. Selecting the internal impedance is shown in Table 182.

TABLE 182: SELECTING THE INTERNAL IMPEDANCE

TERSEL[1:0]	RECEIVE TERMINATION
0h (00)	100Ω
1h (01)	110Ω
2h (10)	75Ω
3h (11)	120Ω

The XRT86L34 has the ability to switch the internal termination to "High" impedance by programming RxTSEL in the appropriate channel register. For internal termination, set RxTSEL to "1". By default, RxTSEL is set to "0" ("High" impedance). For redundancy applications, a dedicated hardware pin (RxTSEL) is also available to control the receive termination for all channels simultaneously. This hardware pin takes priority over the register setting if RxTCNTL is set to "1" in the appropriate global register. If RxTCNTL is set to "0", the state of this pin is ignored. See Figure 121 for a typical connection diagram using the internal termination.

FIGURE 121. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION



9.1.2 CASE 2: Internal Termination With One External Fixed Resistor for All Modes

Along with the internal termination, a high precision external fixed resistor can be used to optimize the return loss. This external resistor can be used for all modes of operation ensuring one bill of materials. There are three resistor values that can be used by setting the RxRES[1:0] bits in the appropriate channel register. Selecting the value for the external fixed resistor is shown in Table 183.

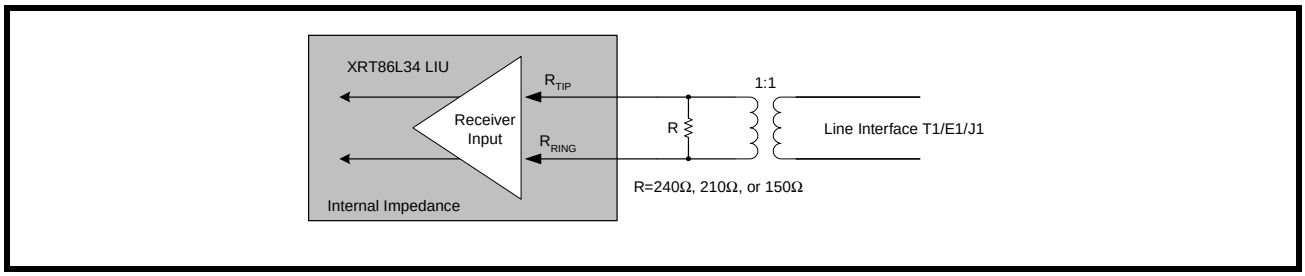
TABLE 183: SELECTING THE VALUE OF THE EXTERNAL FIXED RESISTOR

RXRES[1:0]	EXTERNAL FIXED RESISTOR
0h (00)	None
1h (01)	240Ω
2h (10)	210Ω
3h (11)	150Ω

By default, RxRES[1:0] is set to "None" for no external fixed resistor. If an external fixed resistor is used, the XRT86L34 uses the parallel combination of the external fixed resistor and the internal termination as the input impedance. See Figure 122 for a typical connection diagram using the external fixed resistor.

NOTE: *Without the external resistor, the XRT86L34 meets all return loss specifications. This mode was created to add flexibility for optimizing return loss by using a high precision external resistor.*

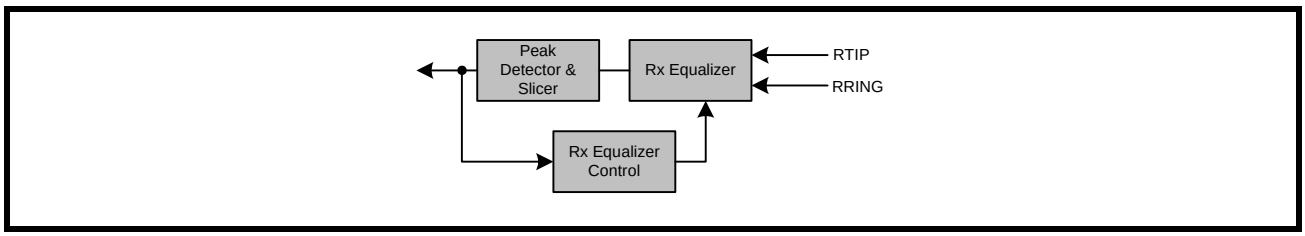
FIGURE 122. TYPICAL CONNECTION DIAGRAM USING ONE EXTERNAL FIXED RESISTOR



9.1.3 Equalizer Control

The main objective of the equalizer is to amplify an input attenuated signal to a pre-determined amplitude that is acceptable to the peak detector circuit. Using feedback from the peak detector, the equalizer will gain the input up to the maximum value specified by the equalizer control bits, in the appropriate channel register, normalizing the signal. Once the signal has reached the pre-determined amplitude, the signal is then processed within the peak detector and slicer circuit. A simplified block diagram of the equalizer and peak detector is shown in Figure 123.

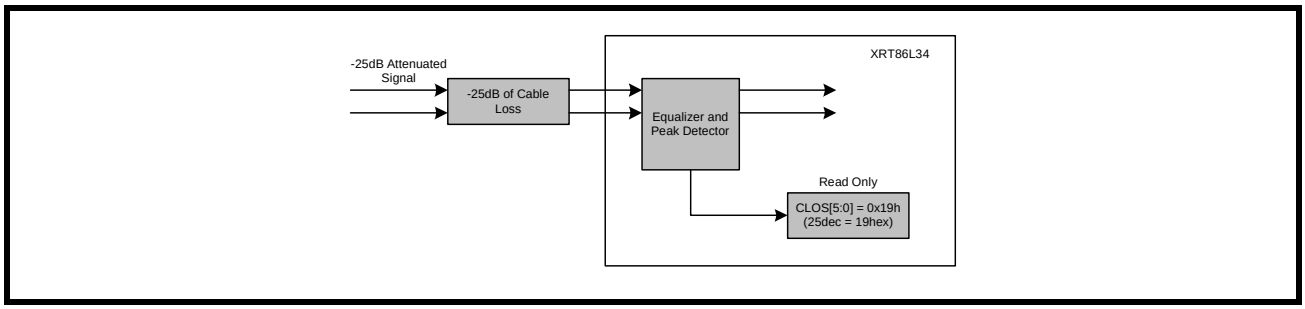
FIGURE 123. SIMPLIFIED BLOCK DIAGRAM OF THE EQUALIZER AND PEAK DETECTOR



9.1.4 Cable Loss Indicator

The ability to monitor the cable loss attenuation of the receiver inputs is a valuable feature. The XRT86L34 contains a per channel, read only register for cable loss indication. CLOS[5:0] is a 6-Bit binary word that reports the value of cable loss in 1dB steps with an absolute accuracy of ±1dB. An example of -25dB cable loss attenuation is shown in Figure 124.

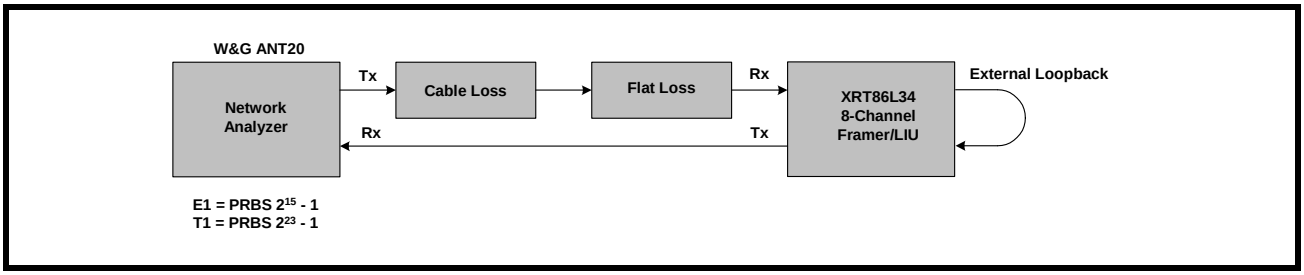
FIGURE 124. SIMPLIFIED BLOCK DIAGRAM OF THE CABLE LOSS INDICATOR



9.2 RECEIVE SENSITIVITY

To meet Long Haul receive sensitivity requirements, the XRT86L34 can accept T1/E1/J1 signals that have been attenuated by 43dB cable attenuation in E1 mode or 36dB cable attenuation in T1 mode without experiencing bit errors, LOF, pattern synchronization, etc. Short haul specifications are for 12dB of flat loss in E1 mode. T1 specifications are 655 feet of cable loss along with 6dB of flat loss in T1 mode. The XRT86L34 can tolerate cable loss and flat loss beyond the industry specifications. The receive sensitivity in the short haul mode is approximately 4,000 feet without experiencing bit errors, LOF, pattern synchronization, etc. Although data integrity is maintained, the RLOS function (if enabled) will report an RLOS condition according to the receiver loss of signal section in this datasheet. The test configuration for measuring the receive sensitivity is shown in Figure 125.

FIGURE 125. TEST CONFIGURATION FOR MEASURING RECEIVE SENSITIVITY



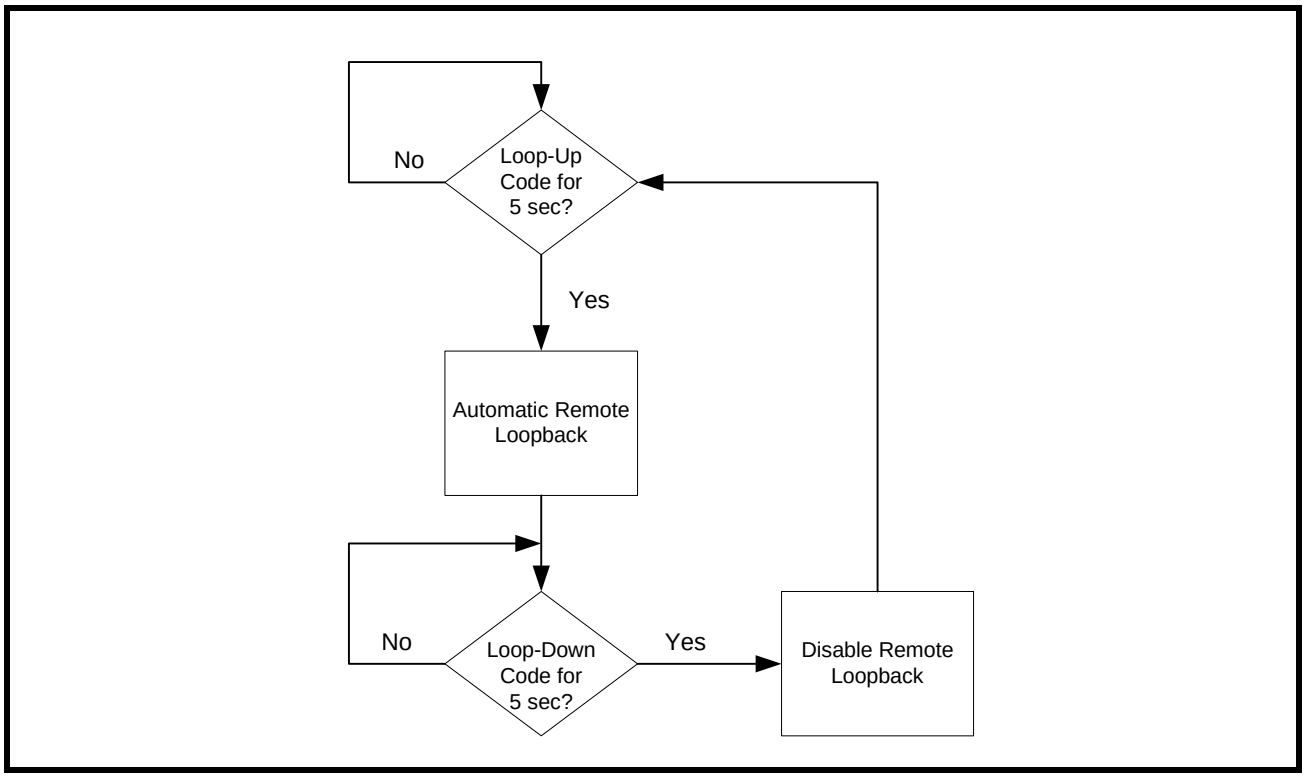
9.2.1 AIS (Alarm Indication Signal)

The XRT86L34 adheres to the ITU-T G.775 specification for an all ones pattern. The alarm indication signal is set to "1" if an all ones pattern (at least 99.9% ones density) is present for T, where T is 3ms to 75ms in T1 mode. AIS will clear when the ones density is not met within the same time period T. In E1 mode, the AIS is set to "1" if the incoming signal has 2 or less zeros in a 512-bit window. AIS will clear when the incoming signal has 3 or more zeros in the 512-bit window.

9.2.2 NLCD (Network Loop Code Detection)

The Network Loop Code Detection can be programmed to detect a Loop-Up, Loop-Down, or Automatic Loop Code. If the network loop code detection is programmed for Loop-Up, the NLCD will be set "High" if a repeating pattern of "00001" occurs for more than 5 seconds. If the network loop code detection is programmed for Loop-Down, the NLCD will be set "High" if a repeating pattern of "001" occurs for more than 5 seconds. If the network loop code detection is programmed for automatic loop code, the LIU is configured to detect a Loop-Up code. If a Loop-Up code is detected for more than 5 seconds, the XRT86L34 will automatically program the channel into a remote loopback mode. The LIU will remain in remote loopback even if the Loop-Up code disappears. The channel will continue in remote loop back until a Loop-Down code is detected for more than 5 seconds (or, if the automatic loop code is disabled) and then automatically return to normal operation with no loop back. The process of the automatic loop code detection is shown in Figure 126.

FIGURE 126. PROCESS BLOCK FOR AUTOMATIC LOOP CODE DETECTION



9.2.3 FLSD (FIFO Limit Status Detection)

The purpose of the FIFO limit status is to indicate when the Read and Write FIFO pointers are within a pre-determined range (over-flow or under-flow indication). The FLSD is set to "1" if the FIFO Read and Write Pointers are within ±3-Bits.

9.2.4 Receive Jitter Attenuator

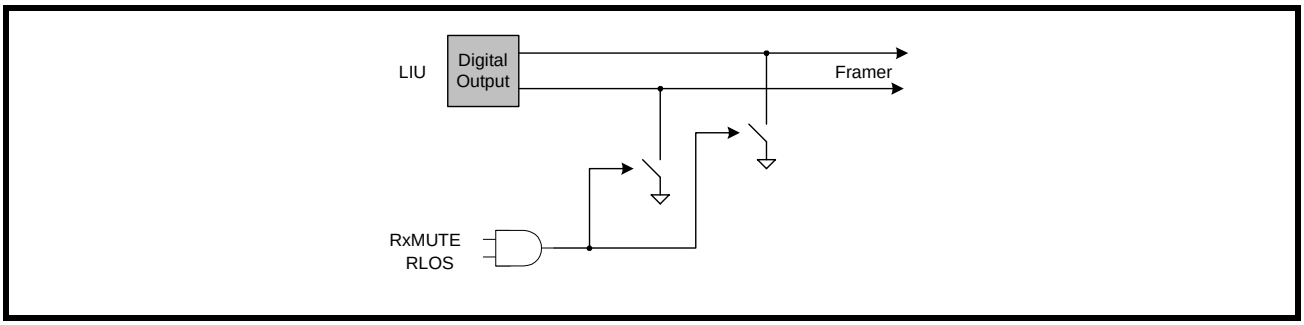
The receive path has a dedicated jitter attenuator to reduce phase and frequency jitter in the recovered clock. The jitter attenuator uses a data FIFO (First In First Out) with a programmable depth of 32-bit or 64-bit. If the LIU is used for line synchronization (loop timing systems), the JA should be enabled in the receive path. When the Read and Write pointers of the FIFO are within 2-Bits of over-flowing or under-flowing, the bandwidth of the jitter attenuator is widened to track the short term input jitter, thereby avoiding data corruption. When this condition occurs, the jitter attenuator will not attenuate input jitter until the Read/Write pointer's position is outside the 2-Bit window. In T1 mode, the bandwidth of the JA is always set to 3Hz. In E1 mode, the bandwidth is programmable to either 10Hz or 1.5Hz (1.5Hz automatically selects the 64-Bit FIFO depth). The JA has a clock delay equal to ½ of the FIFO bit depth.

NOTE: *The Transmit Path has a dedicated jitter attenuator. See the Transmit Path Line Interface Section.*

9.2.5 RxMUTE (Receiver LOS with Data Muting)

The receive muting function can be selected by setting RxMUTE to "1" in the appropriate global register. If selected, any channel that experiences an RLOS condition will automatically pull the output of the LIU section "Low" to prevent data chattering. If RLOS does not occur, the RxMUTE will remain inactive until an RLOS on a given channel occurs. The default setting for RxMUTE is "0" which is disabled. A simplified block diagram of the RxMUTE function is shown in Figure 127.

FIGURE 127. SIMPLIFIED BLOCK DIAGRAM OF THE RXMUTE FUNCTION



10.0 ALARMS AND ERROR CONDITIONS

The XRT86L34 T1/J1/E1 Octal Framer can be configured to monitor quality of received DS1 frames. It can generate error indicators if the local receive framer has received error frames from the remote terminal. If corresponding interrupt is enabled, the local microprocessor operation is interrupted by these error conditions. Upon microprocessor interruption, the user can intervene by looking into the error conditions.

At the same time, the user can configure the XRT86L34 framer to transmit alarms and error indications to remote terminal. Different alarms and error indications will be transmitted depending on the error condition.

The section below gives a brief discussion of the error conditions that can be detected by the XRT86L34 framer and error indications that will be generated.

10.1 AIS ALARM

As we discussed before, transmission of Alarm Indication Signal (AIS) or Blue Alarm by the intermediate node indicates that the equipment is still functioning but unable to offer services. It is an all ones (except for framing bits) pattern which can be used by the equipment further down the line to maintain clock recovery and timing synchronization.

The XRT86L34 framer can detect two types of AIS in DS1 mode:

- Framed AIS
- Unframed AIS

Unframed AIS is an all ones pattern. If unframed AIS is sent, the equipment further down the line will be able to maintain timing synchronization and be able to recover clock from the received AIS signal. However, due to the lack of framing bits, the equipment farther down the line will not be able to maintain frame synchronization and will declare Loss of Frame (LOF).

On the other hand, the payload portion of a framed AIS pattern is all ones. However, a framed AIS pattern still has correct framing bits. Therefore, the equipment further down the line can still maintain frame synchronization as well as timing synchronization. In this case, no LOF or Red alarm will be declared.

The Alarm indication logic within the Receive Framer block of the XRT86L34 framer monitors the incoming DS1 frames for AIS. AIS alarm condition are detected and declared according to the following procedure:

1. The incoming DS1 frames are monitored for AIS detection. AIS detection is defined as an unframed or framed pattern with less than three zeros in two consecutive frames.
2. An AIS detection counter within the Receive Framer block of the XRT86L34 counts the occurrences of AIS detection over a 6 ms interval. It will indicate a valid AIS flag when twenty-two or more of a possible twenty-four AIS are detected.
3. Each 6 ms interval with a valid AIS flag increments a flag counter which declares AIS alarm when 255 valid flags have been collected.

Therefore, AIS condition has to be persisted for 1.53 seconds before AIS alarm condition is declared by the XRT86L34 framer.

If there is no valid AIS flag over a 6ms interval, the Alarm indication logic will decrement the flag counter. The AIS alarm is removed when the counter reaches 0. That is, AIS alarm will be removed if over 1.53 seconds, there is no valid AIS flag.

The Alarm Indication Signal Detection Select [1:0] bits of the Alarm Generation Register (AGR) enable the two types of AIS detection that are supported by the XRT86L34 framer. The table below shows configurations of the Alarm Indication Signal Detection Select [1:0] bits of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR) (ADDRESS = 0XN108H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	AIS Detection Select	R/W	00 - AIS alarm detection is disabled.When this bit is set to 01:Detection of unframed AIS alarm of all ones pattern is enabled. 10 - AIS alarm detection is disabled.When this bit is set to 00:Detection of framed AIS alarm of all ones pattern except for framing bits is enabled.

If detection of unframed or framed AIS alarm is enabled by the user and if AIS is present in the incoming DS1 frame, the XRT86L34 framer can generate a Receive AIS State Change interrupt associated with the setting of Receive AIS State Change bit of the Alarm and Error Status Register to one.

To enable the Receive AIS State Change interrupt, the Receive AIS State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) have to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive AIS State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (ADDRESS = 0XNB03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive AIS State Change Interrupt Enable	R/W	0 - The Receive AIS State Change interrupt is disabled. 1 - The Receive AIS State Change interrupt is enabled.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and AIS is present in the incoming DS1 frame, the XRT86L34 framer will declare AIS by doing the following:

- Set the read-only Receive AIS State bit of the Alarm and Error Status Register (AESR) to one indicating there is AIS alarm detected in the incoming DS1 frame.
- Set the Receive AIS State Change bit of the Alarm and Error Status Register to one indicating there is a change in state of AIS. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive AIS State Change status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive AIS State Change	RUR / WC	0 - There is no change of AIS state in the incoming DS1 payload data. 1 - There is change of AIS state in the incoming DS1 payload data.

The Receive AIS State bit of the Alarm and Error Status Register (AESR), on the other hand, is a read-only bit indicating there is AIS alarm detected in the incoming DS1 frame.

The table below shows the Receive AIS State status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Receive AIS State	R	0 - There is no AIS alarm condition detected in the incoming DS1 payload data. 1 - There is AIS alarm condition detected in the incoming DS1 payload data.

10.2 RED ALARM

The Alarm indication logic within the Receive Framer block of the XRT86L34 framer monitors the incoming DS1 frames for red alarm or Loss of Frame (LOF) condition. Red alarm condition are detected and declared according to the following procedure:

1. The red alarm is detected by monitoring the occurrence of Loss of Frame (LOF) over a 6 ms interval.
2. An LOF valid flag will be posted on the interval when one or more LOF occurred during the interval.
3. Each interval with a valid LOF flag increments a flag counter which declares RED alarm when 63 valid intervals have been accumulated.
4. An interval without valid LOF flag decrements the flag counter. The Red alarm is removed when the counter reaches zero.

If LOF condition is present in the incoming DS1 frame, the XRT86L34 framer can generate a Receive Red Alarm State Change interrupt associated with the setting of Receive Red Alarm State Change bit of the Alarm and Error Status Register to one.

To enable the Receive Red Alarm State Change interrupt, the Receive Red Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Red Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (ADDRESS = 0XNB03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Red Alarm State Change Interrupt Enable	R/W	0 - The Receive Red Alarm State Change interrupt is disabled. No Receive Loss of Frame (RxLOF) interrupt will be generated upon detection of LOF condition. 1 - The Receive Red Alarm State Change interrupt is enabled. Receive Loss of Frame (RxLOF) interrupt will be generated upon detection of LOF condition.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and Red Alarm is present in the incoming DS1 frame, the XRT86L34 framer will declare Red Alarm by doing the following:

- Set the read-only Receive Red Alarm State bit of the Alarm and Error Status Register (AESR) to one indicating there is Red Alarm detected in the incoming DS1 frame.
- Set the Receive Red Alarm State Change bit of the Alarm and Error Status Register to one indicating there is a change in state of Red Alarm. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Red Alarm State Change status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Red Alarm State Change	RUR / WC	0 - There is no change of Red Alarm state in the incoming DS1 payload data. 1 - There is change of Red Alarm state in the incoming DS1 payload data.

The Receive Red Alarm State bit of the Alarm and Error Status Register (AESR), on the other hand, is a read-only bit indicating there is Red Alarm detected in the incoming DS1 frame.

The table below shows the Receive Red Alarm State status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Red Alarm State	R	0 - There is no Red Alarm condition detected in the incoming DS1 payload data. 1 - There is Red Alarm condition detected in the incoming DS1 payload data.

10.3 YELLOW ALARM

The Alarm indication logic within the Receive Framer block of the XRT86L34 framer monitors the incoming DS1 frames for Yellow Alarm condition. The yellow alarm is detected and declared according to the following procedure:

1. Monitor the occurrence of Yellow Alarm pattern over a 6 ms interval. A YEL valid flag will be posted on the interval when Yellow Alarm pattern occurred during the interval.
2. Each interval with a valid YEL flag increments a flag counter which declares YEL alarm when 80 valid intervals have been accumulated.
3. An interval without valid YEL flag decrements the flag counter. The YEL alarm is removed when the counter reaches zero.

If Yellow Alarm condition is present in the incoming DS1 frame, the XRT86L34 framer can generate a Receive Yellow Alarm State Change interrupt associated with the setting of Receive Yellow Alarm State Change bit of the Alarm and Error Status Register to one.

To enable the Receive Yellow Alarm State Change interrupt, the Receive Yellow Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Yellow Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (ADDRESS = 0XNB03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Receive Yellow Alarm State Change Interrupt Enable	R/W	0 - The Receive Yellow Alarm State Change interrupt is disabled. Any state change of Receive Yellow Alarm will not generate an interrupt. 1 - The Receive Yellow Alarm State Change interrupt is enabled. Any state change of Receive Yellow Alarm will generate an interrupt.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and Yellow Alarm is present in the incoming DS1 frame, the XRT86L34 framer will declare Yellow Alarm by doing the following:

- Set the read-only Receive Yellow Alarm State bit of the Alarm and Error Status Register (AESR) to one indicating there is Yellow Alarm detected in the incoming DS1 frame.
- Set the Receive Yellow Alarm State Change bit of the Alarm and Error Status Register to one indicating there is a change in state of Yellow Alarm. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Yellow Alarm State Change status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR)(ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Receive Yellow Alarm State Change	RUR / WC	0 - There is no change of Yellow Alarm state in the incoming DS1 payload data. 1 - There is change of Yellow Alarm state in the incoming DS1 payload data.

The table below shows the Receive AIS State Change status bits of the Alarm and Error Status Register.

The Receive Yellow Alarm State bit of the Alarm and Error Status Register (AESR), on the other hand, is a read-only bit indicating there is Yellow Alarm detected in the incoming DS1 frame.

The table below shows the Receive Yellow Alarm State status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Yellow Alarm State	R	0 - There is no Yellow Alarm condition detected in the incoming DS1 payload data. 1 - There is Yellow Alarm condition detected in the incoming DS1 payload data.

10.4 BIPOLAR VIOLATION

The line coding for the DS1 signal should be bipolar. That is, a binary "0" is transmitted as zero volts while a binary "1" is transmitted as either a positive or negative pulse, opposite in polarity to the previous pulse. A Bipolar Violation or BPV occurs when the alternate polarity rule is violated. The Alarm indication logic within the Receive Framer block of the XRT86L34 framer monitors the incoming DS1 frames for Bipolar Violations.

If a Bipolar Violation is present in the incoming DS1 frame, the XRT86L34 framer can generate a Receive Bipolar Violation interrupt associated with the setting of Receive Bipolar Violation bit of the Alarm and Error Status Register to one.

To enable the Receive Bipolar Violation interrupt, the Receive Bipolar Violation Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Bipolar Violation Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (ADDRESS = 0XNB03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Bipolar Violation Interrupt Enable	R/W	0 - The Receive Bipolar Violation interrupt is disabled. Occurrence of one or more bipolar violations will not generate an interrupt. 1 - The Receive Bipolar Violation interrupt is enabled. Occurrence of one or more bipolar violations will generate an interrupt.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and one or more Bipolar Violations are present in the incoming DS1 frame, the XRT86L34 framer will declare Receive Bipolar Violation by doing the following:

- Set the Receive Bipolar Violation bit of the Alarm and Error Status Register to one indicating there are one or more Bipolar Violations. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Bipolar Violation status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Bipolar Violation State Change	RUR / WC	0 - There is no change of Bipolar Violation state in the incoming DS1 payload data. 1 - There is change of Bipolar Violation state in the incoming DS1 payload data.

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (ADDRESS = 0XNB03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Loss of Signal Interrupt Enable	R/W	0 - The Receive Loss of Signal interrupt is disabled. Occurrence of Loss of Signals will not generate an interrupt. 1 - The Receive Loss of Signal interrupt is enabled. Occurrence of Loss of Signals will generate an interrupt.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and one or more Loss of Signals are present in the incoming DS1 frame, the XRT86L34 framer will declare Receive Loss of Signal by doing the following:

- Set the Receive Loss of Signal bit of the Alarm and Error Status Register to one indicating there is one or more Loss of Signals. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Loss of Signal status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Loss of Signal State	RUR / WC	0 - There is no change of Loss of Signal state in the incoming DS1 payload data. 1 - There is change of Loss of Signal state in the incoming DS1 payload data.

11.0 PERFORMANCE MONITORING (PMON)

The function of Performance Monitoring is designed to accumulate error events like line code (bipolar) violations, parity errors, frame alignment errors, etc. using saturating counters. When an accumulation interval is signaled by a one-second interrupt (if enabled), the current counter value can be accessed by the microprocessor. After a read by the microprocessor, the counters are reset and begin accumulating error events for the next interval. The counters are reset in such a manner that error events during the reset period are not missed.

11.1 RECEIVE LINE CODE VILOATION COUNTER (16-BIT)

A line code violation is any event of pulses that does not comply with B8ZS or HDB3 encoding standards. Line code violations and bi-polar violations cause the LCV counter to increment if this feature is enabled. The MSB is stored in register 0xn900h and the LSB is stored in register 0xn901h.

11.2 16-BIT RECEIVE FRAME ALIGNMENT ERROR COUNTER (16-BIT)

A framing bit error event is defined as a error pattern found in FAS or bit 2 of the non-FAS. This counter is disabled during loss of frame synchronization conditions. It is not disabled during loss of synchronization at either the CAS or CRC-4 multiframe stage. The MSB is stored in register 0xn902h and the LSB is stored in register 0xn903h.

11.3 RECEIVE SEVERELY ERRORED FRAME COUNTER (8-BIT)

A severely errored frame event is defined as the occurrence of two consecutive errored frame alignment signals that are not responsible for loss of frame alignment. The contents of this register are stored in 0xn904h.

11.4 RECEIVE CRC-6/4 BLOCK ERROR COUNTER (16-BIT)

A synchronization bit error event is defined as a CRC-6/4 error received. The counter is disabled during loss of sync at either the Frame/FAS or ESF/CRC4 level, but it will not be disabled if loss of multiframe sync occurs at the CAS level. The MSB is stored in register 0xn905h and the LSB is stored in register 0xn906h.

11.5 RECEIVE FAR-END BLOCK ERROR COUNTER (16-BIT)

11.6 RECEIVE SLIP COUNTER (8-BIT)

A slip event is defined as a replication or deleton of a T1/E1 frame by the receiving slip buffer. The contents of this register are stored in 0xn909h.

11.7 RECEIVE LOSS OF FRAME COUNTER (8-BIT)

A LOFC is a count of the number of times a Loss of FAS Frame has been declared. This parameter provides the capability to measure an accumulation of short failure events. The contents of this register are stored in 0xn90Ah.

11.8 RECEIVE CHANGE OF FRAME ALIGNMENT COUNTER (8-BIT)

A COFA is declared when the newly-locked framing is different from the one offered by off-line framer. The contents of this register are stored in 0xn90Bh.

11.9 FRAME CHECK SEQUENCE ERROR COUNTERS 1, 2, AND 3 (8-BIT EACH)

These counters accumulate the times of occurrence the receive frame check sequence error is detected by the LAPD controllers. The contents forLAPD 1 are stored in register 0xn90Ch. The contents for LAPD 2 are stored in register 0xn91Ch. The contents for LAPD 3 are stored in register 0xn92Ch.

11.10 PRBS ERROR COUNTER (16-BIT)

This counter contains the 16-bit PRBS bit error event. The MSB is stored in register 0xn90Dh and the LSB is stored in register 0xn90Eh.

11.11 TRANSMIT SLIP COUNTER (8-BIT)

A slip event is defined as a replication or deletion of a T1/E1 frame by the transmit slip buffer. The contents of this register are stored in 0xn90Fh.

11.12 EXCESSIVE ZERO VIOLATION COUNTER (16-BIT)

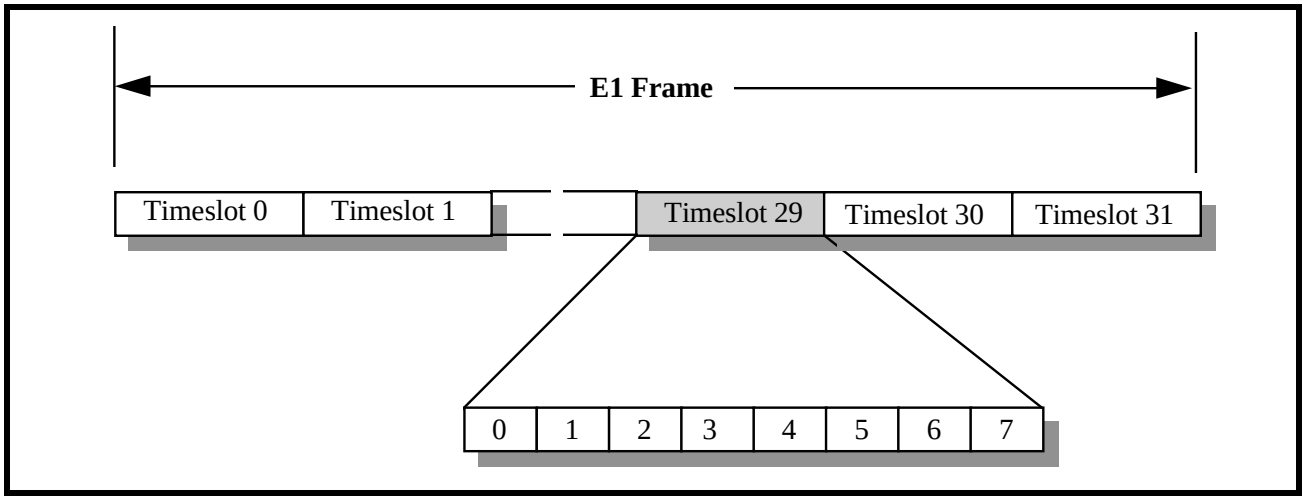
This register contains the accumulation of the events in which excessive zeros have occured. This is defined as more than 3-bit for HDB3, more than 7-bits for B8ZS, and more than 15-bits for AMI. The MSB is stored in register 0xn910h and the LSB is stored in register 0xn911h.

12.0 APPENDIX A: DS-1/E1 FRAMING FORMATS

12.1 THE E1 FRAMING STRUCTURE

A single E1 frame consists of 256 bits which is created 8000 times a second; thereby yielding a bit-rate of 2.048Mbps. The 256 bits within each E1 frame is grouped into 32 octets or timeslots. These timeslots are numbered from 0 to 31. Figure 128 presents a diagram of a single E1 frame.

FIGURE 128. SINGLE E1 FRAME DIAGRAM



A single E1 frame consists of 32 timeslots. However, not all of these timeslots are available to transmit voice or user data. For instance, timeslot 0 is always reserved for system use and timeslot 16 is sometimes used (reserved) by the system. Hence, within each E1 frame, either 30 or 31 of the 32 timeslots are available for transporting user or voice data.

TIMESLOT 0

In general, there are two types of E1 frames.

- FAS (Frame Alignment Signaling) frames
- non-FAS frames

In any E1 data stream, the E1 frame type alternates between the FAS and non-FAS frames.

The timeslot 0 octet within the FAS E1 frame contains a framing alignment pattern and therefore supports framing. The timeslot 0 octet within the non-FAS E1 frame contains bits that support signaling or data link message transmission.

TIMESLOT 0 OCTETS WITHIN FAS FRAMES

The bit-format of a timeslot 0 octet within a FAS frame is presented in Table 184.

TABLE 184: BIT FORMAT OF TIMESLOT 0 OCTET WITHIN A FAS E1 FRAME

BIT	0	1	2	3	4	5	6	7
Value	SI	0	0	1	1	0	1	1
Function	International Bit	Frame Alignment Signaling (FAS) Pattern						
DESCRIPTION-OPERATION	In practice, the Si bit within the FAS E1 Frame carries the results of a CRC-4 calculation, which is discussed in greater detail in Section 12.2.1.	The fixed framing pattern (e.g., 0, 0, 1, 1, 0, 1, 1) is used by the Receive E1 Framer at the Remote terminal for frame synchronization/alignment purposes.						

The table above indicates that the FAS frame timeslot 0 octet consists of a single International Bit within bit-field 0, Si, followed by a fixed 7-bit pattern within bit-fields 1 through 7.

BIT 0—SI (INTERNATIONAL BIT)

The Si bit within the FAS E1 Frame typically carries the results of a CRC-4 calculation, which is discussed in greater detail in Section 12.2.1. The fixed framing pattern (e.g., 0, 0, 1, 1, 0, 1, 1) will be used by the Receive E1 Framer at the Remote terminal for frame synchronization/alignment purposes. Section 7.0 discusses how the Receive E1 Framer uses these bits.

Timeslot 0 octets within non-FAS frames

The bit-format of a timeslot 0 octet within a non-FAS frame is presented in Table 185.

TABLE 185: BIT FORMAT OF TIMESLOT 0 OCTET WITHIN A NON-FAS E1 FRAME

BIT	7	6	5	4	3	2	1	0
Value	Sa8	Sa7	Sa6	Sa5	Sa4	A	1	Si
Function6	National bits					Yellow Alarm	Fixed Value	International Bit
Description-Operation	**National Bits** These bit-fields can be used to carry data link information from the Local transmitting terminal to the Remote receiving terminal. Since the National bits only exist in the non-FAS frames, they offer a maximum signaling data link bandwidth of 20kbps.					**FAS Frame Yellow Alarm Bit** This bit-field is used to transmit a Yellow alarm to the Remote Terminal. This bit-field is set to "0" during normal conditions, and is set to "1" whenever the Receive E1 Framer detects an LOS (Loss of Signal) or LOF (Loss of Framing) condition in the incoming E1 frame data.	**Fixed at "1"** Bit-field "1" contains a fixed value "1". This bit-field will be used for FAS framing synchronization/alignment purposes by the Remote Receive E1 Framer.	**International Bit** The Si bit within the non-FAS E1 Frame typically carries a specific value that will be used by the Receive E1 Framer for CRC Multi-frame alignment purposes.

The table above indicates the non-FAS frame timeslot 0 octet consists of a single international bit, Si, within bit-field 0.

BIT 0—SI (INTERNATIONAL BIT)

The Si bit, within the non-FAS E1 Frame carries a specific value that will be used by the Receive E1 Framer, for CRC Multi-frame alignment purposes. Section 7 discusses the exact role of the Si bit-field within the non-FAS frames.

BIT 1—FIXED AT "1"

Bit-field "1" contains a fixed value "1". This bit-field will be used for FAS framing synchronization/alignment purposes by the Remote Receive E1 Framer. Section _ discusses how the Receive E1 Framer uses this bit-field.

BIT 2—A (FAS FRAME YELLOW ALARM BIT)

This bit-field is used to transmit a Yellow alarm to the Remote Terminal. This bit-field is set to "0" during normal conditions, and is set to "1" whenever the Receive E1 Framer detects an LOS (Loss of Signal) or LOF (Loss of Framing) condition in the incoming E1 frame data.

BIT 3 THROUGH 7—SA4–SA8 (NATIONAL BITS)

These bit-fields can be used to carry data link information from the Local transmitting terminal to the Remote receiving terminal. Since the National bits only exist in the non-FAS frames, they offer a maximum signaling data link bandwidth of 20kbps.

12.2 THE E1 MULTI-FRAME STRUCTURE

The 86L34 Octal Framer supports two kinds of E1 Multi-frame structures:

- CRC Multi-frame
- CAS Multi-frame

12.2.1 The CRC Multi-frame Structure

A CRC Multi-frame consists of 16 consecutive E1 frames, with the first of these frames being a FAS frame. From a Frame Alignment point of view, the timeslot 0 octets of each of these E1 frames within the Multi-frame are the most important 16 octets. Table 186 presents the bit-format for all timeslot 0 octets within a 16 frame CRC Multi-frame.

TABLE 186: BIT FORMAT OF ALL TIMESLOT 0 OCTETS WITHIN A CRC MULTI-FRAME

SMF	FRAME NUMBER	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1	0	C1	0	0	1	1	0	1	1
	1	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	2	C2	0	0	1	1	0	1	1
	3	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	4	C3	0	0	1	1	0	1	1
	5	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	6	C4	0	0	1	1	0	1	1
	7	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
2	8	C1	0	0	1	1	0	1	1
	9	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	10	C2	0	0	1	1	0	1	1
	11	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	12	C3	0	0	1	1	0	1	1
	13	E	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	14	C4	0	0	1	1	0	1	1
	15	E	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

Table 186 has the CRC Multi-frame divided into 2 sub Multi-Frames. Sub-Multi-Frame 1 is designated as SMF1 and Sub-Multi-Frame 2 is designated as SMF2.

SMF1 consists of E1 frames 0 through 7 consisting of 4 FAS frames and 4 non-FAS frames.

There are two interesting things to note in Table 186. First, all of the bit-field 0 positions within each of the FAS frames are designated as C1, C2, C3 and C4. These four bit-fields contain the CRC-4 values which has been computed over the previous SMF. Hence, while the Transmit E1 Framer is assembling a given SMF, it computes the CRC-4 value for that SMF and inserts these results into the C1 through C4 bit-fields within the very next SMF. These CRC-4 values ultimately are used by the Remote Receive E3 Framer for error-detection purposes.

NOTE: *This framing structure is referred to as a CRC Multi-Frame because it permits the remote receiving terminal to locate and verify the CRC-4 bit-fields.*

The second interesting thing to note regarding Table 186 is that the bit-field 0 positions within each of the non-FAS frames are of a fixed six (6) bit pattern: 0, 0, 1, 0, 1, 1; along with two bits, each designated at “E”. This six bit pattern is referred to as the CRC Multi-Frame alignment pattern. This six-bit pattern will ultimately be used by the Remote Receive E1 Framer for CRC Multi-Frame synchronization/alignment. Section 7.0 discusses how the Receive E1 Framer uses this 6-bit CRC Multi-frame alignment pattern for frame synchronization/alignment. The "E" bits are used to indicate that the Local Receive E1 framer has detected errored sub-Multi-Frames.

12.2.2 CAS Multi-Frames and Channel Associated Signaling

CAS Multi-Frames are only relevant if the user is using CAS or Channel Associated Signaling. If the user is implementing Common Channel Signaling then the CAS Multi-Frame is not available. The exact role of CAS Multi-Frames is discussed in some detail in Section 7.0, Channel Associated Signaling.

12.2.2.1 Channel Associated Signaling

If the user operates an E1 channel in Channel Associated Signaling (CAS) mode, then the timeslot 16 octets within each E1 frame will be reserved for signaling. Such signaling would convey information such as On-

Hook, Off-Hook conditions, call set-up, control, etc. In CAS, this type of signaling data that is associated with a particular voice channel will be carried within timeslot 16 of a particular E1 frame within a CAS Multi-Frame.

The CAS is carried in a Multi-Frame structure which consists of 16 consecutive E1 frames. The framing/byte format of a CAS Multi-Frame is presented in Figure 129.

FIGURE 129. FRAME/BYTE FORMAT OF THE CAS MULTI-FRAME STRUCTURE

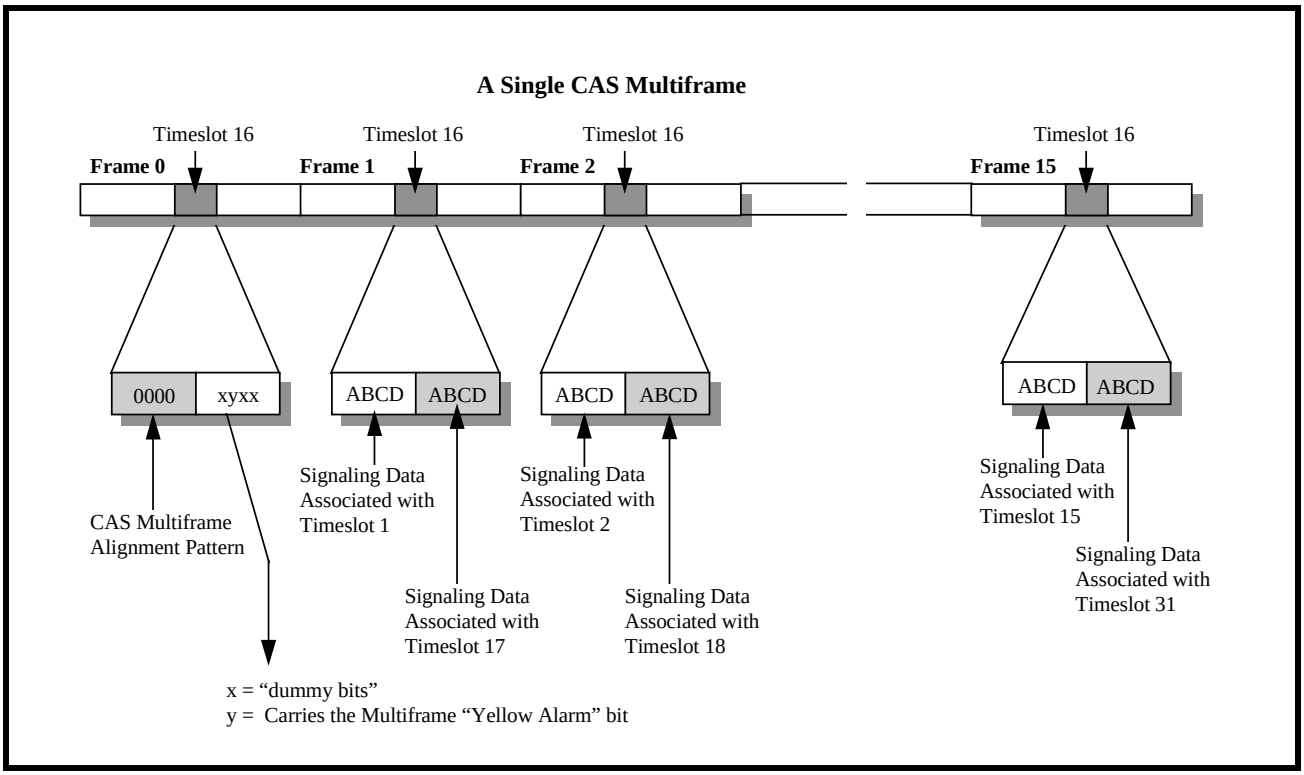


Figure 129 indicates that timeslot 16 within Frame 1 of the CAS Multi-Frame, contains 4 bits of signaling data for voice channel 1 and 4 bits of signaling data for voice channel 17. Likewise, timeslot 16 within Frame 2 contains 4 bits of signaling data for voice channel 2 and 4 bits of signaling data for voice channel 18; and so on. Timeslot 16 within frame 0 is a special octet that is used for two purposes.

1. To convey CAS Multi-Frame alignment information, and
2. To convey Multi-Frame alarm information to the Remote Terminal.

The bit-format of timeslot 16 within frame 0 of a CAS Multi-Frame is 0000 xyxx.

The upper nibble of this octet contains all zeros and is used to identify itself as the CAS Multi-Frame alignment signal. If CAS is used, then the user is advised to insure that none of the other timeslot 16 octets contain the value "0000". The lower nibble of this octet contains the expression "xyxx". In this case, the x-bits are the spare bits and should be set to "0" if not used. The y-bit is used to indicate a Multi-Frame alarm condition to the Remote terminal. During normal operation, this bit-field is cleared to "0". However, if the Local Receive E1 Framer detects a problem with the incoming Multi-Frames, then the Local Transmit E1 Framer will set this bit-field within the next outbound CAS Multi-Frame to "1".

NOTE: *The Local Transmit E1 Framer will continue to set the y-bit to "1" for the duration that the Local Receive E1 Framer detects this problem.*

12.2.2.2 Common Channel Signaling (CCS)

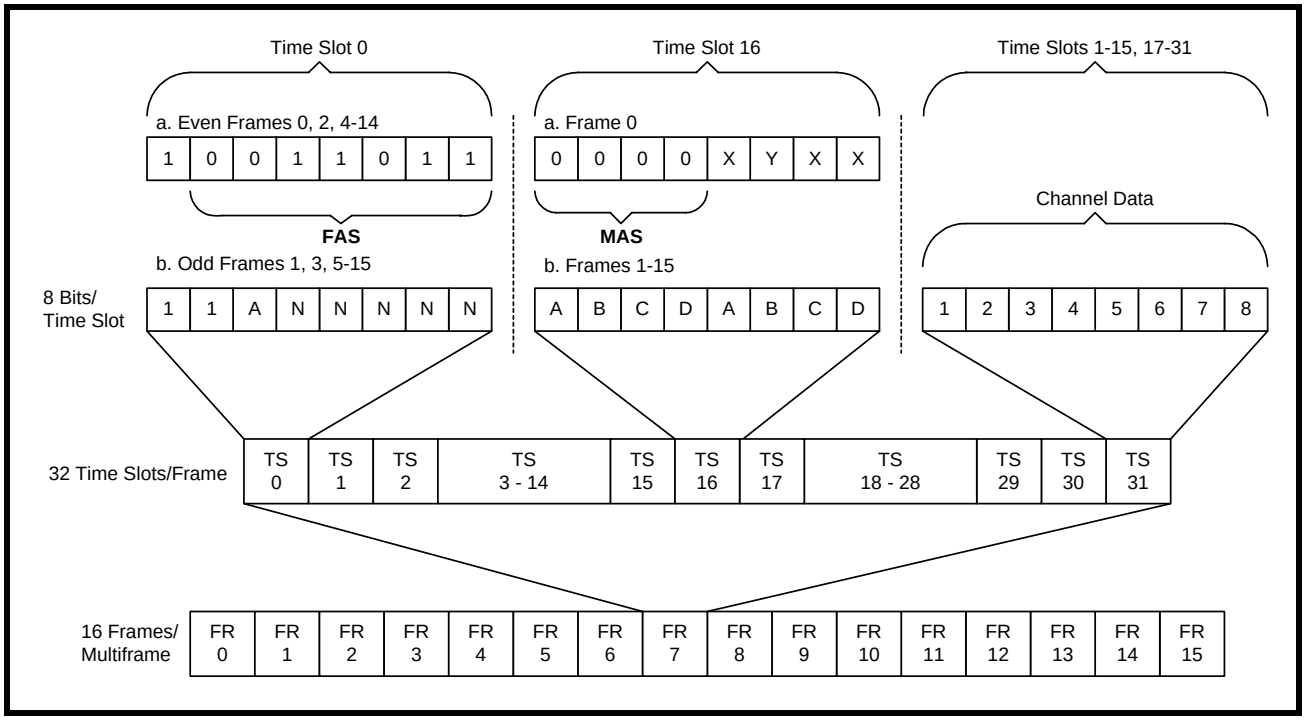
Common Channel Signaling is an alternative form of signaling from Channel Associated Signaling. In CCS, whatever signaling data which is transported via the outbound E1 data stream, carries information that applies

to all of the voice channels as a set (e.g., timeslots 1 through 15 and 17 through 31) in the E1 frame. There are numerous other variations of Common Channel Signaling that are available. Some of these are listed below.

- 31 Voice Channels with the common channel signaling being transported via the National Bits.
- 30 Voice Channels with the common channel signaling data being transported via the National Bits and CAS data being transported via timeslot 16.
- 30 Voice Channels with the Common Channel Signaling being processed via timeslot 16. (e.g., Primary Rate ISDN Signaling).

A more detailed discussion of these forms of Common Channel signaling are discussed in Section 11.0.

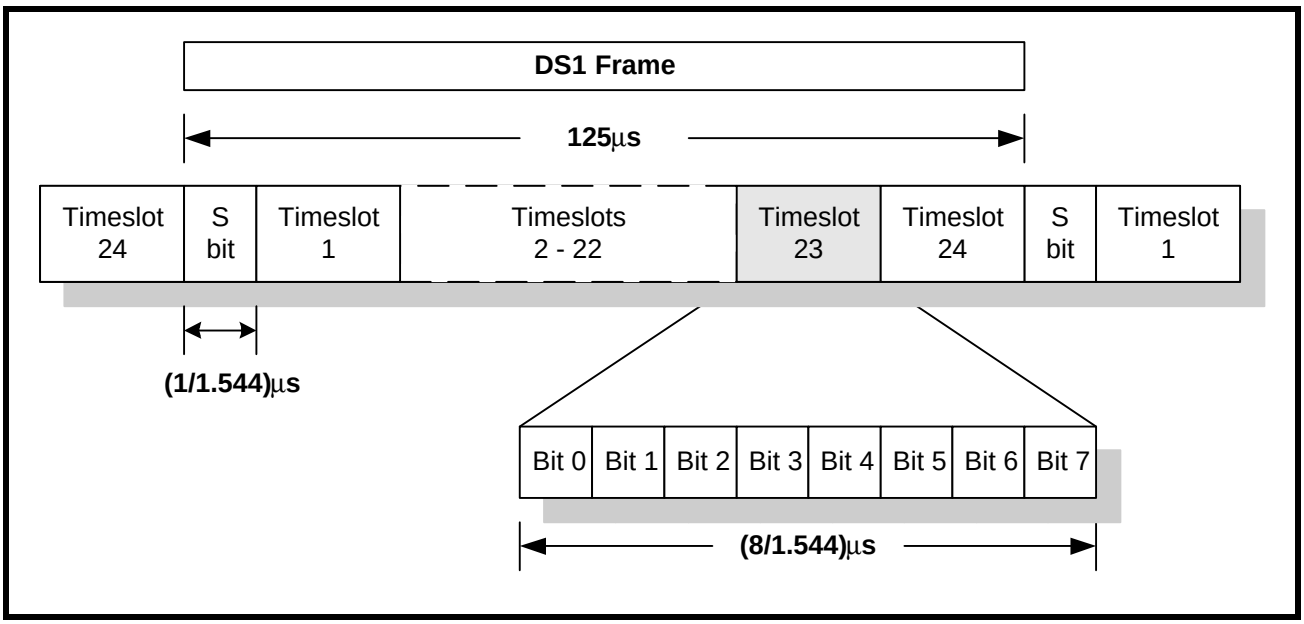
FIGURE 130. E1 FRAME FORMAT



12.3 THE DS1 FRAMING STRUCTURE

A single T1 frame is 193 bits long and is transmitted at a frame rate of 8000Hz. This results in an aggregate bit rate of 193 bits X 8000/sec = 1.544 Mbits/sec. Basic frames are divided into 24 timeslots numbered 1 thru 24 and a framing bit, see Figure 131. Each timeslot is 8 bits in length and is transmitted most significant bit first, numbered bit 0. This results in a single timeslot data rate of 8 bits x 8000/sec = 64 kbits/sec.

FIGURE 131. T1 FRAME FORMAT



12.4 T1 SUPER FRAME FORMAT (SF)

The Superframe Format (SF), is also referred to as the D4 format. The requirement for associated signaling in frames 6 and 12 dictates that the frames be distinguishable. This leads to a multiframe structure consisting of 12 frames per superframe (SF). See Figure 132 and Table 187.

The SF structure consists of a multiframe of 12 frames. Each frame has 24 timeslots, plus an F-bit and 8 bits per timeslot. A timeslot is equivalent to one voice circuit or one 64kb/s data circuit.

This structure of frames and multiframes is defined by the F-bit pattern. The F-bit is designated alternately as an Ft bit (terminal framing bit) or Fs bit (signalling framing bit). The Ft bit carries a pattern of alternating zeros and ones (101010) in odd frames that defines the boundaries so that one timeslot may be distinguished from another. The Fs bit carries a pattern of (001110) in even frames and defines the multiframe boundaries so that one frame may be distinguished from another.

FIGURE 132. T1 SUPERFRAME PCM FORMAT

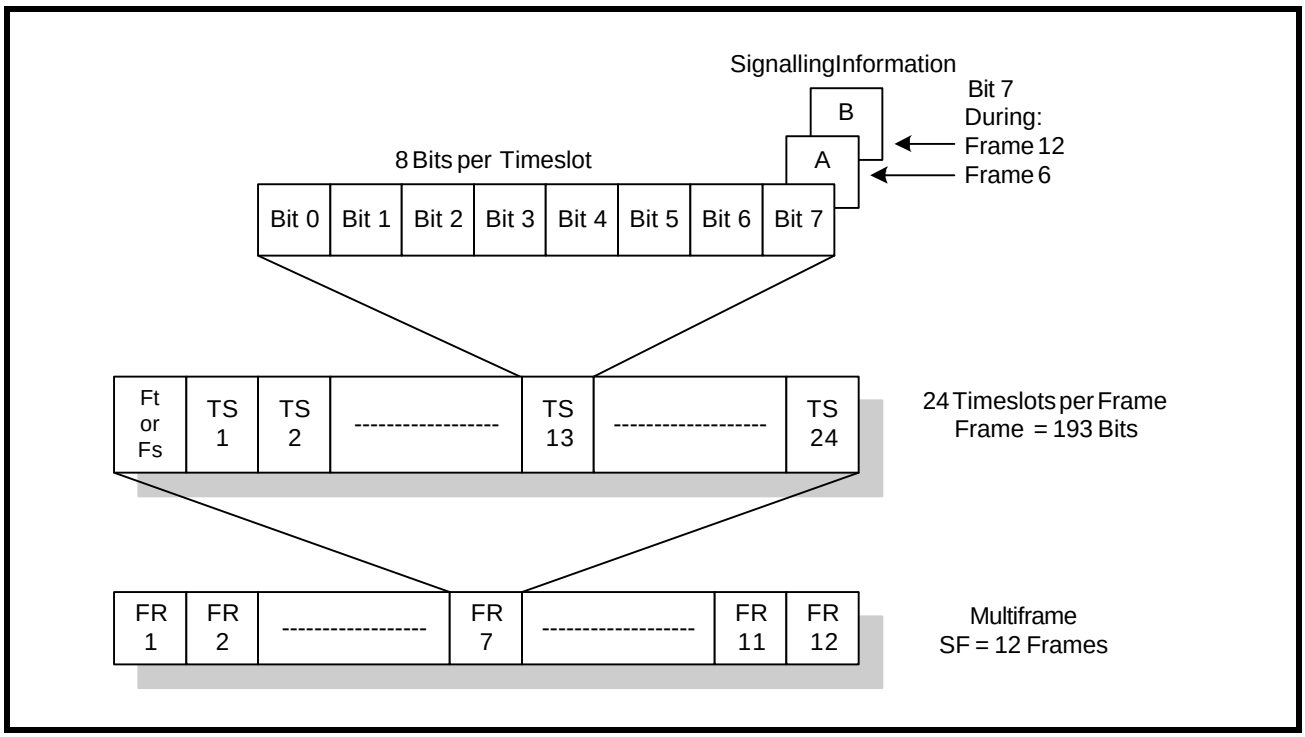


TABLE 187: SUPERFRAME FORMAT

FRAME	BIT	F-BITS		BIT USE IN EACH TIMESLOT		SIGNALLING CHANNEL
		TERMINAL FRAMING FT	TERMINAL FRAMING FS	TRAFFIC	SIG	
1	0	1	----	1-8	----	----
2	193	----	0	1-8	----	----
3	386	0	----	1-8	----	----
4	579	----	0	1-8	----	----
5	772	1	----	1-8	----	----
6	965	----	1	1-7	8	A
7	1158	0	----	1-8	----	----
8	1351	----	1	1-8	----	----
9	1544	1	----	1-8	----	----
10	1737	----	1	1-8	----	----
11	1930	0	----	1-8	----	----
12	2123	----	0	1-7	8	B

12.5 T1 EXTENDED SUPERFRAME FORMAT (ESF)

In Extended Superframe Format (ESF), as shown in Figure 133 and Table 188, the multiframe structure is extended to 24 frames. The timeslot structure is identical to D4 (SF) format. Robbed-bit signaling is accommodated in frame 6 (A-bit), frame 12 (B-bit), frame 18 (C-bit) and frame 24 (D-bit).

The F-bit pattern of ESF contains three functions:

1. Framing Pattern Sequence (FPS), which defines the frame and multiframe boundaries.
2. Facility Data Link (FDL), which allows data such as error-performance to be passed within the T1 link.
3. Cyclic Redundancy Check (CRC), which allows error performance to be monitored and enhances the reliability of the receiver's framing algorithm.

FIGURE 133. T1 EXTENDED SUPERFRAME FORMAT

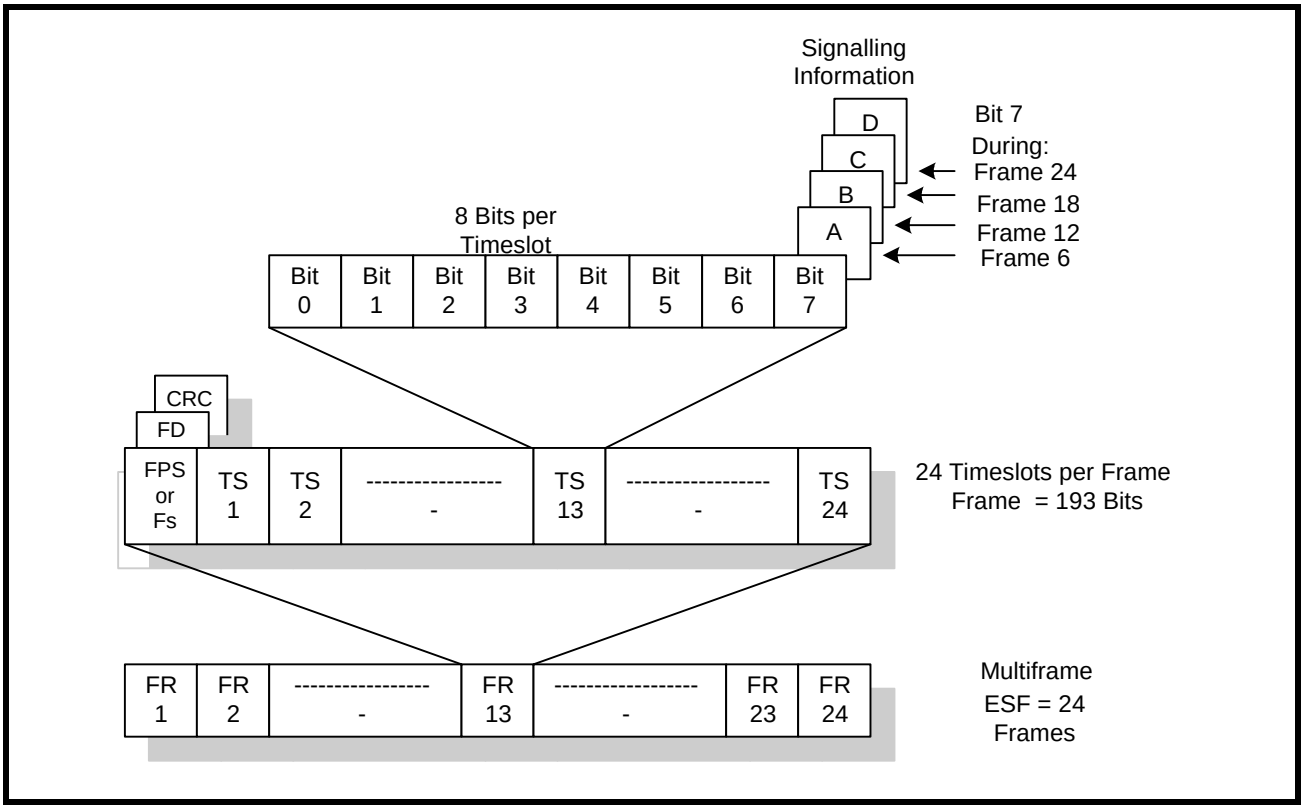


TABLE 188: EXTENDED SUPERFRAME FORMAT

FRAME	BIT	F-BITS			BIT USE IN EACH TIMESLOT		SIGNALLING CHANNEL		
		FPS	DL	CRC	TRAFFIC	SIG	16	4	2
1	0	----	m	----	1-8	----	----	----	----
2	193	----	----	C1	1-8	----	----	----	----
3	386	----	m	----	1-8	----	----	----	----
4	579	0	----	----	1-8	----	----	----	----
5	772	----	m	----	1-8	----	----	----	----
6	965	----	----	C2	1-7	8	A	A	A
7	1158	----	m	----	1-8	----	----	----	----
8	1351	0	----	----	1-8	----	----	----	----
9	1544	----	m	----	1-8	----	----	----	----
10	1737	----	----	C3	1-8	----	----	----	----
11	1930	----	m	----	1-8	----	----	----	----
12	2123	1	----	----	1-7	8	B	B	B
13	2316	----	m	----	1-8	----	----	----	----
14	2509	----	----	C4	1-8	----	----	----	----
15	2702	----	m	----	1-8	----	----	----	----
16	2895	0	----	----	1-8	----	----	----	----
17	3088	----	m	----	1-8	----	----	----	----
18	3281	----	----	C5	1-7	8	C	C	A
19	3474	----	m	----	1-8	----	----	----	----
20	3667	1	----	----	1-8	----	----	----	----
21	3860	----	m	----	1-8	----	----	----	----
22	4053	----	----	C6	1-8	----	----	----	----
23	4246	----	m	----	1-8	----	----	----	----
24	4439	1	----	----	1-7	8	D	B	A

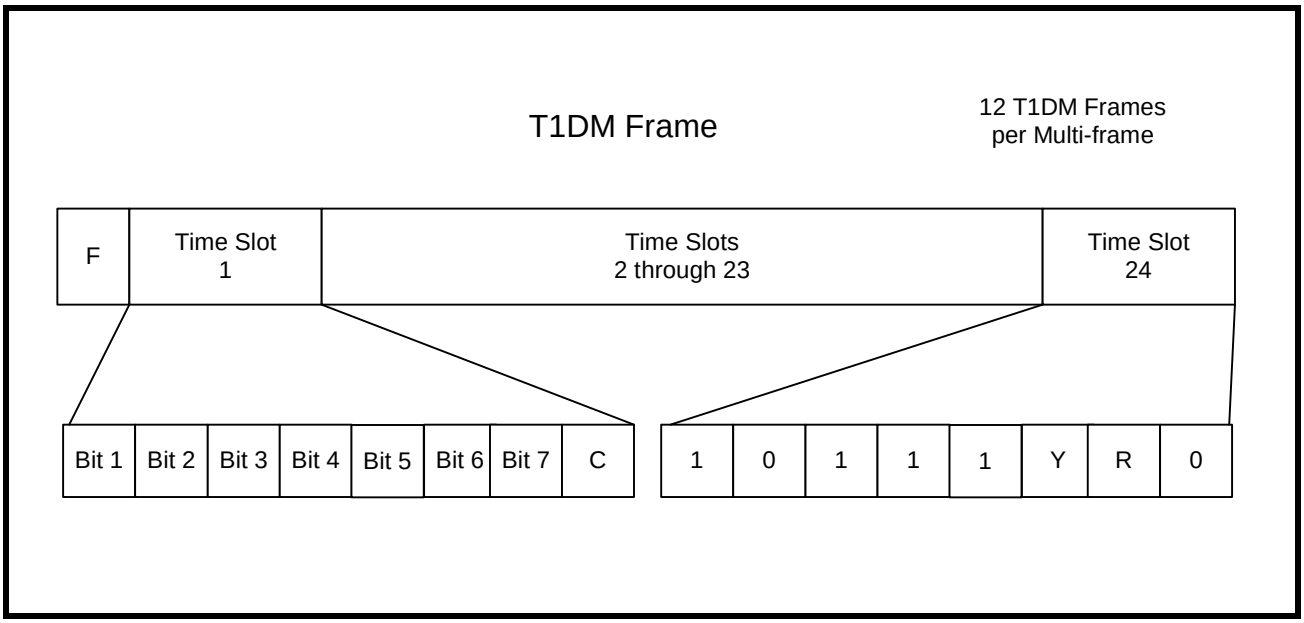
NOTES:

1. *FPS indicates the Framing Pattern Sequence (...001011...)*
2. *DL indicates the 4kb/s Data Link with message bits m.*
3. *CRC indicates the cyclic redundancy check with bits C1 to C6*
4. *Signaling options include 16 state, 4 state and 2 state.*

12.6 T1 DATA MULTIPLEXED FRAMING FORMAT (T1DM)

T1DM uses a similar framing structure as the SF (D4), such that the Fs and Ft bits on the individual frame boundaries remain the same. The differentiation between T1DM and SF is within the payload time slots. Time slot 24 cannot be used for data when configured for T1DM. Time slot 24 is dedicated for a special synchronization byte as shown in Figure 134. The Y-bit is to carry the status of the Yellow Alarm. The R-bit is dedicated for a remote signaling bit typically not used. However, the framer allows this bit to carry an HDLC message. Time slots 1 through 23 are used to carry the seven bit word from each of the 23 DS-0 signals.

FIGURE 134. T1DM FRAME FORMAT



12.7 SLC-96 FORMAT (SLC-96)

SLC framing mode allows synchronization to the SLC®96 data link pattern. This pattern described in Bellcore TR-TSY-000008, contains both signaling information and a framing pattern that overwrites the Fs bit of the SF framer pattern. See Table 189.

TABLE 189: SLC®96 FS BIT CONTENTS

FRAME #	FS BIT	FRAME #	FS BIT	FRAME #	FS BIT
2	0	26	C2	50	0
4	0	28	C3	52	M1
6	1	30	C4	54	M2
8	1	32	C5	56	M3
10	1	34	C6	58	A1
12	0	36	C7	60	A2
14	0	38	C8	62	S1
16	0	40	C9	64	S2
18	1	42	C10	66	S3
20	1	44	C11	68	S4
22	1	46	0	70	1
24	C1	48	1	72	0

NOTES:

1. *The SLC®96 frame format is similar to that of SF as shown in Table 187 with the exceptions shown in this table.*
2. *C1 to C11 are concentrator bit fields.*
3. *M1 to M3 are Maintenance bit fields.*
4. *A1 and A2 are alarm bit fields.*
5. *S1 to S4 are line switch bit fields.*
6. *The Fs bits in frames 46, 48 and 70 are spoiler bitswhich are used to protect against false mutiframing.*

ELECTRICAL CHARACTERISTICS (FRAMER BLOCK)

ABSOLUTE MAXIMUMS

Power Supply..... -0.5V to +3.465V		Power Dissipation TBGA Package..... TBD
Storage Temperature .....-65°C to 150°C		Input Logic Signal Voltage (Any Pin) .....-0.5V to + 5.5V
Operating Temperature Range.....-40°C to 85°C		ESD Protection (HBM).....>2000V
Supply Voltage ..... GND-0.5V to +VDD + 0.5V		Input Current (Any Pin) ..... ± 100mA

DC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{DD}	Power Supply Current		TBD		mA	All Channels on
I_{LL}	Data Bus Tri-State Bus Leakage Current	-10		+10	µA	
V_{IL}	Input Low voltage			0.8	V	
V_{IH}	Input High Voltage	2.0		VDD	V	
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = -1.6mA
V_{OH}	Output High Voltage	2.4		VDD	V	I_{OH} = 40µA
I_{OC}	Open Drain Output Leakage Current				µA	
I_{IH}	Input High Voltage Current	-10		10	µA	V_{IH} = VDD
I_{IL}	Input Low Voltage Current	-10		10	µA	V_{IL} = GND

ELECTRICAL CHARACTERISTICS

TABLE 190: XRT83L38 POWER CONSUMPTION

VDD=3.3V±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED									
MODE	SUPPLY VOLTAGE	IMPEDANCE	TERMINATION RESISTOR	TRANSFORMER RATIO		TYP.	MAX.	UNIT	TEST CONDITIONS
				RECEIVER	TRANSMITTER				
E1	3.3V	75Ω	Internal	1:1	1:2	TBD TBD		mW mW	50% “1’s” 100% “1’s”
E1	3.3V	120Ω	Internal	1:1	1:2	TBD TBD		mW mW	50% “1’s” 100% “1’s”
T1	3.3V	100Ω	Internal	1:1	1:2	TBD TBD		mW mW	50% “1’s” 100% “1’s”
---	3.3V	---	---	---	---	TBD		mW	All transmitters and receivers off

TABLE 191: E1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD=3.3V±5%, T_A= -40° TO 85°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Receiver loss of signal:					Cable attenuation @1024kHz
Number of consecutive zeros before RLOS is set		32			
Input signal level at RLOS	15	20		dB	ITU-G.775, ETSI 300 233
RLOS De-asserted	12.5			% ones	
Receiver Sensitivity (Short Haul with cable loss)	11			dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application. With -18dB interference signal added.
Receiver Sensitivity (Long Haul with cable loss)	0		43	dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application. With -18dB interference signal added.
Input Impedance		13		kΩ	
Input Jitter Tolerance:					
1 Hz	37			UIpp	ITU G.823
10kHz-100kHz	0.2			UIpp	
Recovered Clock Jitter					
Transfer Corner Frequency	-	36		kHz	ITU G.736
Peaking Amplitude			-0.5	dB	
Jitter Attenuator Corner Frequency (-3dB curve) (JABW=0)	-	10	-	Hz	ITU G.736
(JABW=1)		1.5		Hz	
Return Loss:					
51kHz - 102kHz	14	-	-	dB	ITU-G.703
102kHz - 2048kHz	20			dB	
2048kHz - 3072kHz	16			dB	

TABLE 192: T1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD=3.3V±5%, T_A=-40° TO 85°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Receiver loss of signal:					
Number of consecutive zeros before RLOS is set	160	175	190		
Input signal level at RLOS	15	20	-	dB	Cable attenuation @772kHz
RLOS Clear	12.5	-	-	% ones	ITU-G.775, ETSI 300 233
Receiver Sensitivity (Short Haul with cable loss)	12	-		dB	With nominal pulse amplitude of 3.0V for 100Ω termination
Receiver Sensitivity (Long Haul with cable loss)		-			With nominal pulse amplitude of 3.0V for 100Ω termination
Normal	0		36	dB	
Extended	0		45	dB	
Input Impedance		13	-	kΩ	
Jitter Tolerance:					
1Hz	138	-	-	UIpp	AT&T Pub 62411
10kHz - 100kHz	0.4	-	-		
Recovered Clock Jitter					
Transfer Corner Frequency	-	9.8	-	KHz	TR-TSY-000499
Peaking Amplitude	-		0.1	dB	
Jitter Attenuator Corner Frequency (-3dB curve)	-	6		-Hz	AT&T Pub 62411
Return Loss:					
51kHz - 102kHz	-	20	-	dB	
102kHz - 2048kHz	-	25	-	dB	
2048kHz - 3072kHz	-	25	-	dB	

TABLE 193: E1 TRANSMIT RETURN LOSS REQUIREMENT

FREQUENCY	RETURN LOSS	
	G.703/CH-PTT	ETS 300166
51-102kHz	8dB	6dB
102-2048kHz	14dB	8dB
2048-3072kHz	10dB	8dB

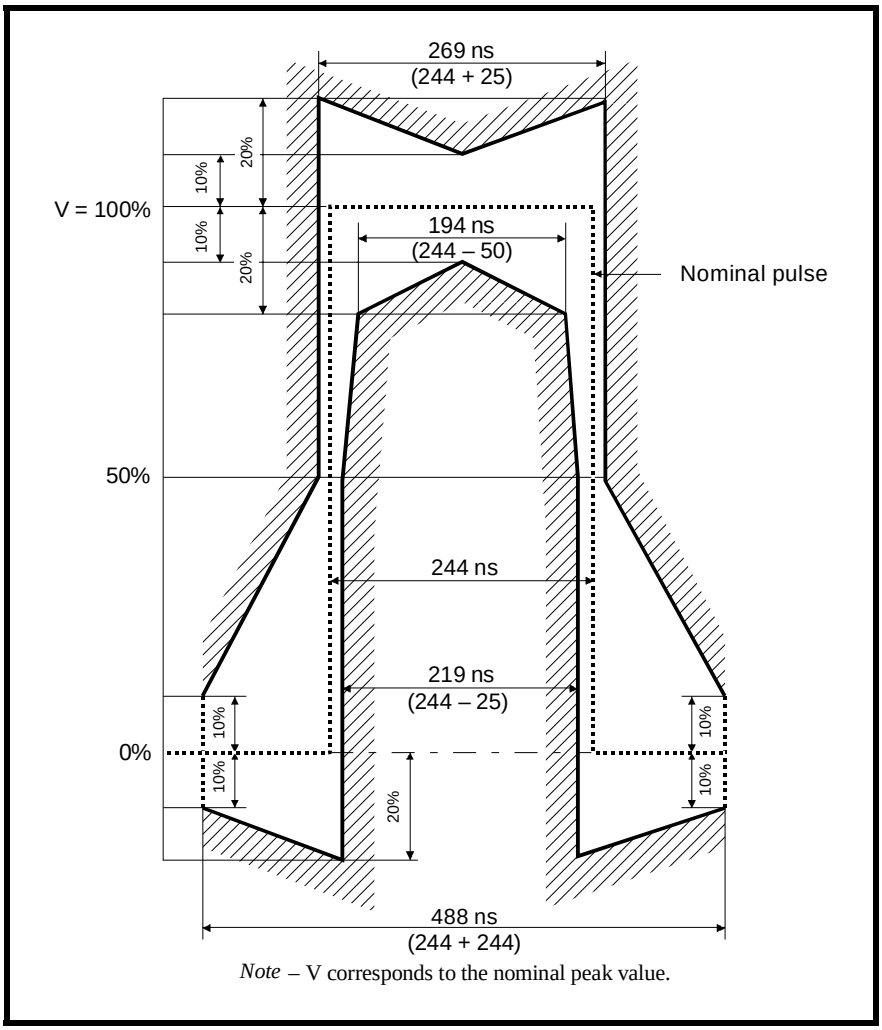
TABLE 194: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD=3.3V±5%, T_A=-40° TO 85°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
AMI Output Pulse Amplitude:					Transformer with 1:2 ratio and 9.1Ω resistor in series with each end of primary.
75Ω Application	2.13	2.37	2.60	V	
120Ω Application	2.70	3.00	3.30	V	
Output Pulse Width	224	244	264	ns	
Output Pulse Width Ratio	0.95	-	1.05	-	ITU-G.703
Output Pulse Amplitude Ratio	0.95	-	1.05	-	ITU-G.703
Jitter Added by the Transmitter Output	-	0.025	0.05	UIpp	Broad Band with jitter free TCLK applied to the input.
Output Return Loss:					
51kHz -102kHz	8	-	-	dB	ETSI 300 166, CHPTT
102kHz-2048kHz	14	-	-	dB	
2048kHz-3072kHz	10	-	-	dB	

TABLE 195: T1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD=3.3V±5%, T_A=-40° TO 85°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
AMI Output Pulse Amplitude:	2.4	3.0	3.60	V	Use transformer with 1:2.45 ratio and measured at DSX-1
Output Pulse Width	338	350	362	ns	ANSI T1.102
Output Pulse Width Imbalance	-	-	20	-	ANSI T1.102
Output Pulse Amplitude Imbalance	-	-	±200	mV	ANSI T1.102
Jitter Added by the Transmitter Output	-	0.025	0.05	UIpp	Broad Band with jitter free TCLK applied to the input.
Output Return Loss:					
51kHz -102kHz	-	15	-	dB	
102kHz-2048kHz	-	15	-	dB	
2048kHz-3072kHz	-	15	-	dB	

FIGURE 135. ITU G.703 PULSE TEMPLATE



Note – V corresponds to the nominal peak value.

TABLE 196: TRANSMIT PULSE MASK SPECIFICATION

Test Load Impedance	75Ω Resistive (Coax)	120Ω Resistive (twisted Pair)
Nominal Peak Voltage of a Mark	2.37V	3.0V
Peak voltage of a Space (no Mark)	0 ± 0.237V	0 ± 0.3V
Nominal Pulse width	244ns	244ns
Ratio of Positive and Negative Pulses Imbalance	0.95 to 1.05	0.95 to 1.05

FIGURE 136. DSX-1 PULSE TEMPLATE (NORMALIZED AMPLITUDE)

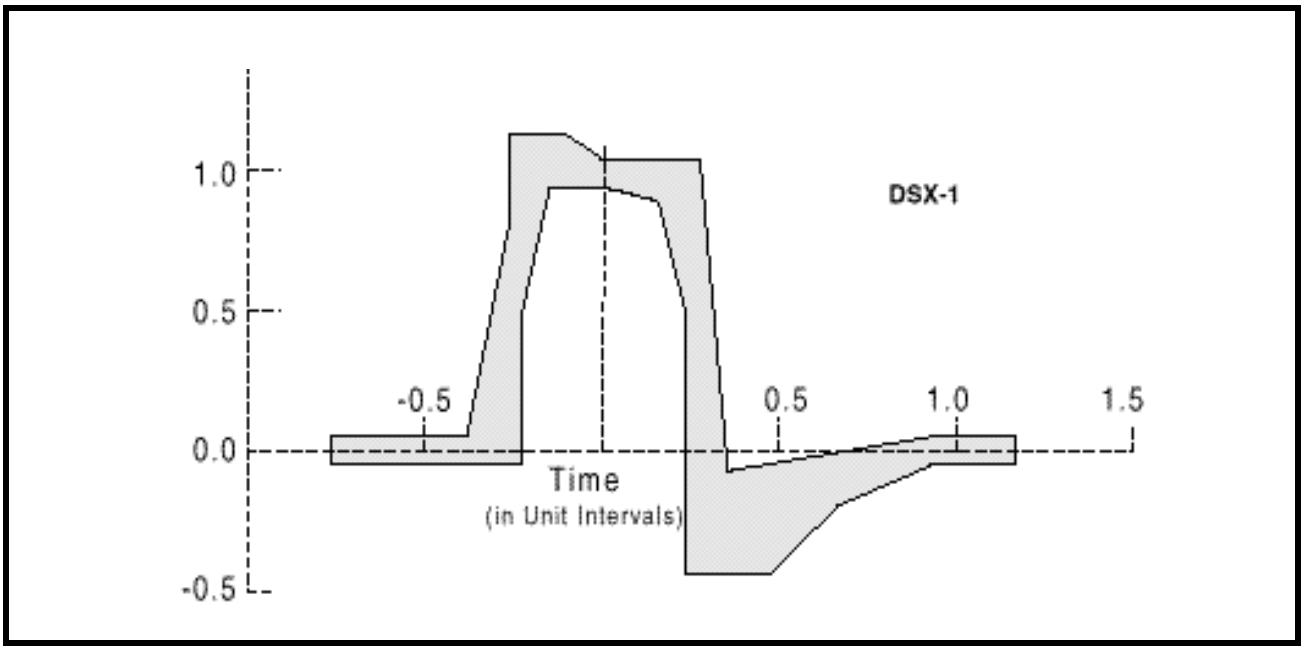


TABLE 197: DSX1 INTERFACE ISOLATED PULSE MASK AND CORNER POINTS

MINIMUM CURVE		MAXIMUM CURVE	
TIME (UI)	NORMALIZED AMPLITUDE	TIME (UI)	NORMALIZED AMPLITUDE
-0.77	-.05V	-0.77	.05V
-0.23	-.05V	-0.39	.05V
-0.23	0.5V	-0.27	.8V
-0.15	0.95V	-0.27	1.15V
0.0	0.95V	-0.12	1.15V
0.15	0.9V	0.0	1.05V
0.23	0.5V	0.27	1.05V
0.23	-0.45V	0.35	-0.07V
0.46	-0.45V	0.93	0.05V
0.66	-0.2V	1.16	0.05V
0.93	-0.05V		
1.16	-0.05V		

TABLE 198: AC ELECTRICAL CHARACTERISTICS

VDD=3.3V±5%, TA=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
E1 MCLK Clock Frequency		-	2.048		MHz
T1 MCLK Clock Frequency		-	1.544		MHz
MCLK Clock Duty Cycle		40	-	60	%
MCLK Clock Tolerance		-	±50	-	ppm

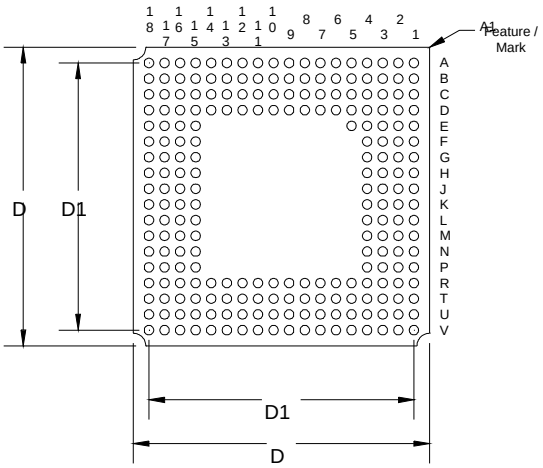
ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86L34IB	225 LEAD TBGA	-40^{0}C to +85^{0}C

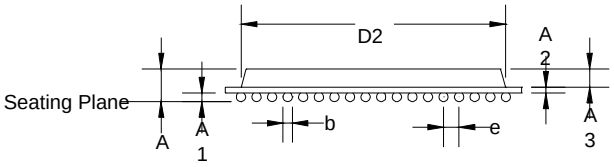
PACKAGE DIMENSIONS

225 Ball Plastic Ball Grid Array (19.0 mm x 19.0 mm, 1.0mm pitch PBGA)

Rev. 1.00



(A1 corner feature is mfger option)



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.049	0.096	1.24	2.45
A1	0.016	0.024	0.40	0.60
A2	0.013	0.024	0.32	0.60
A3	0.020	0.048	0.52	1.22
D	0.740	0.756	18.80	19.20
D1	0.669 BSC		17.00 BSC	
D2	0.665	0.669	16.90	17.00
b	0.020	0.028	0.50	0.70
e	0.039 BSC		1.00 BSC	

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.0	07/07/03	First release of the 4-Channel Framer/LIU Preliminary Datasheet.
P1.0.1	07/15/03	Changed Address Registers (0xn024-0xn027) to (0xn124-0xn127) in the register descriptions.
P1.0.2	10/31/03	Re-arranged the datasheet and altered the Table of Contents. Added registers for additional HDLC controllers, SS7, Automatic Performance Report, Gapped Clock Interface, AIS-CI, and RAI-CI. Cleaned up diagrams.