VITELIC

V61C16 FAMILY
HIGH PERFORMANCE LOW POWER
2K x 8 BIT
CMOS STATIC RAM

Features

- High Speed
  - Maximum access time of 45/55/70 ns
  - Equal access and cycle times
- Low Power
  - 200 mW typical operating
  - 0.5 µW typical standby
  - 0.1 µW typical data retention
- Battery backup
  - 2 volt data retention (L version)
- Six transistor CMOS memory cell
- CMOS process virtually eliminates alpha particle induced soft errors without die coating
- Fully static operation
  - No clock or refresh required
- Pin Compatible with standard 16K static RAMS and EPROMS in 300 and 600 mil DIP
- TTL compatible

Description

The V61C16 is a high speed, low power, 2048-word by 8-bit CMOS static RAM fabricated using high-performance CMOS process technology. This high reliability process, coupled with innovative circuit design techniques, yields access times of 45 ns maximum.

When the chip select is high, the device assumes a standby mode in which the device power dissipation is reduced to 0.5 µW (typically). The low power version has a data retention mode that guarantees that data will remain valid at a minimum power supply voltage of 2.0 volts.

Using CMOS technology, supply voltages from 2.0 to 5.5 volts have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the V61C16 family.

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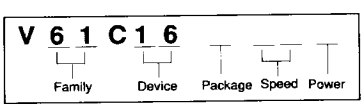
Package	Std.	Skinny	Pin Count
Plastic DIP	P	S	24
SOIC (Mini Flat Pack)	F		24

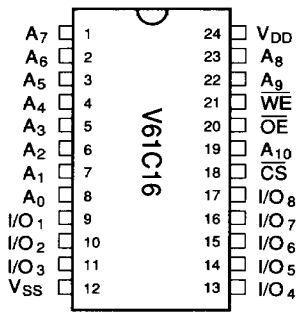


Device Usage Chart

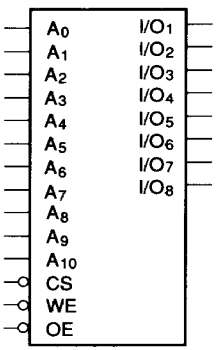
Operating Temperature Range	Package Outline			Access Time (ns)			Power		Temperature Mark
	P	S	F	45	55	70	Low	Std.	
0°C –70°C	•	•	•	•	•	•	•	•	Blank

V61C16 Rev. 01 6/90

24 Pin DIP/SOIC PIN CONFIGURATION
Top View



Logic Symbol



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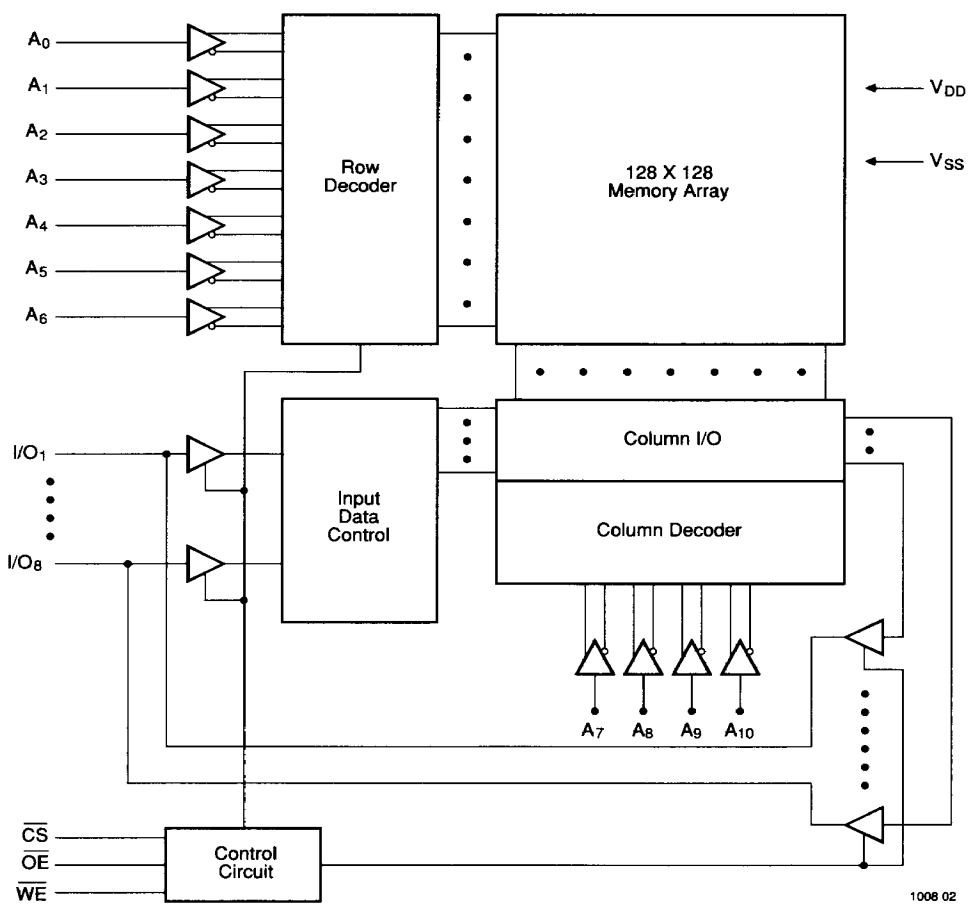
Functional Block Diagram



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Absolute Maximum Ratings[1]

Symbol	Parameter	Rating	Unit
V_{TERM}	Voltage on any Pin with Respect to V_{SS}	-0.5* to +7.0	V
T_A	Operating Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	60	mA

* -3.5V for 20 ns pulse.

NOTE:
1. Operation at or above absolute maximum ratings may affect device reliability.

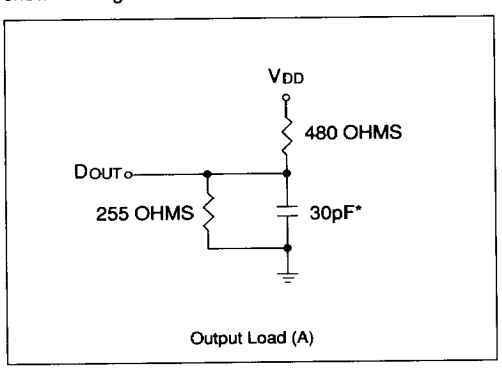
Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0.0	0.0	0.0	V
V_{IH}	Input High Voltage	2.2	3.5	V_{DD}	V
V_{IL}	Input Low Voltage	-0.5*	—	+0.8	V

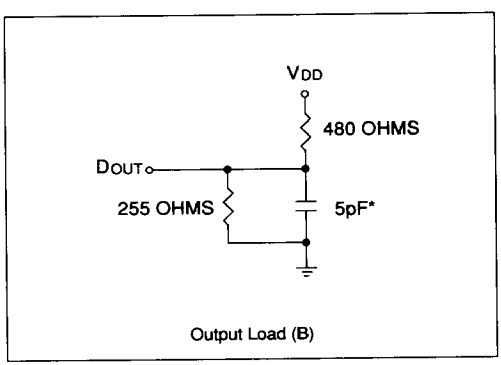
* -3.5V for 20 ns pulse.

AC Test Conditions

Signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.0 to 3.0V, output loading as shown in diagrams below.



Output Load (A)



Output Load (B)

* including scope and jig

Truth Table

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Read	L	H	H	High Z
Write	L	X	L	D_{IN}

Capacitance

T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

NOTE:
These parameters are sampled and not 100% tested.

Commercial Temperature Range
DC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Test Conditions	V61C16 Min.	V61C16 Typ.	V61C16 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = 5.5V, V_{IN} = V_{SS} to V_{DD}	—	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{DD}	—	—	2	µA
I_{DD}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0.0mA Duty Cycle = 100%	—	55	95	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ = V_{IH}	—	2	5	mA
I_{SB1}		$\overline{CS}$ ≥ V_{DD} - 0.2V, V_{IN} = 0.0 to V_{DD}	—	4	1000	µA
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4.0 mA	2.4	—	—	V

Low Power DC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Test Conditions	V61C16***L Min.	V61C16***L Typ.	V61C16***L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = 5.5V, V_{IN} = V_{SS} to V_{DD}	—	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{DD}	—	—	2	µA
I_{DD}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0.0mA Duty Cycle = 100%	—	55	80	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ = V_{IH}	—	2	5	mA
I_{SB1}		$\overline{CS}$ ≥ V_{DD} - 0.2V, V_{IN} = 0.0 to V_{DD}	—	0.1	20	µA
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4.0 mA	2.4	—	—	V

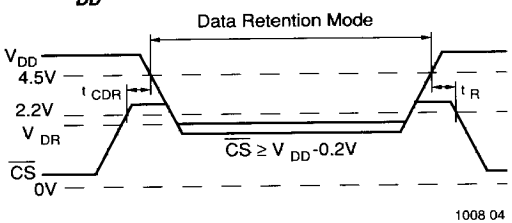
Low V_{DD} Data Retention Characteristics

For low power versions only, T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Parameter	Symbol	Limits Min.	Limits Typ.	Limits Max.	Unit	Test Conditions
Data retention supply voltage	V_{DDDR}	2.0	—	5.5	V	V_{IN} = 0.0 to V_{DD}, $\overline{CS}$ ≥ V_{DD} - 0.2V
Data retention supply current	I_{DDDR}	—	0.05	2.0	µA	V_{DD} = 3.0V, V_{IN} = 0.0 to V_{DD}, $\overline{CS}$ ≥ V_{DD} - 0.2V
Chip deselect to data retention time	t_{CDR}	0.0	—	—	ns	
Operation recovery time	t_R	t_{RC} (1)	—	—	ns	

NOTE:
1. t_{RC} = Read Cycle Time

Low V_{DD} Data Retention Waveform



AC Characteristics

At recommended operating conditions

Read Cycle

Symbol	Parameter	V61C16*45		V61C16*55		V61C16*70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	ns
t_{ACS}	Chip Select Access Time	—	45	—	55	—	70	ns
t_{CLZ}	Chip Selection to Output in Low Z	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	20	—	25	—	50	ns
t_{OLZ}	Output Enable to Output in Low Z	0	—	5	—	5	—	ns
t_{CHZ}	Chip Deselection to Output in High Z	0	20	0	25	0	35	ns
t_{OHZ}	Output Disable to Output in High Z	—	20	—	25	—	35	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns

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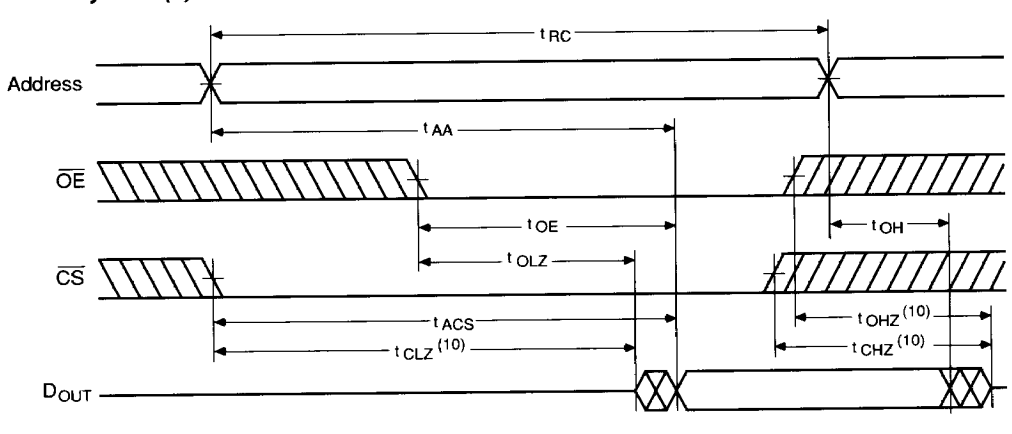
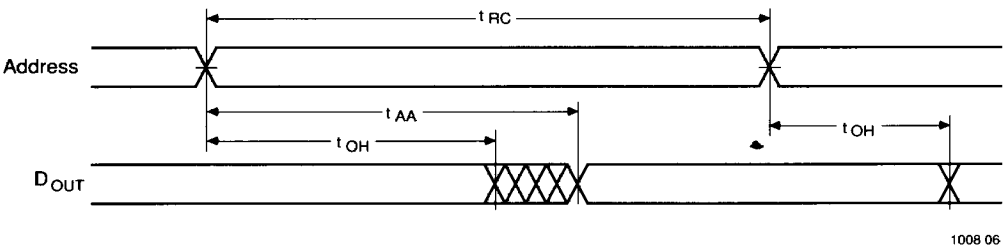
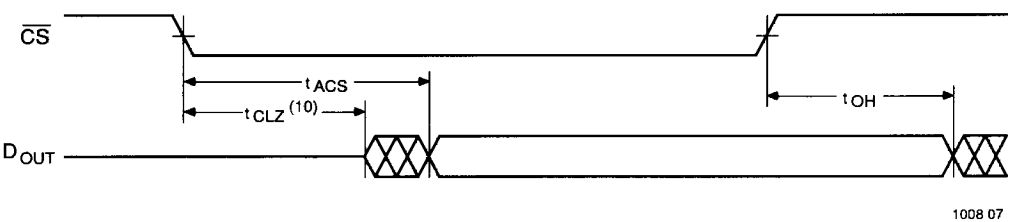
Read Cycle 1 (1)



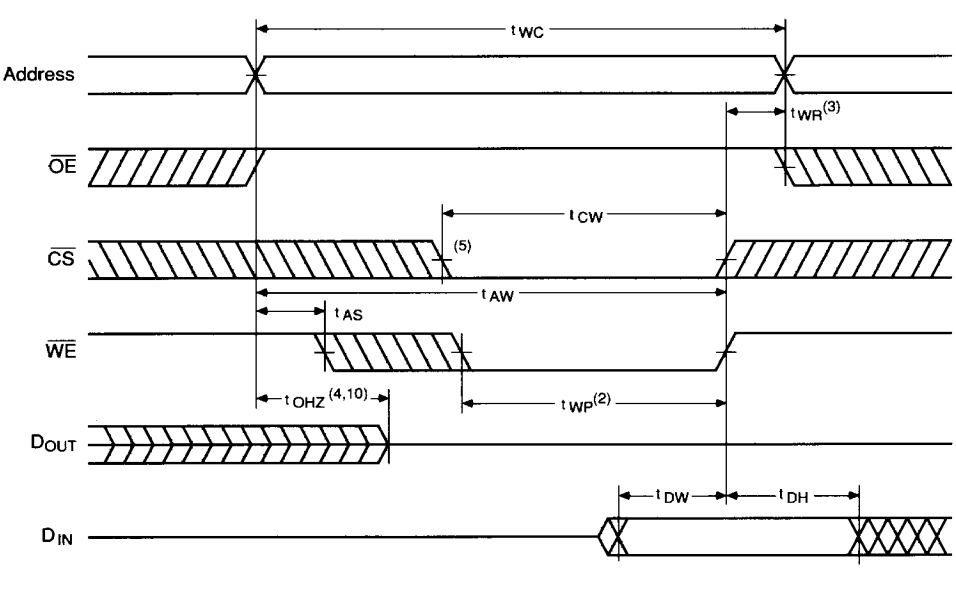
Read Cycle 2 (1, 6)



Read Cycle 3 (1, 6)



Write Cycle 1 (1)



AC Characteristics (1)

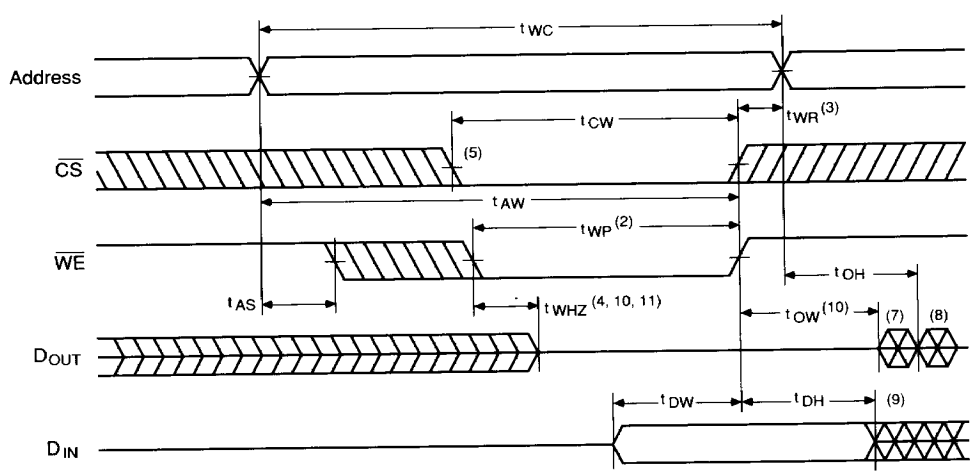
At recommended operating conditions unless otherwise noted.

Write Cycle

Symbol	Parameter	V61C16*45		V61C16*55		V61C16*70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t_{CW}	Chip Selection to End of Write	35	—	40	—	40	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	65	—	ns
t_{AS}	Address Setup Time	0	—	10	—	15	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	5	—	5	—	ns
t_{OHZ}	Output Disable to Output in High Z	—	20	—	25	—	35	ns
t_{WHZ}	Write to Output in High Z	0	20	0	25	0	40	ns
t_{DW}	Data to Write Time Overlap	25	—	30	—	30	—	ns
t_{DH}	Data Hold from Write Time	0	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	ns

NOTE:
1. Test conditions assume signal transition times if 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in Output Load (A).

Write Cycle 2 (1, 6)



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NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state and the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} \leq V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state and the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
11. t_{WHZ} is tested with C_L = 5 pF as in Output Load (B).