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RoHS

# QPI-9
QUIETPOWER®

# Hot-Swap SiP With V•I Chip EMI Filter

## Description

The QPI-9 includes the total hot-swap function along with an EMI filter for V•I Chip applications. The EMI filter is designed to attenuate the conducted common-mode (CM) and differential-mode (DM) noise generated by the higher switching frequencies of the V•I Chips. The QPI-9 is designed for use on a 24 Vdc bus. The in-rush current limit and circuit breaker are designed to deliver over 140 W of power with an input voltage of 24 V on the converter.

The QPI-9's internal fault timer allows it to operate safely in the event of a short across its output. The QPI-9 enters a retry mode where it will attempt to restart until the short condition is removed. The under and over voltage thresholds can be trimmed separately via the UVEN and OV inputs using external series resistors. The QPI-9 provides two Power Good signals, PWRGD1 referenced to the input ground and PWRGD2 to the output ground, which can be used to enable other circuits along with the V•I Chip converter.

## Features

- **>50 dB CM attenuation at 1 MHz**
- **>70 dB DM attenuation at 1 MHz**
- **40 Vdc (max input)**
- **100 Vdc surge 100 msec**
- **707 V hipot hold off to shield**
- **6 A breaker with delay plus 12 A limiter**
- **25 x 25 x 4.5 mm SiP (System in Package)**
- **Low profile LGA package**
- **-40° to +100°C PCB temperature (See Fig. 5)**
- **Hot-swap & filter combined saves PCB space**
- **Efficiency >98%**
- **Connects between OR'ing diodes & power conversion input hold-up capacitance**
- **Patents pending**

## Applications

- **Industrial and Military COTS**

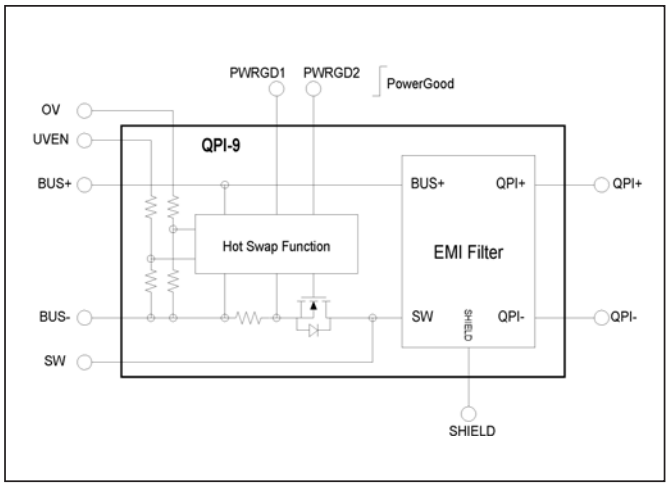



***Figure 1*** *– Block Diagram*

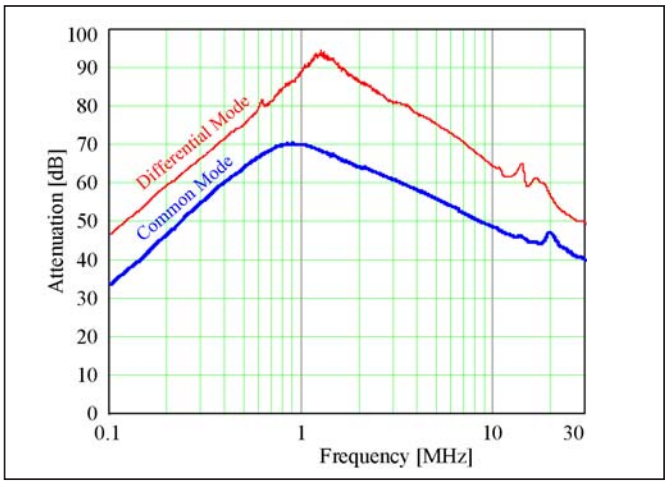



***Figure 2*** *– Typical Attenuation*

## Absolute Maximum Ratings – *Exceeding these parameters may result in permanent damage to the product.*

| Pins | Parameter | Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| BUS+, SW, PWRGD1, PWRGD2 to BUS- | Input voltage | Continuous | -0.5 | | 40 | Vdc |
| BUS+, SW, PWRGD1, PWRGD2 to BUS- | Input voltage | 100 mSec Transient | | | 100 | Vdc |
| BUS+/BUS- to shield | BUS Inputs to shield hipot | | | | +/-707 | Vdc |
| QPI+ to QPI- | Input to output current | Pulsed Limit @ 25°C | | 12 | | Adc |
| Package | Power Dissipation | VBUS = 24 V, 6 Adc, 25°C | | | 3.0 | W |
| Package | Operating Temperature | PCB to QPI Interface | -40 | | 100 | °C |
| Package | Thermal Resistance | Free Air | | | 50 | °C/W |
| Package | Junction Temperature | Tb = 100 °C Pd = 3 W @15 °C/W | | | 145 | °C |
| Package | Thermal Resistance | PCB Layout Dependent (1) | | | 15 | °C/W |
| Package | Storage Temperature | | -40 | | 125 | °C |
| Package | Re-flow Temperature | 20 s exposure @(2) | | | 212 | °C |
| All Pins | ESD | HBM | | | +/-2 | kV |

***Note 1:*** *Refer to Figure 15 and 16 for critical PCB layout guidelines to achieve this thermal resistance when reflowed onto the PCB.*
***Note 2:*** *RoHS compliant product maximum peak temperature is 245°C for 20 seconds.*

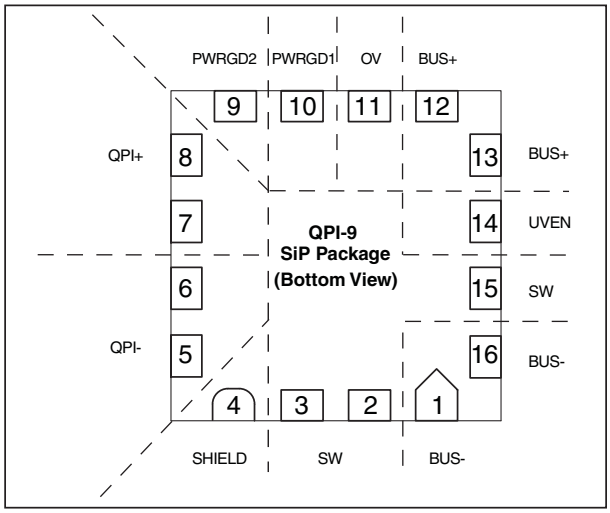
## Electrical Characteristics – *Parameter limits apply over the operating PCB temperature range unless otherwise noted*

| Symbol | Parameter | Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Vb+b- | BUS+ to BUS- input range | Measured at 5 A(3) | UV | | 38 | Vdc |
| V+oi | BUS+ to QPI+ voltage drop | Measured at 5 A(3) | | 110 | | mVdc |
| V-oi | BUS- to QPI- voltage drop | Measured at 5 A(3) | | -380 | | mVdc |
| CMIL | Common-mode insertion loss | VBUS = 48 V frequency =1 MHz | 50 | | | dB |
| DMIL | Differential-mode insertion loss | VBUS = 48 V frequency =1 MHz | 70 | | | dB |
| I BUS+ to BUS- | Input bias current at 80 V | Input current from BUS+ to BUS- | | 10 | | mA |
| IPG QPI+ to QPI- | Load current prior to PWRGD | Critical maximum DC load | | 25 | | mA |
| UV | Undervoltage threshold - rising | Controller disabled to enabled | | 18 | | V |
| UVHYS | Undervoltage hysteresis - falling | Controller enabled to disabled | | UV - 2 V | | V |
| OV | Overvoltage threshold - rising | Controller enabled to disabled | | 38 | | V |
| OVHYS | Overvoltage hysteresis - falling | Controller disabled to enabled | | OV - 2 V | | V |
| PWRGD1SAT | Power Good low voltage | IPWG = 1 mA, referenced to BUS- | 0.2 | | 0.6 | mV |
| PWRGD2SAT | Power Good low voltage | IPWG = 1 mA, referenced to QPI- | 0.2 | | 0.6 | mV |
| PWGLK | Power Good high leakage | VPWG = 40 V | | | 1 | µA |

***Note 3:*** *Refer to Figure 5 for current derating curve.*

## Pad Description

| Pin Number | Name | Description |
|---|---|---|
| **1, 16** | BUS- | Negative bus potential |
| **2, 3, 15** | SW | Negative rail controlled by hot insertion function. |
| **4** | SHIELD | Shield connects to the filter's shield pad and the chassis's common pin |
| **5, 6** | QPI- | Negative input to the converter |
| **7, 8** | QPI+ | Positive input to the converter |
| **10** | PWRGD1 | Open drain, referenced to BUS-, that asserts low when power is NOT good |
| **9** | PWRGD2 | Open drain, referenced to QPI-, that asserts low when power is NOT good |
| **12, 13** | BUS+ | Positive bus potential |
| **14** | UVEN | Highside of UV resistor divider |
| **11** | OV | Highside of OV resistor divider |



## Applications Information

The QPI-9 is an EMI filter especially designed for V•I Chip products, providing conducted common-mode and differential-mode attenuation from 150 kHz to 30 MHz. Designed for the industrial and military bus range, the QPI supports the filtering of system boards using VICOR's V•I Chip technology to the EN55022 class B limit.

The resulting plot in Figure 4 shows the QPI-9 is effective in reducing the V•I Chip total noise spectrum to well below the EN55022 Class B Quasi-peak detection limit.

The plot in Figure 4 was taken using the standard 50/50 µH LISN and measurement conditions, with the Peak detection mode of the spectrum analyzer, for a conducted EMI test. The results are compared to the CISPR22 EN55022 Class B Quasi-peak detection limit and show the total noise spectrum for V•I Chip combination using MP028F036M12AL & MV036F120M010 with QPI-9 connected, as shown in Figure 3.

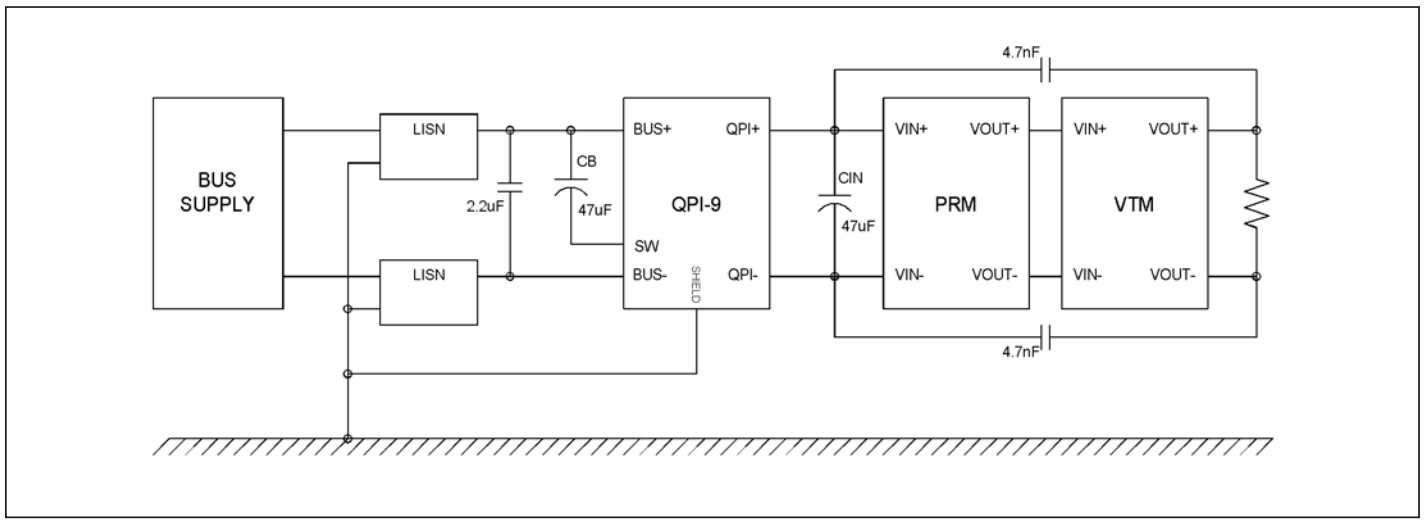



***Figure 3*** *– Standard LISN test setup, 100 W load.*

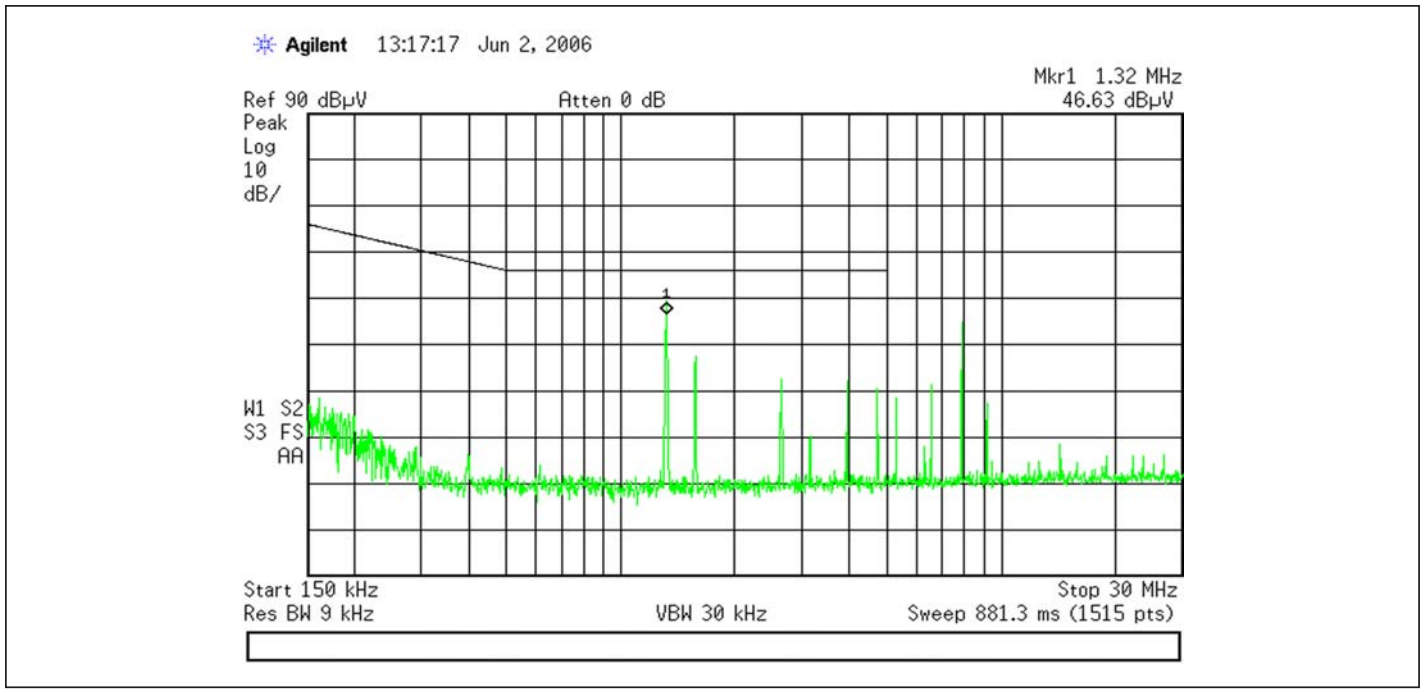



***Figure 4*** *– Conducted EMI profile of V•I Chip with QPI-9 with a 100 W load.*

## Applications Information – Hot-Swap

The QPI-9's high-temperature rating of 6 amps provides filtering for up to 144 W of power from a 24 V bus with a 70°C PCB temperature. The 1.0" x1.0" x 0.2" surface mount LGA package provides ease of manufacturing by eliminating thru-hole assembly. The current derating curve, shown in Figure 5, should be used when the PCB temperature that the QPI-9 is mounted to exceeds 70°C.

The hot-swap feature is created with an internal switch that controls the current path between BUS- and SW pins. The state of the switch can be on, off or in a current control mode depending on the state of the control function.

The QPI-9 has two signal pins that can be used to indicate the power-up status of the QPI-9. Both are active-low when power is not good. PWRGD1 is an open-drain that is referenced to the BUS- rail of the QPI-9. PWRGD2 is an open-drain that is referenced to the QPI- rail, allowing it to directly control the enable pin of the V•I Chip converter, without any kind of signal translation required. An example circuit of both options can be seen in Figures 9a and 9b.

The QPI-9 is designed to have an under-voltage range of 16 V to 18 V set point when the UVEN pin is tied directly to the BUS+ pin. The QPI-9 becomes enabled when the input voltage exceeds 18 V and continues to work down to 16 V before being disabled.

The QPI-9 over-voltage range is designed to be 36 V to 38 V when the OV pin is tied directly to the BUS+ pin. The QPI-9 remains functioning until the input voltage surpasses 38 V, where the QPI-9 will shutdown until the input voltage falls below 36 V.

External resistors can be added to trim the UV and OV trip points higher. The graph in Figure 6 shows the trimming effect for a range of external series resistors.

The equations in Figure 7 can be used to calculate the required series resistor for increasing the preprogrammed trip points.

Figure 8 shows a 5 ms, zero-volt BUS transient event with a 40 W load and 4700 µF of capacitance on the QPI-9's output. The external capacitor CE, shown in Figures 9a and 9b, will provide the required hold-up filtering during the transient event. This filtering will enable the Power-good state of the QPI-9 to remain unchanged during this transient, provided there is enough input energy to maintain the power converter's operation. Without this capacitor, the QPI-9 would detect an under-voltage fault and shut off its internal pass switch. The fault would also initiate a re-start of the hot-swap control and would require up to 45 ms to turn back on its internal switch.

***Note:*** *When using CE in this manner, RUVEN should be used*

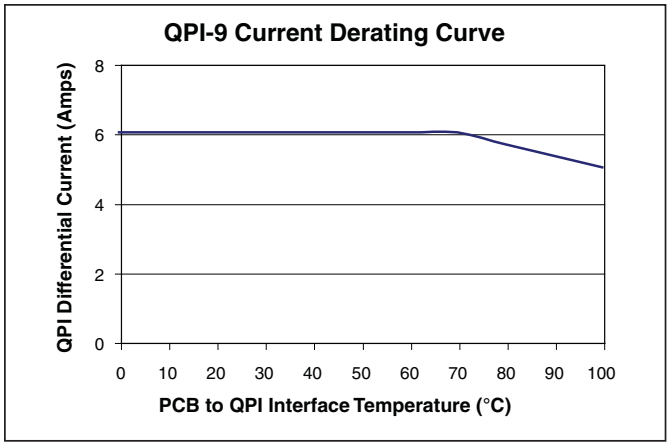



***Figure 5*** *– QPI-9 current derating curve over temperature.*

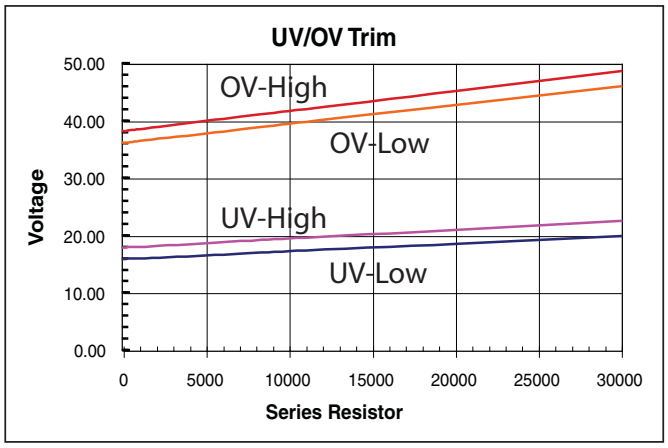



***Figure 6*** *– Trimming UV/OV with an external series resistor.*

$$UVEN_{LO} = \frac{2.5\ V(RUVEN + 118{,}700)}{18700}$$

$$UVEN_{HI} = 2.5\ V + (RUVEN + 100{,}000)(154\ \mu A)$$

$$OV_{LO} = 2.5\ V + (ROV + 102{,}000)(350\ \mu A)$$

$$OV_{HI} = \frac{2.5\ V(ROV + 109{,}150)}{7150}$$

***Figure 7*** *– UVEN and OV resistor equations.*

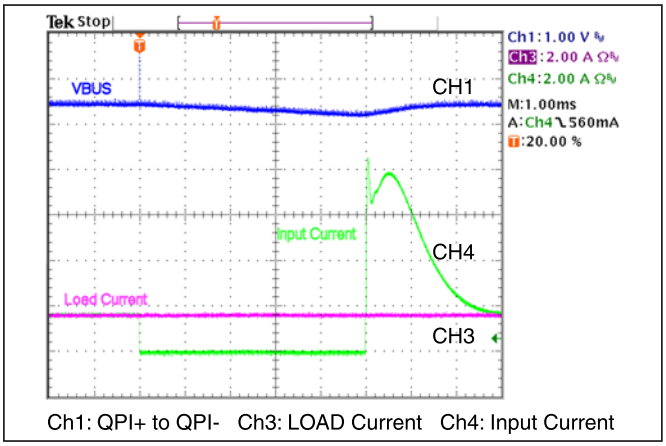



***Figure 8*** *– 5 ms Transient with 40 W Load.*

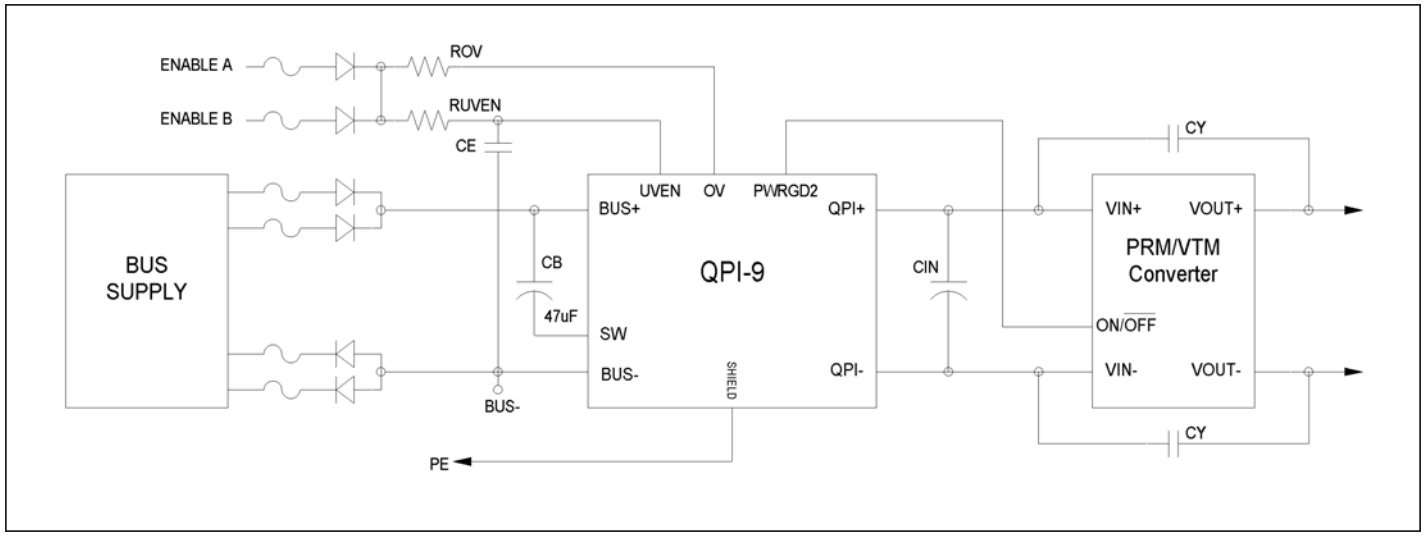



***Figure 9a*** *– Typical ATCA System with QPI-9 and High Enable Converter.*

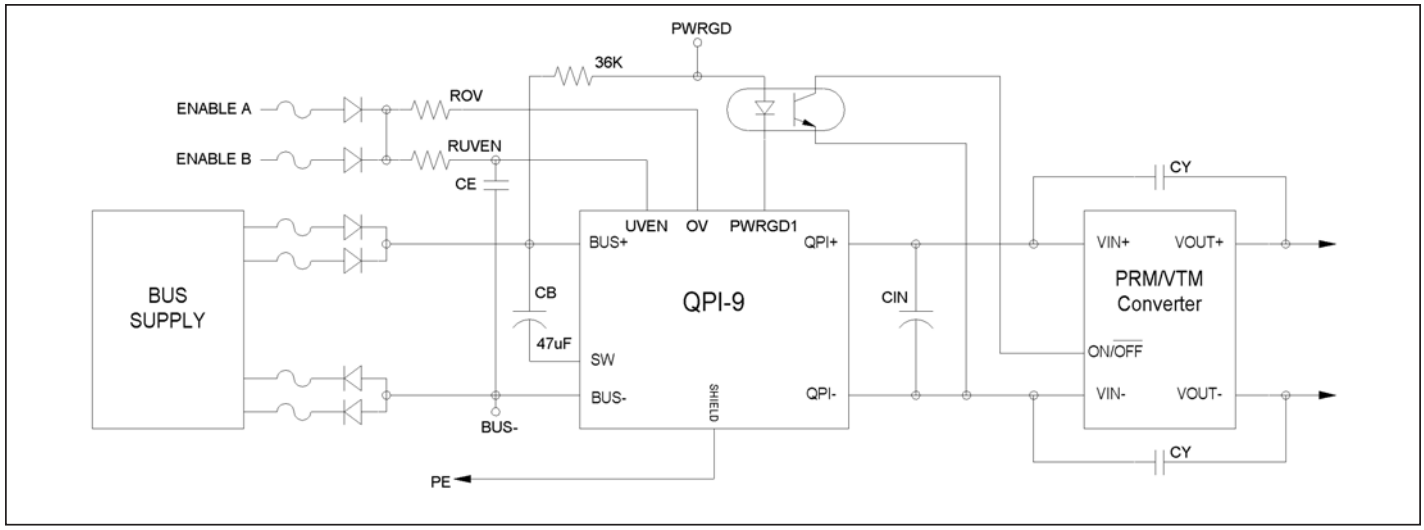



***Figure 9b*** *– Typical ATCA System with QPI-9 and High Enable Converter.*

## Start-up

The following oscilloscope pictures show the hot swap BUS- current, QPI- to Bus- voltage and PWRGD to BUS- output voltage of the QPI-9 during operation. Figures 10 and 11 are the QPI-9's in-rush characteristics under two load capacitance conditions. In Figure 10 a 470 µF capacitor required roughly 330 ms to completely charge from a 24 V bus voltage. The QPI-9 can drive large amounts of bulk capacitance to maintain converter operation during a 0V bus transient event, as shown in Figure 11 with a 4700 µF load capacitance. Under this condition the PWRGD takes about 2.9 seconds to go high after the UVEN input is pulled high upon the complete insertion of the board into the shelf. Figure 11's time-scale is too long to show the current pulses that charge the bulk capacitance.

After insertion, when the UVEN voltage exceeds 18 V the UV detection fault is cleared, the QPI-9 goes through a delay cycle (~45 ms) to allow for system stabilization and de-bounce. After this time, the QPI- to BUS- path is turned on and current is allowed to pass, monitored by the current sense function. Initially the current level exceeds the 6 A circuit breaker limit, the event timer starts and the power good state is not valid. The sense function and linear control loop will allow twice the circuit breaker current to pass. If the current does not drop below the circuit breaker level prior to reaching the timer limit, typically 800 µS, the QPI- to BUS- path will open. The effective duty cycle under the current limit condition is approximately 1%. Once the load capacitors are fully charged to the input bus potential, the load condition falls below 6 A and the PWRGD pin is asserted high, providing that the bus supply is still within the UV and OV range.

## Transient Protection and Recovery

Figures 12 and 13 show the QPI-9's ability to handle low resistance shorts (< 2) at the load terminals to emulate fast and slow blown fuse events. In Figure 12, the transient short is 2 seconds long and the QPI- to BUS- path is opened within 1 ms of this occurrence. Figure 13 demonstrates the QPI-9's performance with a short circuit on its output, where it remains in a low duty cycle mode until the short is removed, then restarts normally.

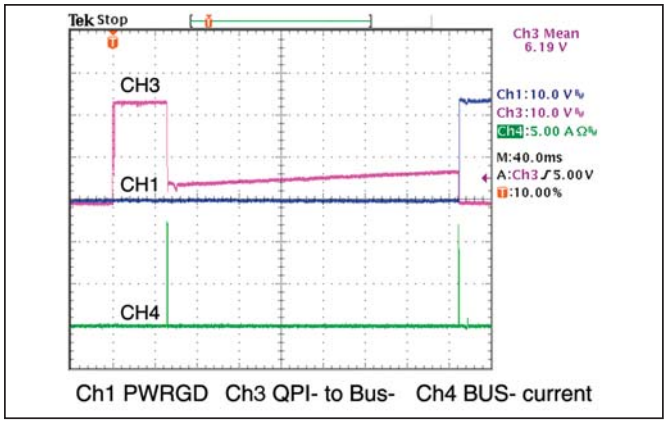



***Figure 10*** *– 470 µF capacitor @ 24 V.*

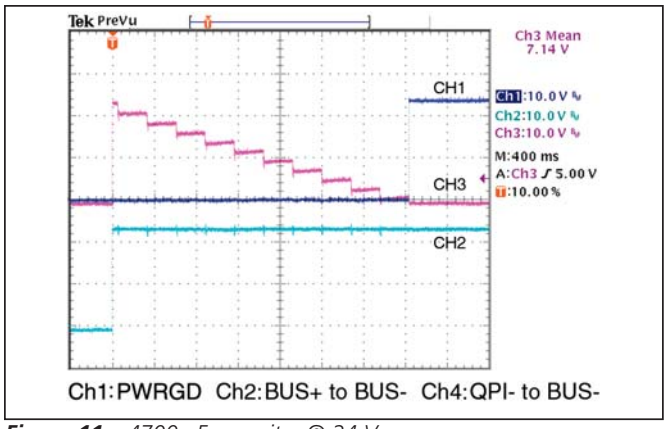



***Figure 11*** *– 4700 µF capacitor @ 24 V.*

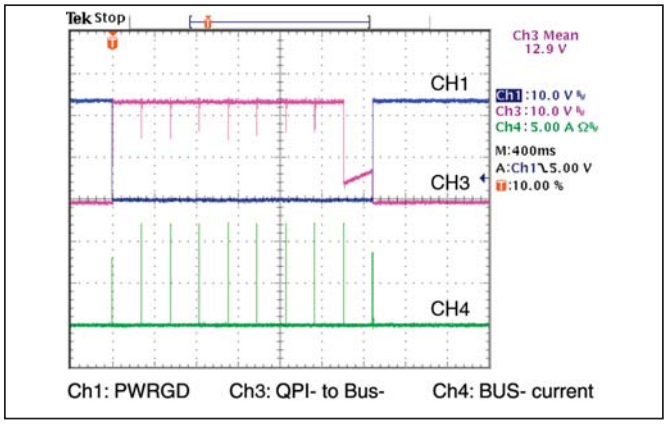



***Figure 12*** *– 2 seconds short-circuit.*

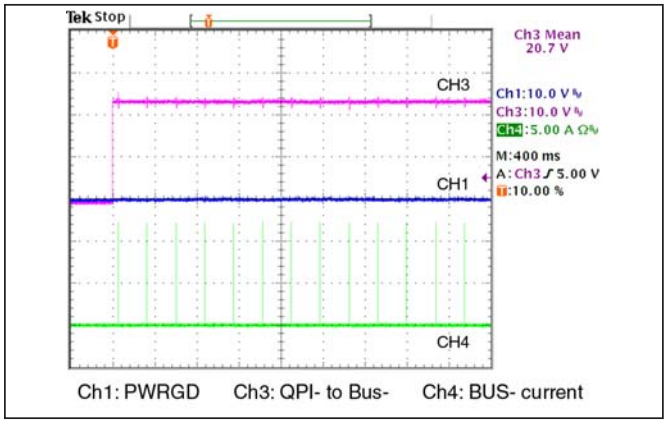



***Figure 13*** *– Start-up into short circuit.*

## Mechanical & Layout Information

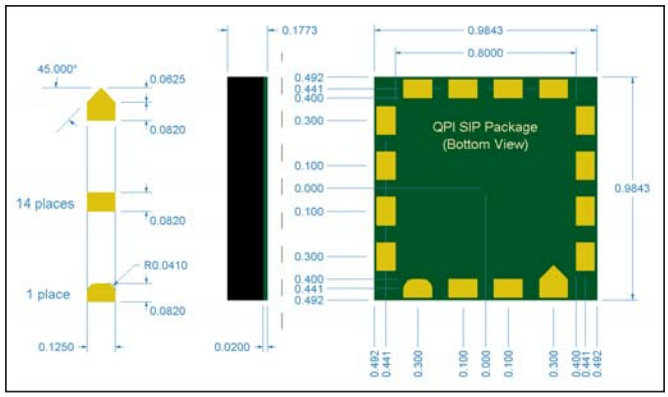



***Figure 14*** *– SiP package mechanicals; LGA pad, package height and pad location dimensions – inches.*

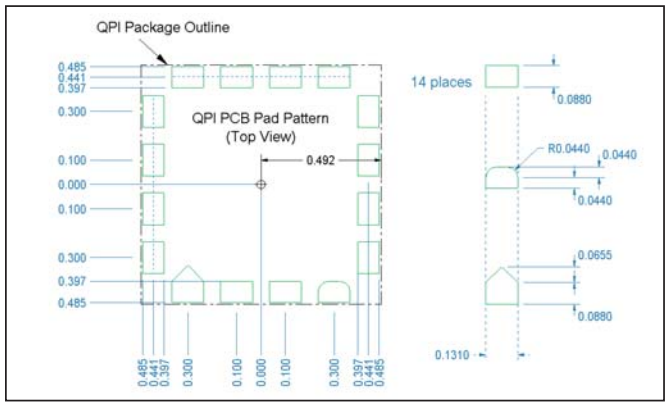



***Figure 16*** *– Recommended PCB receiving footprint.*

## Post Solder Cleaning

*Picor lidded QP SIPs are not hermetically sealed and must not be exposed to liquid, including but not limited to cleaning solvents, aqueous washing solutions or pressurized sprays.*

*When soldering, it is recommended that no-clean flux solder be used, as this will insure that potentially corrosive mobile ions will not remain on, around, or under the module following the soldering process.*

*For applications requiring water wash compatibility the "–01" open frame version should be used.*

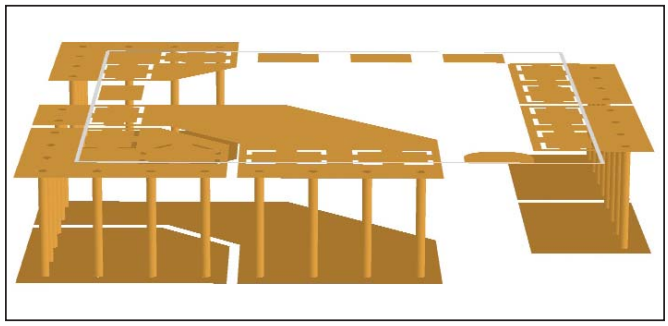


***Figure 17*** *– Recommended PCB layout on a 2 layer board*

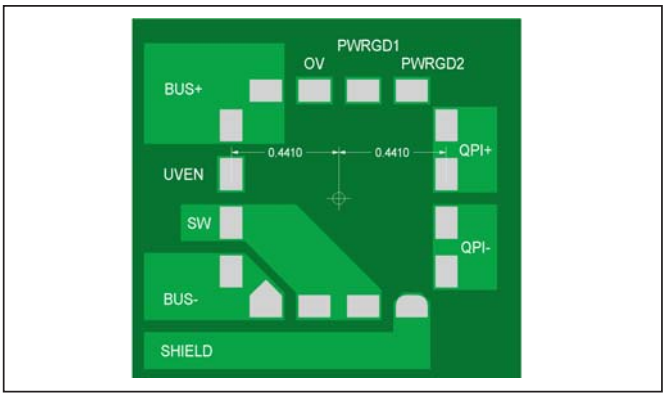



***Figure 15*** *– Recommended PCB Receiving Pattern.*

## QPI-9 PCB Layout Recommendations

The filtering performance of the QPI-9 and –10 is sensitive to capacitive coupling between its input and output pins. Parasitic plane capacitance must be kept below 1 pico-Farad between inputs and outputs using the layout shown above and the recommendations described below to achieve maximum conducted EMI performance.

To avoid capacitive coupling between input and output pins, there should not be any planes or large traces that run under both input and output pins, such as a ground plane or power plane. For example, if there are two signal planes or large traces where one trace runs under the input pins, and the other under the output pins, and both planes over-lap in another area, they will cause capacitive coupling between input and output pins. Also, planes that run under both input and outputs pins, but do not cross, can cause capacitive coupling if they are capacitively by-passed together.

Figure 17 shows the recommended pcb layout on a 2 layer board. Here, the top layer planes are duplicated on the bottom layer so that there can be no over-lapping of input and output planes. This method can be used for boards of greater layer count.

## Ordering Information

| Part Number | Description |
|---|---|
| QPI-9LZ | QPI-9 LGA Package, RoHS Compliant |
| QPI-9LZ-01 | QPI-9 LGA, RoHS Compliant<br>Open Frame Package |

**Vicor's comprehensive line of power solutions includes high-density AC-DC & DC-DC modules and accessory components, fully configurable AC-DC & DC-DC power supplies, and complete custom power systems.**



**Specifications are subject to change without notice.**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