Infrared Emitting Diode Chip, 950 nm, GaAs

FEATURES

- Package type: chip
- Package form: single chip
- Dimensions (L x W x H in mm): 0.37 x 0.37 x 0.265
- Peak wavelength: λ_p = 950 nm
- High reliability
- Low forward voltage
- Suitable for high pulse current operation
- Good spectral matching with Si photodetectors
- Compliant to RoHS directive 2002/95/EC and in accordance to WEEE 2002/96/EC

Pb-free

e4

RoHS COMPLIANT

APPLICATIONS

- Emitter in photo interrupters

DESCRIPTION

T163VU is an infrared, 950 nm emitting diode chip in GaAs technology. Anode is the bond pad on top.

GENERAL INFORMATION

The datasheet is based on Vishay optoelectronics sample testing under certain predetermined and assumed conditions, and is provided for illustration purpose only. Customers are encouraged to perform testing in actual proposed packaged and used conditions. Vishay optoelectronics die products are tested using Vishay optoelectronics based quality assurance procedures and are manufactured using Vishay optoelectronics established processes. Estimates such as those described and set forth in this datasheet for semiconductor die will vary depending on a number of packaging, handling, use, and other factors. Therefore sold die may not perform on an equivalent basis to standard package products.

PRODUCT SUMMARY				
COMPONENT	I_e (mW/sr)	φ (deg)	λ_P (nm)	t_r (ns)
T163VU	1.2	-	950	800

Note

Test conditions see table “Basic Characteristics”

ORDERING INFORMATION			
ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
T163VU-SF-F	Wafer sawn on foil without any frame	MOQ: 25 000 pcs	Chip

Note

MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Forward current		I_F	100	mA
Reverse voltage		V_R	5	V
Surge forward current	t_p = 100 µs	I_{FSM}	1.5	A
Junction temperature		T_j	125	°C
Operating temperature range		T_{amb}	- 40 to + 100	°C
Storage temperature range		T_{stg1}	- 40 to + 100	°C
Storage temperature range on foil		T_{stg2}	- 40 to + 50	°C

Note

T_{amb} = 25 °C, unless otherwise specified

BASIC CHARACTERISTICS						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Forward voltage	I_F = 100 mA, t_p = 20 ms	V_F		1.3		V
	I_F = 1 A, t_p = 100 µs	V_F		1.8		V
Temperature coefficient of V_F	I_F = 100 mA	TK_{VF}		- 1.3		mV/K
Junction capacitance	V_R = 0 V, f = 1 MHz, E = 0	C_j		30		pF
Radiant intensity	I_F = 100 mA, TO-18 gold header assembly	I_e		1.2		mW/sr
Radiant power (epoxy encapsulated)	I_F = 100 mA	ϕ_e		22		mW
Temperature coefficient of ϕ_e	I_F = 100 mA	$TK\phi_e$		- 0.8		%/K
Peak wavelength	I_F = 100 mA	λ_p		950		nm
Spectral bandwidth	I_F = 100 mA	$\lambda_{0.5}$		50		nm
Temperature coefficient of λ_p	I_F = 100 mA	$TK\lambda_p$		0.2		nm/K
Rise time, fall time	I_F = 20 mA	t_r, t_f		800		ns
	I_F = 1 A	t_r, t_f		400		ns

Note

T_{amb} = 25 °C, unless otherwise specified

BASIC CHARACTERISTICS

T_{amb} = 25 °C, unless otherwise specified

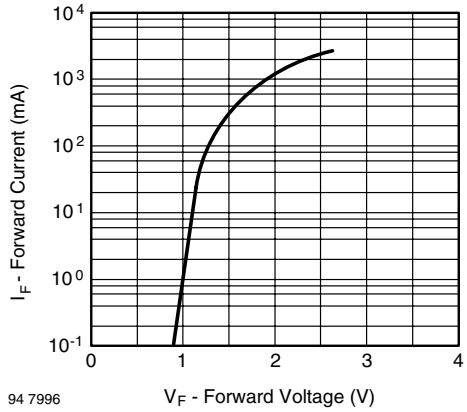

Fig. 1 - Forward Current vs. Forward Voltage

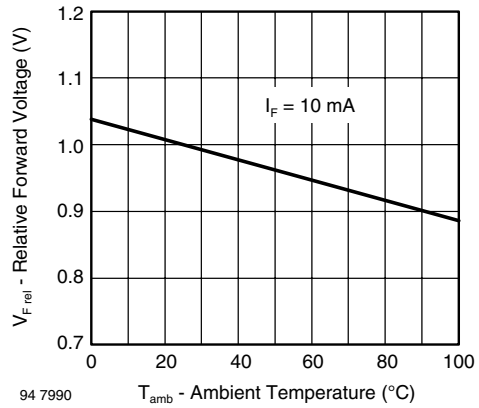

Fig. 2 - Relative Forward Voltage vs. Ambient Temperature

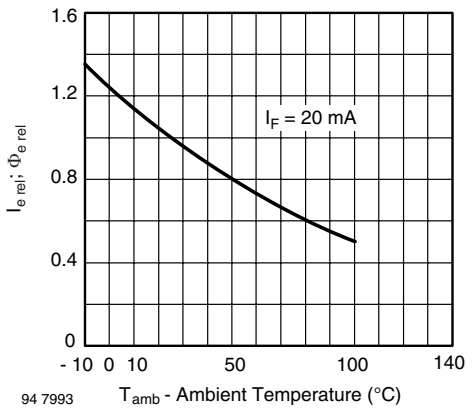

Fig. 3 - Relative Radiant Intensity/Power vs. Ambient Temperature

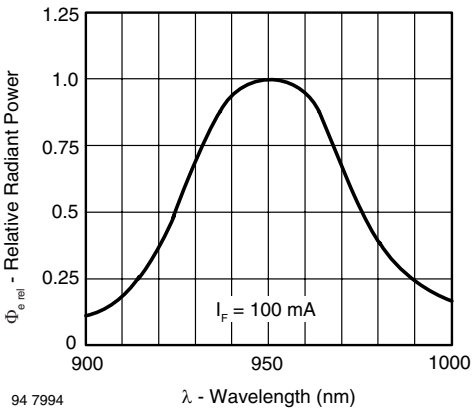

Fig. 4 - Relative Radiant Power vs. Wavelength

MECHANICAL DIMENSIONS					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Length of chip edge (x-direction)	L_x		0.37		mm
Length of chip edge (y-direction)	L_y		0.37		mm
Emission area	A_E		0.34 x 0.34		mm^2
Die height	H		0.265		mm
Diameter of bondpad	d		0.14		mm

ADDITIONAL INFORMATION (1)	
Frontside metallization, anode	Aluminum
Backside metallization, cathode	Gold alloy
Dicing	Sawing
Die bonding technology	Epoxy bonding

Note

(1) All chips are checked in accordance with the Vishay Semiconductor, specification of visual inspection FVOV6870.
The visual inspection shall be made in accordance with the “specification of visual inspection as referenced”. The visual inspection of chip backside is performed with stereo microscope with incident light and 40x to 80x magnification.
The quality inspection (final visual inspection) is performed by production. An additional visual inspection step as special release procedure by QM is not installed.

HANDLING AND STORAGE CONDITIONS

- The hermetically sealed shipment lots shall be opened in temperature and moisture controlled cleanroom environment only. It is mandatory to follow the rules for disposition of material that can be hazardous for humans and environment.
- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Singulated die are not to be handled with tweezers. A vacuum wand with non metallic ESD protected tip should be used.

PACKING

Chips are fixed on adhesive foil. Upon request the foils can be mounted on plastic frame or disco frame. For shipment, the wafers are arranged to stacks and hermetically sealed in plastic bags to ensure protection against environmental influence (humidity and contamination).
Use for recycling reliable operators only. We can help getting in touch with your nearest sales office. By agreement we will take back packing material, if it is sorted. You will have to bear the costs of transport. We will invoice you for any costs incurred for packing material that is returned unsorted or which we are not obliged to accept.

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