HD49323AF-01

CDS/AGC & 10-bit A/D Converter

HITACHI

ADE-207-262A (Z)
2nd Edition
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Description

The HD49323AF-01 is a CMOS IC that provides CCD-AGC analog processing (CDS/AGC) suitable for CCD camera digital signal processing systems together with a 10-bit A/D converter in a single chip.

Functions

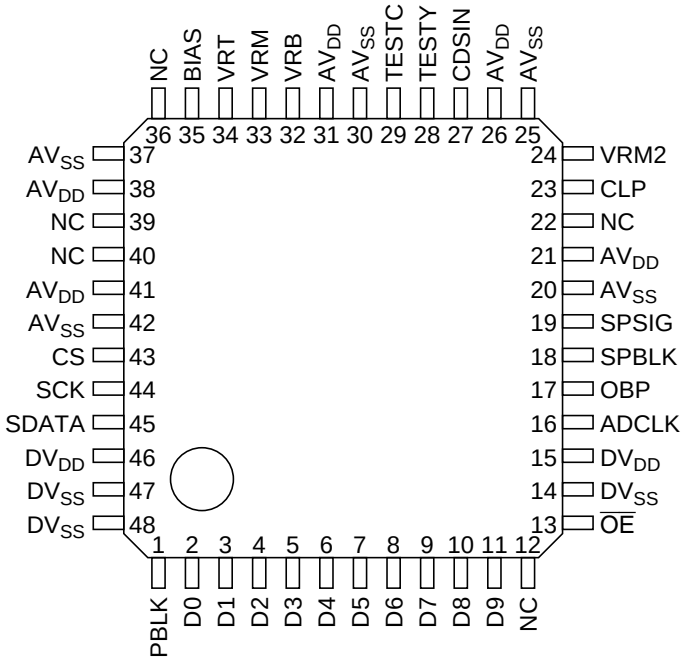
- Correlated Double Sampling
- AGC
- Sample hold
- Offset compensation
- Serial interface control
- 10-bit ADC
- 3 V single operation (2.7 V to 3.6 V)
- Power dissipation: 198 mW (Typ)
- Maximum frequency: 20 MHz (Min)

Features

- Good suppression of CCD output low-frequency noise is achieved through the use of S/H type correlated double sampling.
- A high S/N ratio is achieved through the use of a AGC type amplifier, and high sensitivity is provided by a wide cover range.
- An auto offset circuit provides compensation of output DC offset voltage fluctuations due to variations in AGC amplifier gain.
- AGC, standby mode, offset control, etc., is possible via a serial interface.
- High precision is provided by a 10-bit-resolution A/D converter.
- Version of Hitachi's previous-generation HD49322BF with improved functions and performance, including in particular an approximately 3.0 dB improvement in S/N.

Hitachi semiconductor

Pin Arrangement



(Top view)

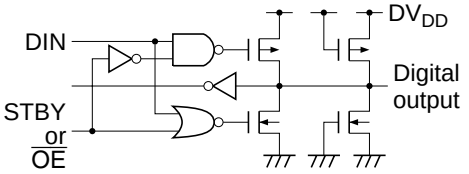
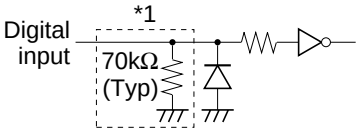
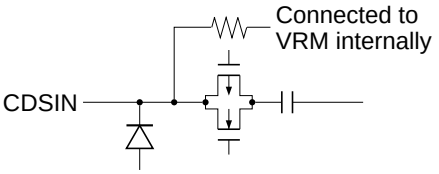
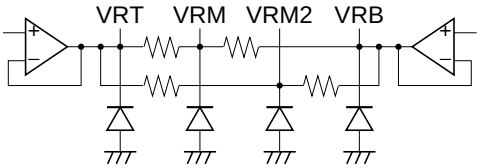
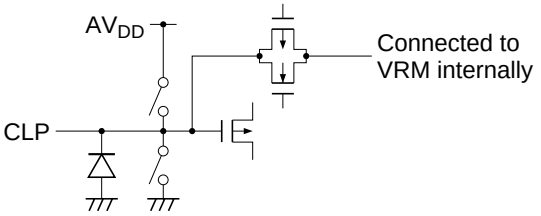
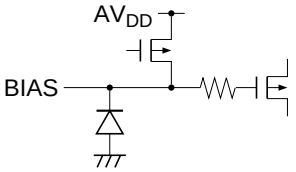
Pin Description

Pin No.	Symbol	Description	I/O	Analog(A) or Digital(D)
1	PBLK	Pre-blanking pin	I	D
2	D0	Digital output (LSB)	O	D
3 to 10	D1 to D8	Digital output	O	D
11	D9	Digital output (MSB)	O	D
12	NC	No connection pin	—	—
13	$\overline{OE}$	Digital output enable control pin	I	D
14	DV_{SS}	Digital ground (0 V)	—	D
15	DV_{DD}	Digital power supply (3 V) Connect off-chip in common with AV_{DD}.	—	D
16	ADCLK	ADC conversion clock input pin	I	D
17	OBP	Optical black pulse input pin	I	D
18	SPBLK	Black level sampling clock input pin	I	D
19	SPSIG	Signal level sampling clock input pin	I	D
20	AV_{SS}	Analog ground (0 V)	—	A
21	AV_{DD}	Analog power supply (3 V) Connect off-chip in common with DV_{DD}.	—	A
22	NC	No connection pin	—	—
23	CLP	Clamp voltage pin Connect a 0.22 µF or more capacitor between CLP and AV_{SS}.	—	A
24	VRM2	Reference voltage pin (for CCD offset cancel)	—	A
25	AV_{SS}	Analog ground (0 V)	—	A
26	AV_{DD}	Analog power supply (3 V) Connect off-chip in common with DV_{DD}.	—	A
27	CDSIN	CDS input pin	I	A
28	TESTY	Test input pin-Y	I	A
29	TESTC	Test input pin-C	I	A
30	AV_{SS}	Analog ground (0 V)	—	A
31	AV_{DD}	Analog power supply (3 V) Connect off-chip in common with DV_{DD}.	—	A
32	VRB	Reference voltage pin 3 Connect a 0.1 µF ceramic capacitor between VRB and AV_{SS}.	—	A
33	VRM	Reference voltage pin 2 Connect a 0.1 µF ceramic capacitor between VRM and AV_{SS}.	—	A
34	VRT	Reference voltage pin 1 Connect a 0.1 µF ceramic capacitor between VRT and AV_{SS}.	—	A

Pin Description (cont)

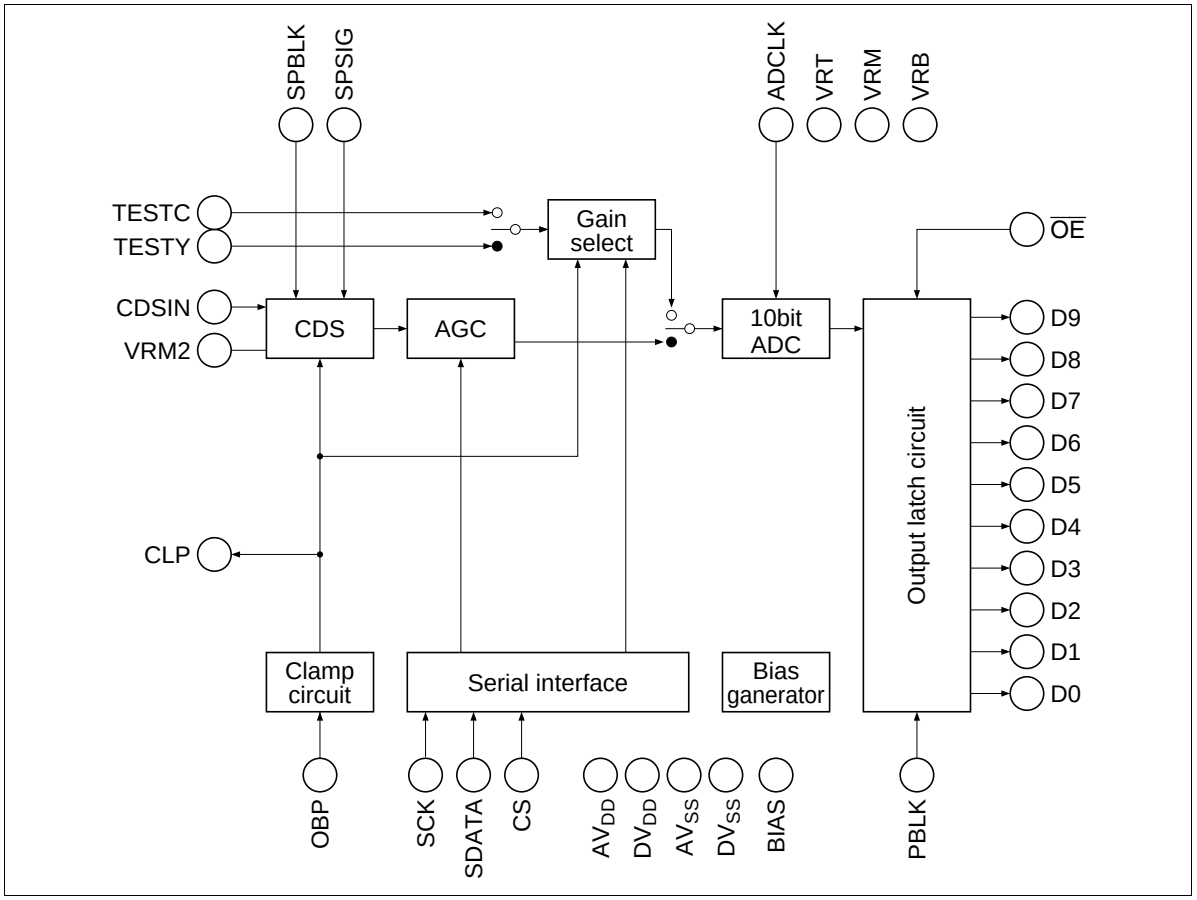
Pin No.	Symbol	Description	I/O	Analog(A) or Digital(D)
35	BIAS	Internal bias pin Connect a 24 kΩ resistor between BIAS and AV_{SS}.	—	A
36	NC	No connection pin	—	—
37	AV_{SS}	Analog ground (0 V)	—	A
38	AV_{DD}	Analog power supply (3 V) Connect off-chip in common with DV_{DD}.	—	A
39, 40	NC	No connection pin	—	—
41	AV_{DD}	Analog power supply (3 V) Connect off-chip in common with DV_{DD}.	—	A
42	AV_{SS}	Analog ground (0 V)	—	A
43	CS	Serial interface control input pin	I	D
44	SCK	Serial clock input pin	I	D
45	SDATA	Serial data input pin	I	D
46	DV_{DD}	Digital power supply (3 V) Connect off-chip in common with AV_{DD}.	—	D
47, 48	DV_{SS}	Digital ground (0 V)	—	D

Input/Output Equivalent Circuit

Pin Name		Equivalent Circuit
Digital output	D0 to D9	
Digital input	ADCLK OBP SPBLK SPSIG CS SCK SDATA PBLK $\overline{OE}$	
Analog input	CDSIN	
Reference voltage input	VRT VRM VRB VRM2	
Clamp	CLP	
Internal bias	BIAS	

Note: 1. Applies to $\overline{OE}$ and PBLK.

Block Diagram



Internal Functions

Functional Description

- CDS (Correlated Double Sampling) circuit
- AGC gain selection (11-bit digital control) *[1]
  - AGC gain can be set in the range 0 dB to 34.7 dB on the (+) side, and –3.3 dB to 0 dB on the (–) side by means of 11-bit serial data.
- Automatic offset adjustment is possible for the IC's offsets (CDS, AGC, ADC) by means of serial data control at power-on.*[1]
- Digital output enable function
- Pre-blanking function
  - Digital output can be fixed at 32 LSB
- CDS offset cancel function

Note: 1. Serial data control

Operating Description

Figure 1 shows CDS/AGC +ADC function block.

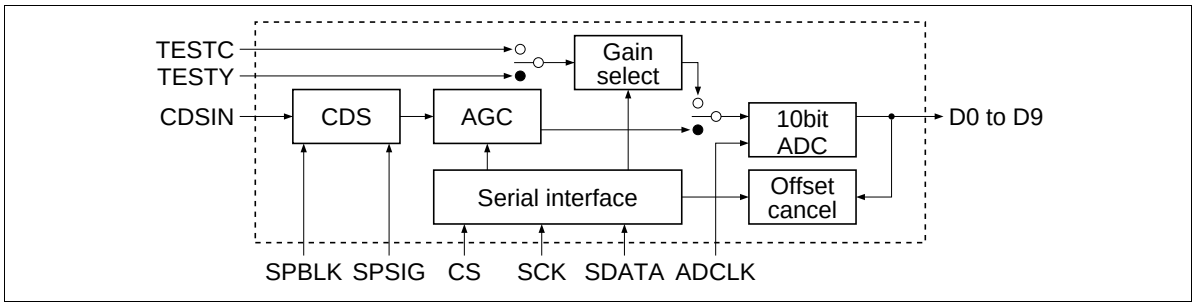


Figure 1 CDS/AGC +ADC Function Block

1. CDS (Correlated Double Sampling) Circuit

   The CCD imaging element alternately outputs a black level (A-period signal) and a signal including the black level (B-period signal). The CDS circuit extracts the differential voltage between the black level and the signal including the black level (see figure 4).

   Black level sampling is performed at the rising edge of the SPBLK pulse, and signal level sampling is performed at the rising edge of the SPSIG pulse. This sequence of operations extracts the differential voltage between the black level and the signal including the black level, and supplies this to the next-stage AGC circuit.

2. Feed back clamp function

   The clamp level is set by means of 5-bit serial data. The setting range is 32 LSB to 56 LSB, in 1 LSB steps. A serial data value of 0 gives a 32 LSB setting, and a value of 24 gives a 56 LSB setting.

3. AGC Circuit

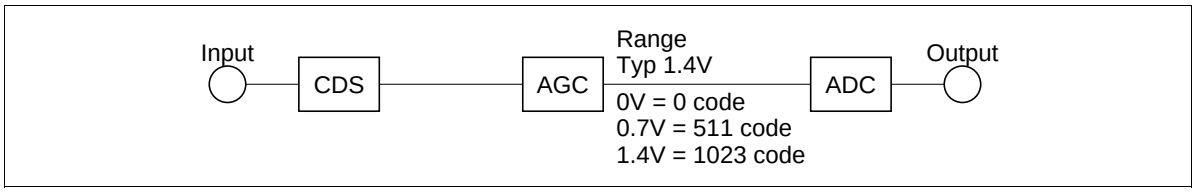
The AGC gain is set by means of 11-bit serial data. The setting range is –3.3 dB to 34.7 dB. Details of the data are given in the following section.

The (–) side gain setting uses setting codes –81 to 0 in 0.0039-multiple steps, and the (+) side gain setting uses setting codes 0 to 1023 in 0.034 dB steps.

- Detailed specifications of HD49323AF-01 AGC gain setting codes

(1) To improve S/N, the AD input dynamic range has been extended to 1.4 V from the 1.0 V of the HD49322BF.

(2) There are two AGC gain ranges: (+) side 0 to 34.7 dB linear gain amp. (0.034 dB/step), and (–) side 0 to –3.3 dB "multiple" linear gain amp. (0.0039 multiple/step).



Considering the case where AGC gain is set so that the ADC output code is 511 when a 150 mV signal is input:

— The HD49322BF AGC gain setting is (code 511)/150 mV multiple = 500 mV/150 mV multiple

— The HD49323AF-01 AGC gain setting is (code 511)/150 mV multiple = 700 mV/150 mV multiple

Table 1 AGC Gain (+) Setting Code Table

Code	BIN (D10 to D0)	dB
0	000 0000 0000	0.000
1	000 0000 0001	0.034
2	000 0000 0010	0.068
3	000 0000 0011	0.102
⋮		
510	001 1111 1110	17.34
511	001 1111 1111	17.37
512	010 0000 0000	17.41
513	010 0000 0001	17.44
⋮		
1020	011 1111 1100	34.68
1021	011 1111 1101	34.71
1022	011 1111 1110	34.75
1023	011 1111 1111	34.78

Table 2 AGC Gain (–) Setting Code Table

Code	BIN (D10 to D0)	Multiple	dB
0	000 0000 0000	1.000	0.000
–1	111 1111 1111	0.996	–0.034
–2	111 1111 1110	0.992	–0.068
–3	111 1111 1101	0.988	–0.102
⋮			
–30	111 1110 0010	0.883	–1.083
–31	111 1110 0001	0.879	–1.121
–32	111 1110 0000	0.875	–1.160
–33	111 1101 1111	0.871	–1.199
⋮			
–78	111 1011 0010	0.695	–3.156
–79	111 1011 0001	0.691	–3.205
–80	111 1011 0000	0.688	–3.255
–81	111 1010 1111	0.684	–3.304

4. Offset cancel circuit

When power is turned on, offset voltages generated by CDS, AGC, ADC, and other circuits by means of serial data control are canceled. (Refer to page 24 (Operating Sequence at Power-On).)

5. Digital output enable function

When the $\overline{OE}$ pin is driven high, digital output goes to the high-Z state.

$\overline{OE}$ Pin	Digital Output
High	High-Z state
Low (or Open, GND)	Output enable

6. Pre-blanking function

When the PBLK pin is driven high, digital output is fixed at 32 LSB. However, this is valid only when the $\overline{OE}$ pin and serial data output mode settings (LINV, MINV, TEST, STBY) are low.

PBLK Pin	Digital Output
High	Fixed at 32 LSB
Low (or Open, GND)	Active

7. CCD offset cancel function

This function cancels the offset voltage (V_{OFCCD}) during the optical black period of the CCD imaging element. The definition of the CCD offset voltage (V_{OFCCD}) is given below.

- The difference between the black level sampling voltage and signal level sampling voltage during the OBP period is designated V_{OFCCD}. This value is positive when (signal level sampling voltage) > (black level sampling voltage).

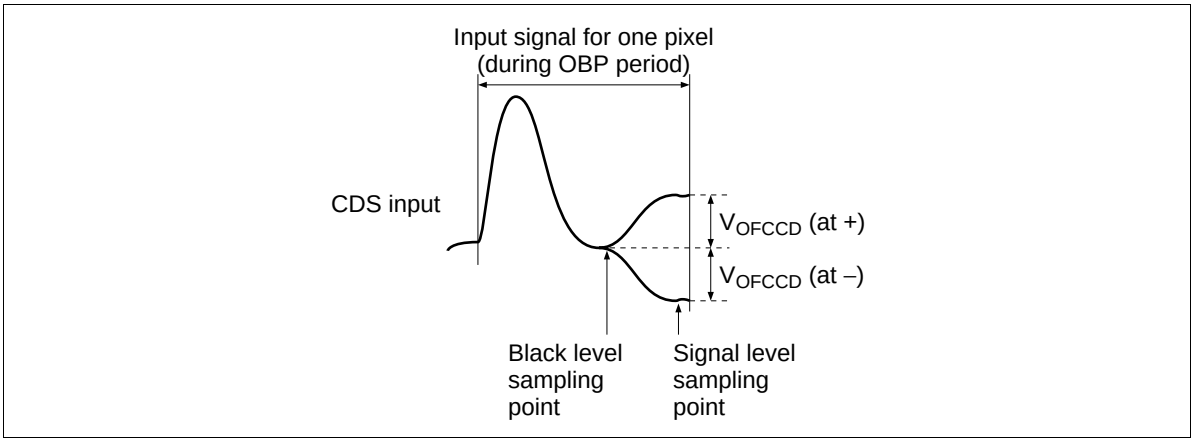


Figure 2 Black Level Signal Level Difference during OBP Period

Table 3 Serial Data Settings

V_{OFCCD} Cancel Function	When Used	When Not Used
Serial data settings	VOFCON bit set to 1 VOFD0—3 (4 bits) set	VOFCON bit cleared to 0

- Determining serial set data VOFD0—3

  (1) Provisional setting

  Serial data VOFD0—3 settings are made according to the value of V_{OFCCD} as shown in table 4.

  (2) Actual setting

  The set data is adjusted so that the CLP pin (pin 23) voltage is closest to 1/2 AV_{DD} when AGC gain is set to the maximum.

  The data obtained in (2) is used as the serial set data.

Table 4 V_{OFCCD} Serial Setting Data Correspondence Table (For Reference)

V_{OFCCD}	Serial Setting Data			
(mV)	VOFD3	VOFD2	VOFD1	VOFD0
–110	0	0	1	0
–90	0	0	1	1
–70	0	1	0	0
–50	0	1	0	1
–30	0	1	1	0
–10	0	1	1	1
+10	1	0	0	0
+30	1	0	0	1
+50	1	0	1	0
+70	1	0	1	1
+90	1	1	0	0
+110	1	1	0	1

Timing Chart

Figure 3 shows the output timing.

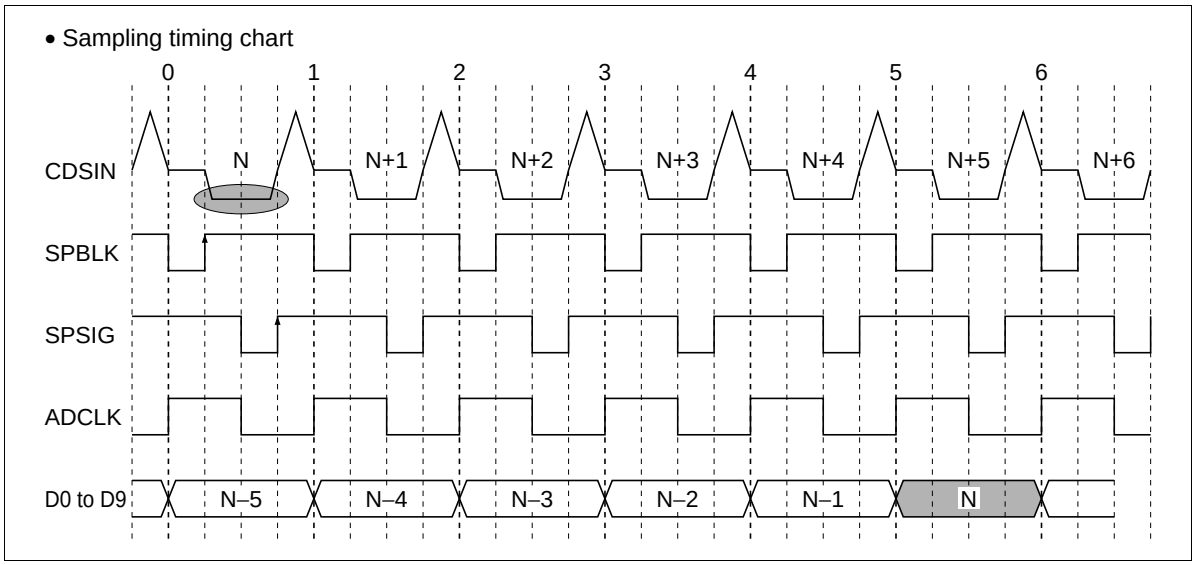
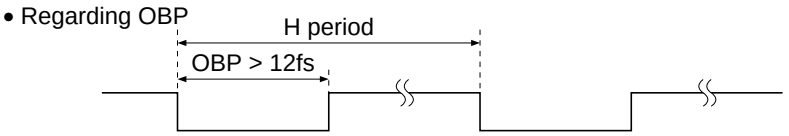


Figure 3 Output Timing

- The ADC output signals (D0 to D9) are output at the rising edge of ADCLK.
- The pipeline delay is 5 clocks.



Note: The phase of OBP is for a low setting of the serial data OBP INV bit.

Details of Timing Specifications

Details of Timing Specifications

Details of the timing specifications are shown in figure 4, and the timing specifications are summarized in table 5.

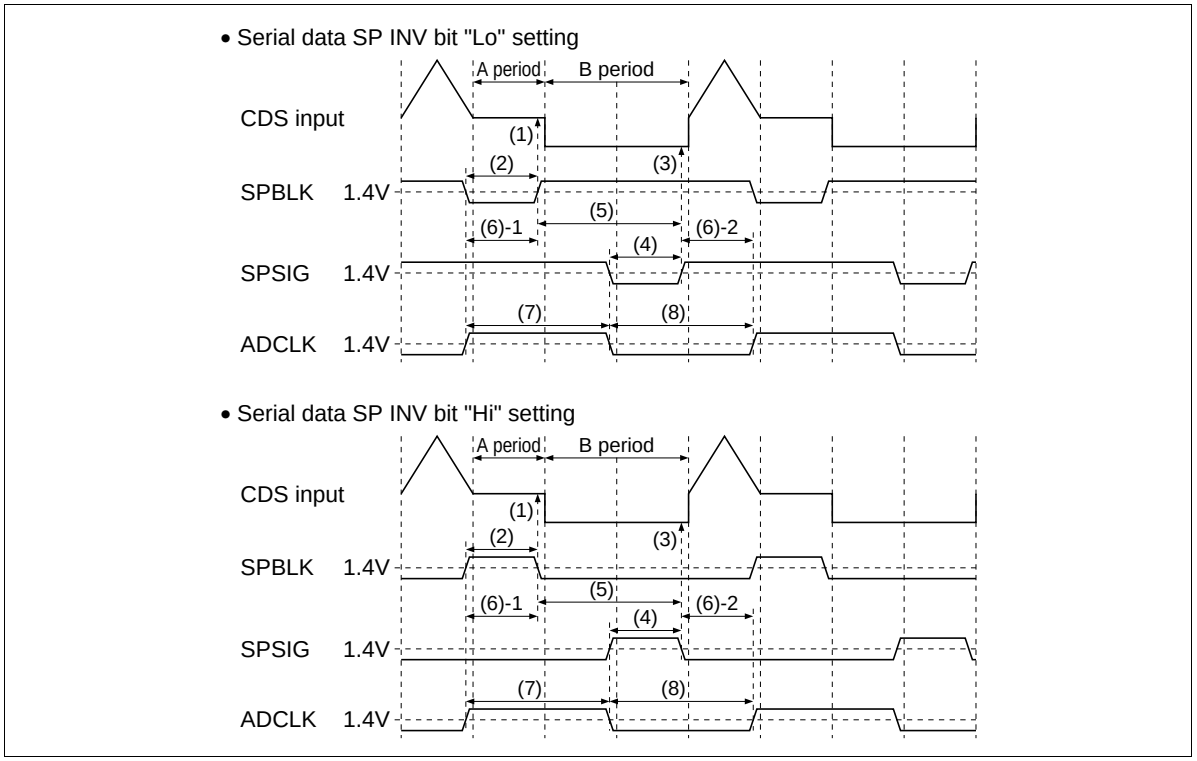
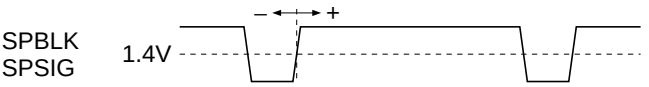


Figure 4 Details of Timing Specifications

Table 5 Each Timing Specifications

No.	Timing	Symbol	Min	Typ	Max	Unit	Note
(1)	Black level signal read-in time	t_{CDS1}	0	5	10	ns	1
(2)	SPBLK "Lo" period	t_{CDS2}	11	$1/4f_{ADCLK}$	Typ × 1.2	ns	2
(3)	Signal level read-in time	t_{CDS3}	0	5	10	ns	1
(4)	SPSIG "Lo" period	t_{CDS4}	11	$1/4f_{ADCLK}$	Typ × 1.2	ns	2
(5)	SPBLK rise to SPSIG rise	t_{CDS5}	20	$1/2f_{ADCLK}$	Typ × 1.15	ns	2
(6)-1	ADCLK rise to SPBLK rise	t_{CDS6-1}	25	—	—	ns	2
(6)-2	SPSIG rise to ADCLK rise	t_{CDS6-2}	0			ns	2
(7), (8)	ADCLK t_{WH} Min / t_{WL} Min	$t_{CDS7, 8}$	22			ns	

Note: 1. Negative when data before the rising edge of SPBLK/SPSIG is sampled, and positive when data after the rising edge is sampled.
2. The polarity of SPBLK and SPSIG is for a low setting of the serial data SP INV bit.



Detailed Timing Specifications for Digital Output Enable Control

Detailed timing specifications in the case of digital output enable control are shown in figure 5. When the $\overline{OE}$ pin is high, output disable mode is entered and output goes to the high-Z state.

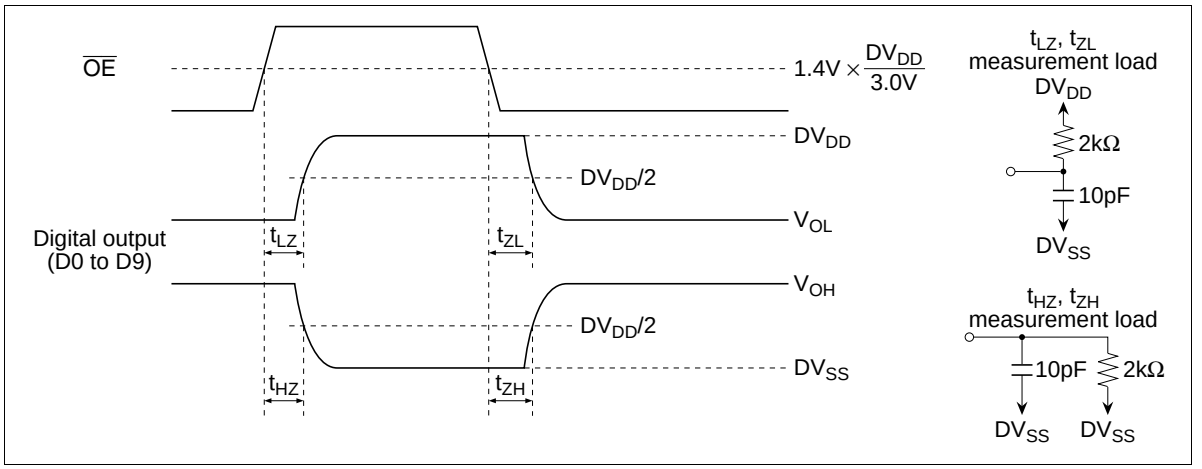


Figure 5 Detailed Timing Specifications for Digital Output Enable Control

Detailed Timing Specifications for Pre-Blanking

Detailed timing specifications for pre-blanking are shown in figure 6. When the PBLK pin is high, digital output is fixed at 32 LSB. However, the $\overline{OE}$ pin and serial data output mode settings (LINV, MINV, TEST, STBY) take precedence.

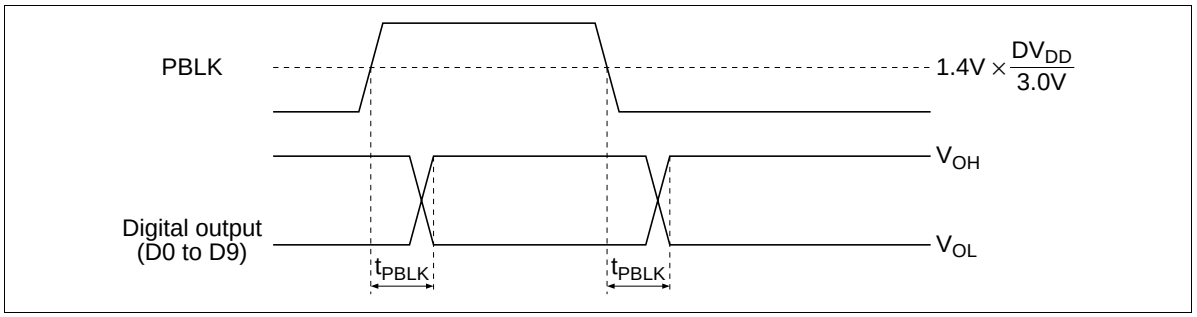


Figure 6 Detailed Timing Specifications for Pre-Blanking

Output Code Table

Table 6 Function Table

$\overline{OE}$	STBY	TEST	LINV	MINV	PBLK	Digital Output D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Operation Mode
H	X	X	X	X	X	Hi-Z										Output Hi-Z
L	H	X	X	X	X	Hi-Z										Low power standby
	L	L	L	L	L	Table 7 as follows										Normal operation
			L	H	L	In the table 7 below, D9 is inverted										
			H	L	L	In the table 7 below, D8 to D0 are inverted										
			H	H	L	In the table 7 below, D9 to D0 are inverted										
			L	L	H	L	L	L	L	H	L	L	L	L	L	Pre-blanking
		H	L	L	X	L	H	L	H	L	H	L	H	L	H	Test mode
			L	H	X	H	H	L	H	L	H	L	H	L	H	
			H	L	X	L	L	H	L	H	L	H	L	H	L	
			H	H	X	H	L	H	L	H	L	H	L	H	L	

Note: 1. STBY, TEST, LINV, and MINV mode setting is performed by means of serial data.
2. $\overline{OE}$ and PBLK mode setting is performed by means of external input pins.
3. Pre-blanking mode is enabled when the PBLK pin is high and all other pins are low.

Table 7 Output Code Table

Output Pin			D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Input Level
Output code	Step	0	L	L	L	L	L	L	L	L	L	L	→0V
		1	L	L	L	L	L	L	L	L	L	H	
		2	L	L	L	L	L	L	L	L	H	L	
		3	L	L	L	L	L	L	L	L	H	H	
		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
		511	L	H	H	H	H	H	H	H	H	H	→0.7V
		512	H	L	L	L	L	L	L	L	L	L	
		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
		1020	H	H	H	H	H	H	H	H	L	L	
		1021	H	H	H	H	H	H	H	H	L	H	
		1022	H	H	H	H	H	H	H	H	H	L	
		1023	H	H	H	H	H	H	H	H	H	H	→1.4V

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Power supply voltage	$V_{DD(max)}$	6.0	V
Power dissipation	$P_{D(max)}$	400	mW
Analog input voltage	$V_{IN(max)}$	–0.3 to AV_{DD} +0.3	V
Digital input voltage	$V_{I(max)}$	–0.3 to 6.0	V
Operating temperature	Topr	–10 to +85	°C
Storage temperature	Tstg	–55 to +125	°C

Note: 1. V_{DD} indicates AV_{DD} and DV_{DD}.

2. Common connection of AV_{DD} and DV_{DD} should be made off-chip. If AV_{DD} and DV_{DD} are isolated by a noise filter, the phase difference should be 0.3 V or less at power-on and 0.1 V or less during operation.

Electrical Characteristics (Unless othewide specified, Ta = 25°C, AV_{DD} = 3.0 V, DV_{DD} = 3.0 V, R_{EXT} = 24 kΩ)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
Power supply voltage range	V_{DD}	2.70	3.00	3.60	V	f_{CLK} = 20 MHz	
Conversion	f_{CLK} max	20	—	—	MHz		
frequency	f_{CLK} min	—	—	5.5	MHz		
Digital input voltage	V_{IH}	$2.0 \times \frac{DV_{DD}}{3.0}$	—	5.0	V		5 V amplitude input possible
	V_{IL}	0	—	$0.8 \times \frac{DV_{DD}}{3.0}$	V		Digital input pins except CS, SCK, and SDATA
	V_{IH2}	$2.25 \times \frac{DV_{DD}}{3.0}$	—	5.0	V		5 V amplitude input possible
	V_{IL2}	0	—	$0.6 \times \frac{DV_{DD}}{3.0}$	V		CS, SCK, SDATA
Digital output	V_{OH}	DV_{DD} –0.5	—	—	V	I_{OH} = –2 mA	
voltage	V_{OL}	—	—	0.5	V	I_{OL} = +2 mA	
Digital input current	I_{IH}	—	—	50	µA	V_{IH} = 5.0 V	Digital input pins except PBLK and $\overline{OE}$
	I_{IH2}	—	—	250	µA	V_{IH} = 5.0 V	PBLK, $\overline{OE}$
	I_{IL}	–50	—	—	µA	V_{IL} = 0 V	
Digital output	I_{OZH}	—	—	50	µA	V_{OH} = V_{DD}	
current	I_{OZL}	–50	—	—	µA	V_{OL} = 0 V	
ADC resolution	RES	10	10	10	bit		
ADC integration linearity error	INL	—	4	10	LSBp-p	f_{CLK} = 20 MHz	
ADC differentiation	DNL+	—	0.3	0.8	LSB	f_{CLK} = 20 MHz	*1
linearity error	DNL–	–0.8	–0.3	—	LSB		
Digital output delay time	t_{PD}	—	—	35	ns	C_L = 10 pF	
Digital output hold time	t_{HOLD}	10	—	—	ns		

Note: 1. DNL calculate the difference of linearity error between next two codes.

Electrical Characteristics (Unless othewide specified, Ta = 25°C, AV_{DD} = 3.0 V, DV_{DD} = 3.0 V, R_{EXT} = 24 kΩ) (cont)

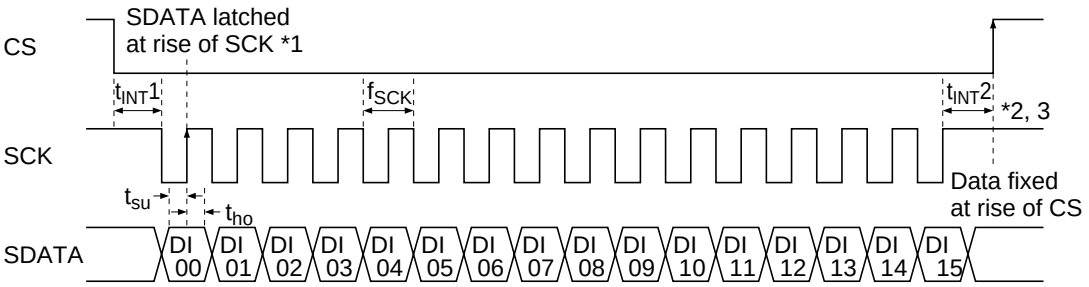
Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
Sleep current	I_{SLP}	–100	0	100	µA	Digital input pins fixed at 0 V, output pins open	
Standby current	I_{STBY}	—	8	12	mA	Digital input pins fixed at 0 V	
ADC Input range	V_{INp-p}	—	(1.4)	—	V		*2
Digital output Hi-Z	t_{HZ}	—	—	100	ns	R_L = 2 kΩ	*3
delay time	t_{LZ}	—	—	100	ns	C_L = 10 pF	
	t_{ZH}	—	—	100	ns		
	t_{ZL}	—	—	100	ns		
Digital output PBLK delay time	t_{PBLK}	—	—	100	ns	C_L = 10 pF	*3
Quiescent current	I_{DD1}	—	66	78	mA	f_{CLK} = 20 MHz	CDSIN use
Timing specification (1)	t_{CDS1}	0	5	10	ns		*3
Timing specification (2)	t_{CDS2}	11	$1/4f_{ADCLK}$	Typ × 1.2	ns		
Timing specification (3)	t_{CDS3}	0	5	10	ns		
Timing specification (4)	t_{CDS4}	11	$1/4f_{ADCLK}$	Typ × 1.2	ns		
Timing specification (5)	t_{CDS5}	20	$1/2f_{ADCLK}$	Typ × 1.15	ns		
Timing specification (6-1)	t_{CDS6-1}	25	—	—	ns		
Timing specification (6-2)	t_{CDS6-2}	0	—	—	ns		
Timing specification (7)	t_{CDS7}	22	—	—	ns		
Timing specification (8)	t_{CDS8}	22	—	—	ns		
Input current	IIN_{CDS}	–60	—	10	µA	f_{CLK} = 20 MHz, Black/signal level difference = 1 V, gain = 0 dB	*4
Clamp level	CLP(00)	—	(32)	—	LSB		*2
	CLP(16)	—	(48)	—	LSB		
	CLP(24)	—	(56)	—	LSB		

Note: 2. Items in parentheses are reference values.
3. Refer to page 12 (Details of Timing Specifications).
4. This is not transition current, but static current.

Electrical Characteristics (Unless othewide specified, Ta = 25°C, AV_{DD} = 3.0 V, DV_{DD} = 3.0 V, R_{EXT} = 24 kΩ) (cont)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
AGC gain(–)	AGC(–081)	–5.3	–3.3	–1.3	dB		
	AGC(0000)	–2.0	0	2.0	dB		
AGC gain(+)	AGC(0000)	–2.0	0	2.0	dB		
	AGC(0128)	2.4	4.4	6.4	dB		
	AGC(0256)	6.7	8.7	10.7	dB		
	AGC(0384)	11.1	13.1	15.1	dB		
	AGC(0512)	15.4	17.4	19.4	dB		
	AGC(0640)	19.8	21.8	23.8	dB		
	AGC(0768)	24.1	26.1	28.1	dB		
	AGC(0896)	28.5	30.5	32.5	dB		
	AGC(1023)	32.3	34.8	37.8	dB		

Serial Interface Specification



Note: 1. SDATA is latched at the rise of SCK.
2. Input 16 SCK clocks while CS is low. If the number of clocks is more or less than 16, the data will be invalid.
3. If data transmission is aborted, the data is invalid.

Figure 7 Serial Interface Specification

Table 8 Serial Data Functions Table

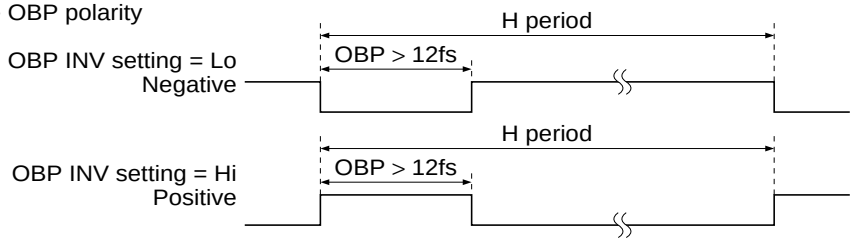
	Resister 0	Resister 1	Resister 2	Resister 3
DI 00 (LSB)	Lo	Hi	Lo	Hi
DI 01	Lo	Lo	Hi	Hi
DI 02	AGC Gain setting (LSB)	SP INV SPSIG/SPBLK inversion	Clamp level adjustment (LSB)	Test mode *2 Use prohibited ALL Low
DI 03	AGC Gain setting	OBP INV Lo→Negative input Hi→Positive input	Clamp level adjustment	
DI 04	AGC Gain setting	CIF Lo→f_{CLK}>10MHz Hi→f_{CLK}<10MHz	Clamp level adjustment	
DI 05	AGC Gain setting	VOFCON Lo→OFF *3 Hi→ON	Clamp level adjustment	
DI 06	AGC Gain setting	VOFD0 (LSB) CCD offset voltage setting	Clamp level adjustment (MSB)	
DI 07	AGC Gain setting	VOFD1 CCD offset voltage setting	Test mode *2 Low	
DI 08	AGC Gain setting	VOFD2 CCD offset voltage setting	Low	
DI 09	AGC Gain setting	VOFD3 (MSB) CCD offset voltage setting	Low	
DI 10	AGC Gain setting	Output mode setting (LINV)	Low	
DI 11	AGC Gain setting	Output mode setting (MINV)	High	
DI 12	AGC Gain setting (MSB)	Output mode setting (TEST)	Low	
DI 13	Test mode Low setting *2	RESET Lo→Reset mode Hi→Normal operation mode	High	
DI 14	Test mode Low setting *2	OFRST Lo→Normal operation mode Hi→Offset cancel mode	High	
DI 15 (MSB)	Output mode setting (STBY) *1	SLP Lo→Normal operation mode *1 Hi→Sleep mode	High	

Notes: 1. STBY: Reference voltage generation circuit is in the operational state.
SLP: All circuits are in the sleep state.
2. Test mode is used for IC testing, and so cannot be used.
Register 2 test mode should be set in accordance with the specification at the right of the column.
For other registers, the setting should only be made in the all-low state.
3. Setting of VOFCON: Lo→CCD offset cancel function OFF
: Hi→CCD offset cancel function ON

Timing Specifications

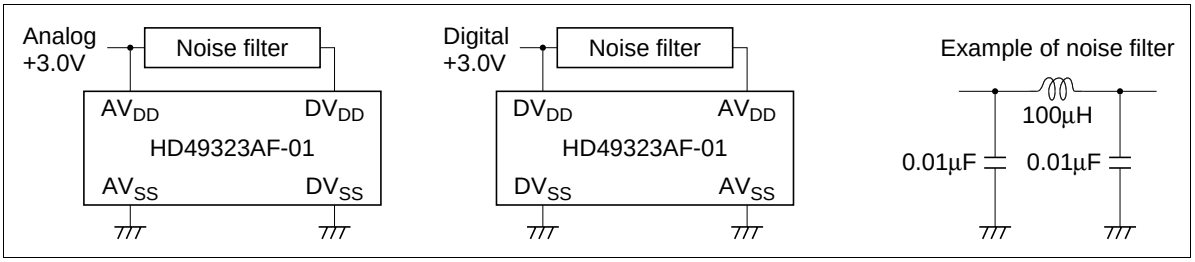
	Min	Max
f_{SCK}	—	3MHz
t_{INT}1, 2	50ns	—
t_{su}	50ns	—
t_{ho}	50ns	—

• OBP polarity



Notice for Use

1. Careful handling is necessary to prevent damage due to static electricity.
2. This product has been developed for consumer applications, and should not be used in non-consumer applications.
3. As this IC is sensitive to power line noise, the ground impedance should be kept as small as possible. Also, to prevent latchup, a ceramic capacitor of 0.1 µF or more and an electrolytic capacitor of 10 µF or more should be inserted between the ground and power supply.
4. Common connection of AV_{DD} and DV_{DD} should be made off-chip. If AV_{DD} and DV_{DD} are isolated by a noise filter, the phase difference should be 0.3 V or less at power-on and 0.1 V or less during operation.
5. If a noise filter is necessary, make a common connection after passage through the filter, as shown in the figure below.



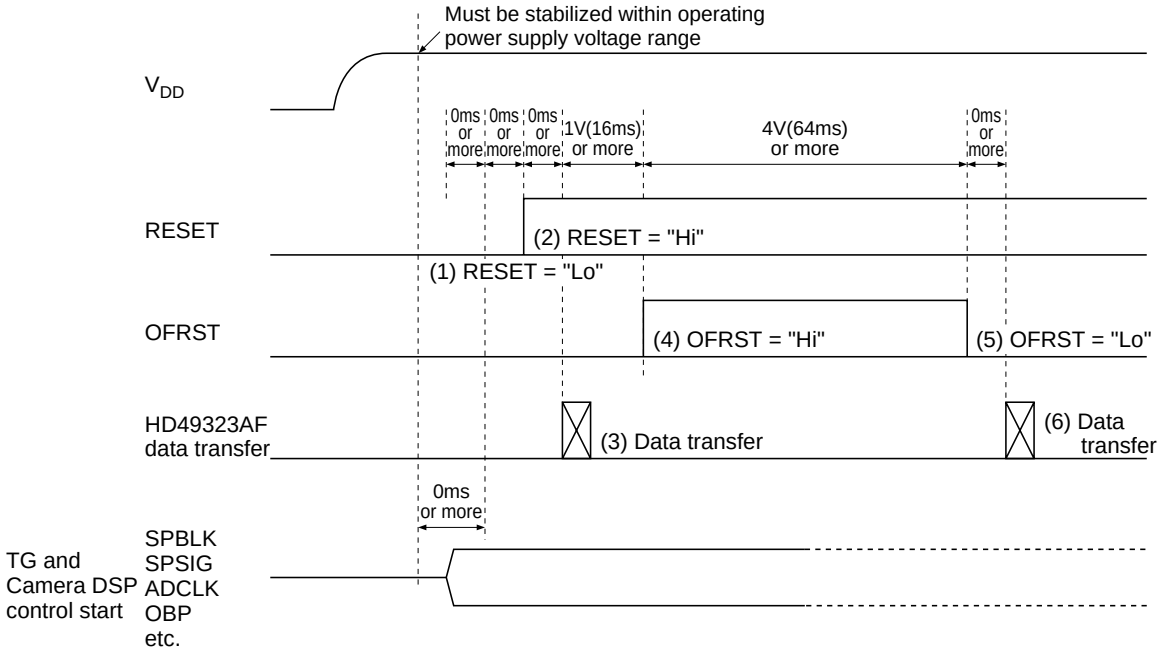
6. Connect AV_{SS} and DV_{SS} off-chip using a common ground. If there are separate analog system and digital system set grounds, connect to the analog system.
7. When V_{DD} is specified in the delivery specification, this indicates AV_{DD} and DV_{DD}.
8. No Connection (NC) pins are not connected inside the IC, but it is recommended that they be used as power supply ground pins or left open to prevent crosstalk in adjacent analog pins.
9. To ensure low thermal resistance of the package, a Cu-type lead material is used. As this material is less tolerant of bending than Fe-type lead material, careful handling is necessary.
10. The infrared reflow soldering method should be used to mount the chip. Note that general heating methods such as solder dipping cannot be used.
11. Depending on the mounting state, picture quality (crosscut noise, wave pattern, etc.) will be dependent upon the timing of the SPBLK, SPSIG, and ADCLK signals. Check the mounting state thoroughly before use.
12. Serial communication should not be performed during the effective video period, since this will result in degraded picture quality. Also, use of dedicated ports is recommended for the SCK and SDATA signals used in the HD49323AF-01. If ports are to be shared with another IC, picture quality should first be thoroughly checked.
13. At power-on, automatic adjustment of the offset voltage generated from CDS, AGC, ADC, etc., must be implemented in accordance with the power-on operating sequence (see page 24).

14. If the phase difference between the black level sampling voltage and the signal level sampling voltage during the CCD imaging element optical black period (the CCD offset voltage) is ±30 mV or greater, the CCD offset cancel function (page 9, item 7, CCD Offset Cancel Function) must be implemented.

    The CCD offset voltage variation after implementation of the CCD offset cancel function should be within ±20 mV.

15. The CDSIN pin is clamped at VRM (≅ AV_{DD}/2) during operation. The IC may suffer permanent damage if used with a pin voltage in the range –0.3 V to AV_{DD} + 0.3 V. Careful attention must therefore be paid to the input signals.

Operating Sequence at Power-On



Note: 1. RESET and OFRST both use serial data transmission.
2. Stable input of SPBLK, SPSIG, ADCLK, and OBP is assumed before RESET is transmitted.
3. Numbers in parentheses in the figure show the order of transfer.

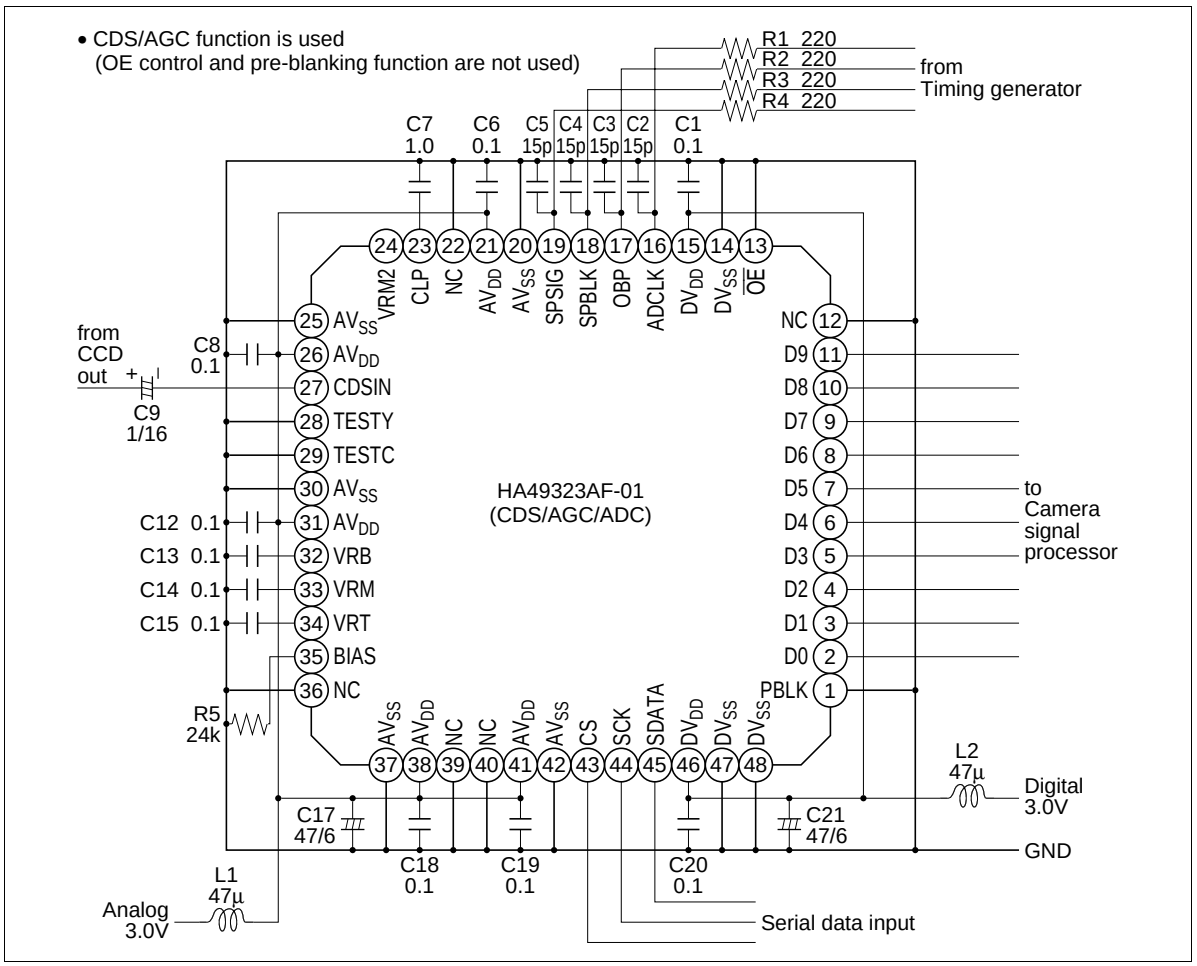
Figure 8 Operating Sequence at Power-On

Serial data transmission contents are shown in table 9.
"X" indicates data for which the clock polarity, clamp level, etc., can be selected. See page 21 (table 8, Serial Data Functions Table) for the purpose of the data.

Table 9 Serial Data

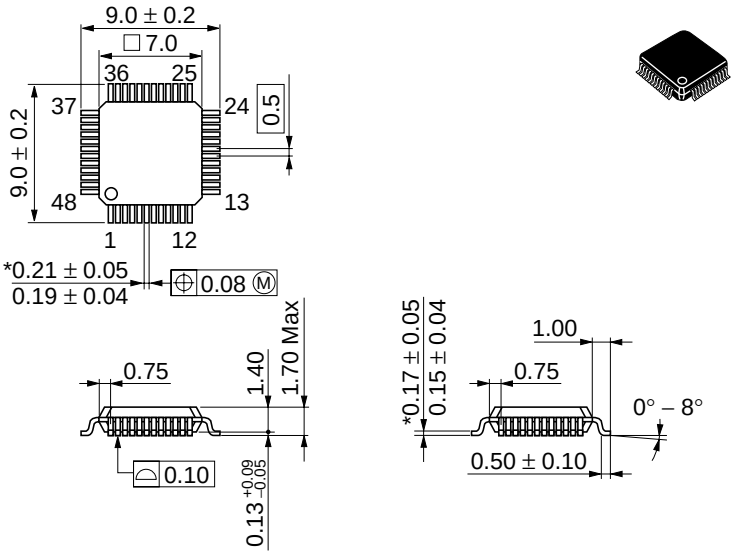
Order of Transfer		MSB 15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	LSB 00	Remarks
(1) RESET = "Lo"	a)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
(2) RESET = "Hi"	b)	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	
(3) Data transfer	c)	0	0	1	0	0	0	X	X	X	X	X	X	X	X	0	1	
	d)	1	1	1	0	1	0	0	0	0	X	X	X	X	X	1	0	
Wait																		1 V (16 ms) or more
(4) OFRST = "Hi"	e)	0	1	1	0	0	0	X	X	X	X	X	X	X	X	0	1	
Wait																		4 V (64 ms) or more
(5) OFRST = "Lo"	f)	0	0	1	0	0	0	X	X	X	X	X	X	X	X	0	1	
(6) Data transfer	g)	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	

Example of Recommended External Circuit



Package Dimensions

Preliminary Unit: mm



Hitachi Code	FP-48C
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.2 g

*Dimension including the plating thickness
Base material dimension

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