2K x 8 RADIATION-HARDENED STATIC RAM HC6216

FEATURES

RADIATION

- Fabricated with RICMOS™ Epitaxial 1.2μm Process
- Total Dose Hardness through $1x10^6$ rad(SiO_2)
- Neutron Hardness through $1x10^{14}$ cm_{-2}
- Dynamic and Static Transient Upset Hardness through $1x10^9$ rad(Si)/s
- Soft Error Rate Range of $1x10^{-6}$ to $1.0x10^{-9}$ upsets/bit-day (80°C)
- Dose Rate Survivability through $1x10^{12}$ rad(Si)/s
- Latchup Free

OTHER

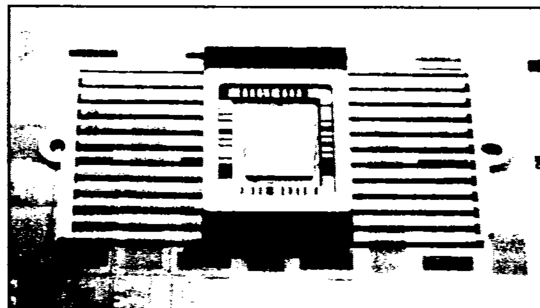
- Typical 45 ns Access TIme
- Low Operating Power
- ULTRA-Low Dynamic Deselected Power
- Asynchronous Operation
- Common Data I/O
- High Output Drive with Tri-State Outputs
- Single 5 V ± 10% Power Supply
- Full Military Temperature Range
- JEDEC Standard Pinout
- TTL & CMOS Compatible I/O
- Available in 24-Lead Flat Pack or DIP

GENERAL DESCRIPTION

The 2K x 8 Radiation-Hardened Static RAM is a high performance 2048 x 8-bit static random access memory with industry-standard functionality. It is fabricated with Honeywell's radiation-hardened CMOS technology, and is designed for use in state-of-the-art digital systems operating in space-level radiation environments. The RAM operates over the full military temperature range and requires only a single 5 V ± 10% power supply.

The typical row address access time of the RAM is 45 ns under nominal pre-radiation conditions. The RAM also features a fast column access mode, with a typical access time of 25 ns. The fast column access mode can be used to reduce RAM cycle times through use of paging or block transfer operations. Both the standard and high speed read operations are fully asynchronous in operation.

Honeywell's enhanced RICMOS™ (Radiation Insensitive CMOS) technology is radiation hardened through the use of advanced and proprietary design, layout, and process hardening techniques. The RICMOS™ process is a 5-volt, n-well CMOS technology with a 250 Å gate oxide and a minimum feature size of 1.2 μm. Additional features include two layers of interconnect metalization, a lightly doped drain (LDD) structure for improved short channel reliability, and an epitaxial starting material for latchup free operation. High resistivity cross-coupled polysilicon resistors have been incorporated for single event upset hardening.



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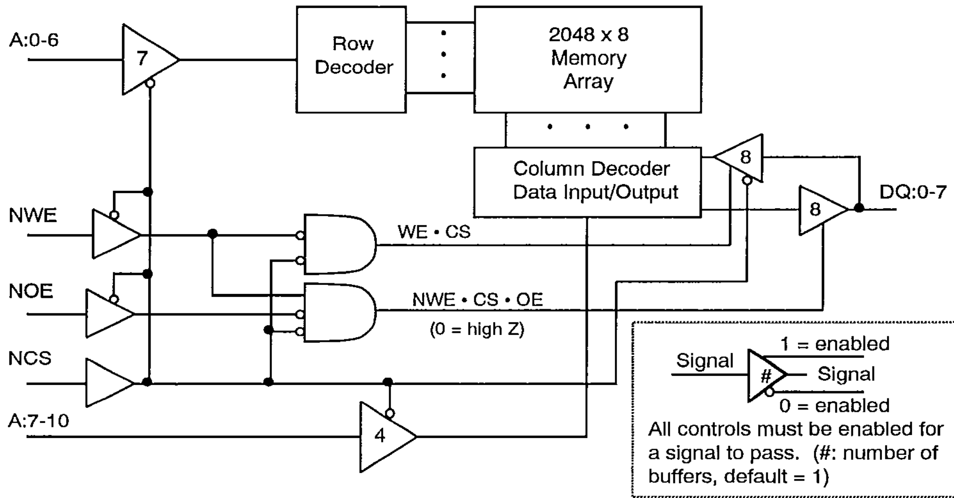
FUNCTIONAL DIAGRAM



SIGNAL DEFINITIONS

A: 0-10 Address input pins (A) which select a particular eight-bit word within the memory array

DQ: 0-7 Bidirectional data pins which serve as data outputs during a read operation and as data inputs during a write operation

NCS Negative chip select, when at a low level, allows a read or write operation. When at a high level it forces the SRAM to a precharge condition and holds the data output drivers in a high impedance state. The input circuits for input pins DQ: 0-7, NOE and A: 0-10 are disabled. If this signal is not used it must be connected to VSS.

NWE Negative write enable, when at a low level, activates a write operation and holds the data output drivers in a high impedance state. When at a high level, it allows normal read operation.

NOE Negative output enable at a high level holds the data output drivers in a high impedance state. When at a low level, data output driver state is defined by NSC and NWE. If this signal is not used it must be tied to VSS.

TRUTH TABLE

NCS	NWE	NOE	MODE	DQ
L	H	L	Read	Data Out
L	L	X	Write	Data In
H	X	XX	Deselected	High Z
XX	XX	XX	Disabled	High Z

Notes
X: VI=VIH or VIL
XX: VSS≤VI≤VDD
NOE=H: High Z output state maintained for NCS=X or NWE=X.

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RADIATION-HARDENED CHARACTERISTICS

Total Ionizing Radiation Dose

The RAM will meet all stated functional and electrical specifications after a total ionizing radiation dose of 1x10^{6} rad(SiO_2) applied at TA = 25°C. All electrical and timing performance parameters will remain within specifications after rebound at VDD = 5.5 V and TA = 125°C extrapolated to ten years of operation. Total dose hardness is assured by wafer level testing of process monitor transistors and RAM product using 10 keV X-ray radiation. RICMOS™ RAM performance and transistor threshold shift correlation have been made between 10 keV X-rays applied at a dose rate of 1x10^{5} rad(SiO_2)/min at TA = 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is equivalent to standard military radiation test environments.

Transient Pulse Ionizing Radiation

The RAM is capable of writing, reading, and retaining stored data during and after exposure to a transient ionizing radiation pulse of ≤ 1 µs duration up to 1x10^{9} rad(Si)/s, when applied under recommended operating conditions. Additionally, the RAM will not be rendered permanently incapable of meeting any functional or electrical specification after exposure to radiation pulse of ≤ 50 ns duration up to 1x10^{12} rad(Si)/s, when applied under recommended operating conditions. Note that the photocurrent induced during the pulse by the RAM inputs, outputs, and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

Neutron Radiation

The RAM will meet all stated functional and electrical specifications after a total neutron fluence of up to 1x10^{14} cm^{-2} applied under recommended operating or storage conditions.

Soft Error Rate

The RAM is capable of soft error rate (SER) performance ranging from 1x10^{-6} to 1x10^{-9} upsets/bit-day at TA=80°C, under recommended operating conditions. This hardness level is defined by the Adams 10% worst case cosmic ray environment. A trade-off exists between soft error rate and write time performance over the operating temperature range. Detailed performance trade-off information is provided later in this data sheet.

Latchup

The RAM will not latch up due to any of the above radiation exposure conditions, when applied under recommended operating conditions. Fabrication with the RICMOS™ p-epi on p+ substrate process and use of proven design techniques such as double guard banding ensure latchup immunity.

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RADIATION-HARDNESS CHARACTERISTICS (1)

Parameter	Limits (2)	Units	Test Conditions
Total Dose	≥1x10^{6}	rad(SiO_2)	TA=25°C
Transient Dose Rate Upset	≥1x10^{9}	rad(Si)/s	Pulse width≤1 µs
Transient Dose Rate Survivability	≥1x10^{12}	rad(Si)/s	Pulse width ≤50 ns, X-ray, VDD=6.6 V, TA=25°C
Soft Error Rate (3)	≤1x10^{-9}	upsets/bit-day	TA=80°C
Neutron Fluence	≥1x10^{14}	cm^{-2}	1 MeV equivalent, Unbiased, TA=25°C

(1) Device will not latchup due to any of the specified radiation exposure conditions.
(2) Operating conditions (unless otherwise specified): VDD=4.5 V to 5.5 V, TA=-55°C to +125°C.
(3) SER and write time performance trade-offs over the operating temperature range are shown later in the data sheet.

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ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating		Units
		Min	Max	
VDD	Positive Supply Voltage (2)	-0.5	7.0	V
VPIN	Voltage on Any Pin (2)	-0.5	VDD+0.5	V
TSTORE	Storage Temperature (Zero Bias)	-65	150	°C
TSOLDER	Soldering Temperature • Time		270•5	°C•s
PD	Power Dissipation		2.5	W
IOUT	DC or Average Output Current		25	mA
VPROT	Electrostatic Discharge Protection Voltage (3)	2000		V
ΘJC	Thermal Resistance (Junction-to-Case)		10	°C/W
TJ	Junction Temperature		175	°C

(1) Stresses in excess of those listed above may result in permanent damage to the HC6216. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to VSS.
(3) Class 2 electrostatic discharge (ESD) input protection voltage per MIL-STD-883, Method 3015.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Description			Units
		Min	Typ	Max	
VDD	Supply Voltage (referenced to VSS)	4.5	5.0	5.5	V
TA	Ambient Temperature	-55	25	125	°C
VPIN	Voltage on any Pin (referenced to VSS)	-0.3		VDD+0.3	V

CAPACITANCE (1)

Symbol	Parameter	Typical	Worst Case		Units	Test Conditions
			Min	Max		
CI	Input Capacitance			11	pF	VI=VDD or VSS, f=1 MHz
CO	Output Capacitance			12	pF	VO=VDD or VSS, f=1 MHz

(1) This parameter is tested during initial device characterization only.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Typical (1)	Worst Case (2) Min	Worst Case (2) Max	Units	Test Conditions
IDDSB1	Standby Supply Current	10		200	µA	VDD=5.5 V, NCS=VIH, VIH=VDD, VIL=VSS
IDDOPW	Operating Supply Current (Write)	5		7	mA	VDD=5.5 V, f=1 MHz IO=0, NWE=NCS=VIL=VSS, VIH=VDD
IDDOPR	Operating Supply Current (Read)	5		7	mA	VDD=5.5 V, f=1 MHz IO=0, NCS=VIL=VSS, NWE=VIH=VDD
IDDOP2	Deselected Dynamic Current	1.5		200	µA	VDD=5.5 V, f=1 MHz IO=0, NCS=VIH, VIH=VDD, VIL=VSS
II	Input Leakage Current	0.01		1.0	µA	VDD=5.5 V, VSS≤VI≤VDD
IOZ	Output Leakage Current	0.01		1.0	µA	VDD=5.5 V, VSS≤VO≤VDD
VDR	Data Retention Voltage (3)		2.5		V	NCS=VDR, VIH=VDD, VIL=VSS
IDR	Data Retention Current	10		150	µA	VDD=3.0 V, NCS=VIH, VIH=VDD, VIL=VSS
VIL_{TTL}	Low Level Input Voltage (TTL)			0.8		
VIH_{TTL}	High Level Input Voltage (TTL)		2.2			
VIL_{CMOS}	Low-Level Input Voltage (CMOS)			0.3(VDD)	V	VDD=4.5 V
VIH_{CMOS}	High-Level Input Voltage (CMOS)		0.7(VDD)		V	VDD=5.5 V
VOL	Low-Level Output Voltage	0.25		0.4	V	VDD=4.5 V, IOL=10 mA
VOH	High-Level Output Voltage	4.35	4.2		V	VDD=4.5 V, IOH=-5 mA

(1) Typical operating conditions: TA=25°C, pre-radiation.
(2) Worst case operating conditions: TA=55°C to +125°C, total dose through 1×10^6 rad(SiO_2).
(3) To maintain valid data storage during transient radiation, VDD must be held within the recommended operating range.

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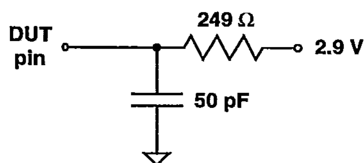
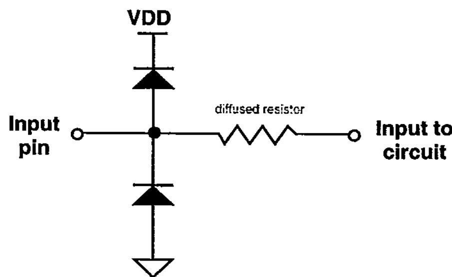


EQUIVALENT LOAD CIRCUIT



EQUIVALENT ESD PROTECTION CIRCUIT

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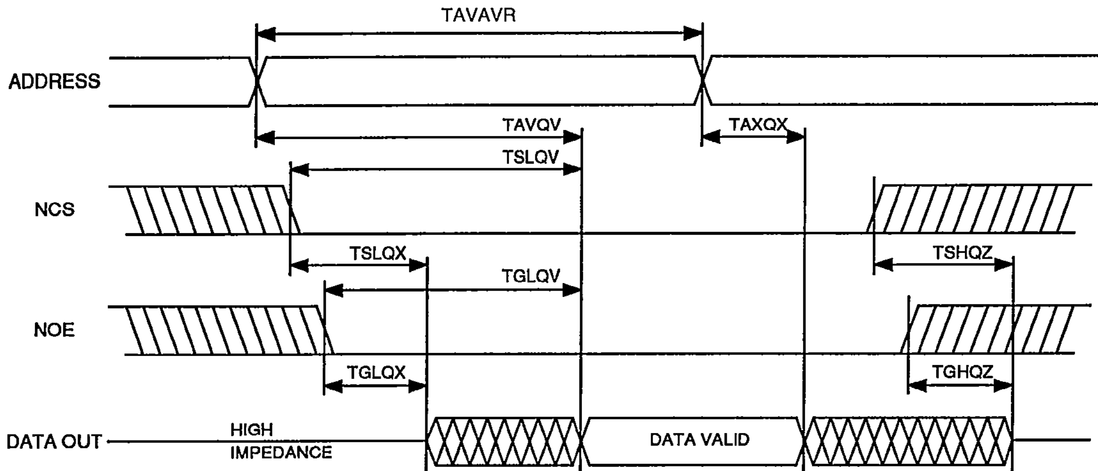
READ CYCLE AC ELECTRICAL CHARACTERISTICS (1)

Symbol	Parameter	Typical (2)	Worst Case (3)		Units
			Min	Max	
TAVAVR	Read Cycle Time (4)	45	100		ns
TAVQV	Address Access Time	45		100	ns
TSLQV	Chip Select Access Time	50		100	ns
TSHQZ	Chip Select Output Disable Time	15		25	ns
TSLQX	Chip Select Output Enable Time (4)	4	2		ns
TGLQX	Output Enable Time (4)	4	2		ns
TGHQZ	Output Enable Output Disable Time	15		30	ns
TGLQV	Output Enable Access Time	20		40	ns
TAXQX	Output Hold After Address Change Time (4)	8	6		ns

(1) Test conditions: input switching levels VIL/VIH=0.2VDD/0.8VDD for CMOS; 0.0V/3.0V for TTL, input rise and fall times <5 ns, input and output timing reference levels=1.5 V, capacitive output loading=50 pF.
(2) Typical operating conditions: VDD=5.0 V, TA=25°C, pre-radiation.
(3) Worst case operating conditions: VDD=4.5 V to 5.5 V, TA=-55°C to +125°C, total dose through $1x10^6$ rad(SiO_2).
(4) Not tested; guaranteed by design.



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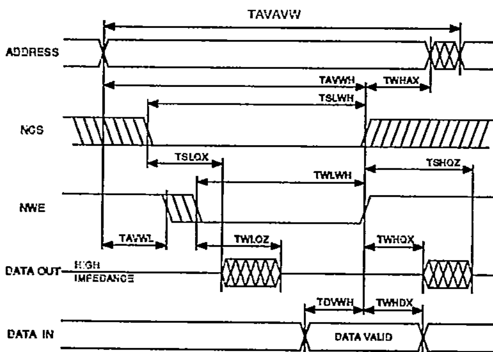
WRITE CYCLE AC ELECTRICAL CHARACTERISTICS (1,2)

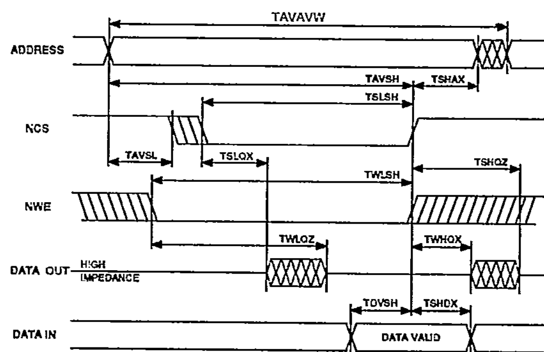
Symbol	Parameter	Typical (3)	Worst Case (4)		Units
			Min	Max	
TAVAVW	Write Cycle Time (5)	50	85		ns
TAVWL	Address Valid Setup to Write Time (5)		0		ns
TAVSL	Address Valid Setup to Write Time (5)		0		ns
TAVWH	Address Valid to End of Write Time	40	70		ns
TAVSH	Address Valid to End of Write Time (5)	40	70		ns
TWLWH	Write Enable Pulse Width Time	40	70		ns
TSLSH	Chip Select Write Pulse Width Time (5)	40	70		ns
TWLSH	Write Enable to End of Write Time (5)	40	70		ns
TSLWH	Chip Select to End of Write Time	40	70		ns
TWHWL	Write Enable Write Disable Pulse Width (5)	10	15		ns
TSHSL	Chip Select Write Disable Pulse Width (5)	10	15		ns
TWHAX	Address Valid Hold after End of Write Time (5)		0		ns
TSHAX	Address Valid Hold after End of Write Time (5)		0		ns
TDVWH	Data Valid to End of Write Time	40	70		ns
TSVSH	Data Valid to End of Write Time (5)	40	70		ns
TWHDX	Data Hold after End of Write Time (5)		0		ns
TSHDX	Data Hold after End of Write Time (5)		0		ns
TWLQZ	Write Enable Output Disable Time	15		30	ns
TWHQX	Write Enable Output Enable Time (5)	6	2		ns

(1) Test conditions: input switching levels VIL/VIH=0.2VDD/0.8VDD for CMOS; 0.0V/3.0V for TTL, input rise and fall times <5 ns, input and output timing reference levels=1.5 V, capacitive output loading=50 pF.
(2) All write time parameters reflect an SER performance level of 1×10^{-7} upsets/bit-day.
(3) Typical operating conditions: VDD=5.0 V, TA=25°C, pre-radiation.
(4) Worst case operating conditions: VDD=4.5 V to 5.5 V, TA=-55°C to +125°C, total dose through 1×10^5 rad(SiO_2).
(5) Not tested; guaranteed by design.

WRITE CYCLE I (NWE CONTROLLED)



WRITE CYCLE II (NCS CONTROLLED)



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DYNAMIC ELECTRICAL CHARACTERISTICS

Read Cycle

The RAM is asynchronous in operation, allowing the read cycle to be controlled by either address or chip select (NCS) edge transitions (refer to Read Cycle timing diagram). To perform a valid read operation, both chip select and output enable (NOE) must be low and write enable (NWE) must be high. The output driver can be controlled independently by the NOE signal. Consecutive read cycles can be executed with both NCS and NOE held continuously low.

For an address activated read cycle, chip select must be valid prior to, coincident with, or within (TAVQV minus TSLQV) time following the address edge transition(s). Any amount of toggling or skew between address edge transitions is permissible; however, data outputs will become valid TAVQV time after the latest occurring address edge transition. The minimum address activated read cycle time is TAVAV. When the RAM is operated at the minimum address activated read cycle time, the data outputs will remain valid on the RAM I/O until TAXQX time following the next sequential address transition.

To control a read cycle with NCS, all addresses must be valid at least (TAVQV minus TSLQV) time prior to the enabling NCS edge transition. Address edges can occur later than the (TAVQV minus TSLQV) setup time to NCS; however, this will be interpreted as an address activated read operation and data outputs will not become valid until TAVQV time after the latest occurring address edge transition. Data outputs will enter a high impedance state TSHQZ time following a disabling NCS edge transition.

Write Cycle

The write operation is synchronous with respect to the address bits and is controlled by write enable (NWE) and/or chip select (NCS) edge transitions (refer to Write Cycle I and Write Cycle II timing diagrams). To perform a write operation, both NWE and NCS must be low. Consecutive write cycles can be performed with either NWE or NCS held continuously low. The desired control signal must then transition to a high state between consecutive write operations.

To write data into the RAM, both NWE and NCS must be held low for at least TWLWH/TSLSH time. Any amount of edge skew between the signals can be tolerated, and either one or both control signals can initiate or terminate the write operations, write pulses must be separated by the minimum specified TWHWL/TSHSL time. Address inputs must remain valid during the entire write time. A valid data overlap to end of write time of TDVWH/TDVSH, and an address valid to end of write time of TAVWH/TAVSH must be provided during the write operations. Hold times for address inputs and data inputs with respect to the disabling NWE or NCS edge transition must be a minimum of TWHAX/TSHAX time and TWHDX/TSHDX time, respectively. The minimum write cycle time is TAVAV.

Write cycle timing parameters listed in the Write Cycle AC Electrical Characteristics table reflect an SER performance level 1 x 10^{-7} cell upsets/cell-day. Performance curves illustrating soft error rate (SER) and write time performance trade-offs over the operating temperature range are shown later in the data sheet.

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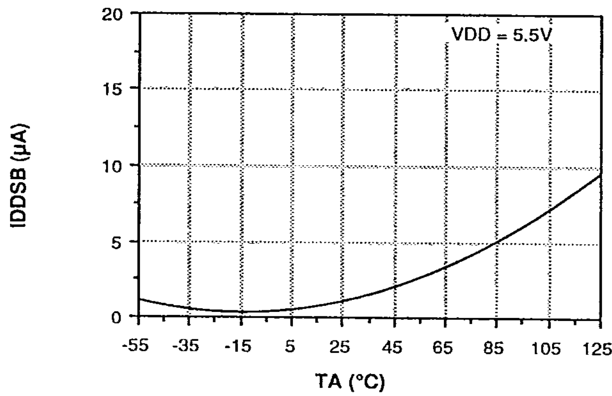
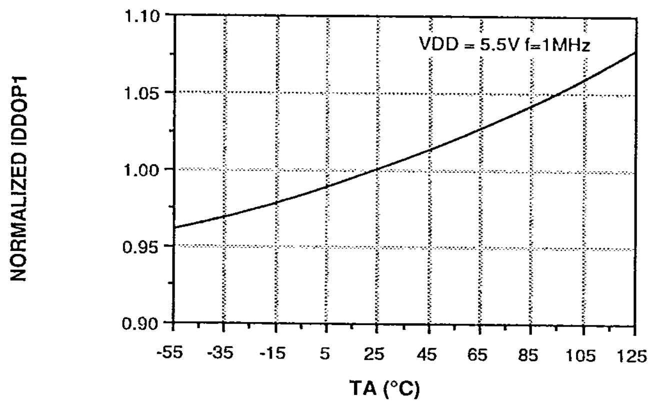
TYPICAL DC AND AC ELECTRICAL PERFORMANCE CHARACTERISTICS

STANDBY CURRENT VS. TEMPERATURE



NORMALIZED OPERATING CURRENT VS. TEMPERATURE



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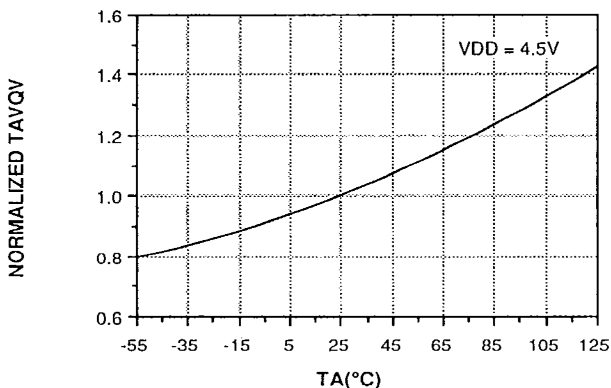
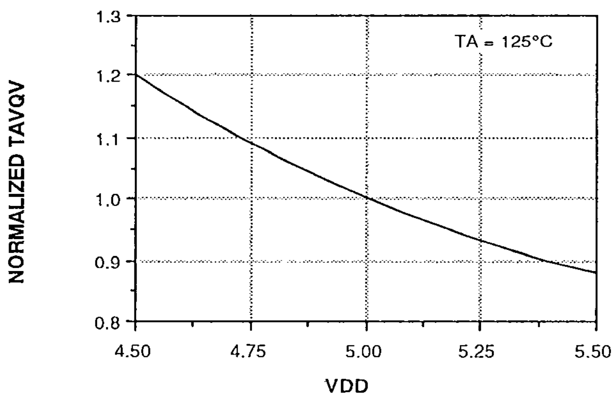
TYPICAL DC AND AC ELECTRICAL PERFORMANCE CHARACTERISTICS

NORMALIZED ACCESS TIME VS. TEMPERATURE



NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



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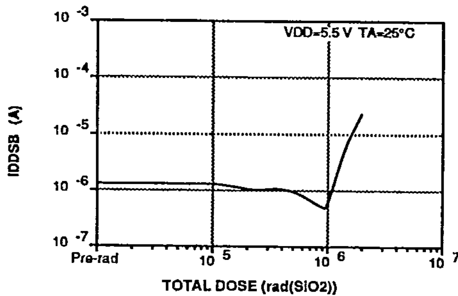
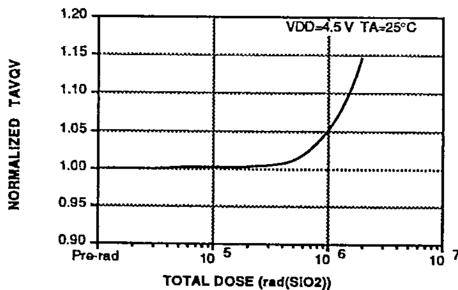
TYPICAL TOTAL DOSE PERFORMANCE CHARACTERISTICS

10 keV X-RAY

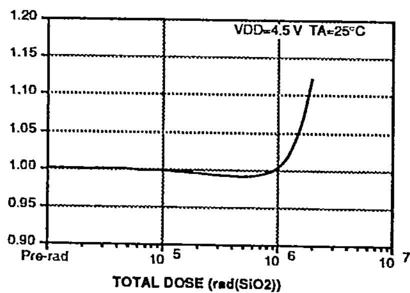
STANDBY CURRENT VS. TOTAL DOSE



NORMALIZED ACCESS TIME VS. TOTAL DOSE

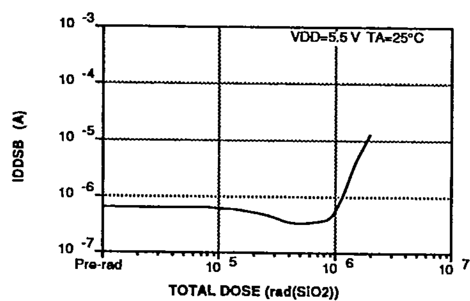


NORMALIZED ADDRESS VALID TO END OF WRITE TIME VS. TOTAL DOSE

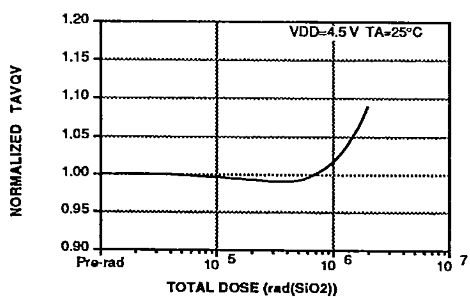


GAMMA RAY (Co^{60})

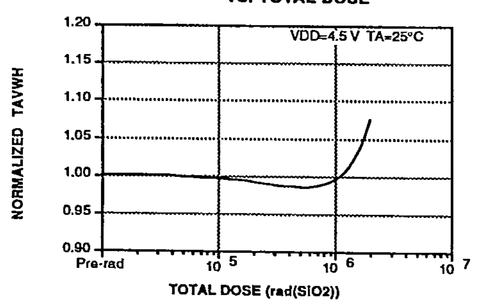
STANDBY CURRENT VS. TOTAL DOSE



NORMALIZED ACCESS TIME VS. TOTAL DOSE



NORMALIZED ADDRESS VALID TO END OF WRITE TIME VS. TOTAL DOSE



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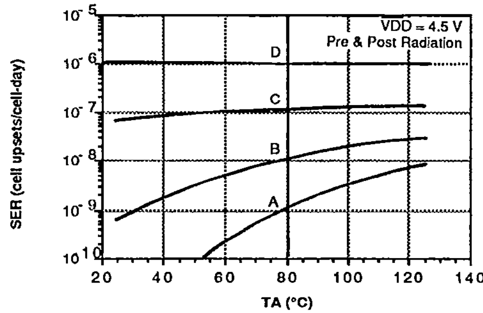
SOFT ERROR RATE AND WRITE TIME PERFORMANCE CHARACTERISTICS

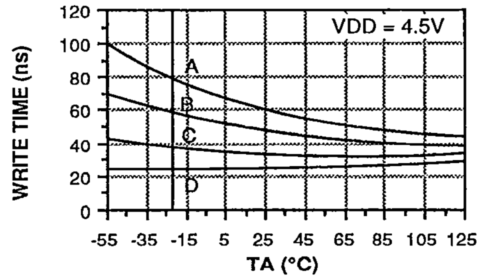
SOFT ERROR RATE VS. TEMPERATURE



WORST CASE SER PERFORMANCE AT 80°C
ADAMS 10% ENVIRONMENT

A: 1×10^{-9} upsets/bit-day
B: 1×10^{-8} upsets/bit-day
C: 1×10^{-7} upsets/bit-day
D: 1×10^{-6} upsets/bit-day

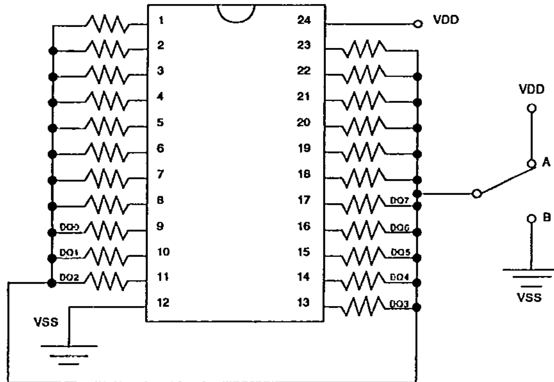
WRITE TIME VS. TEMPERATURE



WORST CASE TIME (TAVWH)
PERFORMANCE AT -20°C

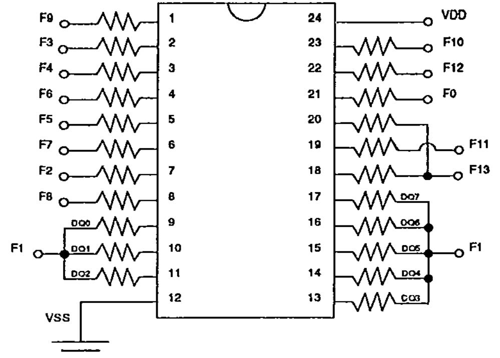
A: 1×10^{-9} upsets/bit-day, 80ns
B: 1×10^{-8} upsets/bit-day, 60ns
C: 1×10^{-7} upsets/bit-day, 38ns
D: 1×10^{-6} upsets/bit-day, 25ns

BURN-IN CIRCUIT



STATIC BURN-IN CIRCUIT

VDD = 5.5 V
Minimum ambient temp = 125°C
All resistors ≤ (10 kΩ ± 10%)



DYNAMIC BURN-IN DIAGRAM

VDD = 5.5 V
Minimum ambient temp = 125°C
All resistors ≤ (10 kΩ ± 10%)
F0 ≥ 100 kHz
F1 = F0/2, F2 = F1/2, ... F13 = F12/2

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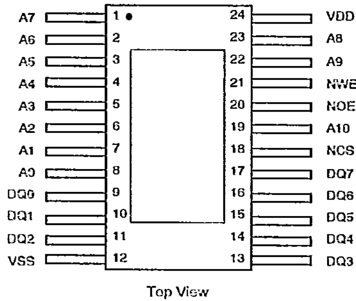
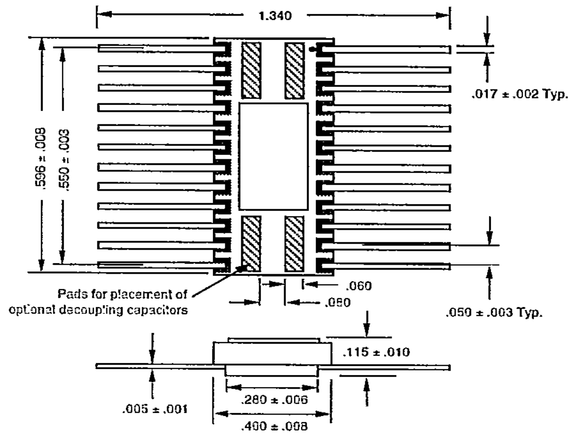
PACKAGE CONFIGURATION

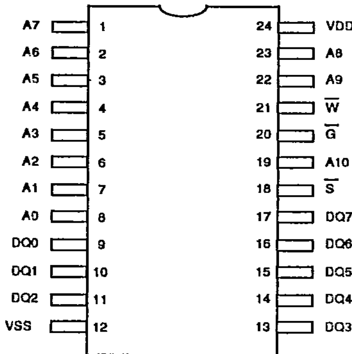
24-LEAD FLAT PACK

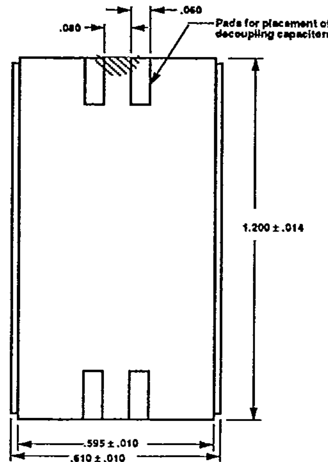
The 2K x 8 SRAM is offered in a custom 24-lead flat pack. This package is constructed of multilayer ceramic (Al_2O_3) and contains internal power and ground planes. Optional capacitors can be mounted onto a ceramic package bottom in special cut-out areas to maximize dose rate hardness and increase component density. The capacitors attach directly to the internal package power and ground planes. This design minimizes resistance and inductance of the bond wire and package, both of which are critical in a transient radiation environment.



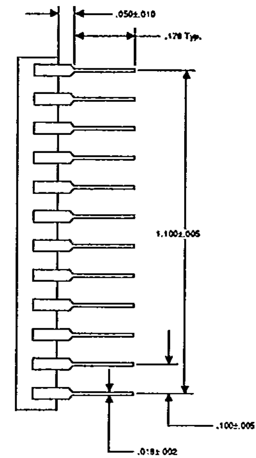


24-LEAD DIP





UNDERSIDE OF PACKAGE



NWE = $\overline{W}$ = Write Enable
NOE = $\overline{G}$ = Output Enable
NCS = $\overline{S}$ = Chip Select

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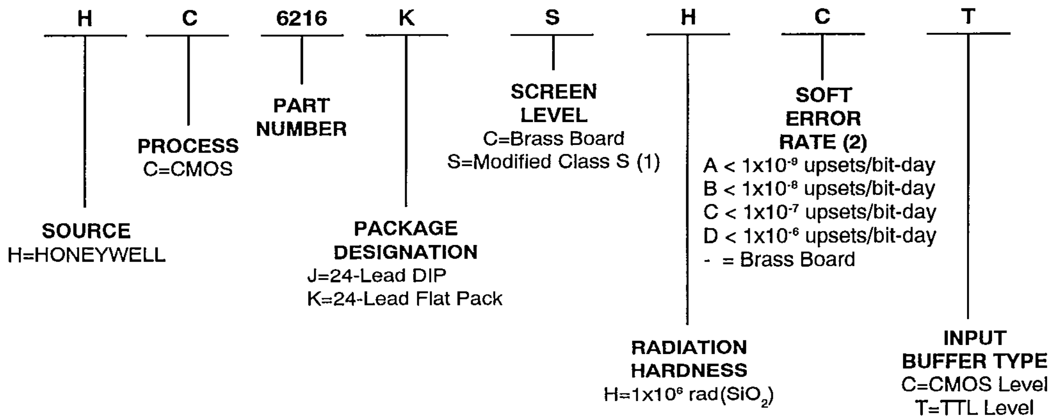
ORDERING INFORMATION



(1) Refer to Assembly and Screening Procedure section for Honeywell's screening procedures.
(2) Soft error rate specifications indicate worst case, high temperature (80°C), post-total dose performance. Note that SER performance trades off with write time performance over the operating temperature range. Performance curves illustrating this trade-off are shown earlier in this data sheet.
(3) The Write Cycle timing parameters for SEE levels A, B, D, and Z are not included in this data sheet. Contact Honeywell for further information on additional SER and write time pairings.

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