512MB – 2x32Mx72 SDRAM, UNBUFFERED, w/PLL

FEATURES

- PC100 and PC133
- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3V ± 0.3V Power Supply
- Dual Rank
- 144 Pin SO-DIMM JEDEC
  - PCB: 31.75mm (1.25")

DESCRIPTION

The WV3DG7266V is a 2x32Mx72 synchronous DRAM module which consists of nine stacked 64Mx8 with 4 banks SDRAM components in TSOP II package, and one 2Kb EEPROM for Serial Presence Detect which are mounted on a 144 pin SO-DIMM multilayer FR4 Substrate.

* This product is under development, is not qualified or characterized and is subject to change without notice.

NOTE: Consult factory for availability of:
- RoHS compliant products
- Vendor source control options
- Industrial temperature option

PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

PINOUT											
PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	Vss	2	Vss	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	Vcc	102	Vcc
7	DQ2	8	DQ34	55	Vss	56	Vss	103	A6	104	A7
9	DQ3	10	DQ35	57	CB0	58	CB4	105	A8	106	BA0
11	Vcc	12	Vcc	59	CB1	60	CB5	107	Vss	108	Vss
13	DQ4	14	DQ36	61	CLK0	62	CKE0	109	A9	110	BA1
15	DQ5	16	DQ37	63	Vcc	64	Vcc	111	A10	112	A11
17	DQ6	18	DQ38	65	RAS#	66	CAS#	113	Vcc	114	Vcc
19	DQ7	20	DQ39	67	WE#	68	CKE1	115	DQM2	116	DQM6
21	Vss	22	Vss	69	CS0#	70	A12	117	DQM3	118	DQM7
23	DQM0	24	DQM4	71	CS1#*	72	NC	119	Vss	120	Vss
25	DQM1	26	DQM5	73	NC	74	CLK1	121	DQ24	122	DQ56
27	Vcc	28	Vcc	75	Vss	76	Vss	123	DQ25	124	DQ57
29	A0	30	A3	77	CB2	78	CB6	125	DQ26	126	DQ58
31	A1	32	A4	79	CB3	80	CB7	127	DQ27	128	DQ59
33	A2	34	A5	81	Vcc	82	Vcc	129	Vcc	130	Vcc
35	Vss	36	Vss	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	Vss	92	Vss	139	Vss	140	Vss
45	Vcc	46	Vcc	93	DQ20	94	DQ52	141	SDA	142	SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	Vcc	144	Vcc

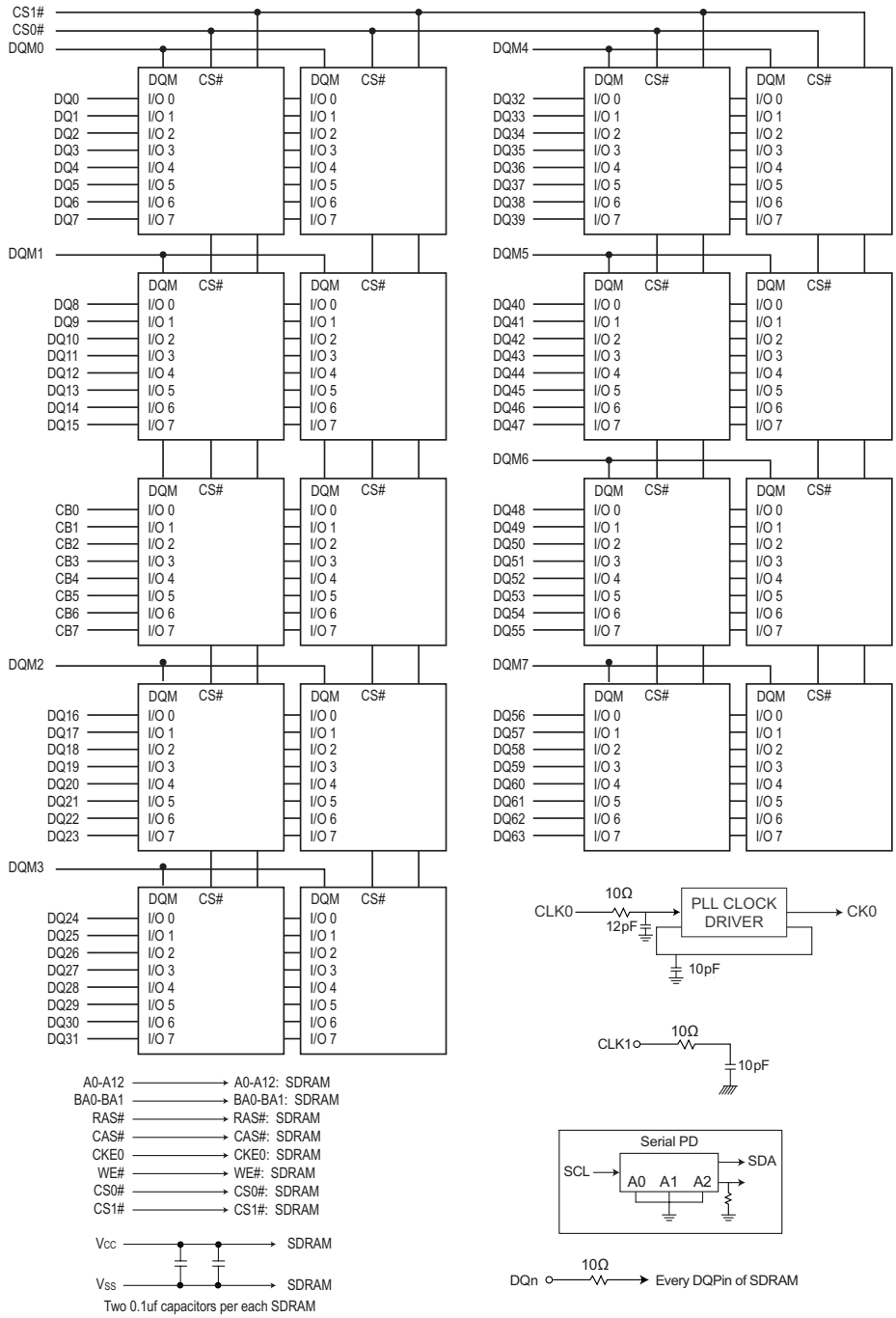
PIN NAMES

A0 – A12	Address Input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CLK0, CLK1	Clock Input
CB0-7	Check Bit (Data-In/Data-Out)
CKE0	Clock Enable Input
CS0#, CS1#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	#Write Enable
DQM0-7	DQM
Vcc	Power Supply (3.3V)
Vss	Ground
SDA	Serial Data I/O
SCL	Serial Clock
DNU	Do Not Use
NC	No Connect

* These pins are not used in this module

** These pins should be NC in the system which does not support SPD.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}, V_{CCQ}	-1.0 ~ 4.6	V
Storage Temperature	T_{STG}	-55 ~ +150	°C
Power Dissipation	P_D	18	W
Short Circuit Current	I_{OS}	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

Voltage Referenced to: V_{SS} = 0V, 0°C ≤ T_A ≤ +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	V_{CCQ} +0.3	V	1
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	2
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH}= -2mA
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL}= -2mA
Input Leakage Current	I_{LI}	-10	—	10	µA	3

Notes:
1. V_{IH} (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{CCQ}
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

T_A = 25°C, f = 1MHz, V_{CC} = 3.3V, V_{REF} = 1.4V ± 200mV

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C_{IN1}	95	pF
Input Capacitance (RAS#,CAS#,WE#)	C_{IN2}	95	pF
Input Capacitance (CKE0)	C_{IN3}	95	pF
Input Capacitance (CLK0)	C_{IN4}	18	pF
Input Capacitance (CS0#, CS1#)	C_{IN5}	50	pF
Input Capacitance (DQM0-DQM7)	C_{IN6}	10	pF
Input Capacitance (BA0-BA1)	C_{IN7}	95	pF
Data Input/Output Capacitance (DQ0-DQ63)	C_{OUT}	16	pF
Data Input/Output Capacitance (CB0-7)	C_{OUT1}	16	pF

OPERATING CURRENT CHARACTERISTICS

(V_{CC} = 3.3V, T_A = 0°C ≤ +70°C)

Parameter	Symbol	Conditions	Value			Units	Note
			7	75	10		
Operating current (One bank active)	I_{CC1}	Burst Length = 1 $t_{RC} \geq t_{RC}$ (min) I_O = 0mA	1170	1080	1080	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	36			mA	3
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	36				
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), CS# ≥ V_{IH}(min), tcc =10ns Input signals are charged one time during 20ns	360			mA	3
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≥V_{IL}(max), t_{CC} = ∞ Input signals are stable	180				
Active standby current in power-down mode	I_{CC3P}	CKE ≥ V_{IL}(max), t_{CC} = 10ns	108			mA	3
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	108				
Active Standby Current in Non-Power Down Mode	I_{CC3N}	CKE ≥ V_{IH}(min), CS# ≥ V_{IH}(min), tcc = 10ns Input signals are changed one time during 20ns	540			mA	3
	I_{CC3NS}	CKE ≤ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable	450			mA	3
Operating Current (Burst mode)	I_{CC4}	Io = mA Page burst 4 Banks activated t_{CCD} = 2CLK	1260	1260	1170	mA	1
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	2250	2070	1980	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	54			mA	3

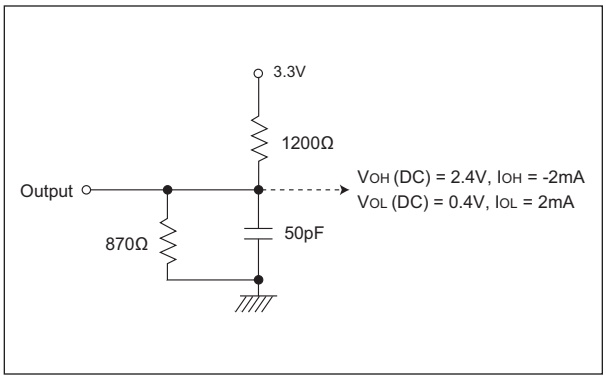
Notes:
1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 3 Drive ICs.

AC OPERATING TEST CONDITIONS

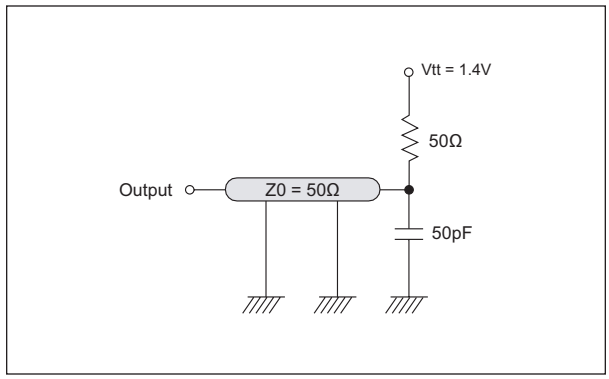
V_{CC} = 3.3v, 0°C - 70°C

Parameter	Value	Unit
AC input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	t_R/t_F = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	

DC OUTPUT LOAD CIRCUIT



AC OUTPUT LOAD CIRCUIT



OPERATING AC PARAMETER

Parameter		Symbol	Version			Unit	Note
			7	75	10		
Row active to row active delay		$t_{RRD(min)}$	15	15	20	ns	1
RAS# to CAS# delay		$t_{RCD(min)}$	15	20	20	ns	1
Row precharge time		$t_{RP(min)}$	15	20	20	ns	1
Row active time		$t_{RAS(min)}$	45	45	50	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time		$t_{RC(min)}$	60	65	70	ns	1
Last data in to row precharge		$t_{RDL(min)}$	2			CLK	2
Last data in to Active delay		$t_{DAL(min)}$	2 CLK + tRP			—	
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Notes:

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

OPERATING AC PARAMETERS

Parameter		Symbol	7		75		10		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	7.5	1000	7.5	1000	10	1000	ns	1
	CAS latency=2		7.5		10		10			
CLK to valid output delay	CAS latency=3	t_{SAC}		5.4		5.4		6	ns	1, 2
	CAS latency=2			5.4		6		6		
Output data hold time	CAS latency=3	t_{OH}	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		t_{CH}	2.5		2.5		3		ns	3
CLK low pulse width		t_{CL}	2.5		2.5		3		ns	3
Input setup time		t_{SS}	1.5		1.5		2		ns	3
Input hold time		t_{SH}	0.8		0.8		1		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1		1		ns	2
CLK to outpu in Hi-Z	CAS latency=3	t_{SHZ}		5.4		5.4		6	ns	
	CAS latency=2			5.4		6		6		

Notes :

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

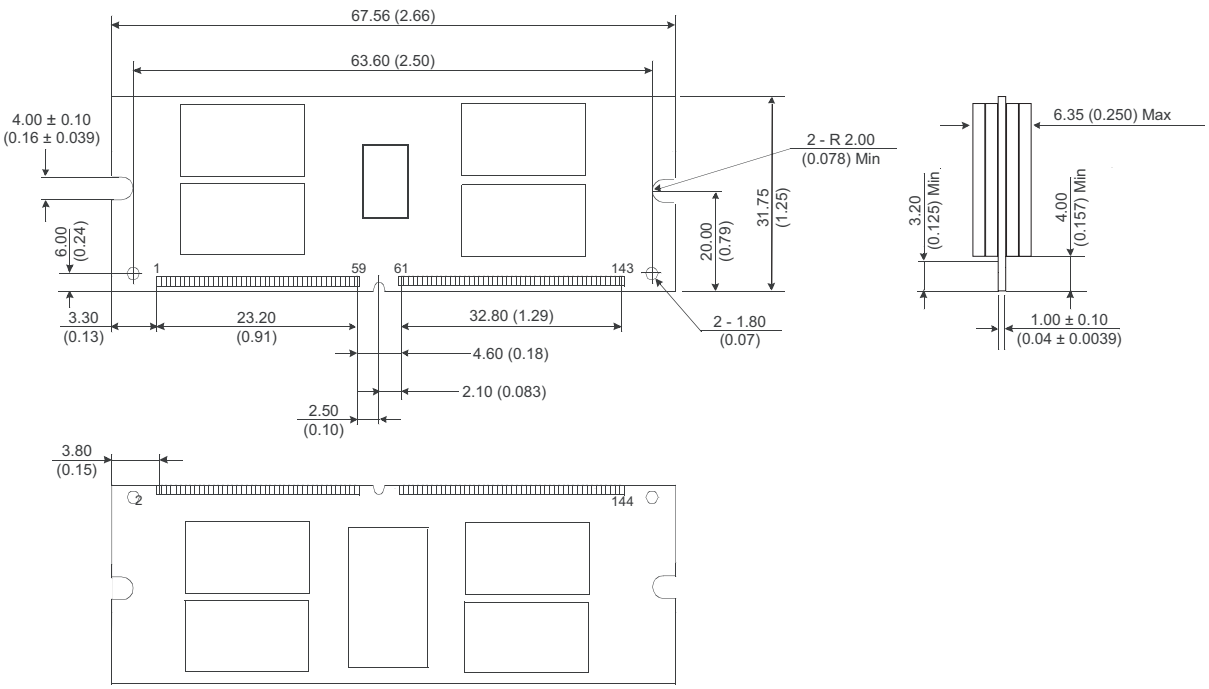
PACKAGE DIMENSIONS FOR D1

Ordering Information	Speed	CAS Latency	Height*
WV3DG7266V10D1	100MHz	CL=2	31.75 (1.250")
WV3DG7266V7D1	133MHz	CL=2	31.75 (1.250")
WV3DG7266V75D1	133MHz	CL=3	31.75 (1.250")

NOTES:

- Consult Factory for availability of Lead-Free products. (F = Lead-Free, G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D1



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES).

Document Title

512MB – 2x32Mx72 SDRAM UNBUFFERED, w/PLL

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	4-05	Preliminary
Rev 1	1.1 Update functional block diagram	8-05	Preliminary