

## 2Mx32 SRAM 3.3V MULTI-CHIP PACKAGE

### FEATURES

- Access Times of 12, 15, 17, 20ns
- Packaging
  - 255 PBGA, 25mm x 25mm, 625mm<sup>2</sup>
- Organized as 2Mx32
- Commercial, Industrial and Military Temperature Ranges
- Low Voltage Operation:
  - 3.3V ± 10% Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Fully Static Operation:
  - No clock or refresh required.
- Three State Output.

\* This product is subject to change without notice.

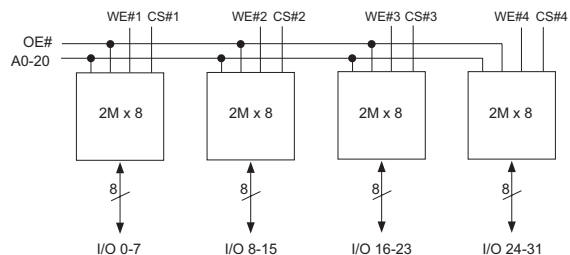
### PIN CONFIGURATION FOR W82M32V-XBX TOP VIEW

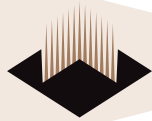
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A		NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	
B	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	
C	NC	NC	NC	A2	A1	A0	GND	GND	V <sub>cc</sub>	V <sub>cc</sub>	A18	A17	A16	GND	NC	NC	
D	NC	NC	CS#2	A3	A4	D14	D15	NC	CS#4	D24	D25	OE#	A15	NC	NC	NC	
E	NC	NC	D9	D8	A19	D12	D13	GND	V <sub>cc</sub>	D26	D27	WE#4	D31	D30	NC	NC	
F	NC	NC	D10	D11	GND	GND	GND	GND	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	D28	D29	NC	NC	
G	NC	NC	WE#2	GND	GND	GND	GND	GND	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	NC	NC	NC
H	NC	NC	GND	GND	GND	GND	GND	GND	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	NC	NC	NC
J	NC	NC	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	GND	GND	GND	GND	GND	GND	NC	NC	NC
K	NC	NC	CS#1	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	GND	GND	GND	GND	GND	GND	NC	NC	NC
L	NC	NC	D1	D0	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	GND	GND	GND	GND	D23	D22	NC	NC	NC
M	NC	NC	D2	D3	A20	D7	D5	V <sub>cc</sub>	GND	D17	D16	CS#3	D20	D21	NC	NC	NC
N	NC	NC	WE#1	A6	A5	D6	D4	NC	WE#3	D19	D18	A14	A13	NC	NC	NC	NC
P	NC	NC	GND	A7	A8	A9	V <sub>cc</sub>	V <sub>cc</sub>	GND	GND	A10	A11	A12	V <sub>cc</sub>	NC	NC	NC
R	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
T	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

### PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-20	Address Inputs
WE#1-4	Write Enables
CS#1-4	Chip Selects
OE#	Output Enable
V <sub>cc</sub>	Power Supply
GND	Ground
NC	Not Connected

### BLOCK DIAGRAM





**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.5	4.6	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	4.6	V

**TRUTH TABLE**

CS#	OE#	WE#	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	3.0	3.6	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	+0.8	V

**CAPACITANCE**

(T<sub>A</sub> = +25°C)

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	30	pF
WE#1-4 capacitance	C <sub>WE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	10	pF
CS#1-4 capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	10	pF
Data I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V, f = 1.0 MHz	10	pF
Address input capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	30	pF

*This parameter is guaranteed by design but not tested.*

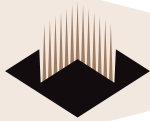
**DC CHARACTERISTICS**

(V<sub>CC</sub> = 3.3V ± 0.3V, -55°C ≤ T<sub>A</sub> ≤ 125°C)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>CC</sub>		10	µA
Output Leakage Current	I <sub>LO</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10	µA
Operating Supply Current (x 32 Mode)	I <sub>CC</sub> x 32	CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 3.6V		1100	mA
Standby Current	I <sub>SB</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 3.6V		400	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA	2.4		V

NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V.

NOTE: Contact factory for low power option.



**AC CHARACTERISTICS**

(V<sub>CC</sub> = 3.3V, -55°C ≤ TA ≤ +125°C)

Parameter Read Cycle	Symbol	-12		-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	12		15		17		20		ns
Address Access Time	t <sub>AA</sub>		12		15		17		20	ns
Output Hold from Address Change	t <sub>OH</sub>	3		3		3		3		ns
Chip Select Access Time	t <sub>ACS</sub>		12		15		17		20	ns
Output Enable to Output Valid	t <sub>OE</sub>		7		8		8		10	ns
Chip Select to Output in Low Z	t <sub>CLZ</sub> <sup>1</sup>	3		3		3		3		ns
Output Enable to Output in Low Z	t <sub>OLZ</sub> <sup>1</sup>	1		1		1		1		ns
Chip Disable to Output in High Z	t <sub>CHZ</sub> <sup>1</sup>		7		8		8		10	ns
Output Disable to Output in High Z	t <sub>OHZ</sub> <sup>1</sup>		7		8		8		10	ns.

1. This parameter is guaranteed by design but not tested

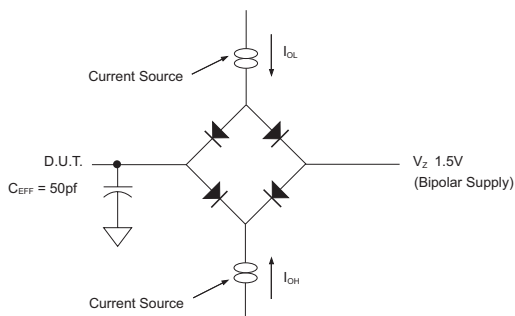
**AC CHARACTERISTICS**

(V<sub>CC</sub> = 3.3V, -55°C ≤ TA ≤ +125°C)

Parameter Write Cycle	Symbol	-12		-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	12		15		17		20		ns
Chip Select to End of Write	t <sub>CW</sub>	10		12		12		14		ns
Address Valid to End of Write	t <sub>AW</sub>	10		12		12		14		ns
Data Valid to End of Write	t <sub>DW</sub>	8		9		9		10		ns
Write Pulse Width	t <sub>WP</sub>	10		12		14		14		ns
Address Setup Time	t <sub>AS</sub>	0		0		0		0		ns
Address Hold Time	t <sub>AH</sub>	0		0		0		0		ns
Output Active from End of Write	t <sub>OW</sub> <sup>1</sup>	2		2		3		3		ns
Write Enable to Output in High Z	t <sub>WHZ</sub> <sup>1</sup>		7		8		8		9	ns
Data Hold Time	t <sub>DH</sub>	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested

**AC TEST CIRCUIT**



**AC TEST CONDITIONS**

Parameter	Typ	Unit
Input Pulse Levels	V <sub>IL</sub> = 0, V <sub>IH</sub> = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:

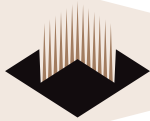
V<sub>Z</sub> is programmable from -2V to +7V.

I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.

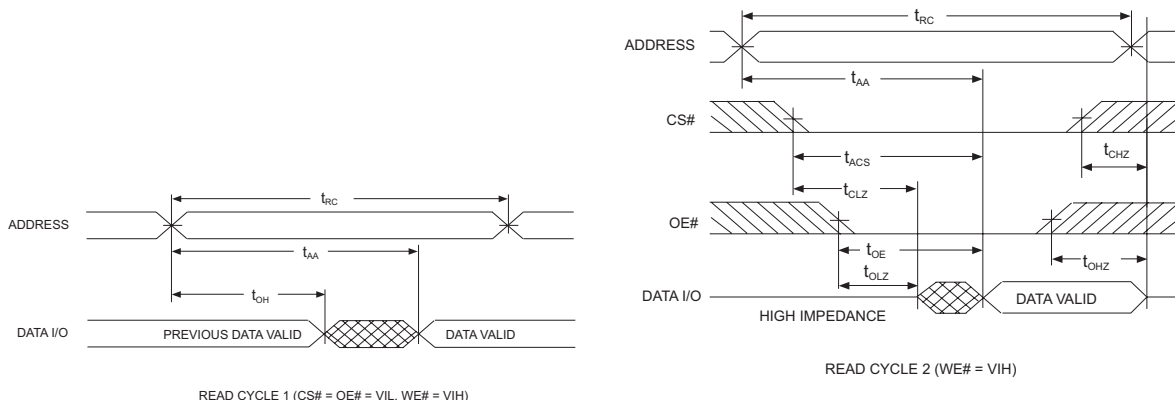
Tester Impedance Z<sub>0</sub> = 75 W.

V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.

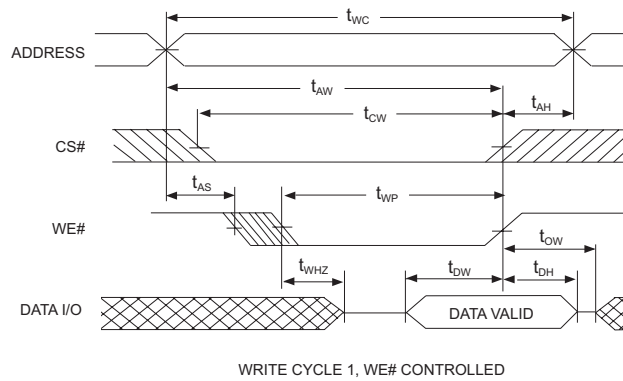
I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit. ATE tester includes jig capacitance.



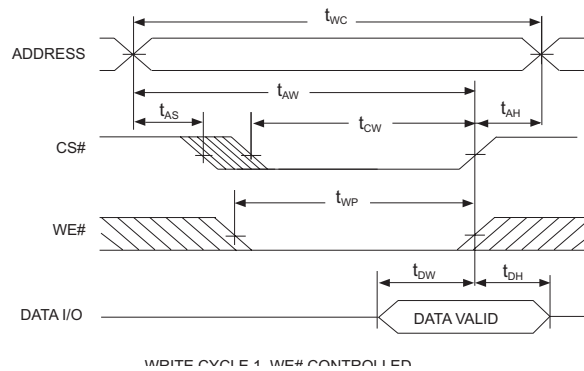
**TIMING WAVEFORM - READ CYCLE**

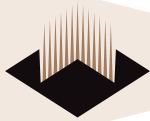


**WRITE CYCLE - WE# CONTROLLED**

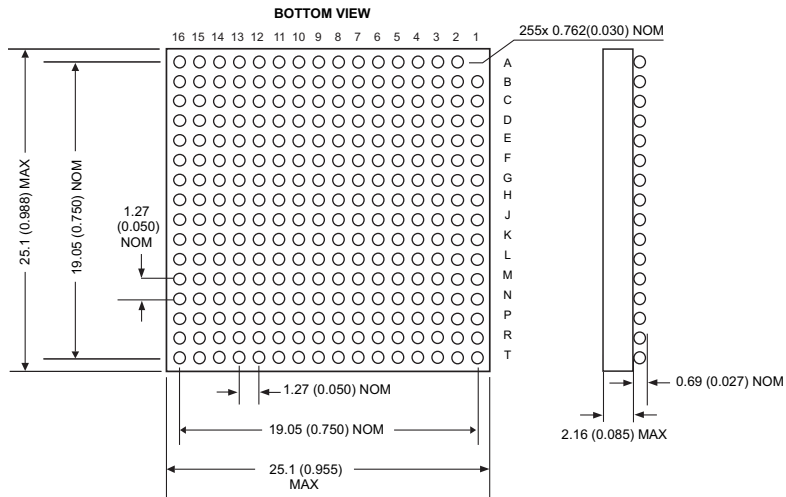


**WRITE CYCLE - CS# CONTROLLED**

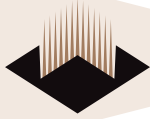




**PACKAGE 781: 255 BALL GRID ARRAY**

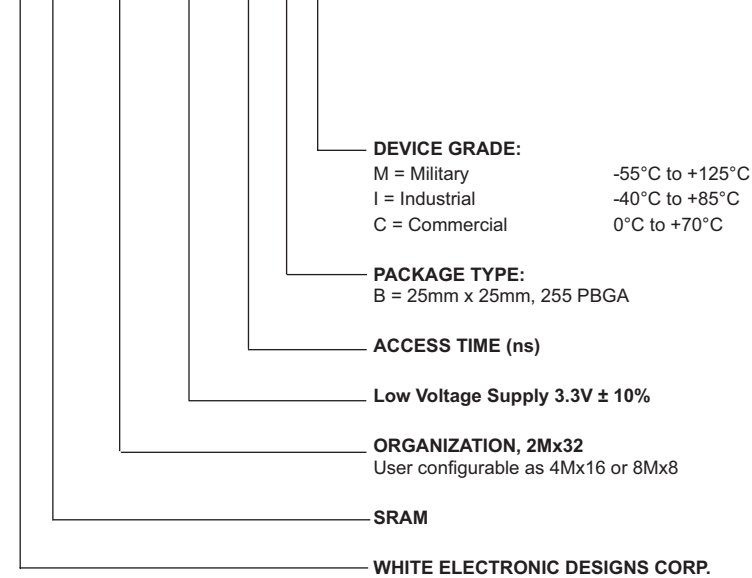


ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



**ORDERING INFORMATION**

**W 8 2M 32 V - XX X X**



**Document Title**

2M x 32 Asynchronous SRAM

**Revision History**

<b><u>Rev #</u></b>	<b><u>History</u></b>	<b><u>Release Date</u></b>	<b><u>Status</u></b>
Rev 0	Initial Release	July 2002	Advanced
Rev 1	Changes 1.1 Add AC/DC Electricals & Timing Diagrams (Pg. 1-7) 1.2 Change Pinout to full 255 (16x16) array 1.3 Change Package Dimension to full 255 (16x16) array	October 2002	Advanced
Rev 2	Changes (Pg.1,5,6,7) 2.1 Change package dimension from 27mm square to 25mm square 2.2 Change package height from 2.20mm to 2.70mm Max	May 2002	Advanced
Rev 3	Changes (Pg.1,5,7) 3.1 Change package mechanical drawing to new format.	November 2003	Advanced
Rev 4	Changes (Pg.1,7) 4.1 Change status to preliminary.	May 2004	Preliminary
Rev 5	Changes (Pg. 1, 7) 5.1 Change status to Final	April 2006	Final