MOTOROLA

MCM6605A

2

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM6605A is a 4096-bit high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 4096 one-bit words, these memories are fabricated using selective oxidation N-channel silicon gate technology to optimize device speed, power and density tradeoffs.

All address and control inputs are TTL compatible except for a single high-level clock (Chip Enable). Complete address decoding is done on chip and address latches are incorporated for ease of use. Refresh of the entire memory can be accomplished by sequentially cycling through addresses A0-A4 (32 cycles) a maximum of every 2.0 milliseconds.

The MCM6605A uses a three-transistor memory cell to simplify internal sense amplifier requirements. Output data is inverted with respect to input data. The outputs are 3-state TTL configuration and require no external sense amplifier. Outputs are in the high impedance (floating) state when either the Chip Enable is in the low state or the $\overline{\text{Chip Select}}$ is in the high state.

- Organized as 4096 Words of 1 Bit

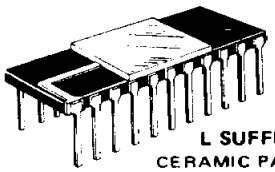
	L1, P1	L2,P2	L, P
• Maximum Access Time =	150 ns	200 ns	300 ns
• Minimum Read Cycle Time =	290 ns	360 ns	470 ns
• Minimum Write Cycle Time =	390 ns	490 ns	590 ns
• Minimum Read Modify Write Cycle Time =	390 ns	490 ns	590 ns

- Low Power Dissipation
  335 mW Typical (Active)
  2.6 mW Typical (Standby with Refresh)
- Easy Refresh – Only 32 Cycles Every 2.0 ms
- TTL Compatible
- 3-State Output
- Address Latches On Chip
- Power Supply Pins on Package Corners for Layout Simplification
- Typical Applications:
  Main Memory
  Buffer Memory
  Peripheral Storage

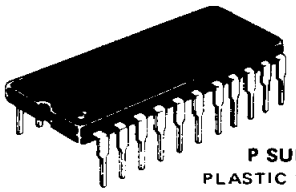
MOS

(N-CHANNEL, SILICON-GATE)

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

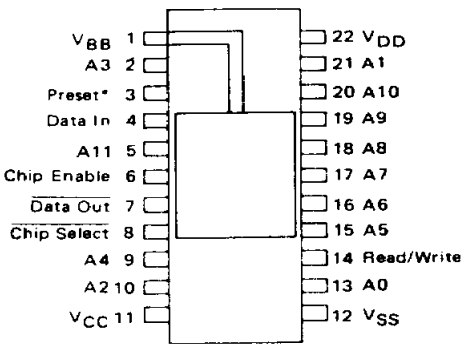


L SUFFIX
CERAMIC PACKAGE
CASE 677



P SUFFIX
PLASTIC PACKAGE
CASE 708

PIN ASSIGNMENT



*See Applications Information

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}	V_{in}, V_{out}	-0.3 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{DD}	11.4	12	12.6	Vdc
	V_{CC}	4.5	5.0	5.5	Vdc
	V_{SS}	0	0	0	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Logic Levels Input High Voltage (A_n, D_{in}, R/W, $\overline{CS}$)	V_{IH}	3.0	–	V_{DD} + 0.6	Vdc
Input Low Voltage (A_n, D_{in}, R/W, $\overline{CS}$)	V_{IL}	-1.0	–	0.8	Vdc
Chip Enable High Voltage	V_{CEH}	V_{DD} - 0.6	–	V_{DD} + 0.6	Vdc
Chip Enable Low Voltage	V_{CEL}	-1.0	–	0.8	Vdc

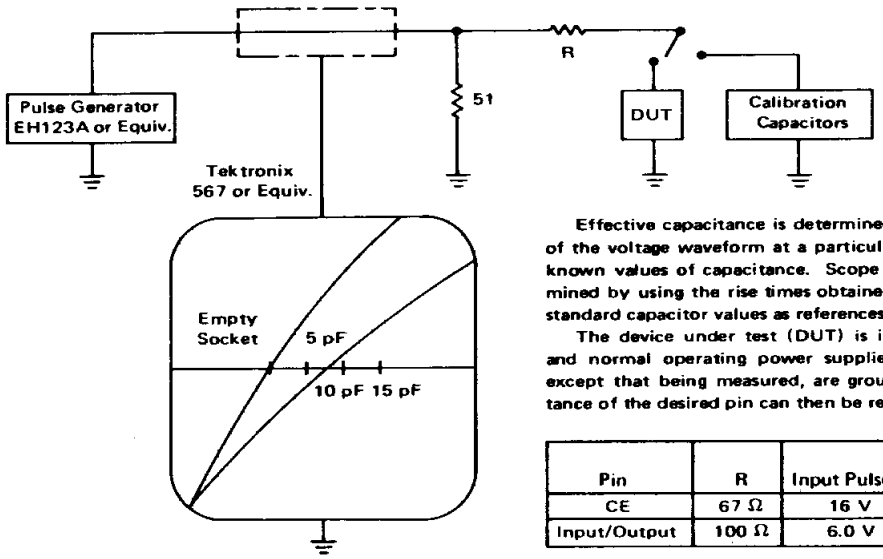
DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (A_n, D_{in}, R/W, $\overline{CS}$, Preset) (V_{in} = 0 to V_{DD} + 1.0 V)	I_{in}	–	–	10	μA
Input Chip Enable Current (V_{in} = 0 to V_{DD} + 1.0 V)	I_{ICE}	–	–	10	μA
Output High Voltage (I_O = -100 μA)	V_{OH}	2.4	-	V_{CC}	Vdc
Output Low Voltage (I_O = 2.0 mA)	V_{OL}	V_{SS}	–	0.45	Vdc
Output Leakage Current (V_O = 0.45 V to V_{CC}, CE = V_{CEL}, or $\overline{CS}$ = V_{IH})	I_{LO}	–	–	10	μA
Average Supply Current, Active Mode ($T_{cyc(W)}$ = min)	I_{DDA}	–	28	36	mA
	I_{CCA}	–	0.05	1.0	mA
	I_{BBA}	–	–	100	μA
Supply Current, Standby Mode (CE = 0.45 V)	I_{DDS}	–	1.0	20	μA
	I_{CCS}	–	-	10	μA
	I_{BBS}	–	1.0	20	μA

EFFECTIVE CAPACITANCE (Test Circuit of Figure 1, full operating voltage and temperature range, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance (A_n, D_{in}, R/W, $\overline{CS}$, Preset)	$C_{in(EFF)}$	–	4.0	5.0	pF
Chip Enable Capacitance	$C_{CE(EFF)}$	-	25	30	pF
Output Capacitance	$C_{out(EFF)}$	-	4.0	5.0	pF

FIGURE 1 – MEASUREMENT OF EFFECTIVE CAPACITANCE



Effective capacitance is determined by comparing the rise time of the voltage waveform at a particular pin to that measured with known values of capacitance. Scope calibration points are determined by using the rise times obtained with the empty socket and standard capacitor values as references.

The device under test (DUT) is inserted into the test socket and normal operating power supplies applied. All input pins, except that being measured, are grounded. The effective capacitance of the desired pin can then be read directly from the scope.

Pin	R	Input Pulse	Measurement Level
CE	67 Ω	16 V	12 V
Input/Output	100 Ω	6.0 V	4.0 V

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

OPERATING MODES

Mode	Control States		Output
	R/W	$\overline{CS}$	
Active (CE = High)			
Read Only	H	L	Valid
Read/Write	H → L	L	Valid
Write Only	L	L	Valid
Read Refresh	H → L	L → H	Valid → Floating
Refresh Only	L	H	Floating
Chip Disable (Unselected)	H	H	Floating
Standby (CE = Low)	X	X	Floating

X = Don't Care

RECOMMENDED AC OPERATING CONDITIONS (Read, Write, and Read Modify Write Cycles)

Parameter		Symbol	Min	Max	Unit
Address Setup Time		t_{AS}	0	–	ns
Address Hold Time		t_{AH}	60	–	ns
CE Pulse Transition Time		t_T	10	100	ns
CE Off Time	MCM6605AL,P/L2,P2	t_{SB}	120	–	ns
	MCM6605AL1,P1		90	–	
Chip Select Delay Time		t_{CSD}	–	70	ns
Chip Select Hold Time		t_{CSH}	0	–	ns
Read Write Delay Time		t_{RWD}	–	70	ns
Read Write Hold Time		t_{RWH}	0	–	ns
Time Between Refresh		t_{REF}	–	2.0	ms

AC CHARACTERISTICS

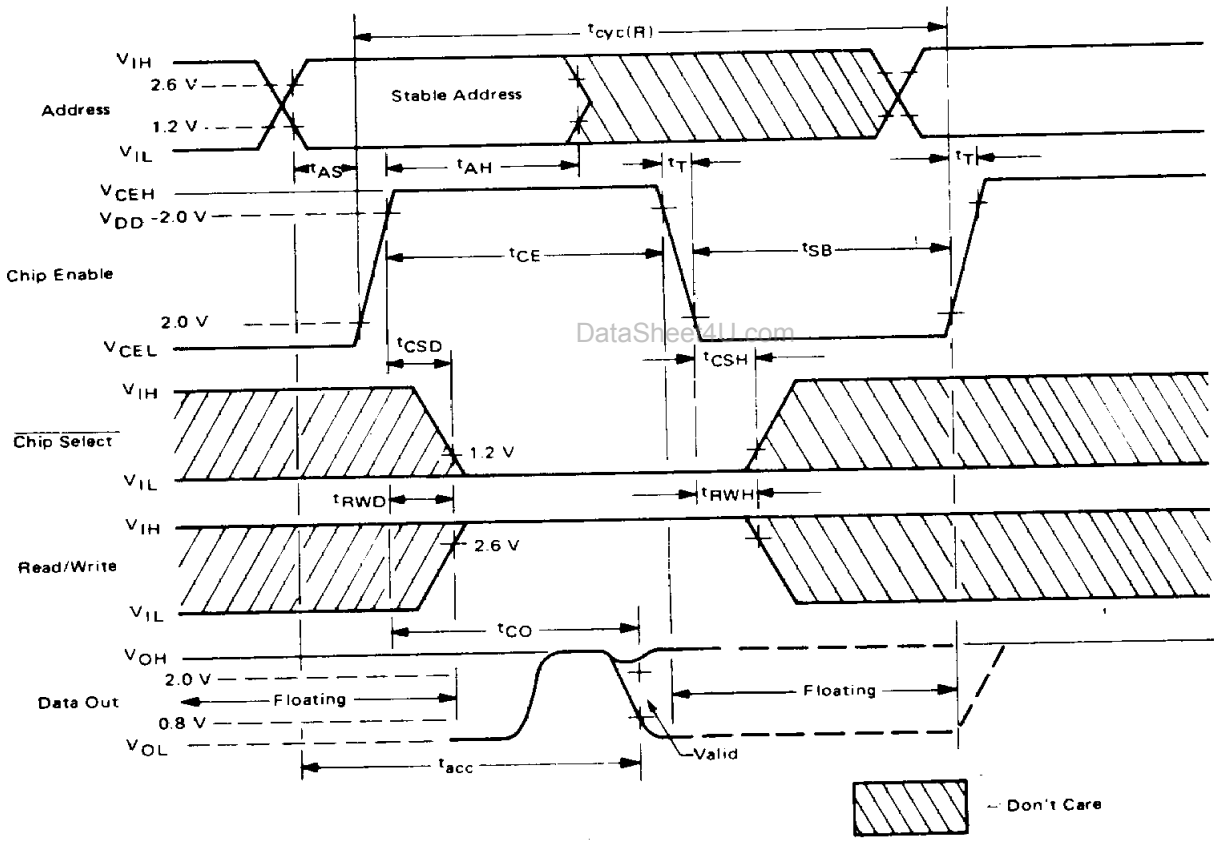
[All timing with t_T = 20 ns; Load = 1 TTL Gate (MC74H00 Series), C_L = 50 pF (effective)]

READ CYCLE (R/W = V_{IH}, $\overline{CS}$ = V_{IL})

Characteristic	Symbol	MCM6605AL,P		MCM6605AL1,P1		MCM6605AL2,P2		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	$t_{cyc(R)}$	470	–	290	–	360	–	ns
Chip Enable On Time	t_{CE}	310	2000	160	2000	200	2000	ns
Chip Enable to Output Delay	t_{CO}	–	280	–	130	–	180	ns
Read Access Time	t_{acc}	–	300	–	150	–	200	ns

2

READ CYCLE TIMING

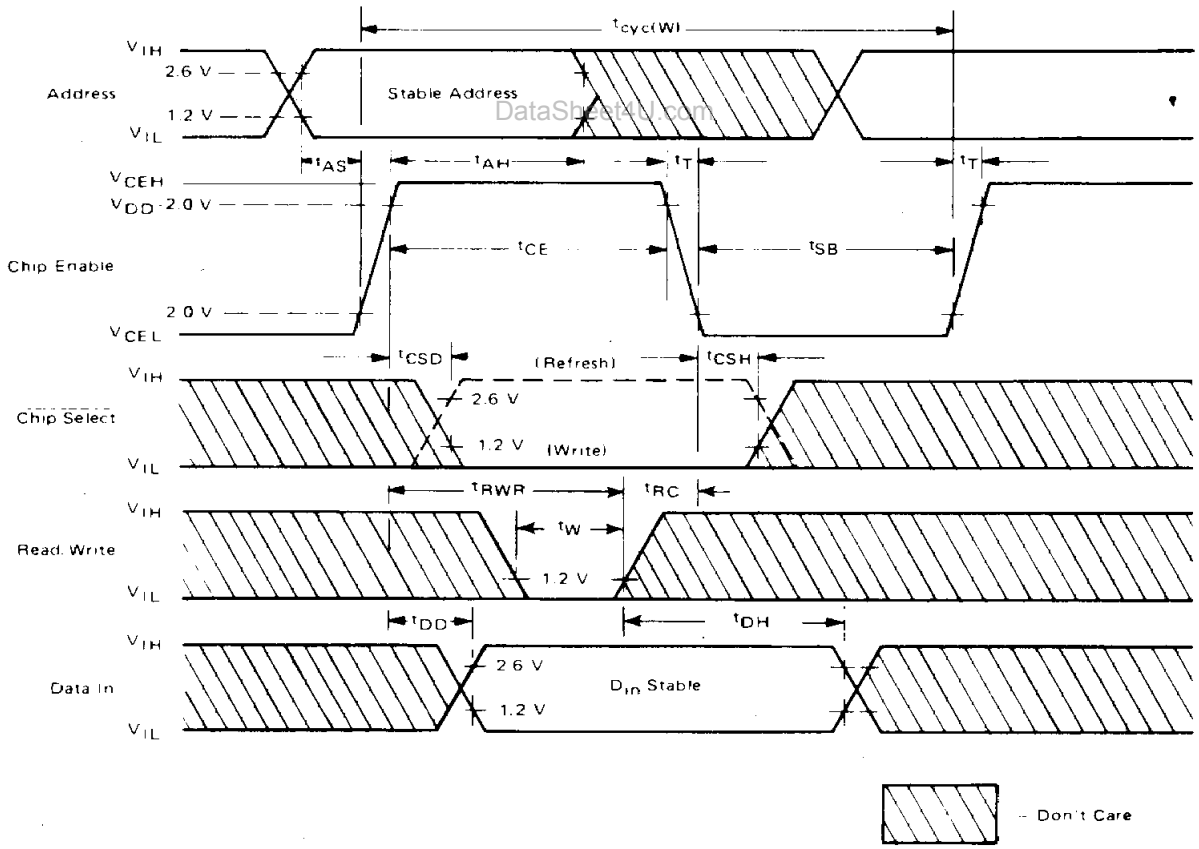


WRITE CYCLE (R/W = V_{IL}, $\overline{CS}$ = V_{IL})
REFRESH CYCLE (R/W = V_{IL}, $\overline{CS}$ = V_{IH})

Characteristic	Symbol	MCM6605AL,P		MCM6605AL1,P1		MCM6605AL2,P2		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	$t_{cyc(W)}$	590	–	390	–	490	–	ns
Chip Enable On Time	t_{CE}	430	2000	260	2000	330	2000	ns
Read-Write Release Time	t_{RWR}	410	2000	240	2000	310	2000	ns
Write Pulse Width	t_W	210	–	160	–	160	–	ns
Read-Write to Chip Enable Separation Time	t_{RC}	0	–	0	–	0	–	ns
Data Delay Time*	t_{DD}	–	70	–	70	–	70	ns
Data Hold Time	t_{DH}	50	–	20	–	50	–	ns

*If a write pulse (t_W) is employed on the R/W line during a write cycle, then the input data setup time is measured from the leading edge of the write pulse. The t_{DS} time is the same as that of the read-modify-write cycle.

WRITE AND REFRESH CYCLE TIMING

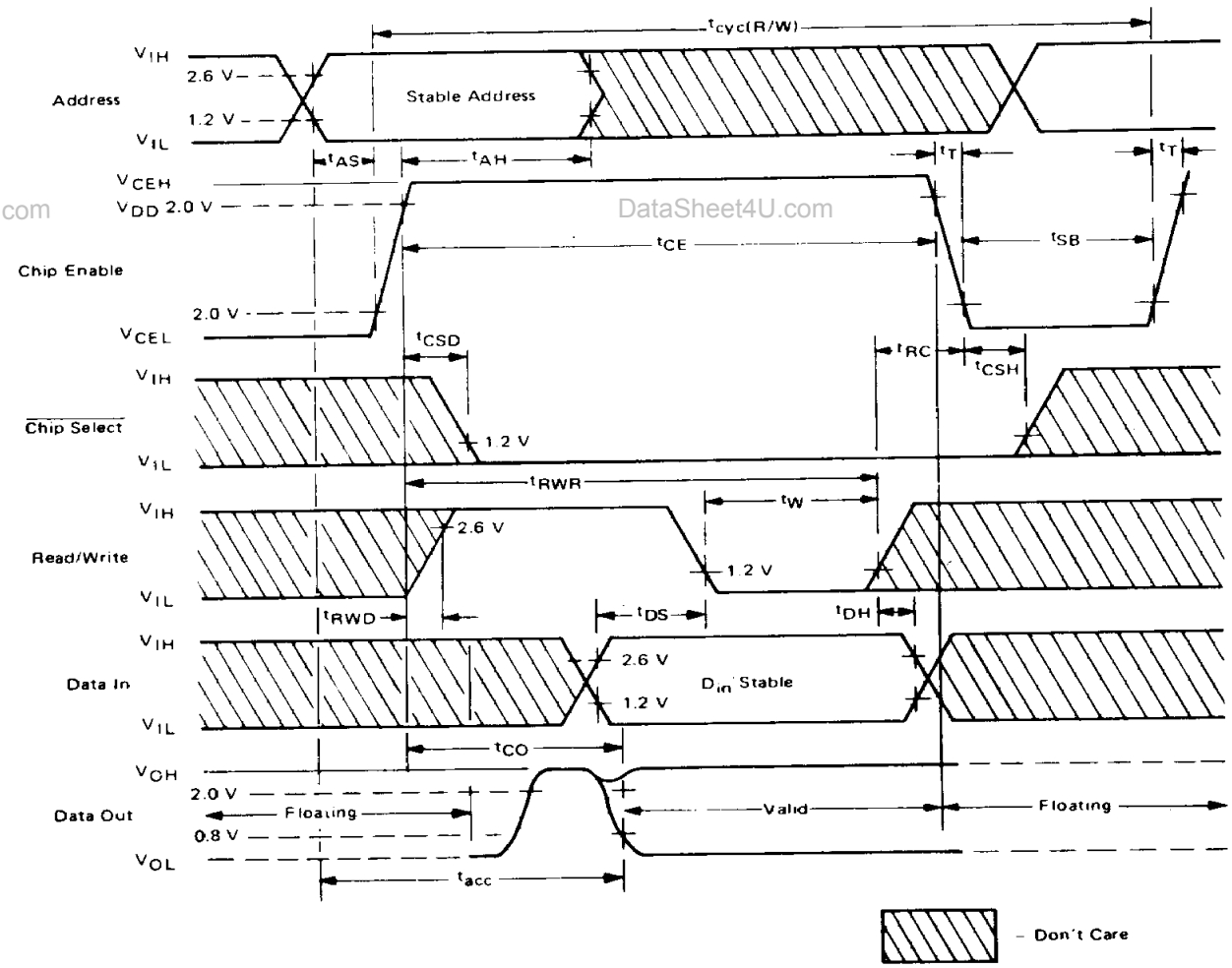


READ-MODIFY-WRITE ($R/\overline{W}$ = V_{IH}→V_{IL}, $\overline{CS}$ = V_{IL})
READ REFRESH (See Note 1)

Characteristic	Symbol	MCM6605AL,P		MCM6605AL1,P1		MCM6605AL2,P2		Unit
		Min	Max	Min	Max	Min	Max	
Read-Modify-Write Cycle Time	$t_{cyc(R/W)}$	590	–	390	–	490	–	ns
Chip Enable On Time	t_{CE}	430	2000	260	2000	330	2000	ns
Read-Write Release Time	t_{RWR}	410	2000	240	2000	310	2000	ns
Write Pulse Width	t_W	210	–	160	–	160	–	ns
Data Setup Time	t_{DS}	0	–	0	–	0	–	ns
Data Hold Time	t_{DH}	50	–	20	–	50	–	ns
Read-Write to Chip Enable Separation Time	t_{RC}	0	–	0	–	0	–	ns
Chip Enable to Output Delay	t_{CO}	–	280	–	130	–	180	ns
Read Access Time	t_{acc}	–	300	–	150	–	200	ns

Note 1: A read refresh cycle is possible by bringing $\overline{CS}$ high after output data is valid and then bringing R/W low to the write position.

READ MODIFY WRITE TIMING



TYPICAL CHARACTERISTICS CURVES

FIGURE 2 – ACCESS TIME versus V_{DD}

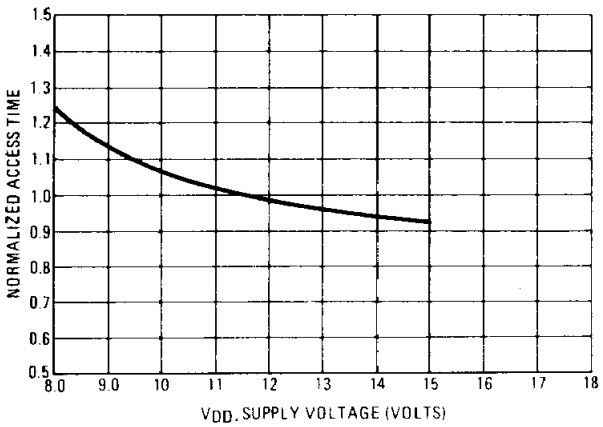


FIGURE 3 – ACCESS TIME versus AMBIENT TEMPERATURE

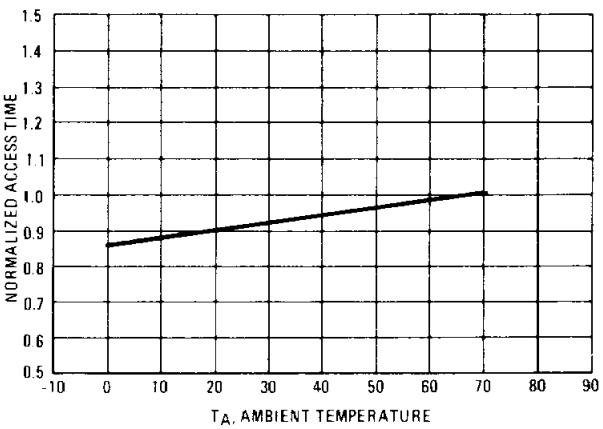


FIGURE 4 – I_{DD} SUPPLY CURRENT versus V_{DD}

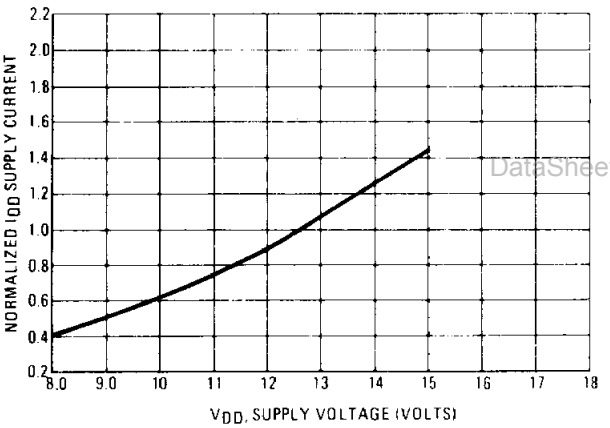


FIGURE 5 – I_{DD} SUPPLY CURRENT versus CYCLE TIME

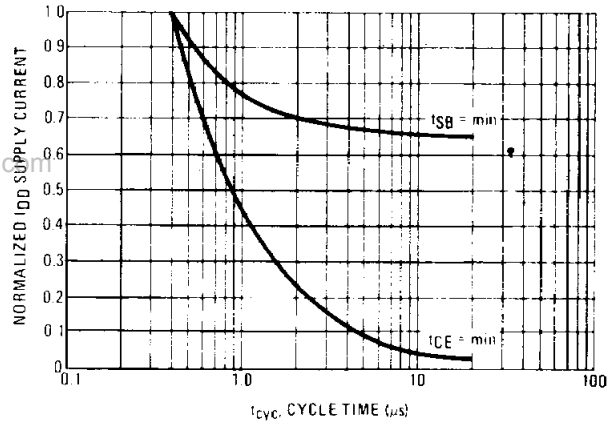


FIGURE 6 – I_{DD} SUPPLY CURRENT versus AMBIENT TEMPERATURE

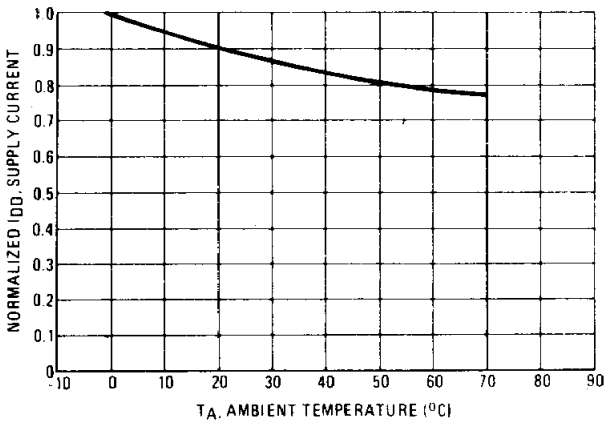
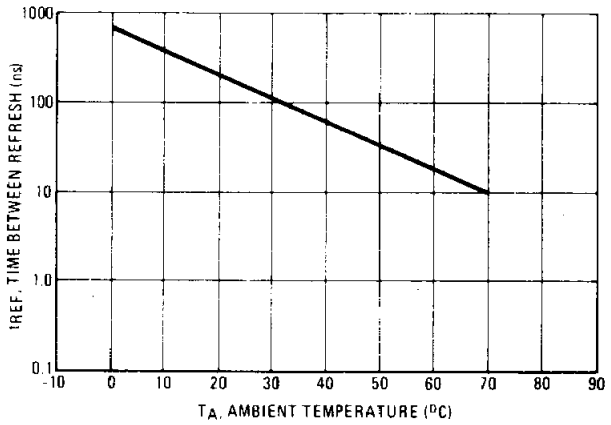


FIGURE 7 – REFRESH TIME versus AMBIENT TEMPERATURE



TYPICAL SUPPLY CURRENT TRANSIENT WAVEFORMS

FIGURE 8 – CHIP ENABLE VOLTAGE

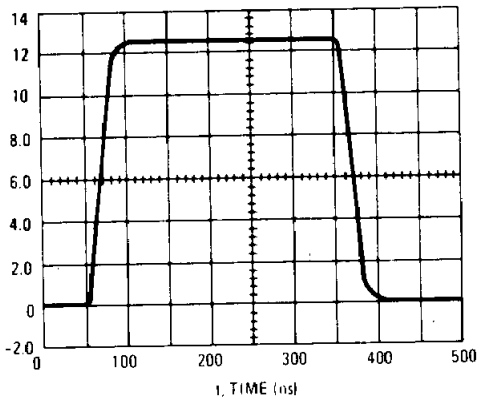


FIGURE 9 – i_{DD} SUPPLY CURRENT

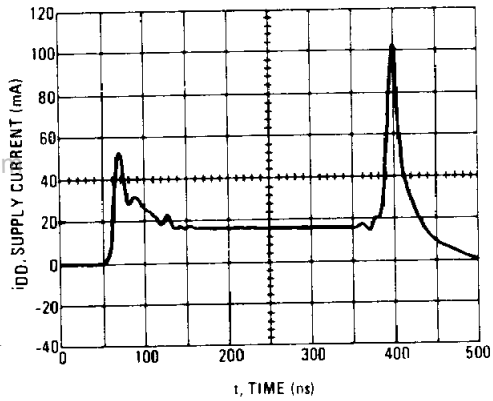


FIGURE 10 – i_{CC} SUPPLY CURRENT

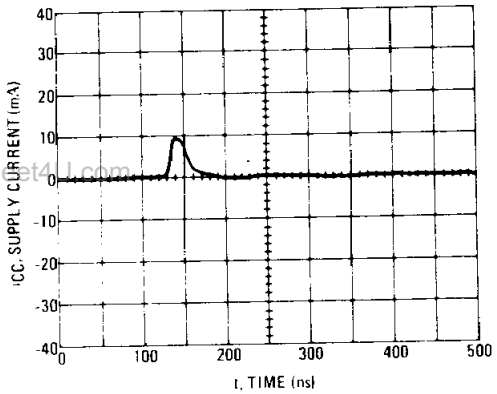


FIGURE 11 – i_{BB} SUPPLY CURRENT

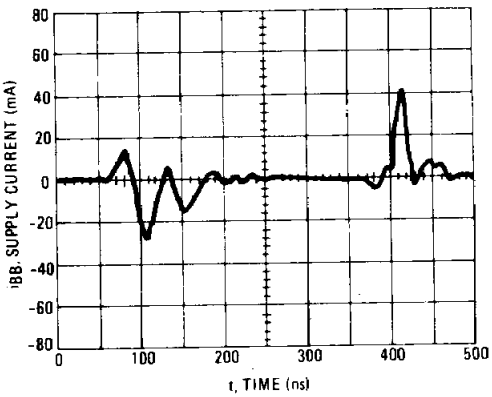
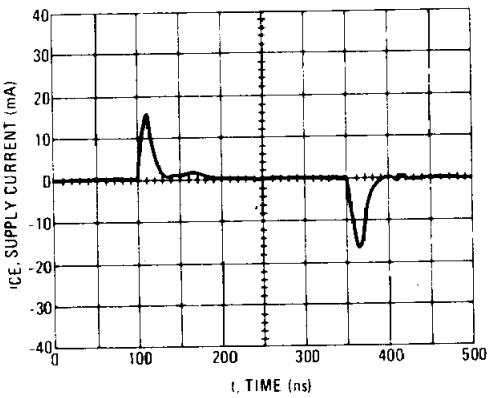
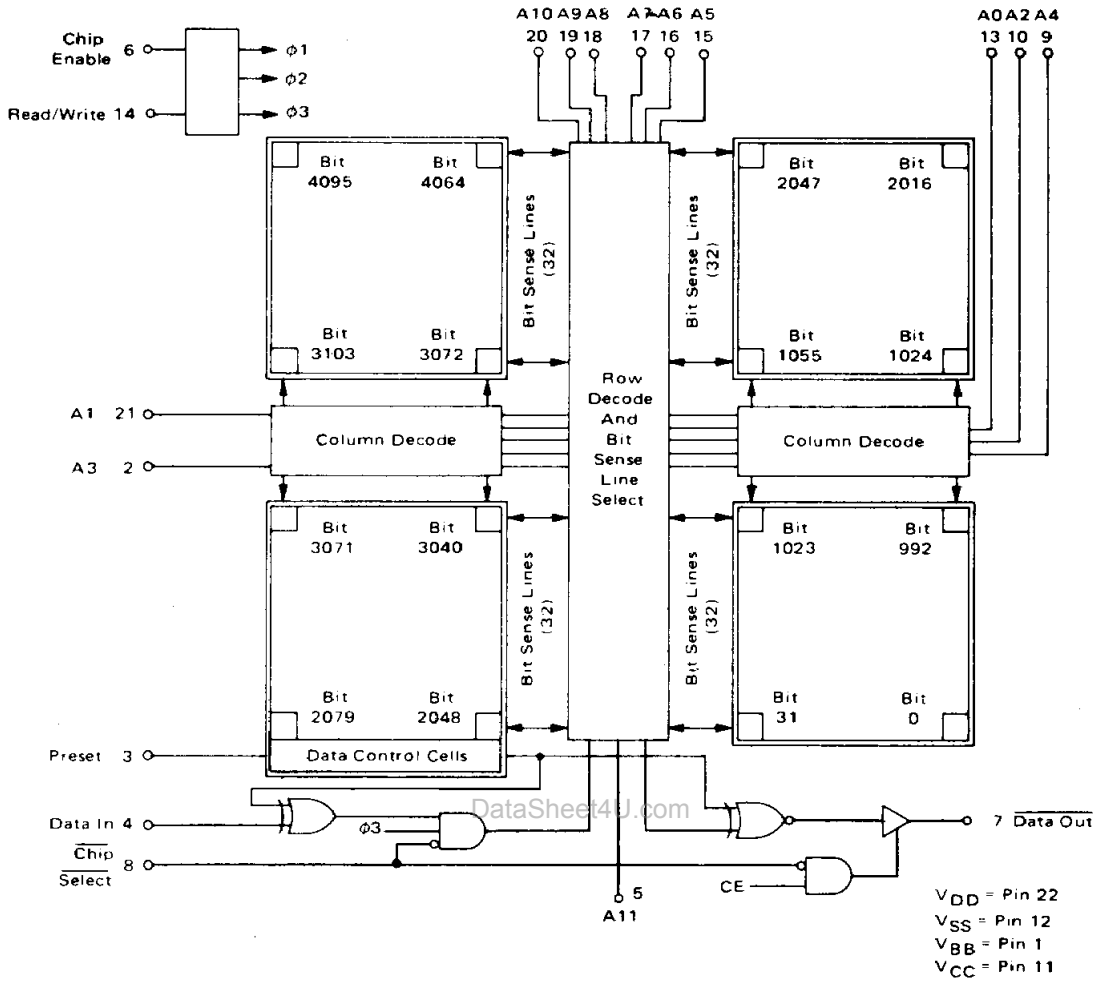


FIGURE 12 – i_{CE} SUPPLY CURRENT



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The MCM6605A 4096-bit dynamic RAM uses a three transistor storage cell in an inverting cell configuration. The single high-level clock (Chip Enable) starts an internal three-phase clock generator which controls the read and write functions of the device. The $\phi 1$ signal, which is high when CE is low (standby mode), preconditions the nodes in the dynamic RAM in preparation for a memory cycle. The $\phi 2$ signal, which comes on as CE goes high, is the read control and transfers data from storage onto bit sense lines. The $\phi 3$ signal, which comes after $\phi 2$ only during a write or refresh cycle, transfers data from the bit sense lines back into storage. The $\phi 3$ signal occurs only if the R/W input is low.

To perform a read cycle, CE is brought high to initiate a $\phi 2$ signal and latch the input addresses. The column decoders select one column in each of the four storage quadrants (see the block diagram) and transfers data from storage onto the 128 bit sense lines. The row decoder selects one of these 128 bit sense lines for read and write operations. During the $\phi 2$ signal, the data on this selected bit sense line is Exclusive ORed with the state of the appropriate data control cell to supply the correct output data. After this data is received by the external system, CE may be brought low to the standby position. This assumes that the R/W signal is held high to prevent an internal $\phi 3$ being generated.

To perform a write or refresh operation, CE is brought high and everything is identical to a read operation up until the 128 bit sense lines are charged with the selected columns of stored data. When R/W is brought low (if it is not already there), a $\phi 3$ signal is generated after $\phi 2$ is over. The $\phi 3$ signal takes the data from the 128 bit sense lines and returns it to the 128 storage locations it came from. Because of the design of the memory array, this $\phi 2$-$\phi 3$, read-write operation inverts the data. Therefore, one extra row of memory cells, called data control cells, is used to

keep track of the polarity of stored data in order to be able to correctly recover it. During the write operation, the input data is Exclusive ORed with these control cells before being stored in the array. A refresh cycle does not modify any of the bit sense lines, but simply returns the data (now inverted) into storage.

All timing signals for the MCM6605A are specified around these operations. The following is a brief description of the input pins and relevant timing requirements.

Chip Enable – CE is a single high level clock which initiates all memory cycles. CE can remain low as long as desired for specific applications as long as the 2.0 ms refresh requirements are met.

Chip Select – This signal controls only the I/O buffers. When $\overline{CS}$ is high, the input is disconnected and the output is in the 3-state high-impedance state. A refresh cycle is, therefore, a write cycle with $\overline{CS}$ high. $\overline{CS}$ has no critical timing with respect to any other signal except that there is a finite delay between activation and data out.

Read/Write – When high, R/W inhibits the internal $\phi 3$ signal, thereby keeping the memory from writing. When R/W is low, a $\phi 3$ will occur soon after $\phi 2$ is finished. For a read cycle, R/W should be high within t_{RWD} of CE to insure that a $\phi 3$ does not start. The only timing requirement on the R/W input for writing is a minimum write pulse defined as the overlap of $\overline{CS}$, CE, and R/W. Refresh cycles require that $\overline{CS}$ be high to inhibit the input buffer before a $\phi 3$ occurs. Thus $\overline{CS}$ should be high within t_{CSD} for a refresh cycle, or before R/W goes low for a read-refresh cycle.

Data In – The input data must be valid for a sufficient time to override the data stored on the selected bit sense line. It must remain valid for the "write pulse" defined under Read/Write. Signals on the D_{in} pin are ignored when either $\overline{CS}$ or R/W is high, or CE is low.

Data Out – Output data is inverted from input data and is valid t_{acc} after CE goes high. The data will remain valid as long as CE is high and $\overline{CS}$ remains low. With either CE low or $\overline{CS}$ high, the output is in a high-impedance state. The data output is initially precharged high when CE goes high and is then either discharged to ground or left high depending on the stored data. This precharging followed by valid data occurs regardless of the state of the R/W input, making the write cycle actually a read-write cycle. The output will also try to precharge during a refresh cycle but will be kept at high impedance by the $\overline{CS}$ being high. If $\overline{CS}$ is originally low and is then brought high (within the t_{CSD} specification) the output may start to precharge before being cut off and returned to high impedance.

Addresses – The addresses are latched when CE goes high, and may be removed after an appropriate hold time.

V_{SS} – Circuit ground.

V_{BB} – The reverse bias substrate supply. Forward biasing this supply with respect to V_{SS} will destroy the memory device.

V_{DD} – Positive supply voltage.

V_{CC} – Output buffer supply. This supply goes only to the data output buffer and draws current only when driving an output load high.

Preset – This pin should be tied to ground. During device testing Preset can be used to preset the data control cells to a logic zero. One 200 ns, 12 V pulse will set all 32 cells simultaneously. Preset has no system use; its only purpose is to ensure a good logic level in the control cells after first power up. In system use, this good logic level will come naturally after the first few refresh cycles.

2

APPLICATIONS INFORMATION

Power Supplies

The MCM6605A is a dynamic RAM which has essentially zero power drain when in the standby (CE low) mode. When operating, the V_{DD} supply may experience transients in the order of 100 mA for a short time (Figure 9). The V_{BB} supply, which has very low dc drain while operating, may see transients of about 40 mA during the edges of CE. Therefore, appropriate bypassing of both supplies is recommended. This bypassing has been simplified by the location of the power supply pins on the corners of the package.

The V_{CC} line supplies only the input leakage of a TTL load on Data Out and should never exceed about 100 μA, presenting little bypassing requirement.

Power dissipation for a system of N chips is much lower than N times the 335 mW typical dissipation for a full speed operating chip. This is because the unselected rows in a memory array card are operating in the standby mode of near zero dissipation. This zero standby power is actually unachievable because of the requirements for refresh. Therefore, power dissipation for an array of N X M chips operating at t_1 cycle time, t_{REF} refresh increment, and maximum CE down time between cycles is:

$$P_D \approx M\left(\frac{490\text{ ns}}{t_1\text{ ns}}\right)335\text{ mW} + (N-1)(M)\left(\frac{15.7}{t_{REF}\ \mu s}\right)335\text{ mW}$$

For a 550-ns-cycle-time, 64 k by 16 system (16 by 16 chip array) with refresh at 2.0 ms, the approximate power dissipation is:

$$P_D \approx 16\left(\frac{490}{550}\right)335 + (15)(16)\left(\frac{15.7}{2000}\right)335$$

$$\approx 4775\text{ mW} + 630\text{ mW} = 5.4\text{ W}$$

A similar one megabyte system, eight bytes wide, would have a dissipation of only 24 W. If the low standby power capability were not used, over 600 W would be dissipated.

Refresh

The MCM6605A is refreshed by performing a refresh (or write) cycle on each of the 32 combinations of the least significant address bits (A0-A4) within a 2.0 ms time period. (A5-A11 must remain constant at proper logic levels.) This refresh can be done in a burst mode (32 cycles starting every 2.0 ms) or in a distributed mode where one cycle is done every 62.5 μs.

A refresh abort can be accomplished by treating a refresh cycle as a read-modify-write cycle with $\overline{CS}$ high. This type of cycle can be aborted any time until the R/W signal has been brought low to allow a $\phi 3$ clock to begin.

Non-Volatile Storage

In many digital systems, it is extremely important to retain data during emergencies such as power failure. Unfortunately, however, most random access read/write semiconductor memories such as the MCM6605A are volatile. That is, if power is removed from the semiconductor memory, stored information is lost. Therefore, non-volatility for a specified period of time becomes highly desirable – as a necessity to maintain irreplaceable information or as a convenience to avoid the time consuming and troublesome task of having to reload the memory.

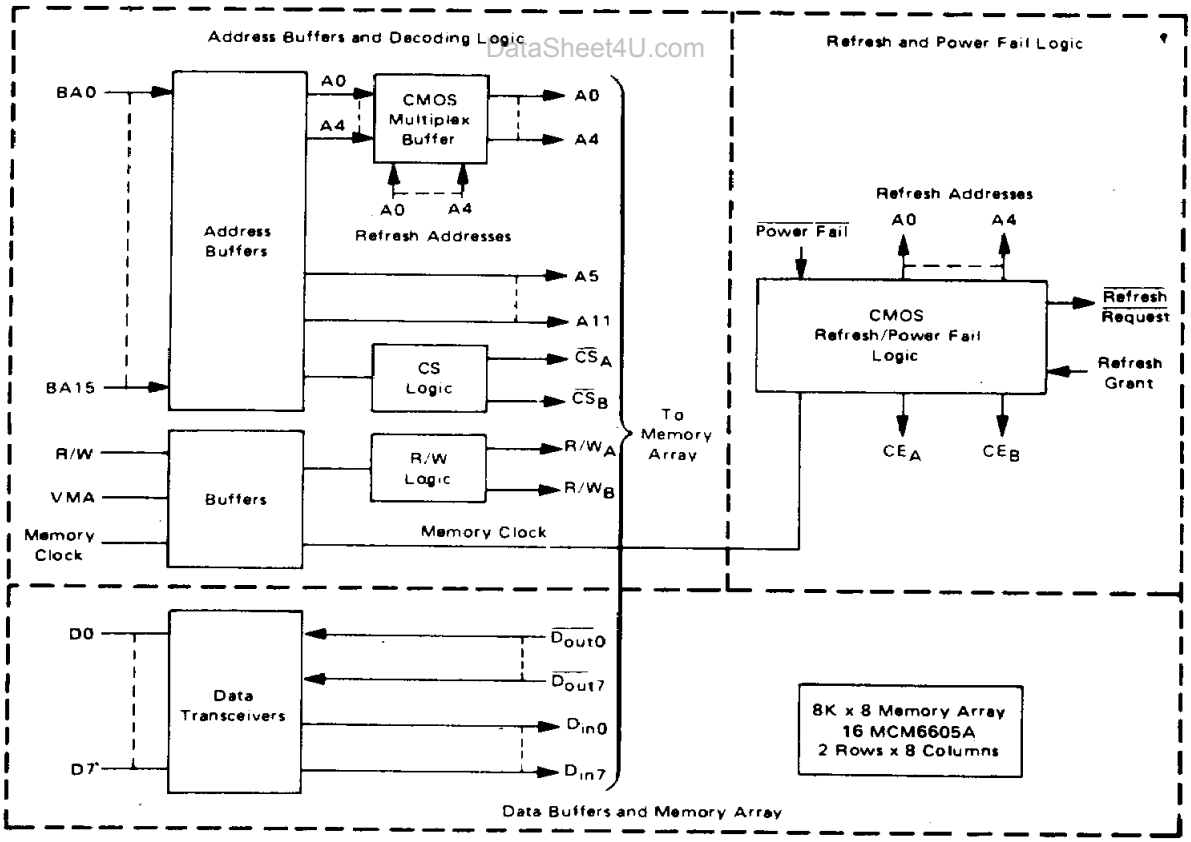
The extremely low standby power dissipation of the MCM6605A makes it ideal for main memory applications requiring battery backup for non-volatility. For example, the MCM6605A can be employed in an 8K byte non-volatile main memory system application for microprocessors. The memory system can be partitioned into three major sections as illustrated in Figure 13. The first section contains the address buffers and the Read/Write and Chip Select decoding logic. The second section consists of the data bus buffering transceivers and the memory array (which consists of 16 MCM6605As) organized into two rows of 4K bytes each.

The third section of the block diagram comprises refresh and control logic for the memory system. This logic interfaces the timing of the refresh handshaking with the microprocessor (MPU) clock circuitry. It handles requests for refresh, the generation of refresh addresses, the synchronization of a $\overline{\text{Power Fail}}$ signal, the multiplexing of the external Memory Clock with the internal clock (used during standby), and the generation of a –5 V supply on the board using a charge-pump method.

The refresh control logic is illustrated in Figure 14. It handles the refreshing of the memory during both operating and standby modes. The timing for this logic is given in Figure 15. Figure 16 gives the memory timing for the standby mode only. Decoding of the memory clock ($\overline{CE_A}$ and $\overline{CE_B}$) and the circuitry to synchronize the $\overline{\text{Power Fail}}$ signal are shown in Figure 17, with the timing given in Figure 18.

The memory device clock ($\overline{CE_A}$ and $\overline{CE_B}$) during standby is created by a monostable multivibrator (MC14528) and buffered from the memory array by three MC14503 buffers in parallel. This clock is multiplexed with the $\overline{\text{Memory Clock}}$ by use of the three-state feature of the

FIGURE 13 – NON-VOLATILE MEMORY SYSTEM BLOCK DIAGRAM



MC14503. The Memory Clock (used during normal operation) is translated to 12 V levels by use of an MC3460 Clock Driver. Decoding of the CE_A and CE_B signals (i.e., clocking only the memory bank addressed) to conserve power is accomplished by the logic within the MC3460.

Since the Power Fail signal will occur asynchronously with both the Memory Clock and the refreshing operation (Refresh Clock), it is necessary to synchronize the Power Fail signal to the rest of the system in order to avoid aborting a memory access cycle or a refresh cycle. An MC14027 dual flip-flop is used as the basic synchronization device. The leading edge of the Refresh Clock triggers a 3 μs monostable multivibrator which is used as a refresh pretrigger. The trailing edge of this pretrigger triggers a 500 ns monostable which creates the CE pulse during standby operation. The 3 μs pretrigger signal is used to set half of the MC14027 flip-flop, the output of which, (B), then inhibits a changeover from the standby to the operating modes (or vice versa). This logic prevents the system from aborting a refresh cycle should the Power Fail signal change states just prior to or during a refresh cycle. The trailing edge of the 500 ns monostable clears the MC14027 flip-flop, enabling the second flip-flop in the package. The state of Power Fail and Power Fail is applied to the K and J inputs of this second flip-flop and is synchronized by clocking with Memory Clock. The outputs of this flip-flop, labeled Bat and Bat, lock the system into the refresh mode and multiplex in the internal clock for standby operation when Bat = "1". The voltage to logic not required for the refresh only mode of operation is removed to conserve power.

By using CMOS for the refresh logic and capacitance drivers, and a low current refresh oscillator, the standby current required for the 8K byte system is extremely small, as noted in Table 1. This low standby current requirement can be easily supplied for several days with standard type +12 V batteries. For more detailed information on this sytem and a large mainframe memory system, see Application Notes AN-732 and AN-740.

2

FIGURE 14 – REFRESH CONTROL LOGIC

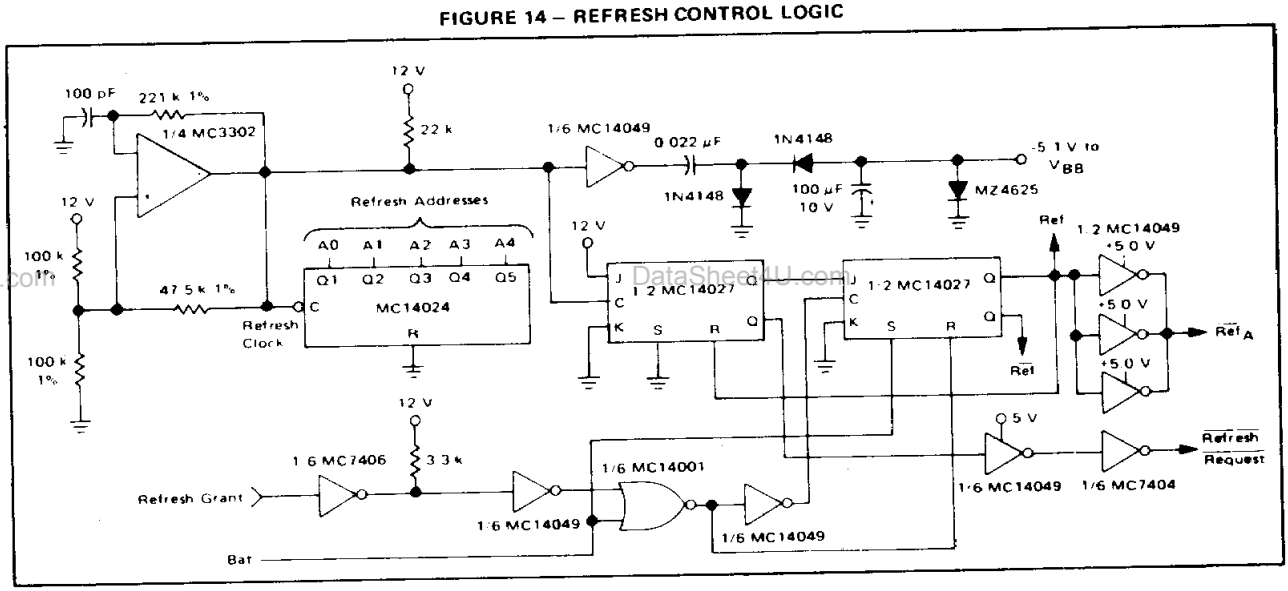


FIGURE 15 – REFRESH TIMING

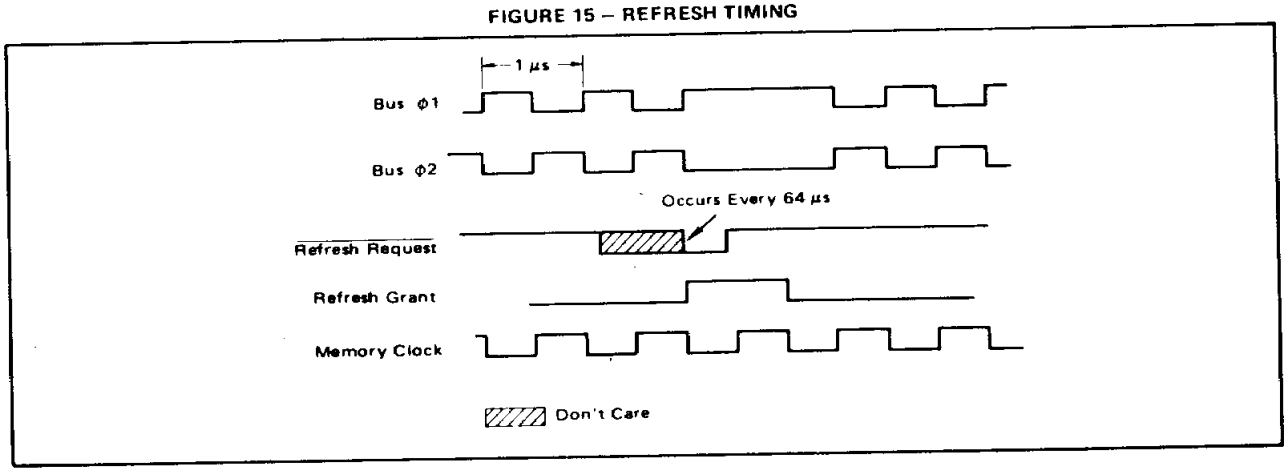


FIGURE 16 – MEMORY TIMING IN STANDBY MODE

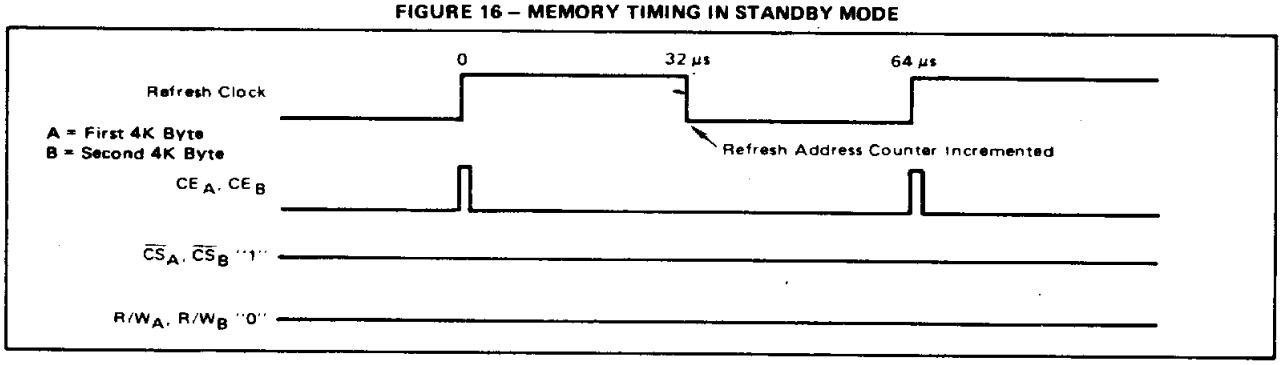


FIGURE 17 – POWER FAIL LOGIC AND CHIP ENABLE DRIVER

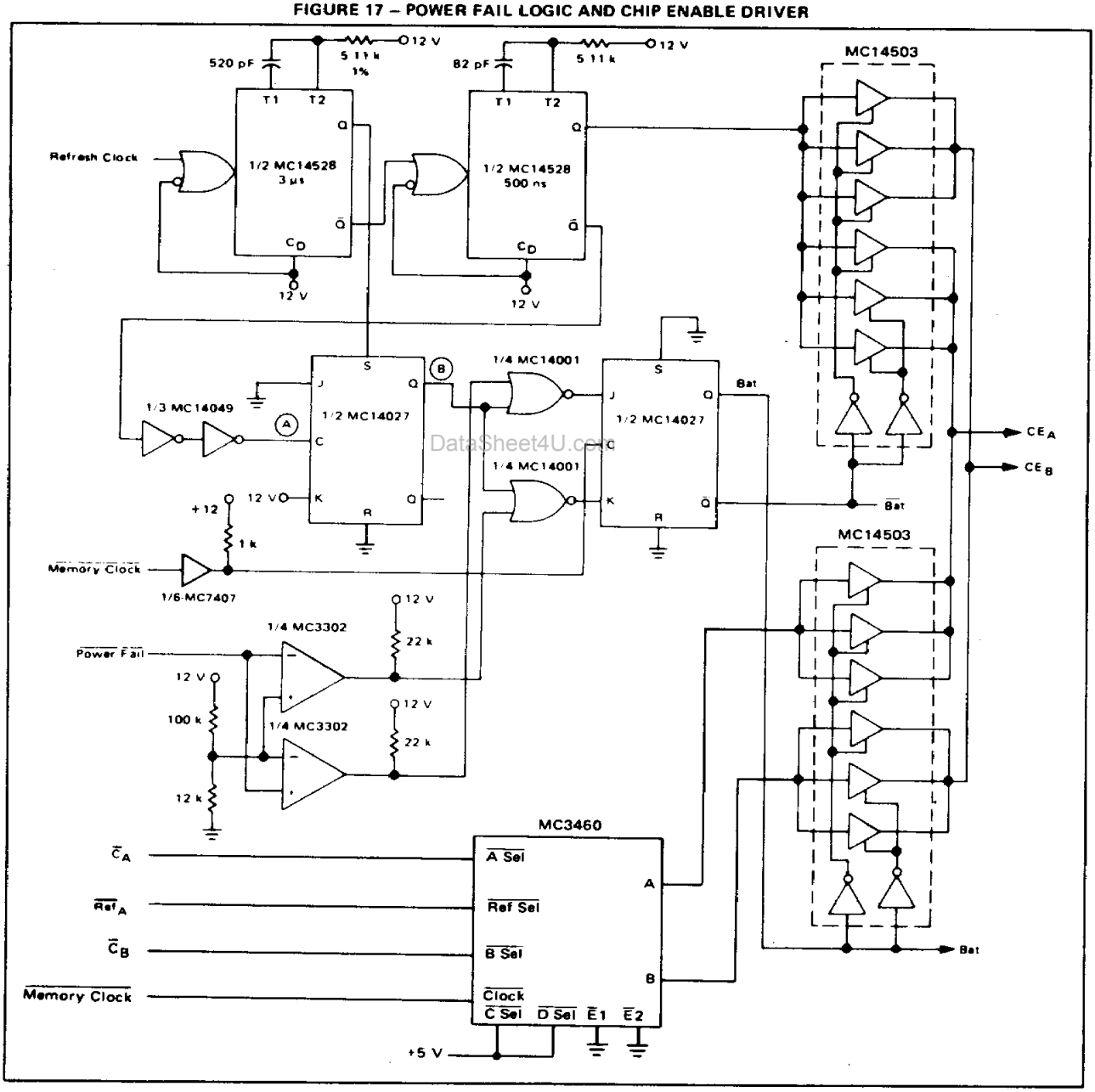


FIGURE 18 – POWER UP/DOWN SYNCHRONIZATION

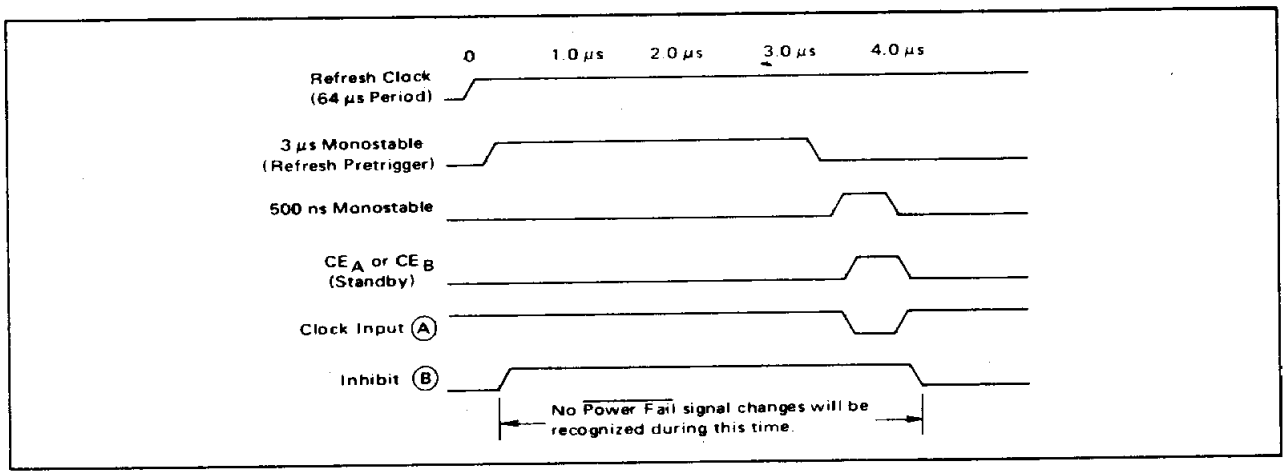


TABLE 1 – STANDBY MODE CURRENT ALLOCATION

Circuit Section	Typical Current
+12 V Current (V_{DD}) for 16 MCM6605A's	5 mA
Charge Pump	3 mA
Comparator	2 mA
Capacitance Drivers	4 mA
Total	14 mA