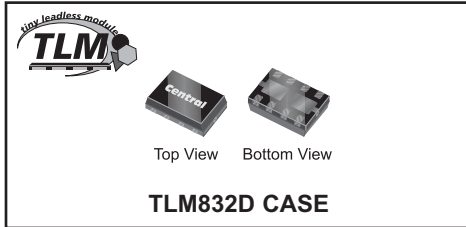


CTLDM7181-M832D

**SURFACE MOUNT
N-CHANNEL AND P-CHANNEL
ENHANCEMENT-MODE
COMPLEMENTARY SILICON MOSFETS**



APPLICATIONS:

- Switching Circuits
- DC - DC Converters
- Battery powered portable devices

MAXIMUM RATINGS: (T_A=25°C)

Drain-Source Voltage	V _{DS}	20	20	V
Gate-Source Voltage	V _{GS}	8.0	8.0	V
Continuous Drain Current (Steady State)	I _D	1.0	0.86	A
Continuous Drain Current, t _≤ 5.0s	I _D	-	0.95	A
Continuous Source Current (Body Diode)	I _S	-	0.36	A
Maximum Pulsed Drain Current, tp=10μs	I _{DM}	4.0	4.0	A
Maximum Pulsed Source Current, tp=10μs	I _{SM}	-	4.0	A
Power Dissipation (Note 1)	P _D	-	1.65	W
Operating and Storage Junction Temperature	T _J , T _{stg}	-65 to +150		°C
Thermal Resistance (Note 1)	θ _{JA}	76		°C/W

ELECTRICAL CHARACTERISTICS: (T_A=25°C)

SYMBOL	TEST CONDITIONS	N-CH (Q1)			P-CH (Q2)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
I _{GSSF} , I _{GSSR}	V _{GS} =8.0V, V _{DS} =0	-	-	10	-	.001	.05	μA
I _{DSS}	V _{DS} =20V, V _{GS} =0	-	-	10	-	.005	0.5	μA
BV _{DSS}	V _{GS} =0, I _D =250μA	20	-	-	20	24	-	V
V _{GS(th)}	V _{DS} =10V, I _D =1.0mA	0.5	-	1.2	-	-	-	V
V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	-	-	-	0.45	0.76	1.0	V
V _{SD}	V _{GS} =0, I _S =1.0A	-	-	1.1	-	-	-	V
V _{SD}	V _{GS} =0, I _S =360mA	-	-	-	-	-	0.9	V
r _{DS(ON)}	V _{GS} =4.5V, I _D =0.5A	-	.075	0.10	-	-	-	Ω
r _{DS(ON)}	V _{GS} =4.5V, I _D =0.95A	-	-	-	-	.085	0.15	Ω
r _{DS(ON)}	V _{GS} =2.5V, I _D =0.5A	-	0.10	0.14	-	-	-	Ω
r _{DS(ON)}	V _{GS} =4.5V, I _D =0.77A	-	-	-	-	.085	0.142	Ω
r _{DS(ON)}	V _{GS} =1.5V, I _D =0.1A	-	0.17	0.25	-	-	-	Ω
r _{DS(ON)}	V _{GS} =2.5V, I _D =0.67A	-	-	-	-	0.13	0.20	Ω
r _{DS(ON)}	V _{GS} =1.8V, I _D =0.2A	-	-	-	-	0.19	0.24	Ω
Q _{g(tot)}	V _{DS} =10V, V _{GS} =4.5V, I _D =1.0A	-	2.4	-	-	3.56	-	nC
Q _{gs}	V _{DS} =10V, V _{GS} =4.5V, I _D =1.0A	-	0.25	-	-	0.36	-	nC
Q _{gd}	V _{DS} =10V, V _{GS} =4.5V, I _D =1.0A	-	0.65	-	-	1.52	-	nC

Notes: (1) FR-4 Epoxy PCB with copper mounting pad area of 54mm².



www.centrasemi.com

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLDM7181-M832D is a Dual complementary N-Channel and P-Channel Enhancement-mode MOSFET, designed for high speed pulsed amplifier and driver applications. These MOSFETs offer Low r_{DS(ON)} and Low Threshold Voltages.

MARKING CODE: CFK

- Device is **Halogen Free** by design

FEATURES:

- Dual complementary MOSFETs
- Low r_{DS(ON)}
- High current
- Logic level compatibility

R2 (2-August 2011)

CTLDM7181-M832D

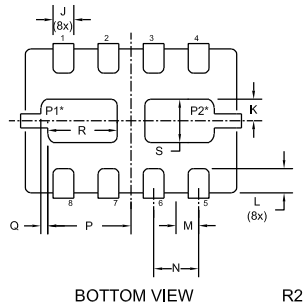
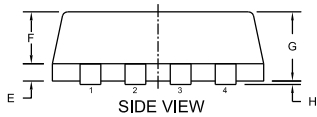
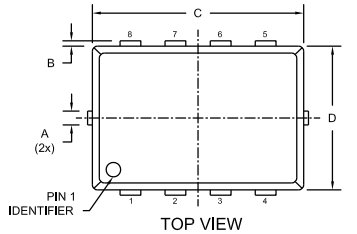
SURFACE MOUNT
N-CHANNEL AND P-CHANNEL
ENHANCEMENT-MODE
COMPLEMENTARY SILICON MOSFETS



ELECTRICAL CHARACTERISTICS - Continued:

SYMBOL	TEST CONDITIONS	N-CH (Q1)		P-CH (Q2)		UNITS
		TYP	MIN	TYP	MIN	
g _{FS}	V _{DS} =10V, I _D =0.5A	4.2	-	-	-	S
g _{FS}	V _{DS} =10V, I _D =810mA	-	2.0	-	-	S
C _{rSS}	V _{DS} =10V, V _{GS} =0, f=1.0MHz	45	-	-	-	pF
C _{rSS}	V _{DS} =16V, V _{GS} =0, f=1.0MHz	-	-	80	-	pF
C _{iSS}	V _{DS} =10V, V _{GS} =0, f=1.0MHz	220	-	-	-	pF
C _{iSS}	V _{DS} =16V, V _{GS} =0, f=1.0MHz	-	-	200	-	pF
C _{oss}	V _{DS} =10V, V _{GS} =0, f=1.0MHz	120	-	-	-	pF
C _{oss}	V _{DS} =16V, V _{GS} =0, f=1.0MHz	-	-	60	-	pF
t _{on}	V _{DD} =10V, V _{GS} =5.0V, I _D =0.5A	25	-	-	-	ns
t _{on}	V _{DD} =10V, V _{GS} =4.5V, I _D =950mA, R _G =6.0Ω	-	-	20	-	ns
t _{off}	V _{DD} =10V, V _{GS} =5.0V, I _D =0.5A	140	-	-	-	ns
t _{off}	V _{DD} =10V, V _{GS} =4.5V, I _D =950mA, R _G =6.0Ω	-	-	25	-	ns

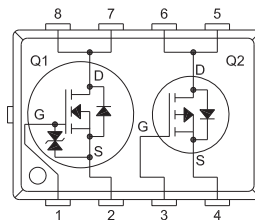
TLM832D CASE - MECHANICAL OUTLINE



SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.007	0.012	0.170	0.300
B	-	0.005	-	0.125
C	0.114	0.122	2.900	3.100
D	0.075	0.083	1.900	2.100
E	0.006	0.010	0.150	0.250
F	0.026	0.030	0.650	0.750
G	0.031	0.039	0.800	1.000
H	0.000	0.002	0.000	0.050
J	0.009	0.013	0.240	0.340
K	0.006	0.014	0.160	0.360
L	0.008	0.018	0.200	0.450
M	0.013		0.325	
N	0.026		0.650	
P	0.040	0.048	1.010	1.210
Q	0.004		0.100	
R	0.032	0.040	0.820	1.020
S	0.017	0.025	0.430	0.630

TLM832D (REV: R2)

PIN CONFIGURATION



LEAD CODE:

- 1) Gate Q1
- 2) Source Q1
- 3) Gate Q2
- 4) Source Q2
- 5) Drain Q2
- 6) Drain Q2
- 7) Drain Q1
- 8) Drain Q1

MARKING CODE: CFK

R2 (2-August 2011)

*** Note:**

- Exposed pad P1 common to pins 7 and 8
- Exposed pad P2 common to pins 5 and 6