CUSTOMER APPROVAL SHEET

Company Name	
MODEL	**A080SN01 V4**
CUSTOMER APPROVED	Title : Name :

- ☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.____)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.____)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver.____)**
- ☐ **CUSTOMER REMARK :**

AUO PM :

P/N : _____

Comment :

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Date : 2009/02/19

Product Specification

8.0" COLOR TFT-LCD PANEL

MODEL NAME: A080SN01 V4

(91.08A07.400)

< □ >Preliminary Specification
< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2008/08/18	All	First Draft.
0.1	2008/11/06	4	Update FPC connnector
		6	Update Recommended connector
		24	Update Viewing Angle
0.2	2008/11/12	24	Update Response time
0.3	2009/01/07	17	Update Serial register table
		18	Delete R1 setting
0.4	2009/02/19	10	Update Electrical characteristics

Contents

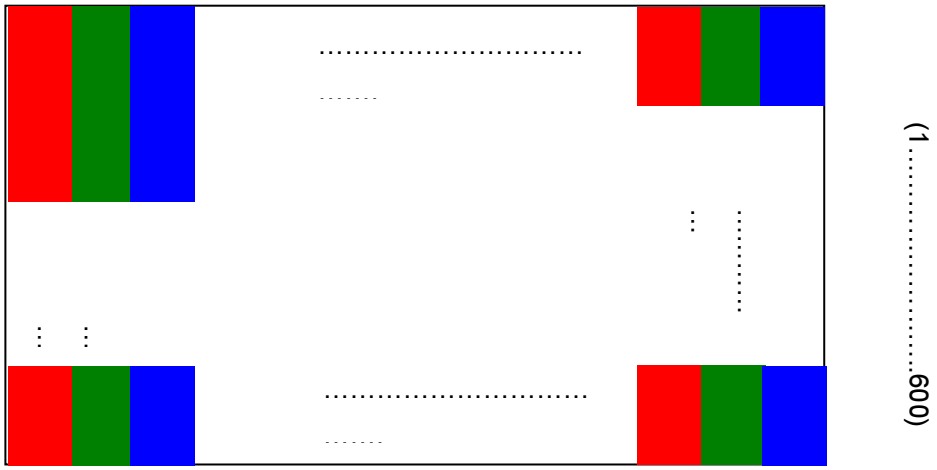
A. General Information

This product is for portable DVD and digital photo frame application.

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	8.0(Diagonal)	
2	Display Resolution	dot	800RGB(H)×600(V)	
3	Overall Dimension	mm	170.1(W) × 132.3(H) × 1.44(D)	Note 1
4	Active Area	mm	162.0(W)x121.5(H)	
5	Pixel Pitch	mm	0.2025(W)x0.2025(H)	
6	Color Configuration	--	R. G. B. Stripe	Note 2
7	Color Depth	--	16.7M Colors	Note 3
8	NTSC Ratio	%	50	
9	Display Mode	--	Normally White	
10	Panel surface Treatment	--	Anti-Glare, 3H	
11	Weight	g	65	
12	Panel Power Consumption	W	2.3	Note 4
13	Backlight Power Consumption	W	xx	
14	Viewing direction		6 o'clock (gray inversion)	

Note 1: Not include blacklight cable and FPC. Refer next page to get further information.

Note 2: Below figure shows dot stripe arrangement.



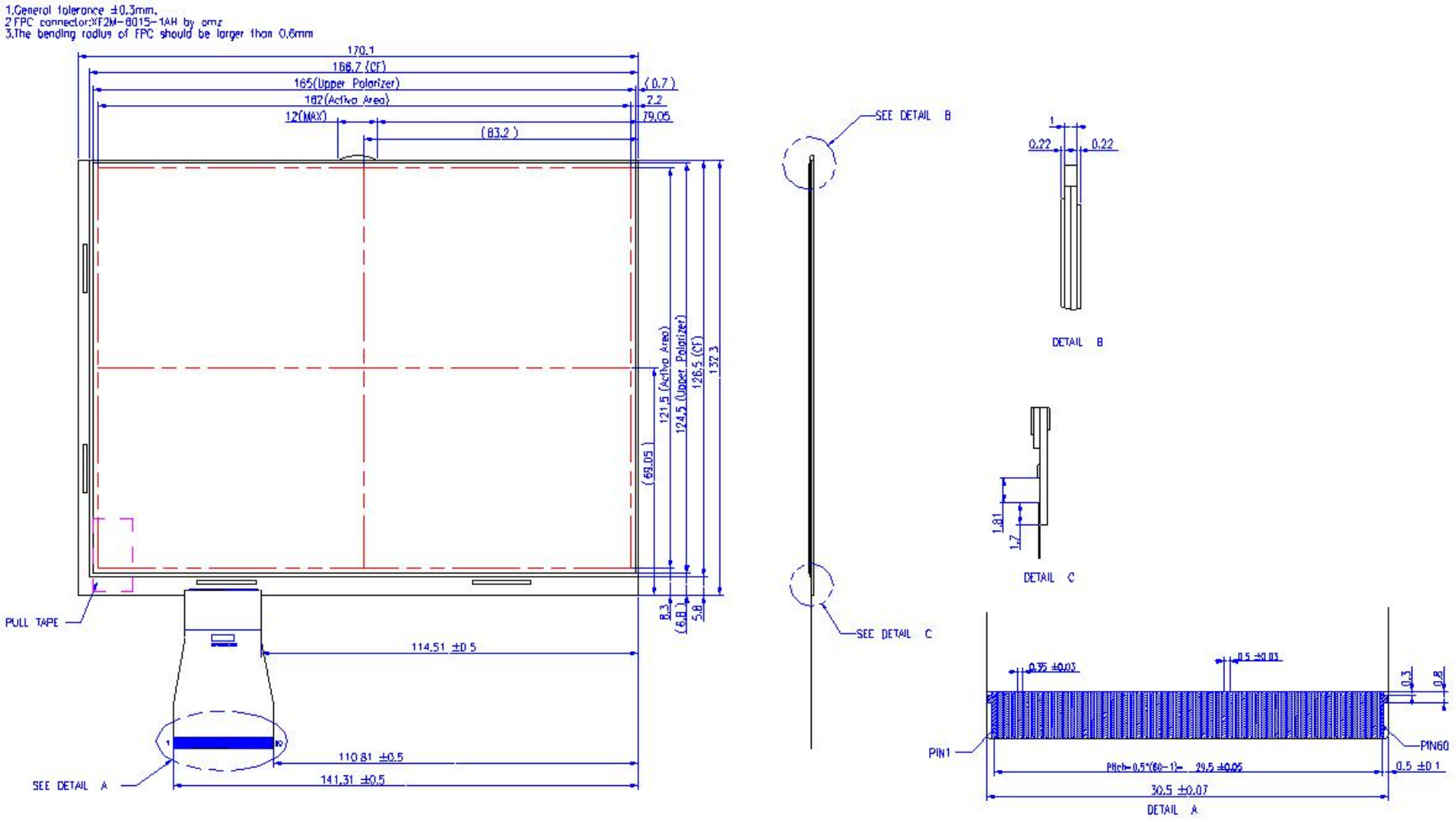
(1 2 3.....2398 2399 2400)

Note 3: The full color display depends on 24-bit data signal (pin 4~27).

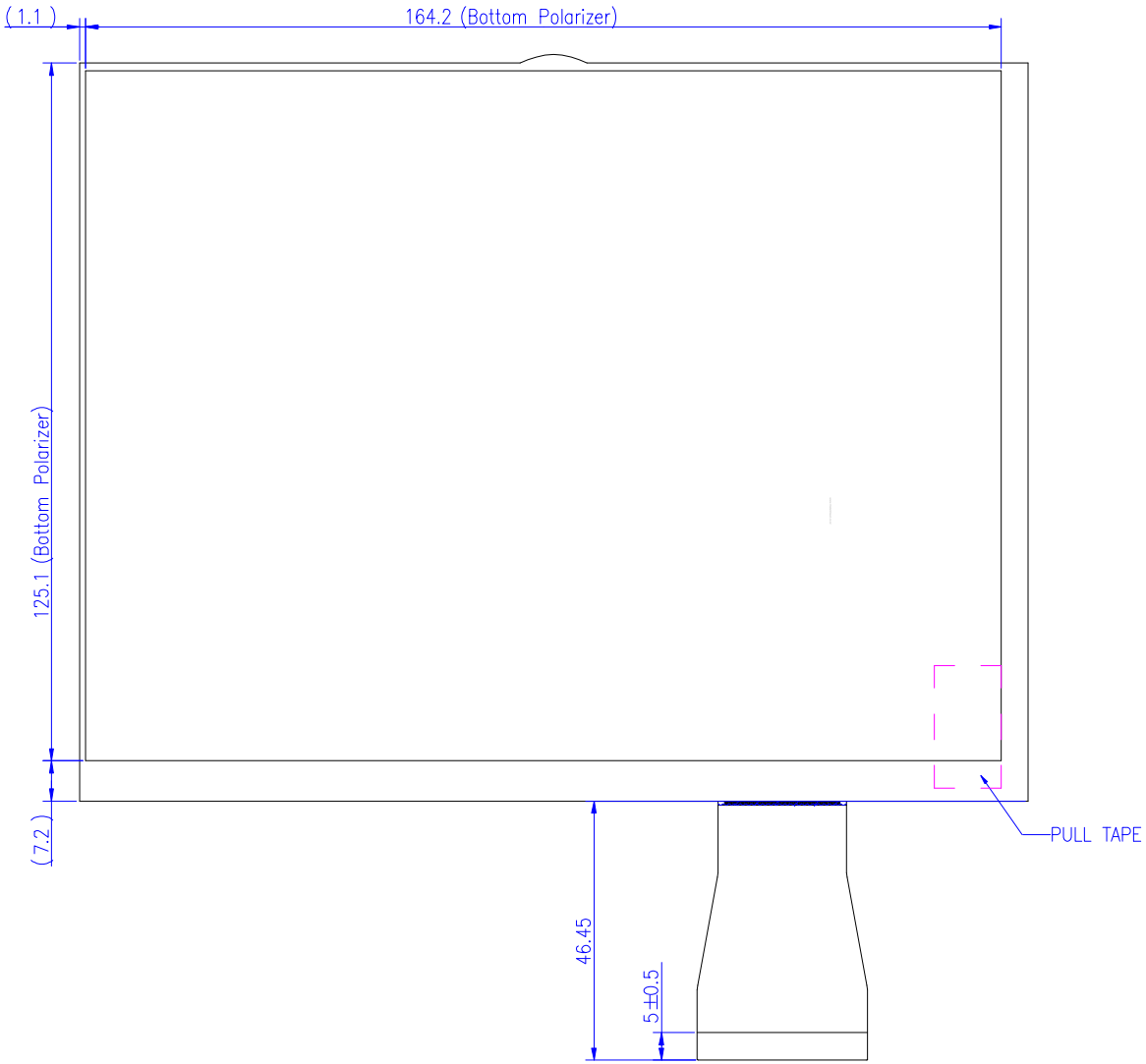
Note 4: Please refer to Electrical Characteristics chapter.

B. Outline Dimension

1. TFT-LCD Module – Front View



2. TFT-LCD Module – Rear View



C. Electrical Specifications

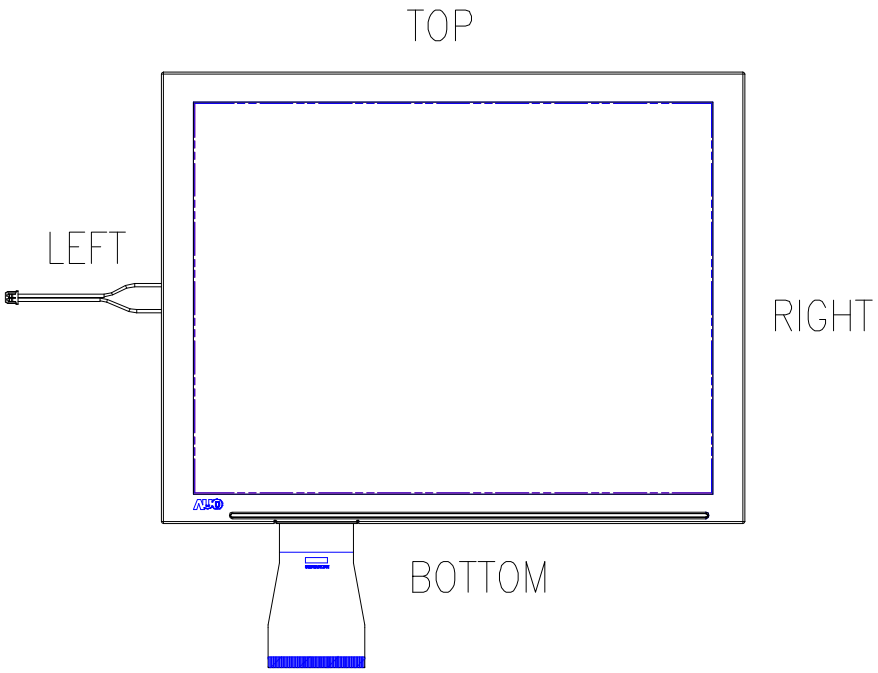
1. TFT LCD Panel Pin Assignment

Recommended connector : XF2M-6015-1AH

Pin no	Symbol	I/O	Description	Remark
1	AGND	P	Analog Ground	
2	AVDDIO	P	Analog Power	
3	VDDIO	P	Digital Power	
4	DR0	I	Red Data input (LSB)	
5	DR1	I	Red Data input	
6	DR2	I	Red Data input	
7	DR3	I	Red Data input	
8	DR4	I	Red Data input	
9	DR5	I	Red Data input	
10	DR6	I	Red Data input	
11	DR7	I	Red Data input (MSB)	
12	DG0	I	Green Data input (LSB)	
13	DG1	I	Green Data input	
14	DG2	I	Green Data input	
15	DG3	I	Green Data input	
16	DG4	I	Green Data input	
17	DG5	I	Green Data input	
18	DG6	I	Green Data input	
19	DG7	I	Green Data input (MSB)	
20	DB0	I	Blue Data input (LSB)	
21	DB1	I	Blue Data input	
22	DB2	I	Blue Data input	
23	DB3	I	Blue Data input	
24	DB4	I	Blue Data input	
25	DB5	I	Blue Data input	
26	DB6	I	Blue Data input	
27	DB7	I	Blue Data input (MSB)	
28	DCLK	I	Data clock Input	
29	DE	I	Data enable Input	
30	HSYNC	I	Horizontal sync input. Negative polarity	
31	VSYNC	I	Vertical sync input. Negative polarity	
32	SCL	I	Serial communication clock input	
33	SDA	I/O	Serial communication data input	

34	CSB	I	Serial communication chip select	
35	FBA	-	For test, do not connect (Please leave it open)	
36	VDDIO	P	Digital Power	
37	DRVA	-	For test, do not connect (Please leave it open)	
38	GND	P	Digital ground	
39	AGND	P	Analog ground	
40	AVDDIO	P	Analog Power	
41	VCOMIN	I	For external VCOM DC input (Optional)	
42	DITH	I	Dithering setting DITH = "L" 6bit resolution(last 2 bits of input data turncated) DITH = "H" 8bit resolution(Default setting)	
43	NC	-	Not connect	
44	VCOM	O	connect a capacitor	
45	V(10)	P	Gamma correction voltage reference	
46	V(9)	P	Gamma correction voltage reference	
47	V(8)	P	Gamma correction voltage reference	
48	V(7)	P	Gamma correction voltage reference	
49	V(6)	P	Gamma correction voltage reference	
50	V(5)	P	Gamma correction voltage reference	
51	V(4)	P	Gamma correction voltage reference	
52	V(3)	P	Gamma correction voltage reference	
53	V(2)	P	Gamma correction voltage reference	
54	V(1)	P	Gamma correction voltage reference	
55	NC	-	Not connect	
56	VGH	P	Positive power for TFT	
57	VDDIO	P	Digital Power	
58	VGL	P	Negative power for TFT	
59	GND	P	Digital Ground	
60	CAP	C	Connected to a capacitor	

I: Input pin; P: Power pin; G: Ground pin; C: capacitor pin



Note 1: FRP is the output of Vcom driver. It is the same phase and amplitude with common electrode driving signal (Vcom). The Vcom amplitude and DC level setting can be adjusted through serial control.

Note 2: The polarity of VCOM should be generated from POL through driving circuit. The H/L voltage level of POL is VDDIO/GND. Hence, it cannot be used as Vcom signal directly.

2. Backlight driving section

No.	Symbol	I/O	Description	Remark
1	VLED	I	LED power supply	--
2	GNDLED	-	LED ground	--

3. Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VDDIO	GND=0	-0.5	5	V	
	AVDDIO	AGND=0	-0.5	15	V	
	V_{GH}	GND=0	-0.3	42	V	
	V_{GL}		-20	0.3	V	
	$V_{GH}-V_{GL}$		-	40	V	
Input signal voltage	V_I		-0.3	VDDIO+0.3	V	Note 1
	VCOM		0	6.5	V	
Operating temperature	Topa		-10	60	℃	
Storage temperature	Tstg		-20	70	℃	

Note 1: HS , VS , DE , Digital Data

Note 2: Functional operation should be restricted under ambient temperature (25℃).

Note 3: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

4. Electrical DC Characteristics

a. Typical Operation Condition (AGND =GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply	VDDIO	2.7	3.3	3.6	V	
	I_{VDDIO}	-	11	14	mA	Black Pattern@VDDIO=3.3
	AVDDIO	11	11.68	12	V	
	I_{AVDDIO}	-	16	20	mA	Black Pattern
	V_{GH}	7	15	VEE+40	V	

		I_{VGH}	-	0.16	0.2	mA	Black Pattern
		V_{GL}	-20	-6.75	-5	V	
		I_{VGL}	-	0.16	0.2	mA	Black Pattern
Power Consumption		P	-	230	260	mW	Black Pattern
VCOM		V_{CDC}	3.9	4.1	4.3	V	DC component
Input signal voltage	H Level	V_{IH}	0.7xVDDIO	-	VDDIO	V	Note 1
	L Level	V_{IL}	0	-	0.3xVDDIO	V	
Input level of V1~V5		Vx	0.4*AVDD	-	AVDD-0.5		Positive gamma correction voltage Note 2
Input level of V6~V10		Vx	0.5	-	0.6*AVDD		Negative gamma correction voltage Note 2

Note 1: HS , VS , DE, Digital Data
Note 2 : AGND <V10<V9V<8V7<V6<V5<V4<V3<V2<V1<AVDD

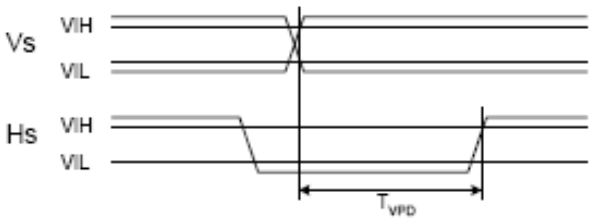
b. Backlight Driving Conditions

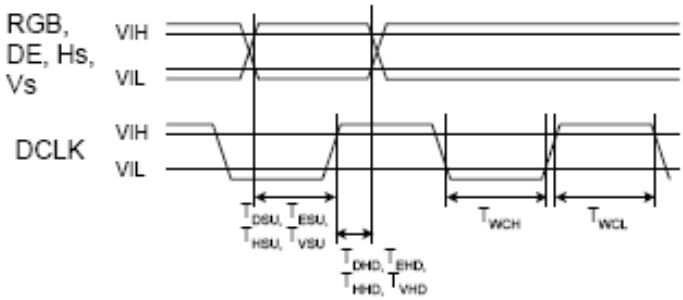
This is panel only module without BLU structure.

5. Electrical AC Characteristics

a. Signal AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Clock High time	T_{WCL}	8	-	-	ns	
Clock Low time	T_{WCH}	8	-	-	ns	
Hsync setup time	T_{HSU}	5	-	-	ns	
Hsync hold time	T_{HHD}	10	-	-	ns	
Vsync setup time	T_{VSU}	0	-	-	ns	
Vsync hold time	T_{VHD}	2	-	-	ns	
Data setup time	T_{DSU}	5	-	-	ns	
Data hold time	T_{DHD}	10	-	-	ns	
Data enable set-up time	T_{ESU}	4	-	-	ns	
Data enable hold time	T_{EHD}	2	-	-	ns	



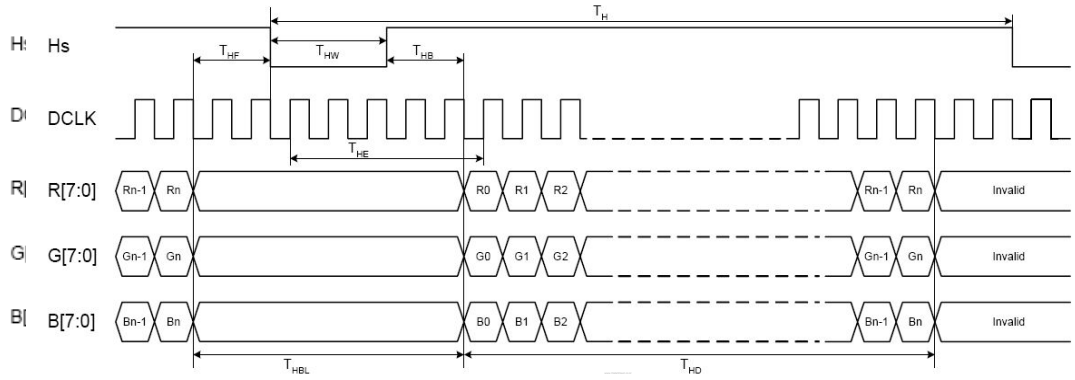


6. RGB Parallel Input Timing

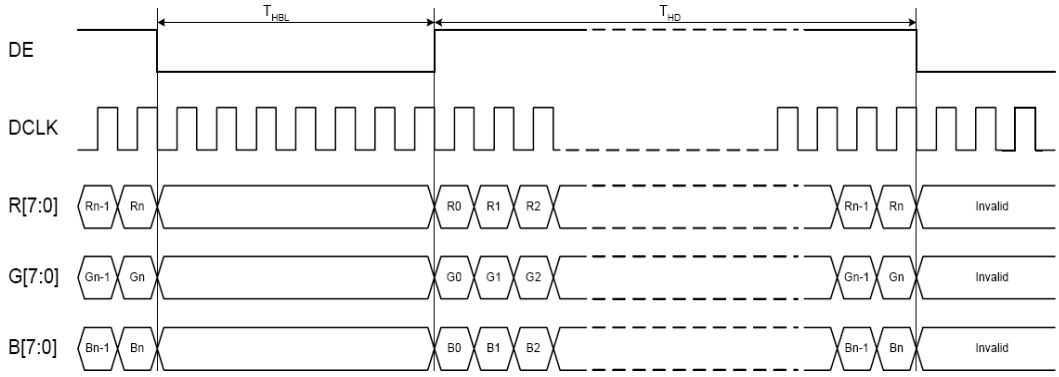
a. Horizontal timing

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency	F_{DCLK}	25	40	45	MHz	
DCLK period	T_{DCLK}	22	25	40	ns	
Hsync period (= T_{HD} + T_{HBL})	T_H	986	1056	1183	DCLK	
Active Area	T_{HD}	-	800	-	DCLK	

Horizontal blanking (= T_{HF} + T_{HE})	T_{HBL}	186	256	383	DCLK	
Hsync front porch	T_{HF}	-	40	-	DCLK	
Delay from Hsync to 1st data input (= T_{HW} + T_{HB})	T_{HE}	88	216	343	DCLK	Function of HDL[7..0] settings
Hsync pulse width	T_{HW}	1	128	136	DCLK	
Hsync back porch	T_{HB}	10	88	342	DCLK	



Horizontal input timing (HV mode)

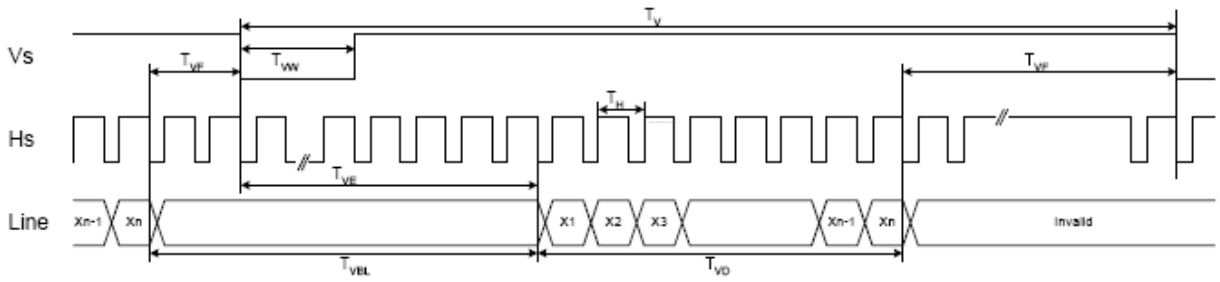


Horizontal input timing (DE mode)

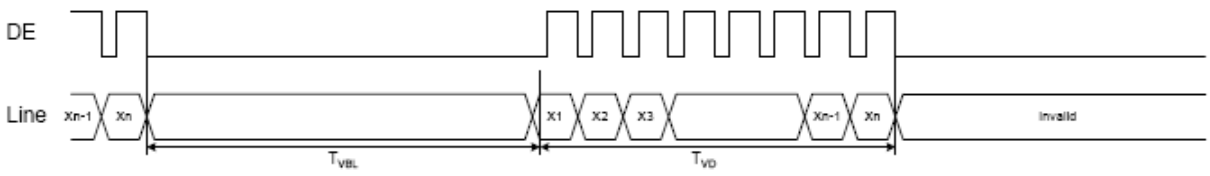
b. Vertical timing

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark

Vsync period (= T_{VD} + T_{VBL})	T_V	620	628	635	Th	
Active lines	T_{VD}	-	600	-		
Vertical blanking (= T_{VF} + T_{VE})	T_{VBL}	20	28	35	Th	
Vsync front porch	T_{VF}	-	1	-	Th	
GD start pulse delay	T_{VE}	19	27	34	HS	Function of VDL[3..0] settings
Vsync pulse width	T_{VW}	1	3	16	Th	
Hsync/Vsync phase shift	T_{VPD}	2	320	-	DCLK	



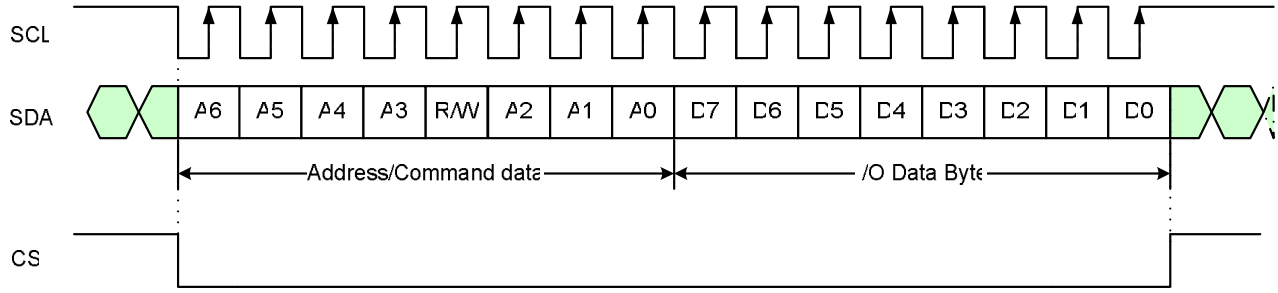
Vertical timing (HV mode)



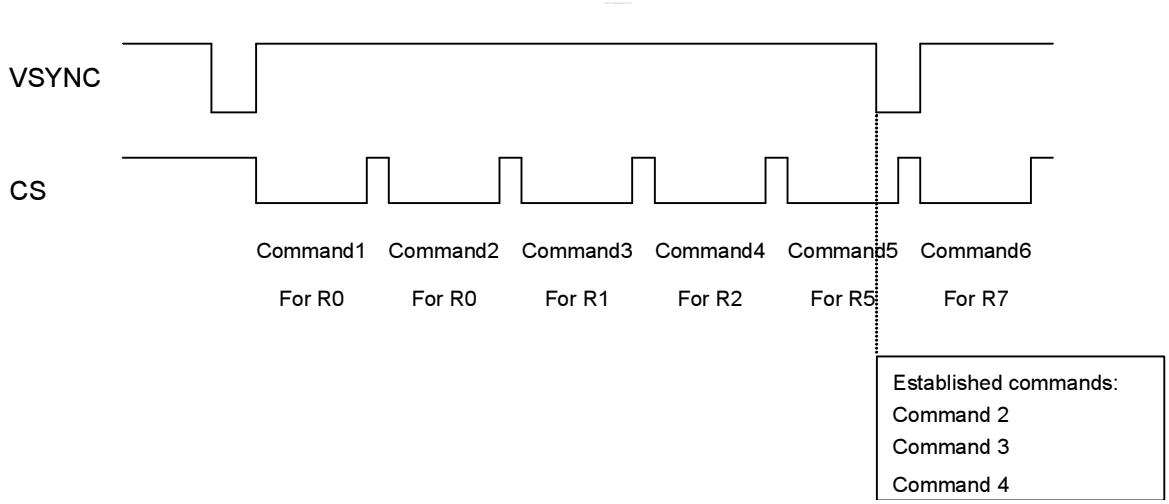
Vertical timing (DE mode)

7. Serial Interface Characteristics

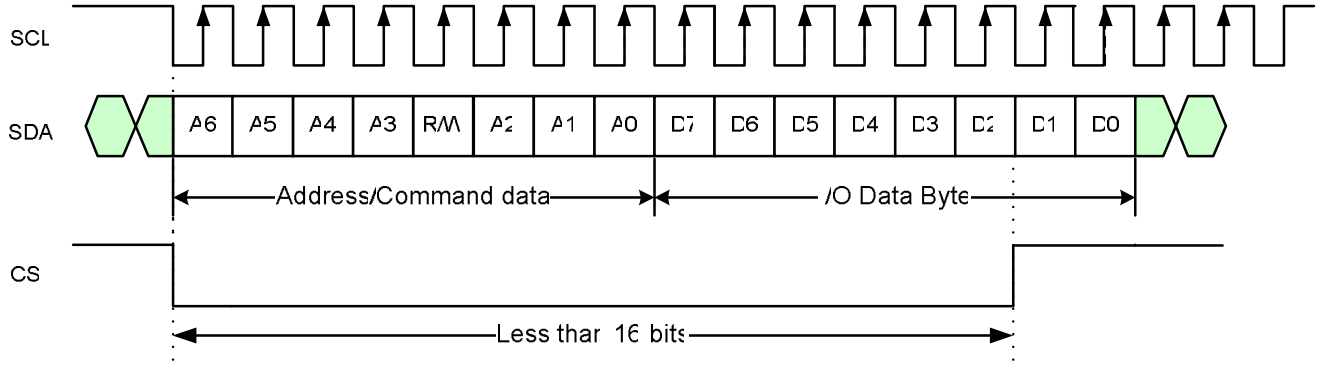
a. Serial Control Interface AC Characteristic



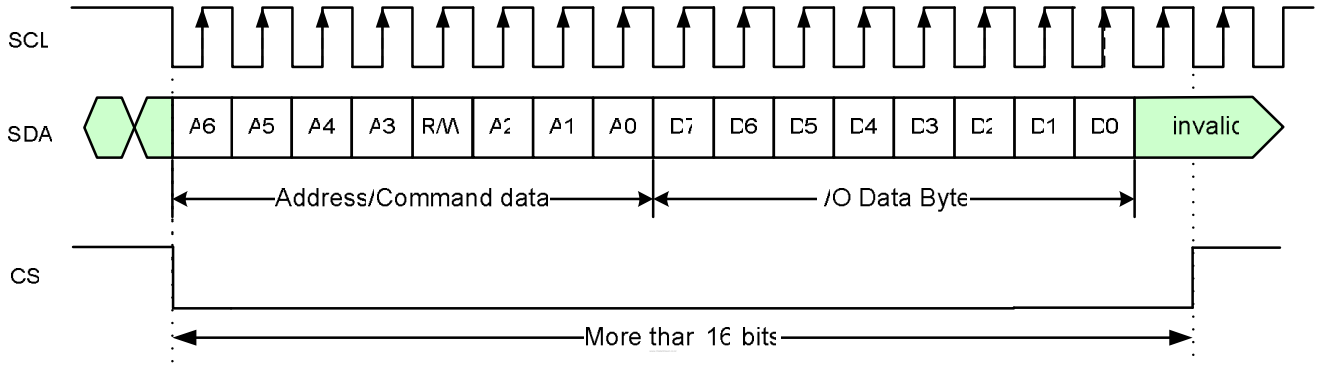
1. Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.
2. Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.
3. The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.



4. If less than 16 bits of SCL are input while CS is low, writing command cannot be established.



5. If 16 bits or more of SCL are input while CS is low, the first 16 bits of transferred data before the rising edge of CS pulse are valid data.



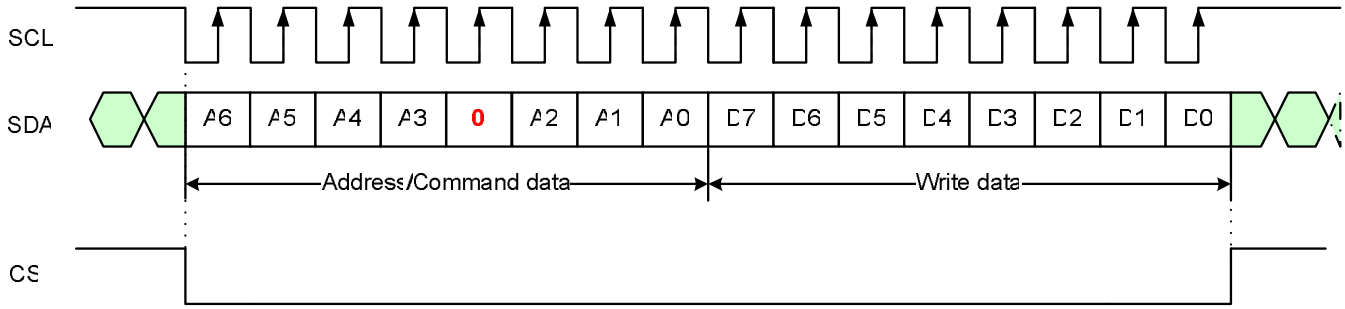
6. Serial block operates with the SCL clock.
7. Serial data can be accepted in the standby (power save) mode.

b Serial Interface Timing

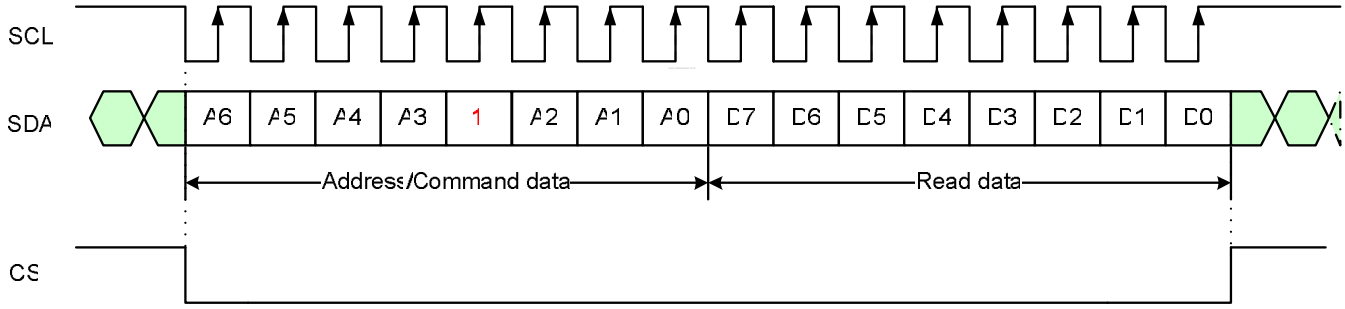
MSB LSB

A6	A5	A4	A3	R/W	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Address				R/W	Address			DATA							

Write Mode:



Read Mode:



c. Register Table (Default Value)

- When GRB is low, all registers reset to default values, which are in the brackets.
- Serial commands are executed at next VSYNC signal.

Reg	ADDRESS				R/W	DATA										
No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	(01)		(01)		(1)	U/D (0)	SHL (1)	(0)	(0)	GRB (1)	STB (1)
R1	0	0	0	1	0	×	(0)	(1)	(01)		(2Fh)					
R2	0	0	1	0	0	×	×	×	HDL (80h)							
R3	0	0	1	1	0	×	×	(0)	(0)	(0)	(0)	(0)	VDL (1000)			
R4	0	1	0	0	0	×	×	(1)	(0)	(0)	(0)	(1)	(1111)			
R6	0	1	1	0	0	×	(0)	EnGB12 (1)	EnGB11 (1)	EnGB10 (1)	(0)	(0)	EnGB5 (1)	EnGB4 (1)	EnGB3 (1)	(0)

"x" => reserved bit, please set to '0'.

<Note>：Sending serial commands periodically is recommended to improve ESD protection ability.

d. Register Description

- When GRB is low, all registers reset to default values, which are in the brackets.
- Serial commands are executed at next VSYNC signal.

1.. R0 setting

Address	Bit	Description		Default
0000	[10..0]	Bits 10-9	AUO Internal Use	01
		Bits7-8	AUO Internal Use	01
		Bit6 (DITH)	Dithering function.	1
		Bit5 (U/D)	Vertical shift direction selection.	0
		Bit4 (SHL)	Horizontal shift direction selection.	1
		Bit3 (SHDB1)	AVDD DC-DC converter shutdown setting.	1
		Bit2	AUO Internal Use	0
		Bit1 (GRB)	Global reset.	1
		Bit0 (STB)	Standby mode setting.	1

Bit6	DITH function
0	DITH off.
1	DITH on. **(default)**

Bit5	U/D function
0	Scan down; First line= Gn -> Gn-1 -> … -> G2 -> Last line=G0. **(default)**
1	Scan up; First line= G0 -> G2 -> … -> Gn-1 -> Last line=Gn

Bit4	SHL function
0	Shift left; First data= Y600 -> Y599 -> … -> Y2 -> Last data=Y1.
1	Shift right; First data= Y1 -> Y2 -> … -> Y599 -> Last data=Y600. **(default)**

Bit3	SHDB1 function
0	AVDD DC-DC converter is off.
1	AVDD DC-DC converter is on. **(default)**

Bit1	GRB function
0	The controller is reset. Reset all registers to default value.
1	Normal operation. **(default)**

Bit0	STB function
0	T-CON, source driver and DC-DCs converters are off. All outputs are set to GND.
1	Normal operation. **(default)**

2. R2 setting

Address	**Bit**	**Description**		**Default**
0010	[7..0]	Bit7-0(HDL)	Horizontal start pulse adjustment function	80H

Bit7-0	HDL function
00h	$T_{HE} = T_{HEtyp}$ - 128 CLK period.
80h	$T_{HE} = T_{HEtyp}$. **(default)**
FFh	$T_{HE} = T_{HEtyp}$ + 127 CLK period.

3. R3 setting

Address	**Bit**	**Description**		**Default**
0011	[8..0]	Bit8	AUO Internal Use	0
		Bit7	AUO Internal Use	0
		Bit6	AUO Internal Use	0
		Bit5	AUO Internal Use	0
		Bit4	AUO Internal Use	0
		Bit3-0(VDL)	Vertical start pulse adjustment function	1000

Bit3-0	VDL function
0000	$T_{VE} = T_{VEtyp} – 8$ Hs period.
0001	$T_{VE} = T_{VEtyp} – 7$ Hs period.
0010	$T_{VE} = T_{VEtyp} – 6$ Hs period.
0011	$T_{VE} = T_{VEtyp} – 5$ Hs period.
0100	$T_{VE} = T_{VEtyp} – 4$ Hs period.
0101	$T_{VE} = T_{VEtyp} – 3$ Hs period.
0110	$T_{VE} = T_{VEtyp} – 2$ Hs period.
0111	$T_{VE} = T_{VEtyp} – 1$ Hs period.
1000	$T_{VE} = T_{VEtyp.}$ (default)
1001	$T_{VE} = T_{VEtyp} – 1$ Hs period.
1010	$T_{VE} = T_{VEtyp} – 2$ Hs period.
1011	$T_{VE} = T_{VEtyp} – 3$ Hs period.
1100	$T_{VE} = T_{VEtyp} – 4$ Hs period.
1101	$T_{VE} = T_{VEtyp} – 5$ Hs period.
1110	$T_{VE} = T_{VEtyp} – 6$ Hs period.
1111	$T_{VE} = T_{VEtyp} – 7$ Hs period.

4. R6 setting

Address	**Bit**	**Description**		**Default**
0110	[9..0]	Bits9	AUO Internal Use	0
		Bits8(EnGB12)	Gamma buffer Enable for V9	1
		Bits7(EnGB11)	Gamma buffer Enable for V8	1
		Bits6(EnGB10)	Gamma buffer Enable for V7	1
		Bits5	AUO Internal Use	0
		Bits4	AUO Internal Use	0
		Bits3(EnGB5)	Gamma buffer Enable for V4	1
		Bits2(EnGB4)	Gamma buffer Enable for V3	1
		Bits1(EnGB3)	Gamma buffer Enable for V2	1
		Bits0	AUO Internal Use	0

Bitx	EnGBx function
0	Gamma buffer for VX is disabled (High Z).
1	Gamma buffer is enabled. VX must be connected externally.

“x” => reserved bit, please set to ‘0’.

<Note>：Sending serial commands periodically is recommended to improve ESD protection ability.

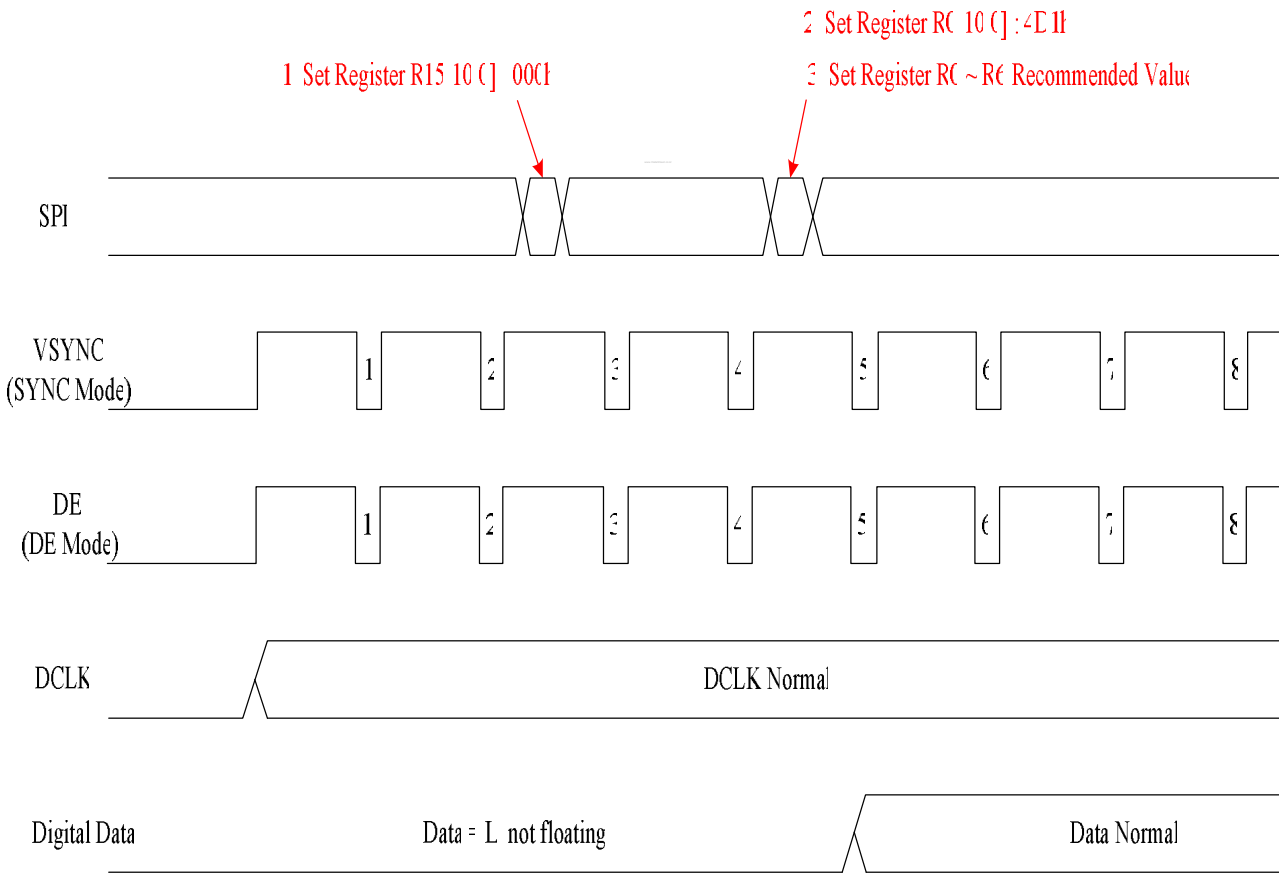
8. Power On/Off Characteristics

a. Recommended Power On Register Setting

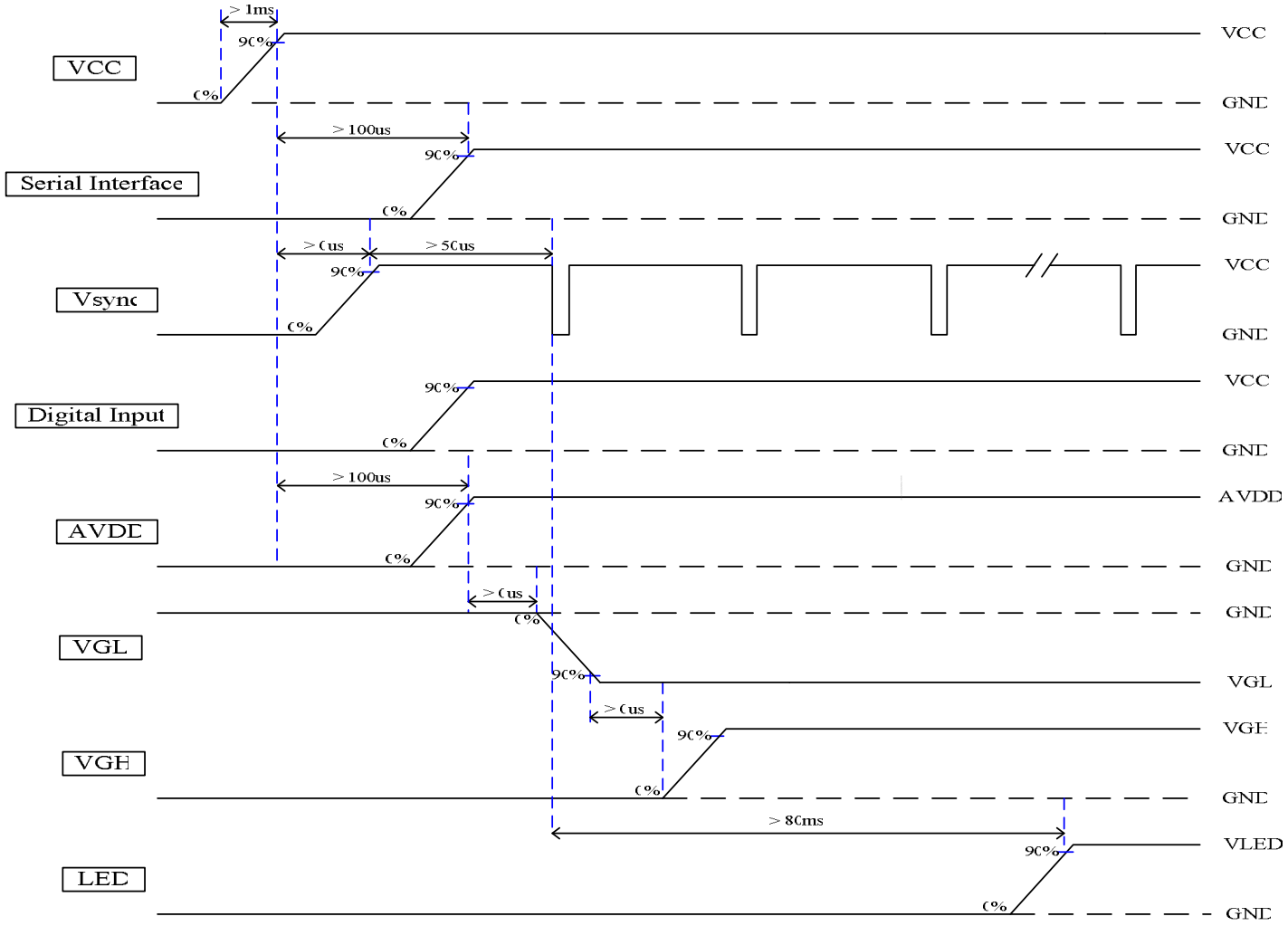
Reg	ADDRESS				R/W	DATA										
No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	10		01		1	0	1	0	0	1	1
R1	0	0	0	1	0	0	01		01		2Fh					
R2	0	0	1	0	0	0	0	0	80h							
R3	0	0	1	1	0	0	0	0	0	0	0	0	1000			
R4	0	1	0	0	0	0	0	1	1	00		1	1111			
R6	0	1	1	0	0	0	0	1	1	1	0	0	1	1	1	0

Note : Start to provide SPI commend at least after 2 frame.

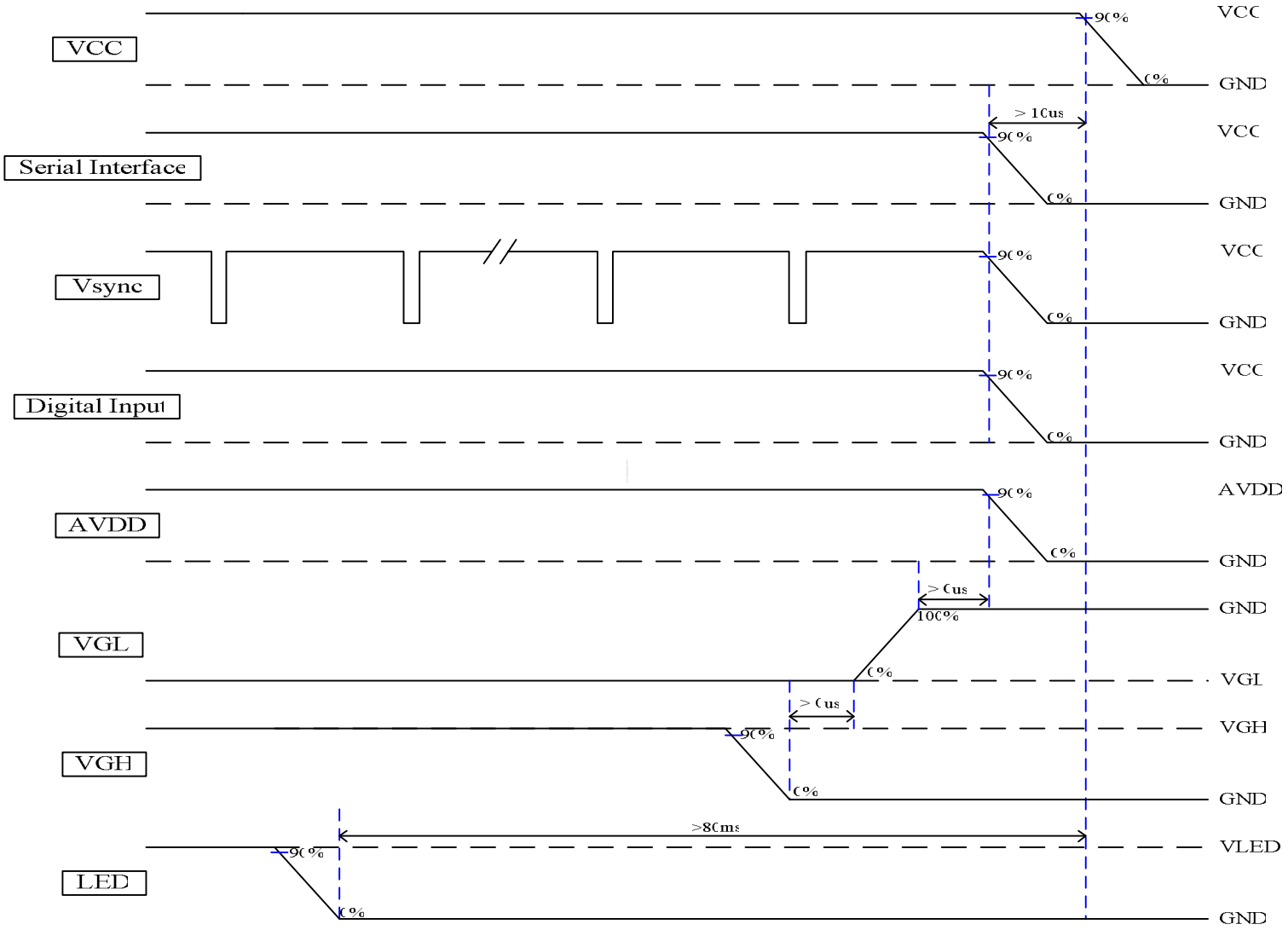
1. Send R15 : 000h(Normal register bank) at first.
2. Wait at least after more than one frame, send R0 : 4D1h(Global Reset)
3. After send Global Reset, start to send R0 to R6 recommend register value.



b. Recommended Power On Sequence



c. Power Off Sequence



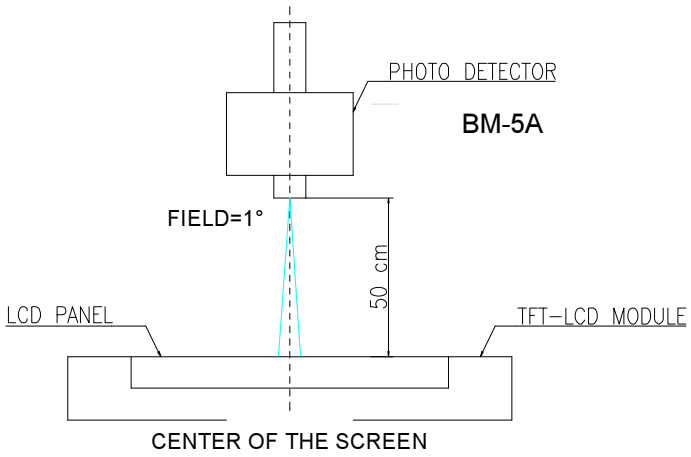
D. Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time								
Rise		Tr	θ=0°	--	4	8	ms	Note 3
Fall		Tf		--	16	32	ms	
Contrast ratio		CR	At optimized viewing angle	300	400	--		Note 4
Viewing Angle	Top		CR≧10	40	50	--	deg.	Note 5
	Bottom			55	65	--		
	Left			60	70	--		
	Right			60	70	--		
Transmission		Y_L	θ=0°	4.0	4.5	--	%	

Note 1: Ambient temperature =25℃, and LED lightbar voltage V_L = 12 V. To be measured in the dark room.

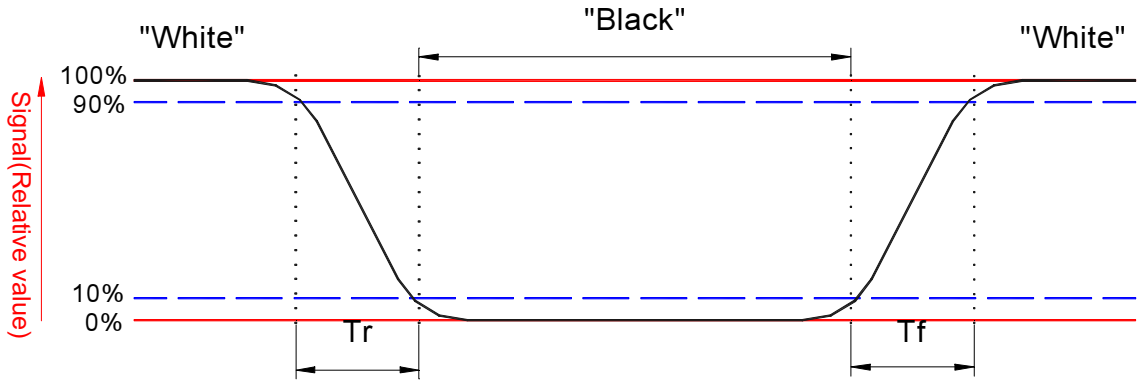
Note 2: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 15 minutes operation.



Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

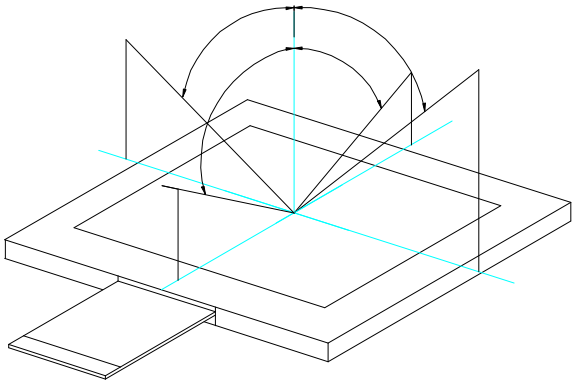


Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

Note 5. Definition of viewing angle, θ, Refer to figure as below.



E. Reliability Test Items

No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 70□ 240Hrs	
2	Low Temperature Storage	Ta= -20□ 240Hrs	
3	High Ttemperature Operation	Tp= 60□ 240Hrs	
4	Low Temperature Operation	Ta= -10□ 240Hrs	
5	High Temperature & High Humidity	Tp= 50□. 80% RH 240Hrs	Operation
6	Heat Shock	-10□~60□, 50 cycle, 1Hrs/cycle	Non-operation
7	Vibration (With Carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
8	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

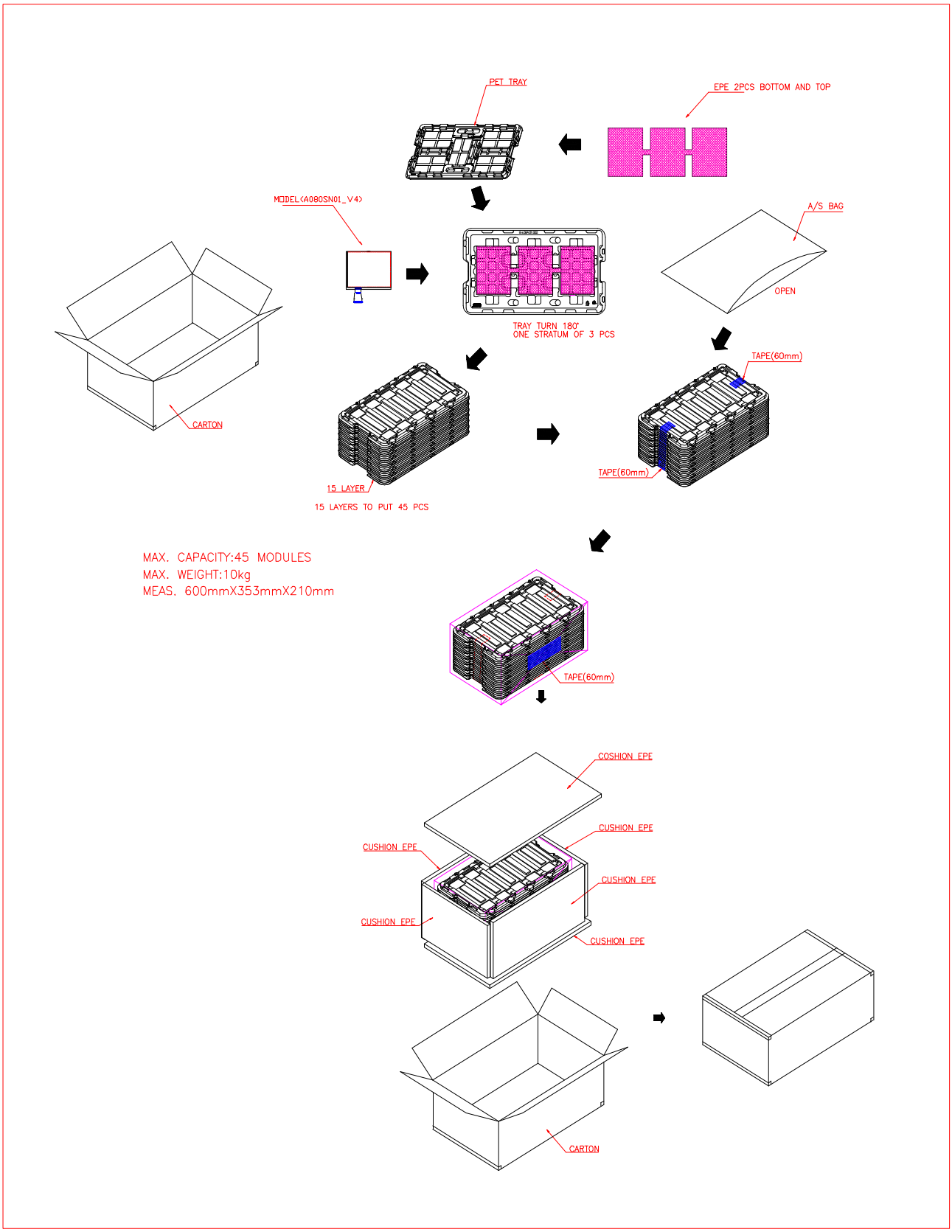
Note 1: Ta: Ambient Temperature. Tp: Panel Surface Temperature

Note 2: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Note 3: All the cosmetic specification is judged before the reliability stress.

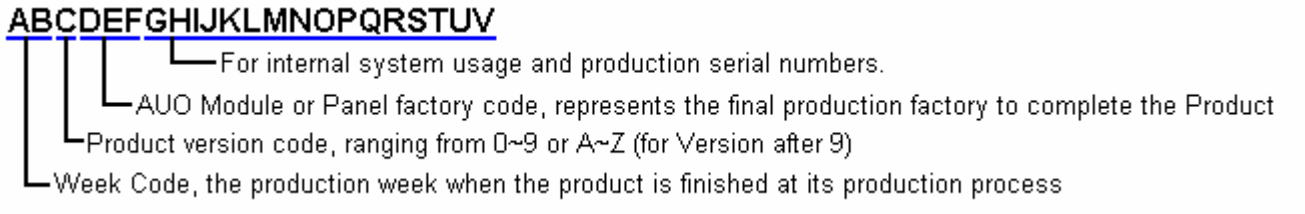
F. Packing and Marking

1. Packing Form



2. Module/Panel Label Information

The module/panel (collectively called as the “Product”) will be attached with a label of Shipping Number which represents the identification of the Product at a specific location. Refer to the Product outline drawing for detailed location and size of the label. The label is composed of a 22-digit serial number and printed with code 39/128 with the following definition:



Example:

501M06ZL06123456781Z05:

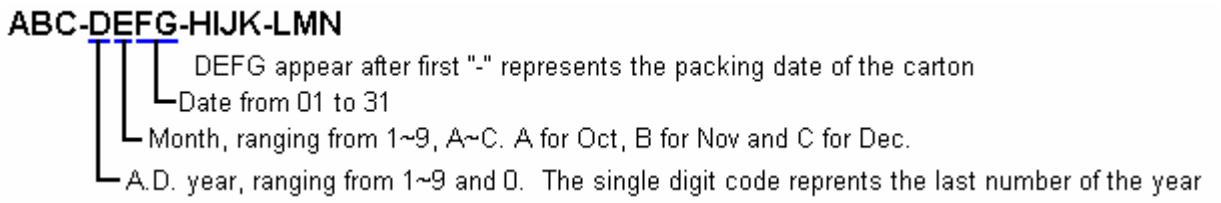
Product Manufacturing Week Code: WK50

Product Version: Version 1

Product Manufactuing Factory: M06

3. Carton Label Information

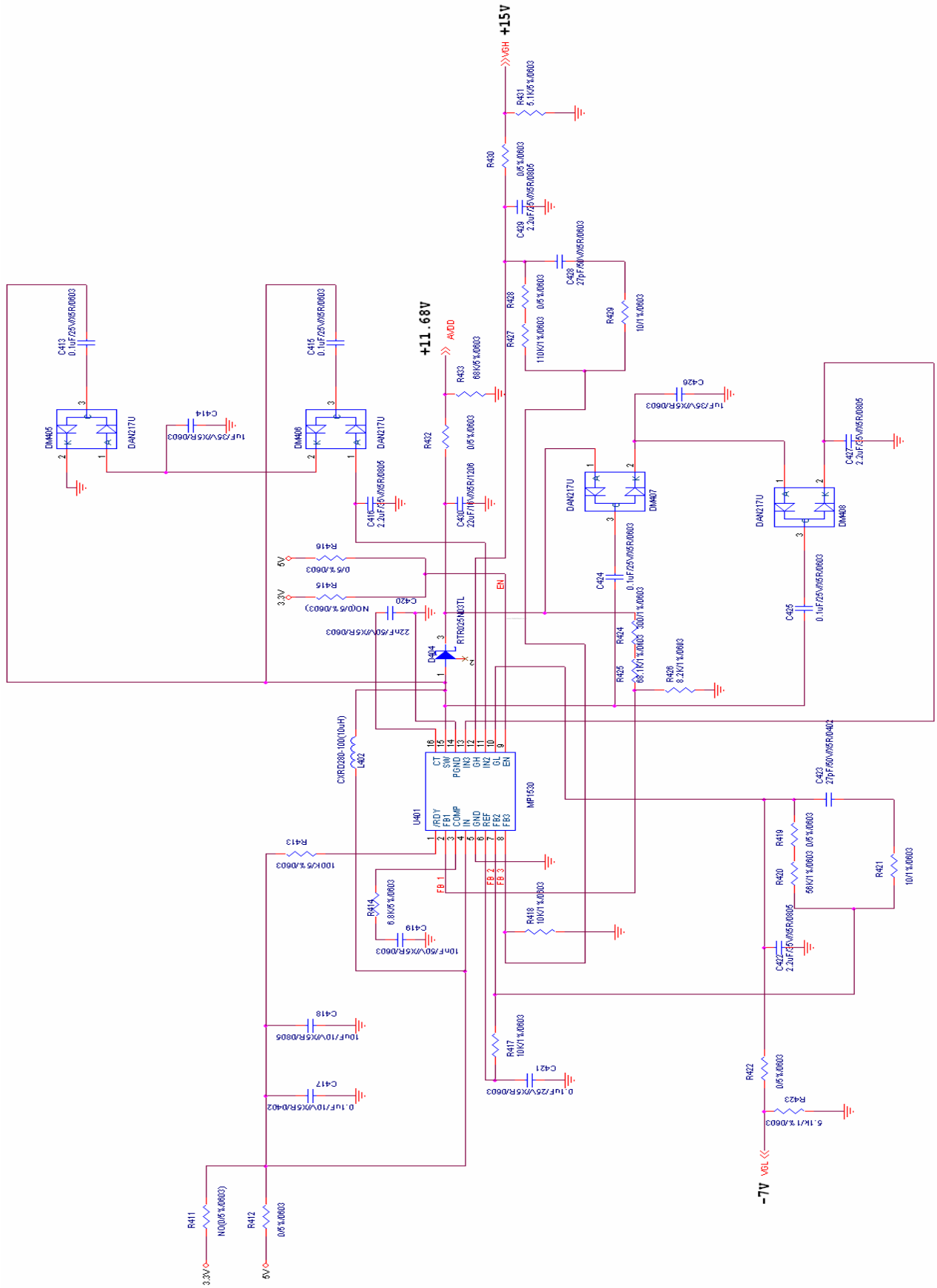
The packing carton will be attached with a carton label where packing Q’ty, AUO Model Name, AUO Part Number, Customer Part Number (Optional) and a series of Carton Number in 13 or 14 digits are printed. The Carton Number is apparing in the following format:

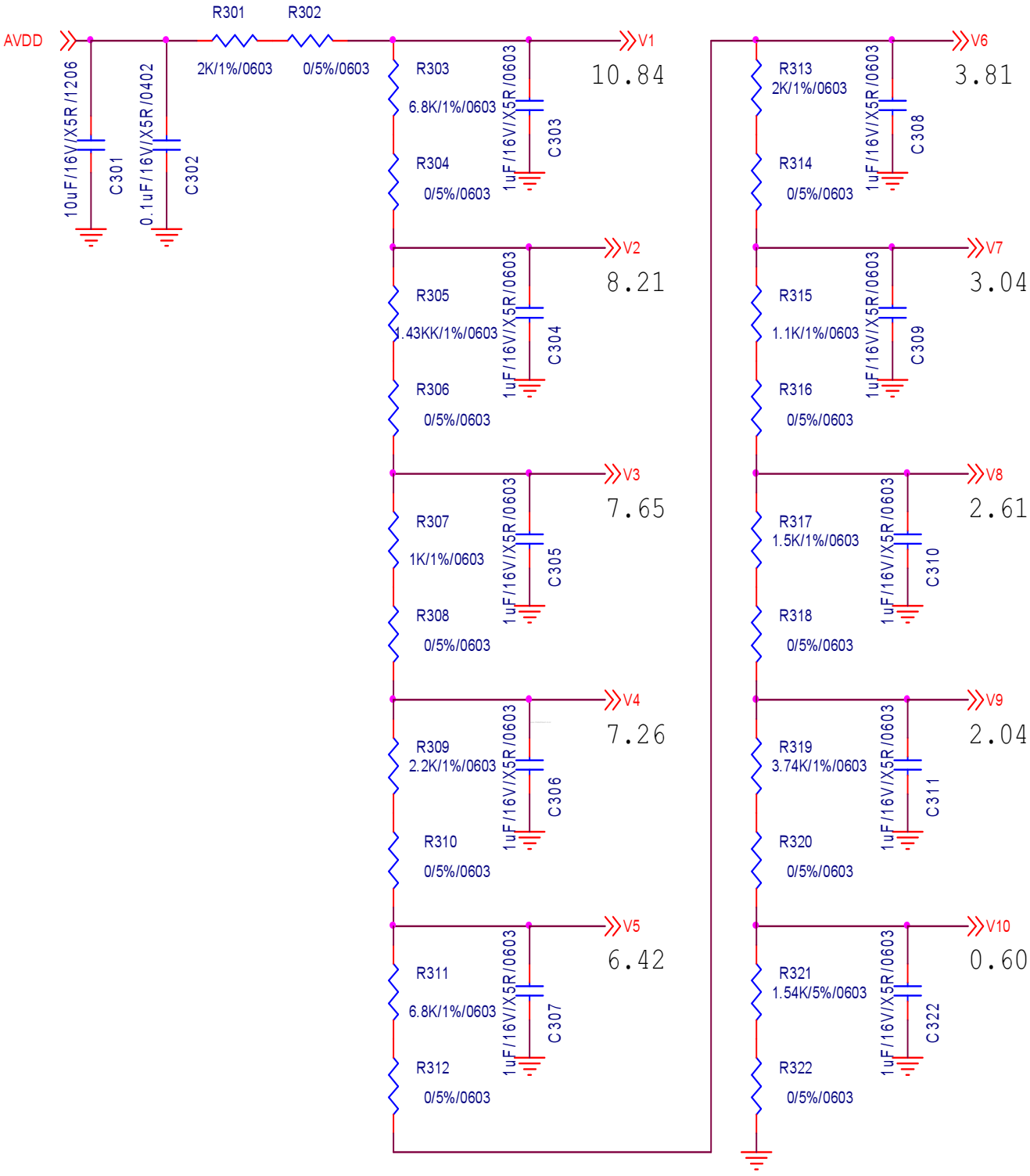


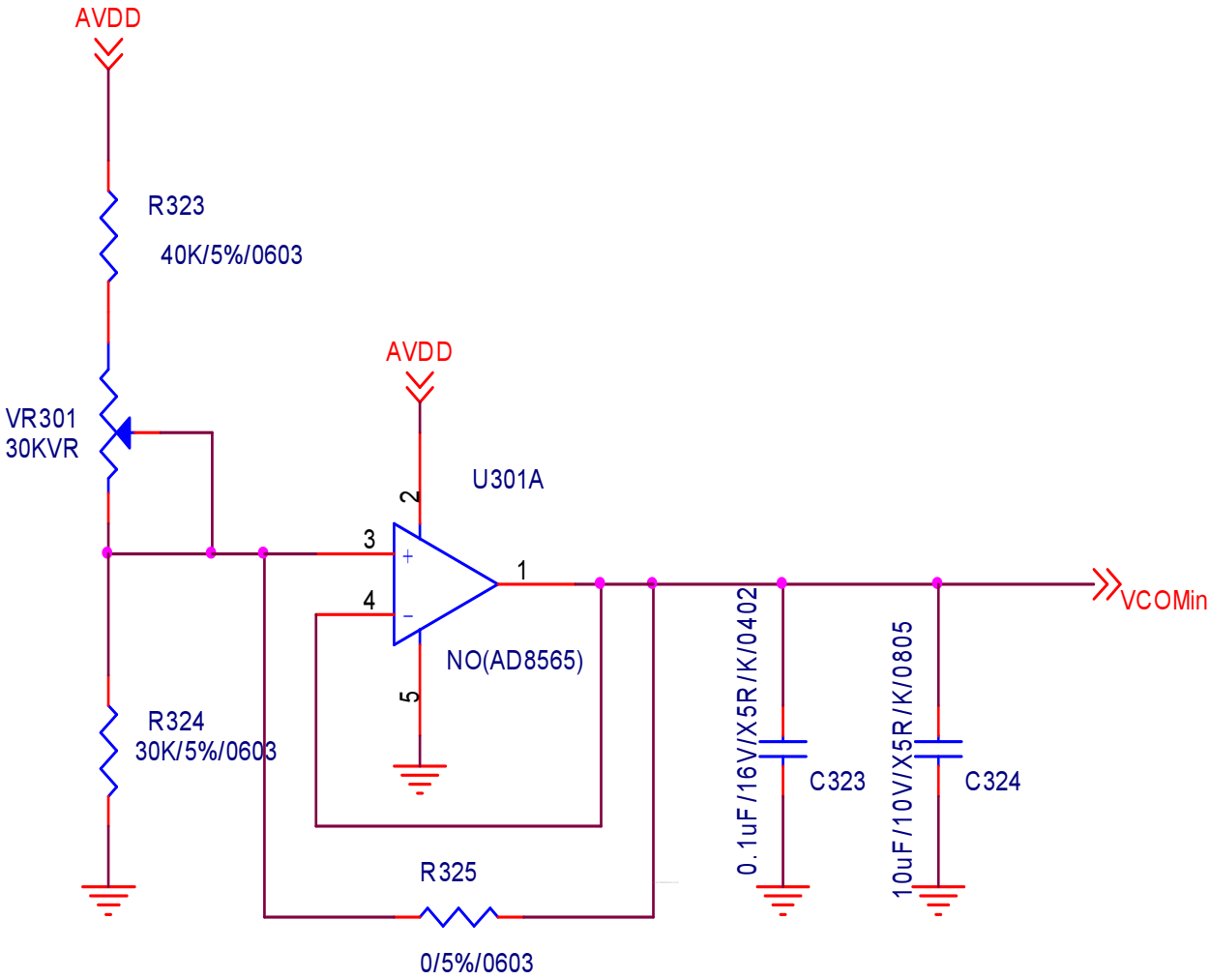
Refer to the drawing of packing format for the location and size of the carton label.

G. Application Note

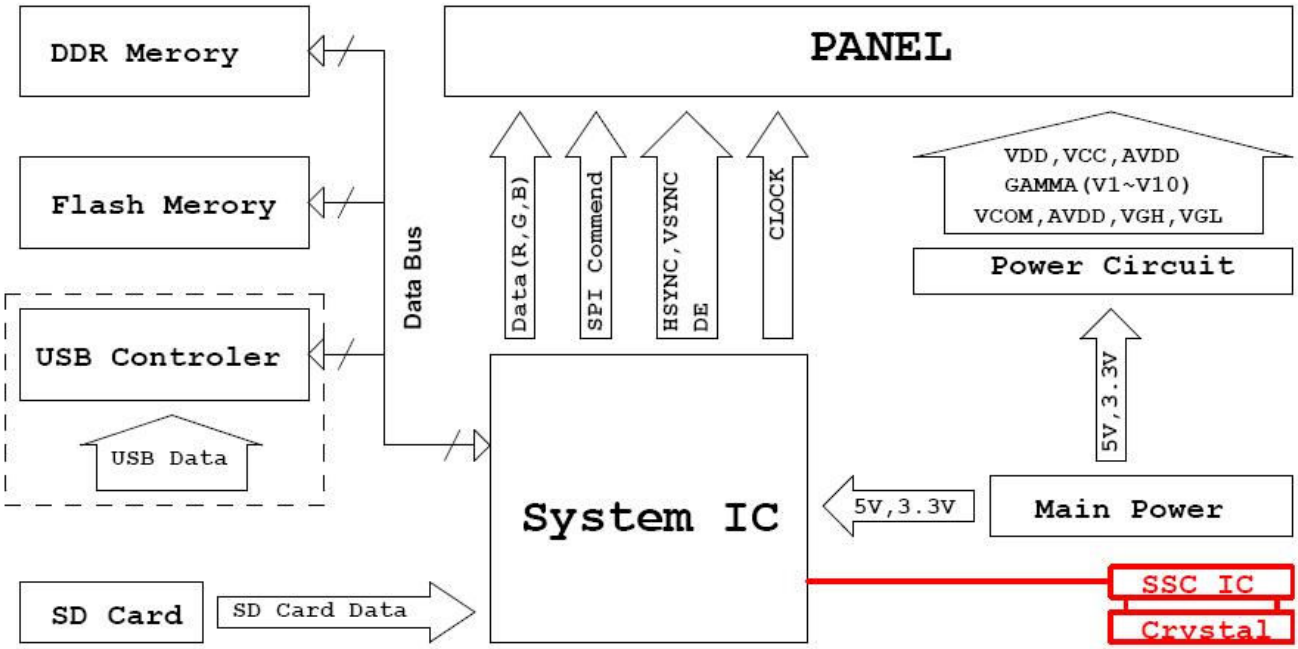
1. Application Circuit







2. System block



According to there are some risks of EMI issue.
Please refer to this function block before design.
If add SSC (Spread Spectrum Clocking) IC on the clock of system may cause USB abnormal work. Please add USB controller to control USB data.

H. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.