



SANYO Semiconductors

# DATA SHEET

## LA6261D — Monolithic Linear IC For Optical Disk Applications 6-channel Driver

### Overview

The LA6261D is a 6-channel driver (BTL: 4ch, H-bridge: 2ch) developed for use in optical disk applications.

### Functions

- Power amplifier 4-channel (BTL), 2-channel (H-bridge) built-in
- $I_O$  max 700mA (Each channel)
- Level shift circuit built-in (BTL AMP)
- Overheat protection circuit (thermal shutdown) built-in
- Separate power supply for H-bridge (2ch)
- 3.3V regulator controller incorporated (output transistor provided externally)
- With each H-bridge output control pin

### Specifications

Maximum Ratings at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}$ max		14	V
Maximum output current	$I_O$ max	Each channel for ch1 to ch6	0.7	A
Maximum input voltage	$V_{INB}$		13	V
Mute pin voltage	$V_{MUTE}$		13	V
Allowable power dissipation	$P_d$ max	Independent IC	1.2	W
Operating temperature	$T_{opr}$		-30 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

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**SANYO Semiconductor Co., Ltd.**

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## Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V <sub>CC</sub>		5.6 to 13	V

## Electrical Characteristics at Ta = 25°C, V<sub>CC1</sub>=V<sub>CC2</sub>=8V, V<sub>REF</sub>=1.65V, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
<b>All Blocks</b>						
No-load current drain ON	I <sub>CC-ON</sub>	All outputs ON *1 FWD = REV = 0V		30	50	mA
VREF Input voltage range	VREF-IN		1		V <sub>CC</sub> -1.5	V
<b>BTL AMP Block</b>						
Output offset voltage	V <sub>OFF</sub>	Voltage difference between channels	-50		50	mV
Input voltage range	V <sub>IN</sub>	Input to V <sub>IN</sub> 1,2,3 and 4	0		V <sub>CC</sub>	V
Output voltage (Saturated)	V <sub>O</sub>	Voltage between each V <sub>O</sub> <sup>+</sup> and V <sub>O</sub> <sup>-</sup> with R <sub>L</sub> = 8Ω	4	5		V
Closed-circuit voltage gain	VG	Gain between input and output		4		Times
Input voltage for MUTE ON	V <sub>MTON</sub>	*3	2		SV <sub>CC</sub>	V
Input voltage for MUTE OFF	V <sub>MTOFF</sub>	*3	0		0.5	V
Slew rate	SR	×2 between the amp and output		0.5		V/μs
<b>H Bridge Block</b>						
Output voltage (Saturated)	V <sub>O-LOAD</sub>	Voltage between each V <sub>O</sub> <sup>+</sup> and V <sub>O</sub> <sup>-</sup> with R <sub>L</sub> =10Ω *2	6.2	6.7		V
Input low-level	V <sub>IN-L</sub>		0		1	V
Input high-level	V <sub>IN-H</sub>		2		SV <sub>CC</sub>	V
Output voltage (Controlled)	V <sub>CONT</sub>	Voltage between each V <sub>O</sub> <sup>+</sup> and V <sub>O</sub> <sup>-</sup> with V <sub>CONT</sub> = 3V and R <sub>L</sub> = 10Ω		2.8		V
<b>Regulator Block</b>						
Output voltage	V <sub>reg</sub>	I <sub>L</sub> = 100mA	3.05	3.3	3.55	V
Fluctuating output load	ΔV <sub>RL</sub>	I <sub>L</sub> = 0 to 200mA	-50	0	10	mV
Fluctuating supply voltage	ΔV <sub>VCC</sub>	V <sub>CC</sub> = 6 to 12V, I <sub>L</sub> = 100mA	-15	21	60	mV

\*1 Total current dissipation of SV<sub>CC</sub>, PV<sub>CC1</sub> and PV<sub>CC2</sub> at no load.

\*2 Output in the saturated condition.

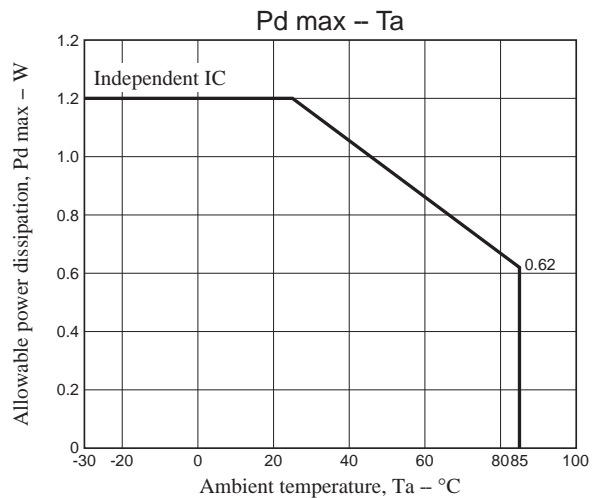
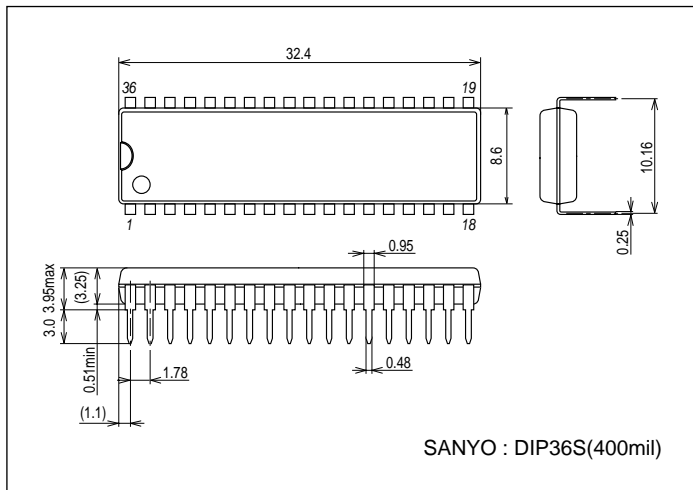
\*3 BTL output ON with MUTE: [H] and BTL output OFF (HI impedance) with MUTE: [L].

\*4 Design value

## Package Dimensions

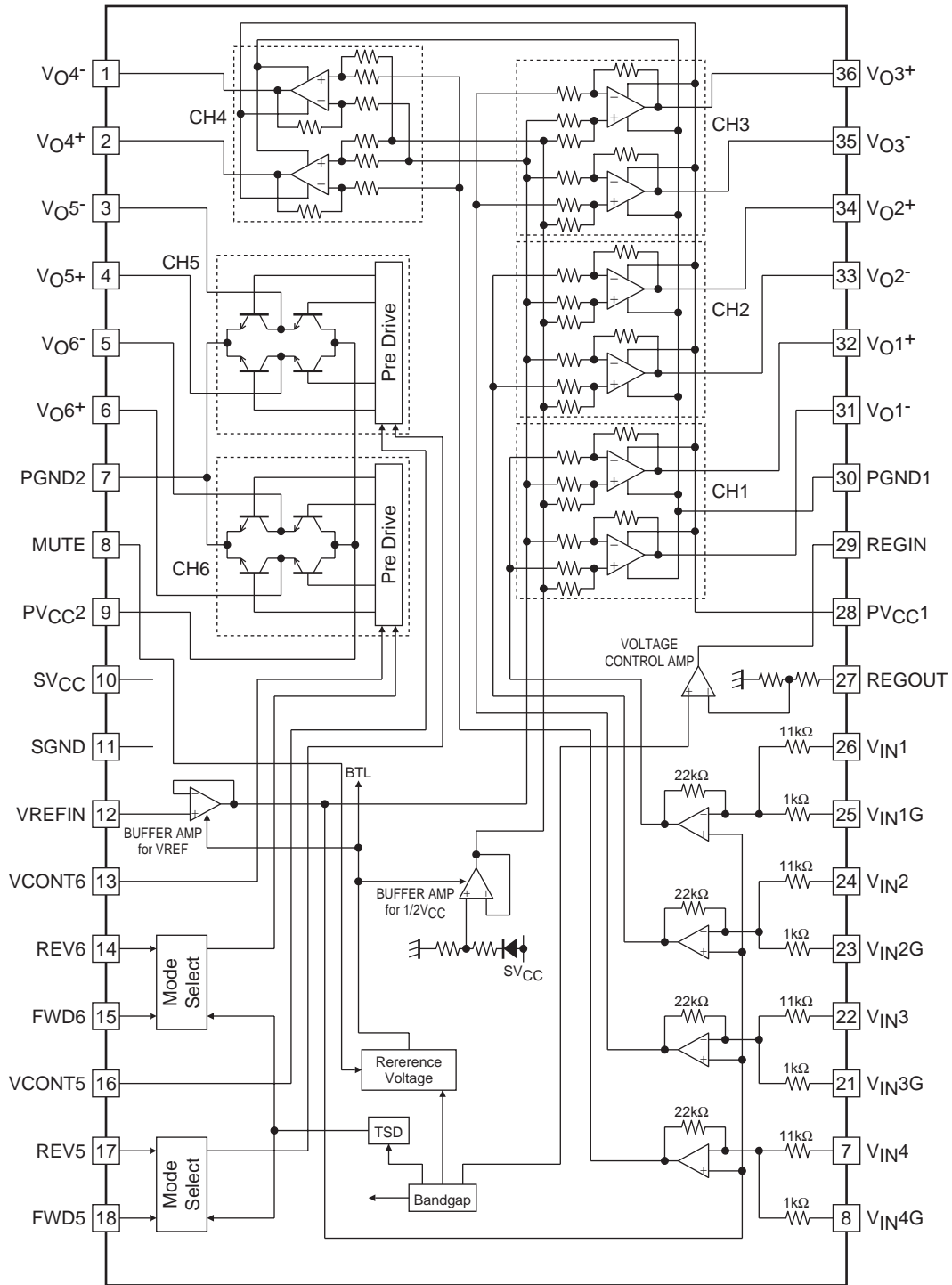
unit : mm (typ)

3170A



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## Block Diagram



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## Pin Function

Pin No.	Pin Name	function	Equivalent circuit
1 2 28 30 31 32 33 34 35 36	V <sub>O</sub> 4 <sup>-</sup> V <sub>O</sub> 4 <sup>+</sup> PV <sub>CC</sub> 1 PGND1 V <sub>O</sub> 1 <sup>-</sup> V <sub>O</sub> 1 <sup>+</sup> V <sub>O</sub> 2 <sup>-</sup> V <sub>O</sub> 2 <sup>+</sup> V <sub>O</sub> 3 <sup>-</sup> V <sub>O</sub> 3 <sup>+</sup>	BTL Output pin (-) for channel 4 BTL Output pin (+) for channel 4 Power for channels 1,2,3 and 4 (BTL), (SV <sub>CC</sub> short-circuited) Power GND for channels 1,2,3 and 4 (BTL) BTL Output pin (-) for channel 1 BTL Output pin (+) for channel 1 BTL Output pin (-) for channel 2 BTL Output pin (+) for channel 2 BTL Output pin (-) for channel 3 BTL Output pin (+) for channel 3	
3 4 5 6 7 9	V <sub>O</sub> 5 <sup>-</sup> V <sub>O</sub> 5 <sup>+</sup> V <sub>O</sub> 6 <sup>-</sup> V <sub>O</sub> 6 <sup>+</sup> PGND2 PV <sub>CC</sub> 2	H-bridge Output pin (-) for channel 5 H-bridge Output pin (+) for channel 5 H-bridge Output pin (-) for channel 6 H-bridge Output pin (+) for channel 6 Power GND for channels 5 and 6 (H-bridge) Power for channels 5 and 6 (H-bridge)	
8	MUTE	Input pin for BTL mute	
12	VREFIN	Reference voltage input pin	
13 16	VCONT6 VCONT5	Input pin for CH6 output voltage control Input pin for CH5 output voltage control	
14 15 17 18	REV6 FWD6 REV5 FWD5	CH6 Output change pin (REV), Logic input for H bridge CH6 Output change pin (FWD), Logic input for H bridge CH5 Output change pin (REV), Logic input for H bridge CH5 Output change pin (FWD), Logic input for H bridge	

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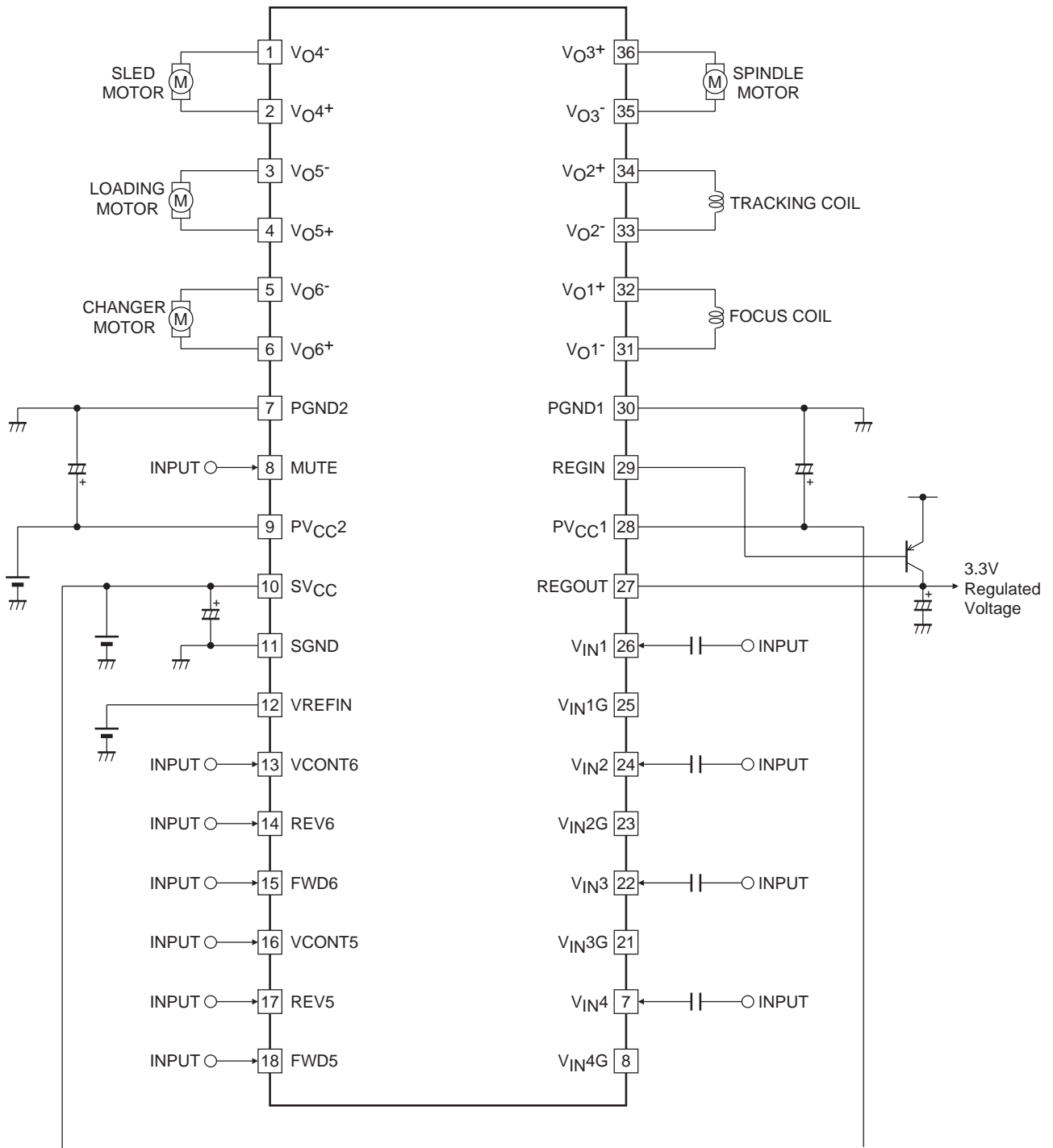
Pin No.	Pin Name	function	Equivalent circuit
19 20 21 22 23 24 25 26	$V_{IN4G}$ $V_{IN4}$ $V_{IN3G}$ $V_{IN3}$ $V_{IN2G}$ $V_{IN2}$ $V_{IN1G}$ $V_{IN1}$	Input pin for channel 4 (for gain control) Input pin for channel 4 Input pin for channel 3 (for gain control) Input pin for channel 3 Input pin for channel 2 (for gain control) Input pin for channel 2 Input pin for channel 1 (for gain control) Input pin for channel 1	
27	REGOUT	Regulator pin (External PNP collector)	
29	REGIN	Regulator pin (External PNP base)	

## Truth Table (H Bridge)

INPUT		OUTPUT	
FWD5(6)	REV5(6)	$V_{O5(6)^+}$	$V_{O5(6)^-}$
L	L	Z	Z
L	H	H	L
H	L	L	H
H	H	L	L

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## Application Circuit Example



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