8-Port 10M/100M Ethernet Switch

GENERAL DESCRIPTION

The MTD508 complies fully with the IEEE802.3, 802.3u and 802.3x specifications and is a non-blocking 8-port 10M/100M Ethernet switch device.

The MTD508 supports 8 RMII ports for 10M/100M operations. 1MBytes/2MBytes memory interface provides maximum 1365 packet buffers for Ethernet packet buffering. Up to 8192 address entries are provided by the MTD508, and the MTD508 uses full Ethernet address to compare algorithm for minimizing hashing collision events.

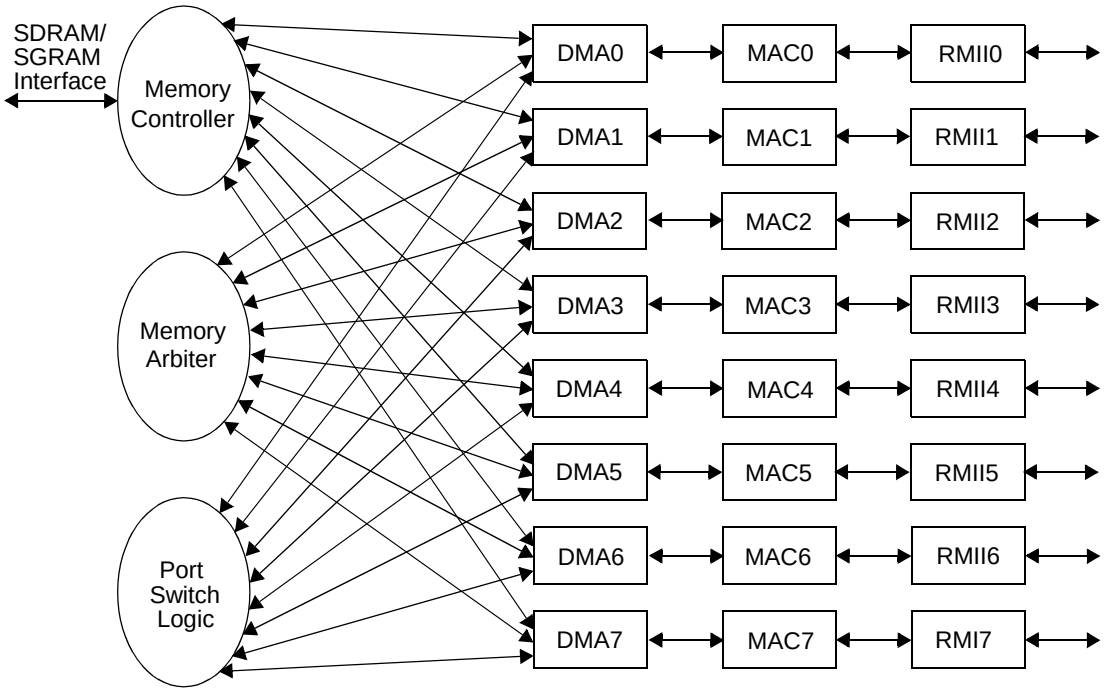
The MTD508 provides EEPROM interface to configure port trunking, port VLAN, static entry, 802.3x flow control threshold, flooding port, broadcast control threshold. Each MTD508 port supports 10M/100M auto-negotiation by MDC/MDIO interface for connecting external PHY devices.

The MTD508 also provides 10 pins for Link/RX activities, packet butter utilization LED display functoin.

FEATURES

- IEEE802.3 and IEEE802.3u compliant.
- Provides 8 RMII (Reduced Media Independent Interface) ports.
- Programmable 1K/8K MAC addresses filtering.
- Store and forward switching function and bad packet filtering function.
- Optional back-pressure/802.3x flow control/ flooding control/broadcast control.
- Optional EEPROM interface for advanced switch configurations.
- 1MB/2MB SGRAM/SDRAM flexible memory interface.
- Port VLAN/trunking.
- Link/Rx activities, packet buffer utilization LED display.
- 75MHz for non-blocking for 8-port switch operation.
- Built-in interna/external memory test function.
- 160-pin PQFP package, 3.3V operating voltage.

BLOCK DIAGRAM

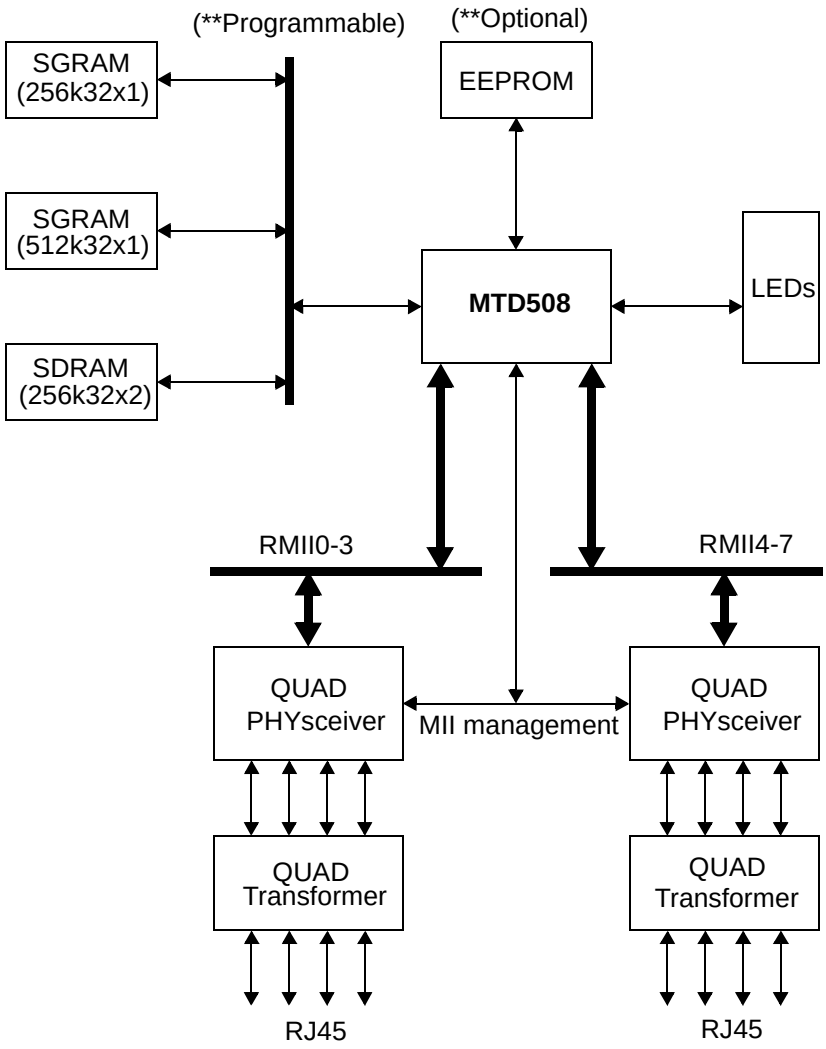


Myson-Century Technology, Inc.
Taiwan:
No. 2, Industry East Rd. III,
Science-Based Industrial Park, Hsin-Chu, Taiwan
Tel: 886-3-5784866 Fax: 886-3-5784349

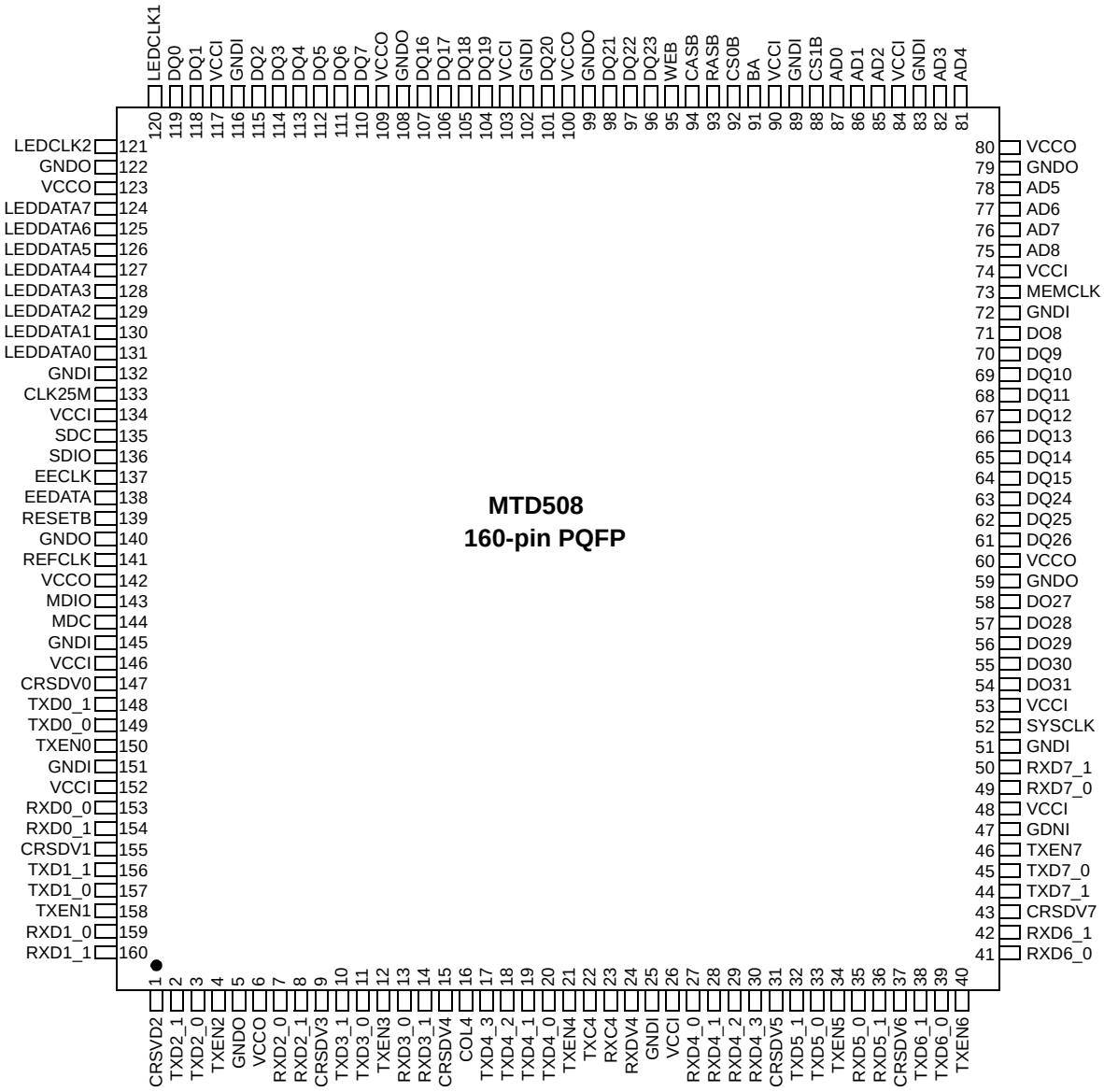
USA:
4020 Moorpark Avenue Suite 115
San Jose, CA, 95117
Tel: 408-243-8388 Fax: 408-243-3188

Sales@myson.com.tw
www.myson.com.tw
www.century-semi.com

SYSTEM DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

RMII/MII Port Interface Pins			
Name	**I/O**	**Pin**	**Description**
CRSDV0	I	147	Port0 RMII receive interface signal, CRSDV0 is asserted high when port0 media is non-idle.
RXD0_0	I	153	Port0 RMII receive data bit0.
RXD0_1	I	154	Port0 RMII receive data bit1.
TXEN0	O	150	Port0 RMII transmit enable signal.
TXD0_0	O	149	Port0 RMII transmit data bit0.
TXD0_1	O	148	Port0 RMII transmit data bit1.
CRSDV1	I	155	Port1 RMII receive interface signal, CRSDV1 is asserted high when port1 media is non-idle.
RXD1_0	I	159	Port1 RMII receive data bit0.
RXD1_1	I	160	Port1 RMII receive data bit1.
TXEN1	O	158	Port1 RMII transmit enable signal.
TXD1_0	O	157	Port1 RMII transmit data bit0.
TXD1_1	O	156	Port1 RMII transmit data bit1.
CRSDV2	I	1	Port2 RMII receive interface signal, CRSDV2 is asserted high when port2 media is non-idle.
RXD2_0	I	7	Port2 RMII receive data bit0.
RXD2_1	I	8	Port2 RMII receive data bit1.
TXEN_2	O	4	Port2 RMII transmit enable signal.
TXD2_0	O	3	Port2 RMII transmit data bit0.
TXD2_1	O	2	Port2 RMII transmit data bit1.
CRSDV3	I	9	Port3 RMII receive interface signal, CRSDV3 is asserted high when port3 media is non-idle.
RXD3_0	I	13	Port3 RMII receive data bit0.
RXD3_1	I	14	Port3 RMII receive data bit1.
TXEN3	O	12	Port3 RMII transmit enable signal.
TXD3_0	O	11	Port3 RMII transmit data bit0.
TXD3_1	O	10	Port3 RMII transmit data bit1.
CRSDV4	I	15	Port4 RMII receive interface signal, CRSDV2 is asserted high when port4 media is non-idle.
RXDV4	I	24	Port4 MII receive data valid. In RMII mode, this pin is not used.
RXCLK4	I	23	Port4 MII receive clock signal. In RMII mode, this pin is not used.
RXD4_3	I	30	Port MII receive data bit3. In RMII mode, this pin is not used.
RXD4_2	I	29	Port MII receive data bit2. In RMII mode, this pin is not used.
RXD4_0	I	27	Port MII receive data bit0.
RXD4_1	I	28	Port MII receive data bit1.
TXEN4	O	21	Port4 RMII transmit enable signal.

RMII/MII Port Interface Pins			
Name	**I/O**	**Pin**	**Description**
TXCLK4	I	22	Port4 RMII transmit clock signal. In RMII mode, this pin is not used.
TXD4_3	O	17	Port4 MII transmit data bit3. In RMII mode, this pin is not used.
TXD4_2	O	18	Port4 MII transmit data bit2. In RMII mode, this pin is not used.
TXD4_0	O	20	Port4 RMII/MII transmit data bit0.
TXD4_1	O	19	Port4 RMII/MII transmit data bit1.
COL4	I	16	Port4 MII collision input. In RMII mode, this pin is not used.
CLK25M	O	155	Port4 MII 25MHz clock output.
CRSDV5	I	31	Port5 RMII receive interface signal, CRSDV5 is asserted high when port5 media is non-idle.
RXD5_0	I	35	Port5 RMII receive data bit0.
RXD5_1	I	36	Port5 RMII received data bit1.
TXEN5	O	34	Port5 RMII transmit enable signal.
TXD5_0	O	33	Port5 RMII transmit data bit0.
TXD5_1	O	32	Port5 RMII transmit data bit1.
CRSDV6	I	37	Port6 RMII receive interface signal, CRSDV6 is asserted high when port5 media is non-idle.
RXD6_0	I	41	Port6 RMII receive data bit0.
RXD6_1	I	42	Port6 RMII received data bit1.
TXEN6	O	40	Port6 RMII transmit enable signal.
TXD6_0	O	39	Port6 RMII transmit data bit0.
TXD6_1	O	38	Port6 RMII transmit data bit1.
CRSDV7	I	43	Port7 RMII receive interface signal, CRSDV7 is asserted high when port5 media is non-idle.
RXD7_0	I	39	Port7 RMII receive data bit0.
RXD7_1	I	50	Port7 RMII received data bit1.
TXEN7	O	46	Port7 RMII transmit enable signal.
TXD7_0	O	45	Port7 RMII transmit data bit0.
TXD7_1	O	44	Port7 RMII transmit data bit1.

SGRAM/SDRAM Interface Pins			
Name	**I/O**	**Pin**	**Description**
AD[8:0]	O	75-78, 81-82, 85-87	Memory row/column address bus outputs. AD[7:0] are row/column address[7:0]. AD[8]: This pin should connect to SGRAM/SDRAM MSB address bit.
DQ[31:0]	I/O	54-58, 61-71, 96-98, 101, 104-107, 110-115, 118-119	Memory data bus.
RASB	O	93	SGRAM/SDRAM row address select.

SGRAM/SDRAM Interface Pins			
Name	**I/O**	**Pin**	**Description**
CASB	O	94	SGRAM/SDRAM column address select.
WEB	O	95	SGRAM/SDRAM write enable.
BA	O	91	SGRAM/SDRAM bank select.
CS0B	O	92	Memory chip select 0.
CS1B	O	88	Memory chip select 1.
MEMCLK	O	73	Memory clock output.

LED Interface Pins			
Name	**I/O**	**Pin**	**Description**
LEDDATA[7:0]	I/O	124-131	LED data output. These LED pins report ports0‘7 Link/Rx activities using LEDCLK1 strobe, and report packet buffer utilization status using LEDCLK2 strobe. LEDDATA [0] [1] [2] [3] [4] [5] [6] [7] LEDCLK1 LR0 LR1 LR2 LR3 LR4 - - - LEDCLK2 Uti0 Uti1 Uti2 Uti3 Uti4 - BFull MFail **Note:** LRn: per port’s Link_RxAct status; Uti0: 5%, Uti1: 10%, Uti: 20%, Uti3: 35%, Uti4: 50% and above; BFull: buffer almost full alarm signal; MFail: external memory poer on test failure.
LEDCLK1	I/O	120	LED strobe 1.
LEDCLK2	I/O	121	LED strobe 2.

Miscellaneous Pins			
Name	**I/O**	**Pin**	**Description**
RESETB	I	139	System reset input, low active.
SYSCLK	I	52	Switch core system clock input, using the same clock source with REFCLK.
REFCLK	I	141	RMII reference clock input, using 50MHz.
MDC	I/O	144	MII management clock inout.
MDIO	I/O	143	MII management data inout.
SDC	I/O	135	MII register clock inout.
SDIO	I/O	136	MII register data inout.
EEDATA	I/O	138	EEPROM data input.
EECLK	I/O	137	EEPROM clock output.

Miscellaneous Pins			
Name	**I/O**	**Pin**	**Description**
VCC	PWR	6, 26, 48, 53, 60, 74, 80, 84, 90, 100, 103, 109, 117, 123, 134, 142, 146, 152	Power pins.
GND	GND	5, 25, 47, 51, 59, 72, 79, 83, 89, 99, 102, 108, 116, 122, 132, 140, 145, 151	Ground pins.

Jumper Configuration After Power On Reset			
Name	**I/O**	**Pin**	**Description**
LEDDATA[0] LEDDATA[1] LEDDATA[2] LEDDATA[3] LEDDATA[4] LEDDATA[5] LEDDATA[6] LEDDATA[7]	I/O		During power on reset duration, these pins are jumper setting pins (pull_high = 1, pull_low = 0). LEDDATA[0]: select SFRAM/SDRAM interface, 1:256K32 x 1 or 512K32 is selected; 0: 256K32 x 2 is selected. The default value is “1”. LEDDATA[1]: configure packet buffer size, 1: 2M bytes buffer size is selected; 0: 1M bytes buffer size is selected. The default value is “0”. LEDDATA[2]: enable memory test function, 1: enable; 0: disable. The default value is “1”. LEDDATA[3]: enable aging function, 1: enable; 0: disable. The default value is “1”. LEDDATA[4]: enable MII polling (MDC/MDIO), 1: enable; 0: disable. The default value is “1”. LEDDATA[5]: enable broadcast storm control, 1: enable; 0: disable. The default value is “1”. LEDDATA[6]: enable backpressure function, 1: enable; 0: disable. The default value is “1”. LEDDATA[7]: enable 802.3x flow control function (in full mode), 1: enable; 0: disable. The default value is “1”.
LEDCLK1	I/O		During power on reset duratoion, this in is a jumper setting pin (pull_high = 1, pull_low = 0). LEDCLK1: select 1K or 8K address entry table, 1: 8K entry address is selected; 0: 1K address entry is selected. The default value is “1”.
LEDCLK2	I/O		During power on reset duration, this in is a jumper setting pin (pull_high = 1, pull_low = 0). LEDCLK2: enable EEPROM interface, 1: enable; 0: disable. The default value is “1”.
EEDATA	I/O		During power on reset duration, this pin is a jumper setting pin (pull_high = 1, pull_low = 0). EEDATA: enable EEPROM auto-load configuration function while EEPROM interface is enabled, 1: enable; 0: disable. The default value is “1”.

Jumper Configuration After Power On Reset			
Name	**I/O**	**Pin**	**Description**
TXEN[2:0]	I/O		During power on reset duration, this pin is a jumper setting pin (pull_high = 1, pull_low = 0). TXEN[2:0]: uplink port (flooding port) 0-7 selection. The default value is “000”.
TXEN[3]	I/O		During power on reset duration, this pin is a jumper setting pin (pull_high = 1, pull_low = 0). TXEN[3]: enable flooding control, 1: enable; 0: disable. The default value is “1”.
TXEN[4]	I/O		During power on reset duration, this pin is a jumper setting pin (pull_high = 1, pull_low = 0). TXEN[4]: enable VLAN tag 1522 bytes receiving, 1: enable; 0: disable. The default value is “0”.
TXEN[5]	I/O		During power on reset duration, this pin is a jumper setting in (pull_high = 1, pull_low = 0). TXEN[5]: select Port7 full/half ability while Port7 is in FX mode, 1: Port7 full duplex is selected; 0: Port7 half duplext is selected. The default value is “0”.
TXEN[7]	I/O		During power on reset duration, this pin is a jumper setting in (pull_high = 1, pull_low = 0). TXEN[7]: enable Port7 FX mode, 1: enable; 0: disable. The default value is “0”.
SDC	I/O		During power on reset duration, this pin is a jumper setting pin (pull_high = 1, pull_low = 0). SDC: Port4 MII/RMII interface selection, 1: Port4 MII interface is selected, and in the meantime, Port5, 6, 7 are automatically disabled; 0: Port4 RMII interface is selected. The default value is “0”.
EECLK	I/O		During power on reset duration, this pin is a jumper setting pin (pull_high = 1, pull_low = 0). EECLK: scan mode enable for debugging purpose, 1: scan mode enable, 0: scan mode disable. The default value is “0”.
MDC	I/O		During power on reset duration, this pin is a jumper setting pin (pull_high = 1, pull_low = 0). MDC: fast mode enable, 1: fast mode enable; 0: fast mode disable. the default value is “0”.

FUNCTIONAL DESCRIPTION

The MTD508 is an 8-port 10/100Mbps fast Ethernet switch controller. It is a low-cost solution for eight ports fast Ethernet SOHO switch design. No CPU interface is required. After power on reset, the MTD508 provides an auto load configuration setting function through a 2-wire serial EEPROM interface to access external EEPROM device, and the MTD508 can easily be configured to support port-trunking, port-VLAN, static entry, 802.3x flow control threshold setting, flooding port assignment... etc. functions. The following descriptions are the MTD508's major function blocks overview.

Packet Store and Fowarding

The MTD508 uses simple store and forward algorithm as packet switching method. Input packet from ports will be stored to external memory first, while packet is good for forwarding (CRC check okay, 64Bytes < length < 1518Bytes, not local packets, in the same VLAN group), if this packet's DA hits, then forward this packet to the destination port, otherwise this packet will be broadcasted.

Learing and Routing

The MTD508 supports 1K or 8K MAC entries for switching. Dynamic address learing is performed by each good unicast packet is completely received. The static address learning achieved by EEPROM configuration. On the other hand, the routing process is performed whenever the packet's DA is captured. If the DA cannot get a hit result, the packet is going to switch broadcast or forward to the dedicated port according to the flooding control selection.

Aging

Only the dynamic address entries are scheduled int he aging machine. If one station does not transmit any packet for a period of time, the belonging MAC address will be kicked out from the address table. The aging out time can be programmed through the EEPROM auto load configuration. (Default value is 300 seconds.)

Buffer Queue Management

The buffer queue manager is implemented to manage the external shared memory (use SDRAM/SGRAM) for packet buffering. The main function of the buffer queue manager is to maintain the linked list sonsisted of buffer IDs, which are used to show the corresponding memory address for each incoming packet. in addition, the buffer queue manager monitors the rested free spaces status of the external memory. If the packet storage achieves the predefined threshold value, the buffer queue manager will raise the alarm signal which is used to enable the flow control mechanism for avoiding transmission ID queue overflow happening. The MTD508 provides 802.3x flow control in full duplex mode and back pressure control in half duplex mode.

Full Duplex 802.3x Flow Control

In full duplex mode, the MTD508 supports the standard flow control defined in IEEE802.3x standard. It enables the stopping of remote node transmissions via a PAUSE frame information interaction. When the "802.3x flow control enable" bit is set during power on reset (LEDDATA[7] pin is external pull_high), it enables the MTD508 supporting 802.3x flow control function in full duplex mode; when output port buffer queue's on-using value reaches the initialization setting threshold value (recommended Xon_TH = 74h when using 2Mbytes external memory; Xon_TH = 2eh when using 1Mbytes external memory), the MTD508 will send out a PAUSE packet with pause time equal to FFF to stop the remote node transmission. When the output port buffer queue's on-using value reduces to the initialization threshold value (recommended Xoff_TH = 30h when using 2Mbytes external memory; Xoff_TH = 18h when using 1Mbytes external memory), the MTD508 will also send a PAUSE packet with pause time equal to zero to inform the remote node to retransmit packet.

Half Duplex Back Pressure Control

In halp duplex mode, the MTD508 provides a back pressure control mechanism to avoid dropping packets during network congestion. When the "back pressure control enable" bit is set during power on reset (LEDDATA[6]pin is

external pull_high), it enables the MTD508 supporting back pressure function in half-duplex mode. When output port buffer queue's on-using value reaches the initialization setting threshold value (same with the Xon_TH value), the MTD508 will send a JAM pattern in the input port when it senses an incoming packet, thus forcing a collision to inform the remote node transmission back off and will effectively avoid dropping packets. If the "back pressure control enable" bit is not set, and there is no free buffer queue available for the incoming packets, the incoming packets will be dropped.

MII Polling

The MTD508 supports PHY management through the serial MDIO/MDC interface. After power on reset, the MTD508 writes related abilities to the advertisement register 4 of connected PHY devices and restarts the auto-negotiation procedure via MDIO/MDC interface using the predefined PHY addresses increasingly from '01000'b to '01100'b. The MTD508 will lperiodically and continuously poll and update the link status and link partner's ability including speed, duplex mode, and 802.3x flow control capable status of the connected PHY devices through MDIO/MDC serial interface.

MAC and DMA Engine

The MTD508's MAC performs all functions in IEEE802.3 protocol, such as frame formatting, frame stripping, CRC checking, bad packet dropping, deferring to line traffic, and collision handling. The MAC Rx_engine checks incoming packets and drops the bad packet including CRC error, alignment error, short packet (less than 64 bytes) and long packet (more than 1518 bytes when the "VLAN tag 1522 bytes receive enable" bit is set during power on reset). Before transmission, the MAC Tx_engine will constantly monitor the line traffic using deferring procedure. Only if it has been idle for a half duplex mode, MAC engine will detect collision; if a collision is detected, the MAC Tx-engine will transmit a JAM pattern and then dalay the re-transmission for a random time period determined by the back-off algorithm (the MTD508 implements the truncated exponential back-off algorithm defined in IEEE802.3 standard). For the full duplex mode, collision signal is ignored.

The MTD508's DMA engine performs the packets non-blocking transmportation between MAC engine and external memory according to a high speed swetching procedure. The switching procedure is completed by address learning/routing process and buffer queue management operation.

EEPROM Interface

The MTD508 provides and auto load configuration setting function through a 2-wire serial EEPROM interface to access external EEPROM device (24C02) after power on reset. The MTD508 can easily be configured to support port-trunking, port-VLAN, static entry, 802.3x flow control threshold setting, flooding port assignment... etc functions. The following table is the EEPROM contents mapping:

Name	EEPROM Address	EEPROM Content Description	Recommended Value Under Basic Operation
EOB	00	Last EEPROM content address value	8h13
AgeLow	01	Aging Time bit [7:0]	8h2c
AgeHigh	02	Aging Time bit [15:8]	8h01
VLAN0	03	Port0 VLAN register	8hfe
VLAN1	04	Port1 VLAN register	8hfd
VLAN2	05	Port2 VLAN register	8hfb
VLAN3	06	Port3 VLAN register	8hf7
VLAN4	07	Port4 VLAN register	8hef
Reserved	08	Reserved	8hdf
Reserved	09	Reserved	8hbf

Name	EEPROM Address	EEPROM Content Description	Recommended Value Under Basic Operation
Reserved	0a	Reserved	8h7f
UpLink10	0b	bit[7:4] ⟶ the flooding port_no of Port1; bit[3:0] ⟶ the flooding port_no of Port0. *ex1: bit[7:4] = 'oo11'b, it means that if the incoming packet of Port1 gets the "un-routed" result, then this incoming packet will be flooded to Port3. *ex2: bit[3:0] = '0111'b, it means that if the incoming packet of Port0 gets the "un-routed" result, then this incoming packet will be flooded to Port7. (Note: Setting value to "4hf" means flooding to all the other ports; setting value to "4h8" to "4he" is forbidden.)	8h0f
UpLink32	0c	bit[7:4] ⟶ the flooding port_no of Port3; bit[3:0] ⟶ the flooding port_no of Port2. (Note: setting value to "4hf" means flooding to all ports; setting value to "4h8" to "4he" is forbidden.)	8h00
UpLink54	0d	bit[7:4] ⟶ reserved; bit[3:0] ⟶ the flooding port_no of Port4. (Note: Setting value to "f" means flooding to all the other ports; setting value to "8" to "h" is forbidden.)	8h00
Reserved	0e	Reserved	8h00
Broadcast TH	0f	Broadcast threshold	8hff
Xon TH	10	Xon threshold	8h74
Xoff TH	11	Xoff threshold	8h30
DisPort	12	Disable Port	8h00
System Control	13	System control byte: bit[0] ⟶ enhanced back pressure enable; bit[7:1] ⟶ reserved.	8h00
Reserved	14 - 1f	None	
StaticSA1	20 -26	Address 26 bit[2:0] ⟶ Port ID; Address 25 bit [7:0] ~ Address 20 bit[7:0] ⟶ static SA[47:0].	
StaticSA2	27 -2d	Address 2d bit[2:0] ⟶ Port ID; Address 2c bit [7:0] ~ Address 20 bit[7:0] ⟶ static SA[47:0].	

Port Based VLAN

The MTD508 supports VLAN configuration by port based methodology. One port selects the certain ports to form its VLAN group by configuring the VLAN register. The packet (including broadcast packet) is not forwarded to the destination port whose VLAN group is different from the source port.

Port Trunking

The port trunking function can also be implemented by VLAN registers. One trunk port isolates the packeting transmitting and receiving from the other trunk ports, which perform a logical trunk topology. The non-trunk port should choose only one trunk port for transmitting, which can achieve the load balancing and maintain the packet sequences.

Memory Interface

Two kinds of external memory interfaces can be selected by user, namely 1Mbyte memory (256K32 x 1) and 2Mbyte (256K32 x 2 or 512K x 1). Maximum 2Mbyte external memory can be used for packet buffering. "-10" speed grade of SGRAM/SDRAM device is recommended. The following table is the SGRAM application pin connection:

Memory Type	Memory Chip No.	A[8]	CS0B	CS1B
256K32	x 1	A8	CS0B	NC
236K32	x 2	A8	CS0B	CS1B
512K32	x 1	A9	CS0B	A8

Internal MII Registers Access and Control

The MTD508 supports 2 serial pins (SDIO/SDC) for internal registers access and control. The detailed registers information is presented in the section on “Internal MII Registers”.

LED Display

The MTD508 uses 10 pins to output two kinds of LED display: LEDDATA[7:0], LEDCLK1, and LEDCLK2. LEDCLK1 rising edge and LEDDATA[7:0] are used to report Port7-0 link/receive activity led status. LEDCLK2 rising edge and LEDDATA[4:0] are used to report packet buffer utilization rating, and LEDDATA[7] is used to report external memory test result (after power reset, the MTD508 will test external SDRAM automatically), and LEDDATA[6] reports the buffer almost full alarm signal.

INTERNAL MII REGISTERS

The MTD508 implements 10 MII global registers and 4-per-dot registers, defined as the following tables:

Table 1. MII Registers

Global Registers					
Reg No.	**Bit**	**Name**	**R/W**	**Description**	**Default**
0		CtlReg0	R/W	Control Register 0	
	8-0			bit[0]: 1 → switch to port 0 registers; bit[1]: 1 → switch to port 1 registers; bit[2]: 1 → switch to port 2 registers; bit[3]: 1 → switch to port 3 registers; bit[4]: 1 → switch to port 4 registers; bit[5]: reserved; bit[6]: reserved; bit[7]: reserved; bit[8]: 1 → switch to global registers.	9h100
	12-9			Scan mode select 3-0.	
	15-13			Scan port select.	
1		CtlReg1	R/W	Control Register 1	16h3084
	7-0	XON		XON threshold.	
	15-8	XOFF		XOFF threshold. While EEPROM is enabled, this register's content will be updated by EEPROM read XON/XOFF threshold data automatically. After EEPROM read is done, this register can be read/write by management cmd. The default value is "16h3084" (2M memory) or "16h1838" (1M memory).	
2		CtlReg2	R/W	Control Register 2	16'd300
	15-0	Aging		bit[15:0] can specify aging time. While EEPROM is enabled, this register's content will be updated by EEPROM read Aging timer data automatically. After EEPROM read is done, this register can be read/write by management cmd.	
3		CtlReg3	R/W	Control Register 3	16h000f
	15-0	Uplink Reg0		bit[15:12] specify uplink port ID of port 3; bit[11:8] specify uplink port ID of port 2; bit[7:4] specify uplink port ID of port 1; bit[3:0] specify uplink port ID of port 0. The default value is "16h000f". Note: The write sequence of this register is Jumper setting → EEPROM content → MII management command.	
4		CtlReg4	R/W	Control Register 4	16h0
	15-0	Uplink Reg1		bit[15:12]: reserved; bit[11:8]: reserved; bit[7:4]: reserved; bit[3:0]: specify port ID of port 4. The default value is "16h0". Note: The write sequence of this register is Jumper setting → EEPROM content → MII management command.	
5		CtlReg5	R/W	Control Register 5	16hff
	7-0			bit[7:0]: specify broadcast threshold.	
	8			bit[8]: enable enhance backpressure.	
	15-9			Reserved. Note: this register can be written by EEPROM content or MII management command.	
6		StsReg0	RO/RC	Status Register 0	

Global Registers					
Reg No.	**Bit**	**Name**	**R/W**	**Description**	**Default**
	7-0			bit[4:0]: output port4-0 RXDMA fifofull; bit[5]: reserved.	
	15-8			bit[12:8]: output port4-0 TXDMA TPUR (fifoempty); bit[15:13]: reserved.	
7		StsReg1	RO	Status Register 1	
				0: BufBistDone; 1: BufBistErr; 2: BufInitDone; 3: AddrTblBistDone; 4: AddrTblBistErr; 5: LthTblBistDone; 6: LthTblBistErr; 7: MemBistDone; 8: MemBistErr; 9: EEDone; 10: FreeCntls0; 15-11: reserved.	
8		CtlReg7	R/W	Control Register 7	
	7-0			bit[4:0]: output MII polling port4-0 flow control information; bit[7:5]: reserved.	
	15-8			bit[12:8]: output MII polling port 4-0 link information; bit[15:13]: reserved. “1” means flow control enable or link good.	
9		CtlReg8	R/W	Control Register 8	
	7-0			bit[4:0]: output MII polling port4-0 speed information; bit[7:5]: reserved.	
	15-8			bit[12:8]: output MII polling port4-0 full information; bit[15:13]: reserved. “1” means 100M or full duplex.	

Port Registers					
Reg No.	**Bit**	**Name**	**R/W**	**Description**	**Default**
1		StsReg1	RO	Status Register 1	
	10-0			bit[10:0]: output Port Tx queue head value.	
	15-11			Reserved.	
2		StsReg2	RO	Status Register 2	
	10-0			bit[10:0]: output Port Tx queue tail value.	
	15-11			Reserved.	
3		StsReg3	RO	Status Register 3	
	10-0			bit[10:0]: output Port Tx queue count value.	
	15-11			Reserved.	
4		CtlReg1	R/W		
	7-0			bit[7:0]: select Port VLAN group.	
	15-8			Reserved.	

“R/W” means read/writable.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{CC}	Power Supply Voltage	-0.3 to 3.6	V
V_{IN}	Input Voltage	-0.3 to V_{CC}+ 0.3	V
V_{OUT}	Output Voltage	-0.3 to V_{CC}+ 0.3	V
T_{STG}	Storage Temperature	-55 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Power Supply	3.0	3.3	3.6	V
V_{IN}	Input Voltage	0	-	V_{CC}	V
T_A	Free-air Ambient Temperature	0	25	70	°C

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IL}	Input Leakage Current	no pull-up or down	-1		1	uA
I_{OZ}	Tri-state Leakage Current		-1		1	uA
C_{IN}	Input Capacitance			2.8		pF
C_{OUT}	Output Capacitance		2.7		4.9	pF
C_{BID3}	Bi-directional buffer Capacitance		2.7		4.9	pF
V_{IL}	Input Low Voltage	CMOS			0.3*V_{CC}	V
V_{IH}	Input High Voltage	CMOS	0.7*V_{CC}			V
V_{OH}	Output High Voltage	I_{OL} = 2, 4, 6, 8, 12, 16, 24mA			0.4	V
V_{OL}	Output Low Voltage	I_{OH} = 2, 4, 6, 8, 12, 16, 24mA	2.4			V
R_I	Input Pull-up/down Resistance	V_{IL} = 0V or V_{IH} = V_{CC}		75		KOhm

(Under recommended operating conditions and VCC = 3.0 ~ 3.6V, Tj = 0 to 115°C)

ELECTRICAL CHARACTERISTICS

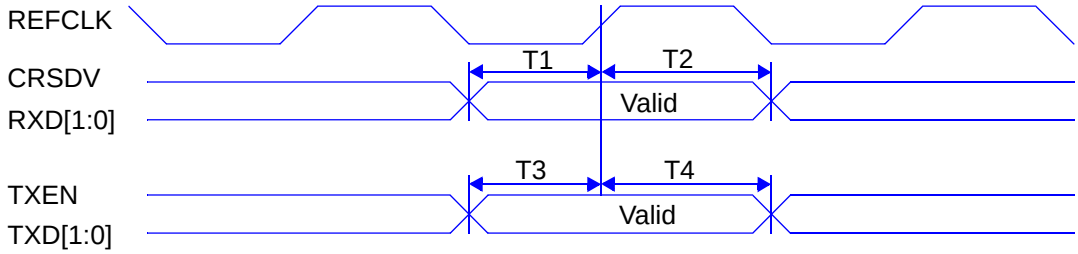


Figure-1 RMII Timing

Symbol	Parameter	Min	Typ	Max	Unit
T1	RMII input setup time	1			nS
T2	RMII input hold time	1			nS
T3	RMII output setup time	3			nS
T4	RMII output hold time	5			nS

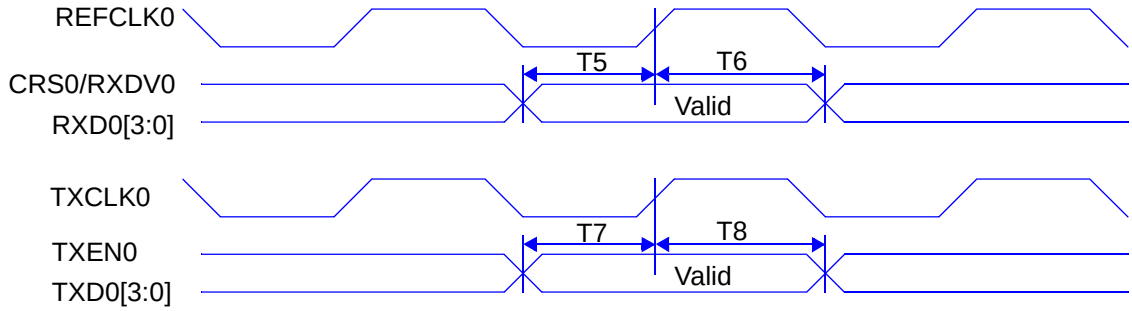


Figure-2 MII Timing

Symbol	Parameter	Min	Typ	Max	Unit
T5	MII input setup time	10			nS
T6	MII input hold time	10			nS
T7	MII output setup time	3			nS
T8	MII output hold time	5			nS

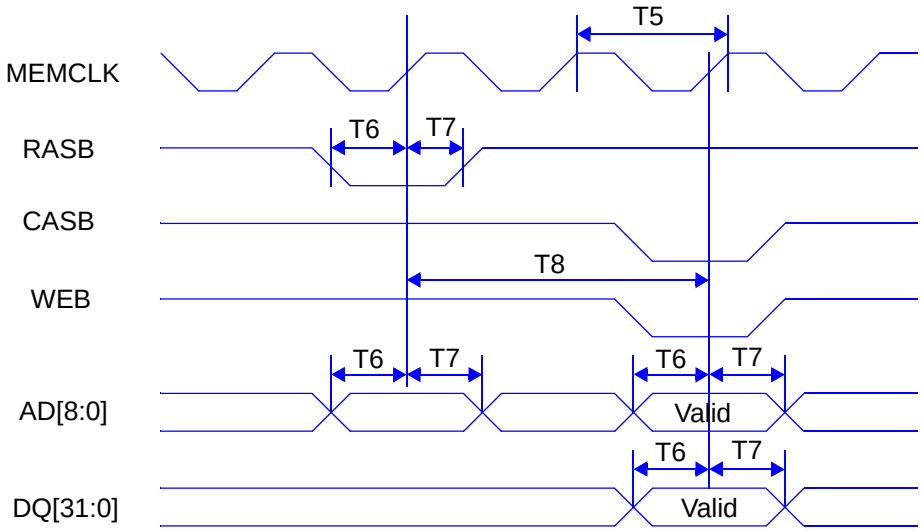


Figure-3 Memory Write Timing

Symbol	Parameter	Min	Typ	Max	Unit
T5	Memory clock cycle	12			nS
T6	Memory command/address/data setup time	6			nS
T7	Memory command/address/data hold time	2			nS
T8	Row active to burst write		2		CLK

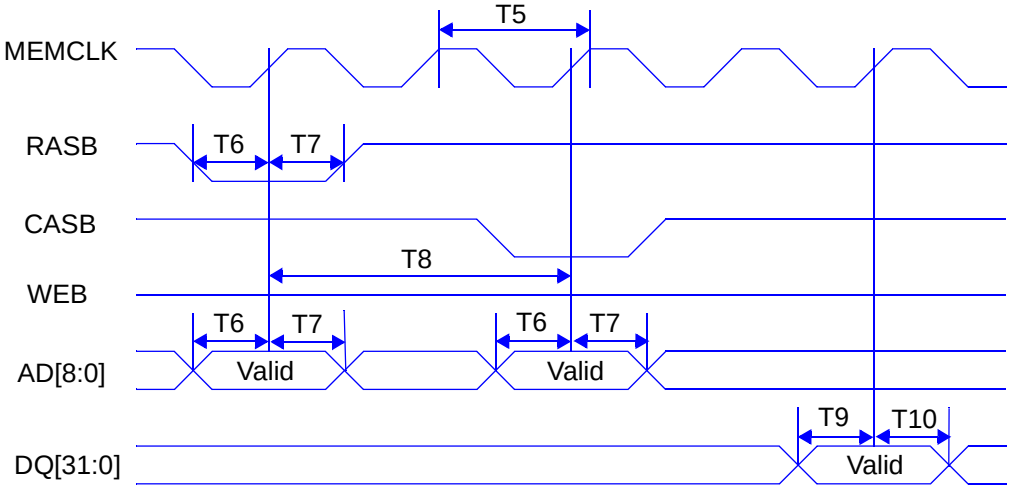


Figure-4 Memory Read Timing

Symbol	Parameter	Min	Typ	Max	Unit
T10	Memory read data setup time	2			nS
T11	Memory read data hold time	2			nS

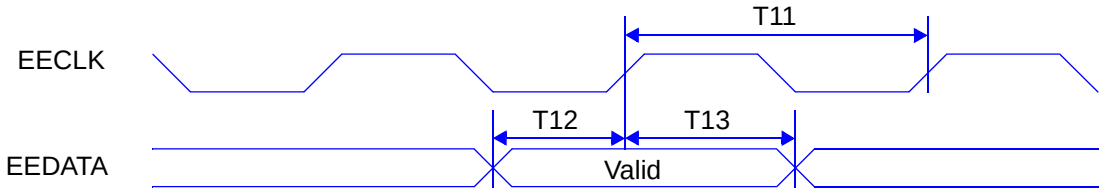


Figure-5 EEPROM Timing

Symbol	Parameter	Min	Typ	Max	Unit
T11	EEPROM clock cycle		10		uS
T12	EEDDATA input setup time	1			nS
T13	EEDATA input hold time	1			nS

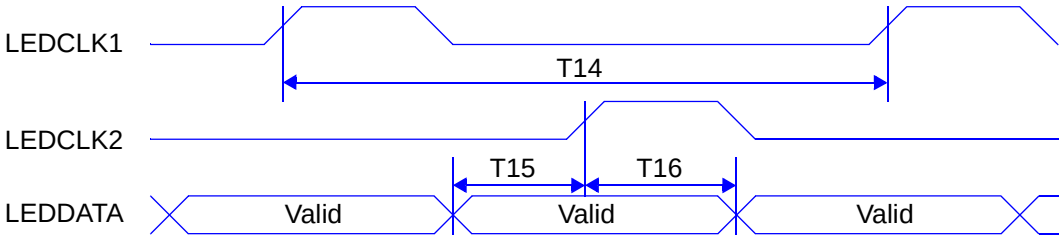
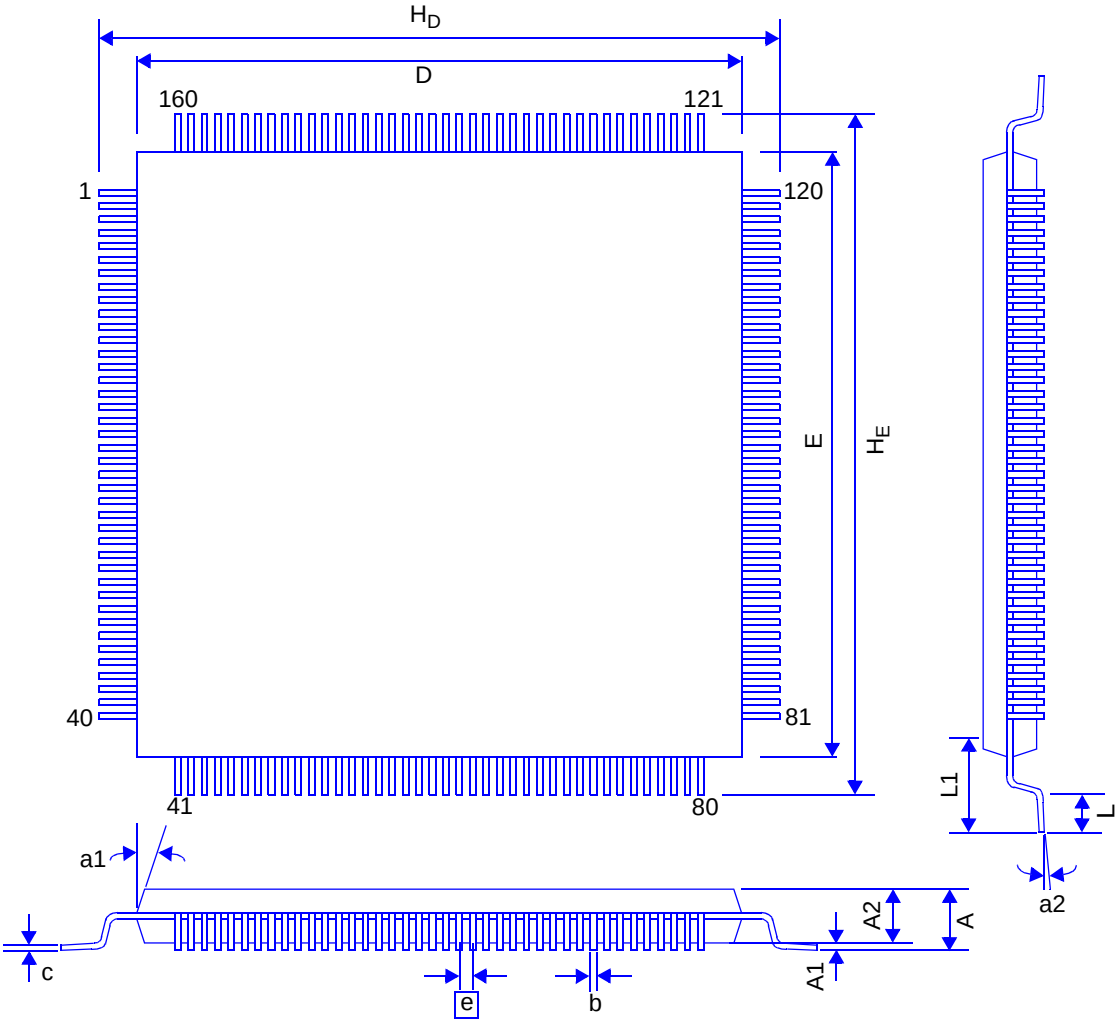


Figure-6 LED Interface

Symbol	Parameter	Min	Typ	Max	Unit
T14	EEPROM clock cycle		20		uS
T15	EEDDATA input setup time		5		uS
T16	EEDATA input hold time		5		uS

PACKAGE OUTLINE



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	3.683	-	-	0.145
A1	0.152	-	-	0.006	-	-
A2	2.73	2.85	2.97	0.107	0.112	0.117
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09	-	0.20	0.004	-	0.008
D	23.00	23.20	23.40	0.906	0.913	0.921
D1	19.90	20.00	20.10	0.783	0.787	0.791
E	17.00	17.00	17.40	0.669	0.677	0.685
E1	13.90	13.90	14.10	0.547	0.551	0.555
e		0.50BCS			0.020BCS	
L	0.73	0.88	1.03	0.029	0.035	0.041
L1		1.60BCS			0.063BCS	
y	-	-	0.10	-	-	0.004
z	0°	-	7°	0°	-	7°