



# MICROPOWER RRO Operational Amplifier with Shutdown

## Features

- Tiny SOT23-6 Package
- Guaranteed specs at 1.8V, 2.2V, 2.7V, 3V and 5V
- Less than 1µA idle current.
- Very Low operating Supply current typically 150µA@3V
- Rail-to-Rail Output
- Simple shutdown mode(with logic level control)
- Typical Total Harmonic Distortion of 0.02% at 3V
- 2.7MHz Typical Gain Bandwidth Product
- 2V/µs Typical Slew Rate

## Applications

- Mobile Communications
- Cellular Phones
- Portable Equipment
- Notebooks and PDAs
- Electronic Toys

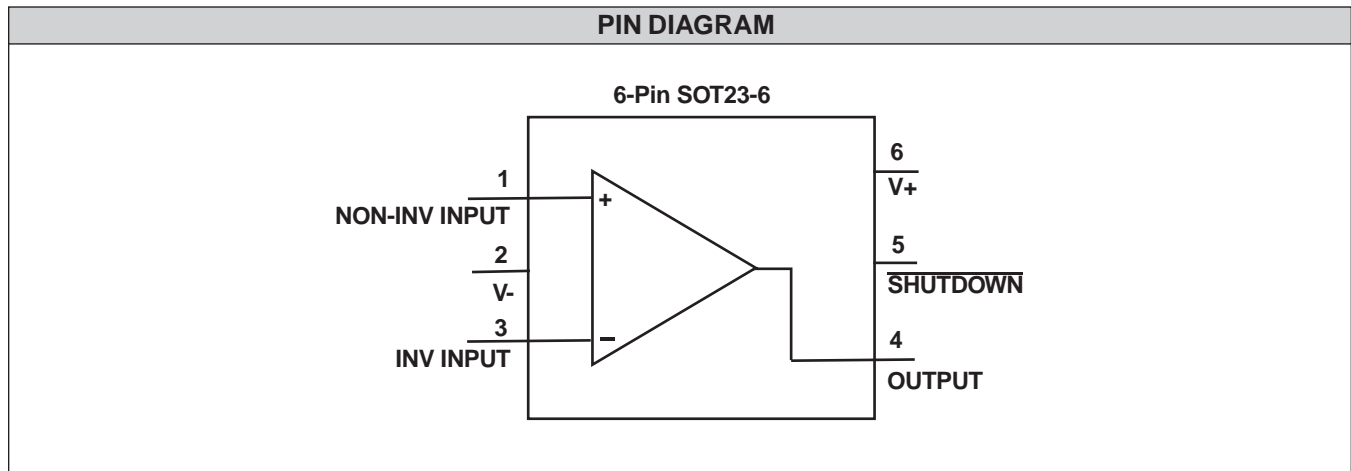
## Product Description

The CMV1036 is a high performance CMOS operational amplifier available in a small SOT23-6 package. Operating with very low supply current, it is ideal for battery operated applications where power, space and weight are critical.

Performance is similar to CAMD's CMV1030 SOT Amp, with the addition of a shutdown pin to greatly

reduce supply current when idle. The shutdown mode is controlled by an extra pin, and is compatible with most logic family signal levels.

Ideal for use in personal electronics such as cellular handsets, pagers, cordless telephones and other products with limited space and battery power.



STANDARD PART ORDERING INFORMATION			
Package		Ordering Part Number	
Pins	Style	Tape & Reel	Part Marking
6	SOT23-6	CMV1036Y/R	1016



ABSOLUTE MAXIMUM RATINGS (NOTE 1)		
Parameter	Rating	Unit
ESD Protection (HBM, Note 2)	2000	V
Differential Input Voltage	+/- Supply Voltage	V
Voltage at input/output Pin	(V+) +0.3, (V-) -0.3	V
Temperature: Storage	-65 to 150	
Operating Junction (Note 4)	125	°C
Lead (Soldering, 10s)	260	
Supply Voltage (V+ to V-)	7.5	V
Current at Input Pin	5	mA
Current at Output Pin (Note 3)	15	mA
Current at Power Supply Pins	15	mA

OPERATING CONDITIONS (unless specified otherwise)		
Parameter	Rating	Unit
Supply Voltage	1.8 to 7	V
Junction Temperature	-40 to 85	°C
Thermal Resistance	325	°C / W

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating conditions indicate ratings for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Operating Characteristics.

**Note 2:** Human Body Model, 1.5K $\Omega$  in series with 100pF.

**Note 3:** Applies to both single-supply and split-supply operation. Continuous short ckt operation at elevated ambient temperatures can result in exceeding the maximum allowed junction temperature of 150°C.

**Note 4:** The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $\theta_{JA}$  and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$ . All numbers apply for packages soldered directly to a PC board.



1.8V ELECTRICAL OPERATING CHARACTERISTICS (Unless otherwise specified T <sub>j</sub> = 25°C, V <sub>+</sub> = 1.8V, V <sub>-</sub> = 0V, R <sub>L</sub> > 1MΩ)					
Symbol	Parameter	Conditions	Typ	Limit	Unit
V <sub>OS</sub>	Input Offset Voltage	V <sub>OUT</sub> = 0.9V		9	mV
I <sub>B</sub>	Input Bias Current		1		pA
I <sub>OS</sub>	Input Offset Current		0.5		pA
R <sub>IN</sub>	Input Resistance		1		TΩ
I <sub>S</sub>	Supply Current	Amplifier ON V <sub>SD</sub> = 1.8V	120	240	μA
I <sub>S</sub>	Supply Current	Amplifier OFF V <sub>SD</sub> = 0V	0.01	1	μA
GBW	Gain Bandwidth Product		2		MHz
A <sub>V</sub>	Large Signal Voltage Gain	V <sub>OUT</sub> = 0.2V to 1.6V	80	60	dB
SR	Slew Rate	A <sub>V</sub> = -1, R <sub>L</sub> = 100K	1.4	0.35	V/μs
PSRR	Power Supply Rejection Ratio	V <sub>+</sub> = 0.9V to 1.2V V <sub>-</sub> = -0.9V to -1.2V V <sub>CM</sub> = 0V	70	50	dB
CMRR	Common Mode Rejection Ratio	0V < V <sub>CM</sub> < 0.8V	60	40	dB
V <sub>CM</sub>	Common Mode Input Range		0 1.1		V
THD	Total Harmonic Distortion	A <sub>V</sub> = -1, f = 1KHz, V <sub>OUT</sub> = 1V p-p R <sub>L</sub> = 100K	0.026		%
I <sub>SC</sub>	Output Short Circuit Current	Source/Sink	5		mA
V <sub>O</sub>	Output Swing from either rail	R <sub>L</sub> = 10K	20	150	mV
V <sub>SDIH</sub>	Amplifier ON Logic level	Amplifier ON		1.2	V
V <sub>SDIL</sub>	Amplifier OFF Logic level	Amplifier OFF		0.6	V
I <sub>IN</sub>	Logic Pin Current	V <sub>SD</sub> = V <sub>+</sub> or GND		1	μA
T <sub>ON</sub>	Turn On Time		18		μs
T <sub>OFF</sub>	Turn Off Time		1		μs

2.2V ELECTRICAL OPERATING CHARACTERISTICS (Unless otherwise specified T <sub>j</sub> = 25°C, V <sub>+</sub> = 2.2V, V <sub>-</sub> = 0V, R <sub>L</sub> > 1MΩ)					
Symbol	Parameter	Conditions	Typ	Limit	Unit
V <sub>OS</sub>	Input Offset Voltage	V <sub>OUT</sub> = 1.1V		9	mV
I <sub>B</sub>	Input Bias Current		1		pA
I <sub>OS</sub>	Input Offset Current		0.5		pA
R <sub>IN</sub>	Input Resistance		1		TΩ
I <sub>S</sub>	Supply Current	Amplifier ON V <sub>SD</sub> = 2.2V	135	270	μA
I <sub>S</sub>	Supply Current	Amplifier OFF V <sub>SD</sub> = 0V	0.01	1	μA
GBW	Gain Bandwidth Product		2.4		MHz
A <sub>V</sub>	Large Signal Voltage Gain	V <sub>OUT</sub> = 0.2V to 2V	80	60	dB
SR	Slew Rate	A <sub>V</sub> = -1, R <sub>L</sub> = 100K	1.8	0.45	V/μs
PSRR	Power Supply Rejection Ratio	V <sub>+</sub> = 1.1V to 1.4V V <sub>-</sub> = -1.1V to -1.4V V <sub>CM</sub> = 0V	70	50	dB
CMRR	Common Mode Rejection Ratio	0V < V <sub>CM</sub> < 1.2V	60	40	dB
V <sub>CM</sub>	Common Mode Input Range		0 1.5		V
THD	Total Harmonic Distortion	A <sub>V</sub> = -1, f = 1KHz, V <sub>OUT</sub> = 1.4Vp-p R <sub>L</sub> = 100K	0.02		%
I <sub>SC</sub>	Output Short Circuit Current	Source/Sink	7		mA
V <sub>O</sub>	Output Swing from either rail	R <sub>L</sub> = 10K	20	150	mV
V <sub>SDIH</sub>	Amplifier ON Logic level	Amplifier ON		1.6	V
V <sub>SDIL</sub>	Amplifier OFF Logic level	Amplifier OFF		0.6	V
I <sub>IN</sub>	Logic Pin Current	V <sub>SD</sub> = V <sub>+</sub> or GND		1	μA
T <sub>ON</sub>	Turn On Time		15		μs
T <sub>OFF</sub>	Turn Off Time		1		μs



2.7V ELECTRICAL OPERATING CHARACTERISTICS (Unless otherwise specified T <sub>j</sub> = 25°C, V <sub>+</sub> = 2.7V, V <sub>-</sub> = 0V, R <sub>L</sub> > 1MΩ)					
Symbol	Parameter	Conditions	Typ	Limit	Unit
V <sub>OS</sub>	Input Offset Voltage	V <sub>OUT</sub> = 1.35V		6	mV
I <sub>B</sub>	Input Bias Current		1		pA
I <sub>OS</sub>	Input Offset Current		0.5		pA
R <sub>IN</sub>	Input Resistance		1		TΩ
I <sub>S</sub>	Supply Current	Amplifier ON V <sub>SD</sub> = 2.7V	150	300	μA
I <sub>S</sub>	Supply Current	Amplifier OFF V <sub>SD</sub> = 0V	0.01	1	μA
GBW	Gain Bandwidth Product		2.7		MHz
A <sub>V</sub>	Large Signal Voltage Gain	V <sub>OUT</sub> = 0.2V to 2.5V	85	65	dB
SR	Slew Rate	A <sub>V</sub> = -1, R <sub>L</sub> = 100K	2	0.5	V/μs
PSRR	Power Supply Rejection Ratio	V <sub>+</sub> = 1.35V to 1.65V V <sub>-</sub> = -1.35V to 1.65V V <sub>CM</sub> = 0V	70	50	dB
CMRR	Common Mode Rejection Ratio	0V < V <sub>CM</sub> < 1.7V	60	45	dB
V <sub>CM</sub>	Common Mode Input Range		0 2		V
THD	Total Harmonic Distortion	A <sub>V</sub> = -1, f = 1KHz, V <sub>OUT</sub> = 1.9Vp-p R <sub>L</sub> = 100K	0.02		%
I <sub>SC</sub>	Output Short Circuit Current	Source/Sink	12		mA
V <sub>O</sub>	Output Swing from either rail	R <sub>L</sub> = 10K	20	150	mV
V <sub>SDIH</sub>	Amplifier ON Logic Level	Amplifier ON		2	V
V <sub>SDIL</sub>	Amplifier OFF Logic Level	Amplifier OFF		0.8	V
I <sub>IN</sub>	Logic Pin Current	V <sub>SD</sub> = V <sub>+</sub> or GND		1	μA
T <sub>ON</sub>	Turn On Time		11		μs
T <sub>OFF</sub>	Turn Off Time		1		μs



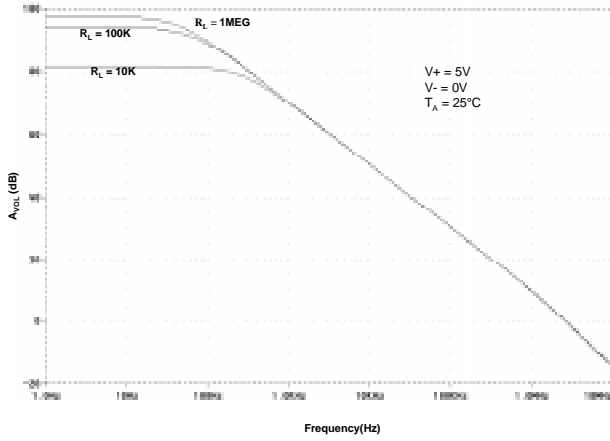
3V ELECTRICAL OPERATING CHARACTERISTICS (Unless otherwise specified T <sub>j</sub> = 25°C, V <sub>+</sub> = 3V, V <sub>-</sub> = 0V, R <sub>L</sub> > 1MΩ)					
Symbol	Parameter	Conditions	Typ	Limit	Unit
V <sub>OS</sub>	Input Offset Voltage	V <sub>OUT</sub> = 1.5V		5	mV
I <sub>B</sub>	Input Bias Current		1		pA
I <sub>OS</sub>	Input Offset Current		0.5		pA
R <sub>IN</sub>	Input Resistance		1		TΩ
I <sub>S</sub>	Supply Current	Amplifier ON V <sub>SD</sub> = 3V	150	300	μA
I <sub>S</sub>	Supply Current	Amplifier OFF V <sub>SD</sub> = 0V	0.01	1	μA
GBW	Gain Bandwidth Product		2.7		MHz
A <sub>V</sub>	Large Signal Voltage Gain	V <sub>OUT</sub> = 0.2V to 2.8V	85	65	dB
SR	Slew Rate	A <sub>V</sub> = -1, R <sub>L</sub> = 100K	2	0.5	V/μs
PSRR	Power Supply Rejection Ratio	V <sub>+</sub> = 1.5V to 1.8V V <sub>-</sub> = -1.5V to -1.8V V <sub>CM</sub> = 0V	80	55	dB
CMRR	Common Mode Rejection Ratio	0V < V <sub>CM</sub> < 2V	70	50	dB
V <sub>CM</sub>	Common Mode Input Range		0 2.3		V
THD	Total Harmonic Distortion	A <sub>V</sub> = -1, f = 1KHz, V <sub>OUT</sub> = 2Vp-p R <sub>L</sub> = 100K	0.02		%
I <sub>SC</sub>	Output Short Circuit Current	Source/Sink	15		mA
V <sub>O</sub>	Output Swing from either rail	R <sub>L</sub> = 10K	20	150	mV
V <sub>SDIH</sub>	Amplifier ON Logic Level	Amplifier ON		2.2	V
V <sub>SDIL</sub>	Amplifier OFF Logic Level	Amplifier OFF		1	V
I <sub>IN</sub>	Logic Pin Current	V <sub>SD</sub> + V <sub>+</sub> or GND		1	μA
T <sub>ON</sub>	Turn On Time		9		μs
T <sub>OFF</sub>	Turn Off Time		1		μs



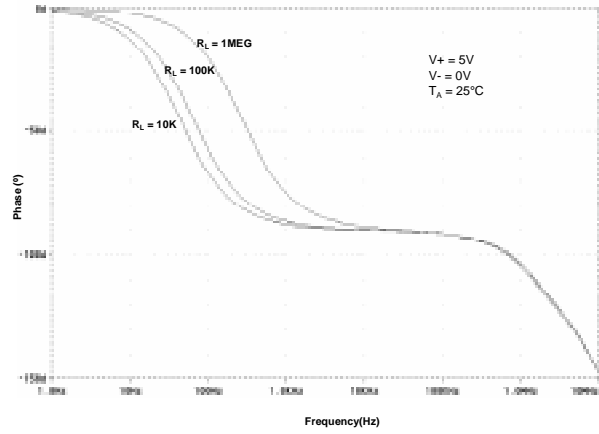
5V ELECTRICAL OPERATING CHARACTERISTICS (Unless otherwise specified $T_j = 25^\circ\text{C}$ , $V_+ = 5\text{V}$ , $V_- = 0\text{V}$ , $R_L > 1\text{M}\Omega$ )					
Symbol	Parameter	Conditions	Typ	Limit	Unit
$V_{OS}$	Input Offset Voltage	$V_{OUT} = 1.5\text{V}$		5	mV
$I_B$	Input Bias Current		1		pA
$I_{OS}$	Input Offset Current		0.5		pA
$R_{IN}$	Input Resistance		1		$\text{T}\Omega$
$I_S$	Supply Current	Amplifier ON $V_{SD} = 5\text{V}$	180	360	$\mu\text{A}$
$I_S$	Supply Current	Amplifier OFF $V_{SD} = 0\text{V}$	0.01	1	$\mu\text{A}$
GBW	Gain Bandwidth Product		2.9		MHz
$A_V$	Large Signal Voltage Gain	$V_{OUT} = 0.2\text{V}$ to $2.8\text{V}$	90	70	dB
SR	Slew Rate	$A_V = -1$ , $R_L = 100\text{K}$	2.3	0.575	$\text{V}/\mu\text{s}$
PSRR	Power Supply Rejection Ratio	$V_+ = 1.5\text{V}$ to $1.8\text{V}$ $V_- = -1.5\text{V}$ to $-1.8\text{V}$ $V_{CM} = 0\text{V}$	80	55	dB
CMRR	Common Mode Rejection Ratio	$0\text{V} < V_{CM} < 2\text{V}$	70	50	dB
$V_{CM}$	Common Mode Input Range		0 4.3		V
THD	Total Harmonic Distortion	$A_V = -1$ , $f = 1\text{KHz}$ , $V_{OUT} = 2\text{Vp-p}$ $R_L = 100\text{K}$	0.02		%
$I_{SC}$	Output Short Circuit Current	Source/Sink	25		mA
$V_O$	Output Swing from either rail	$R_L = 10\text{K}$	20	150	mV
$V_{SDIH}$	Amplifier ON Logic Level	Amplifier ON		4	V
$V_{SDIL}$	Amplifier OFF Logic Level	Amplifier OFF		1	V
$I_{IN}$	Logic Pin Current	$V_{SD} + V_+$ or GND		1	$\mu\text{A}$
$T_{ON}$	Turn On Time		7.5		$\mu\text{s}$
$T_{OFF}$	Turn Off Time		1		$\mu\text{s}$



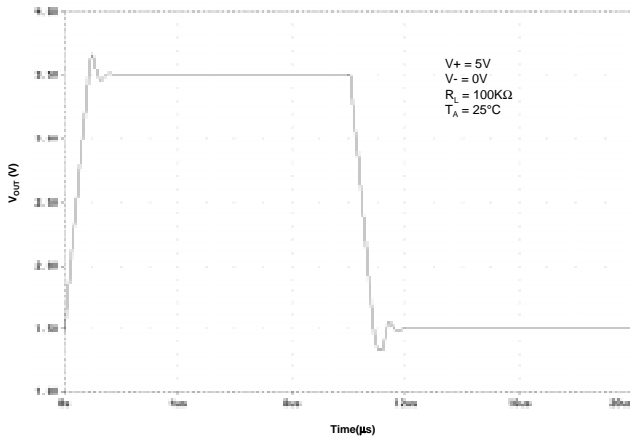
Open Loop Voltage Gain Response



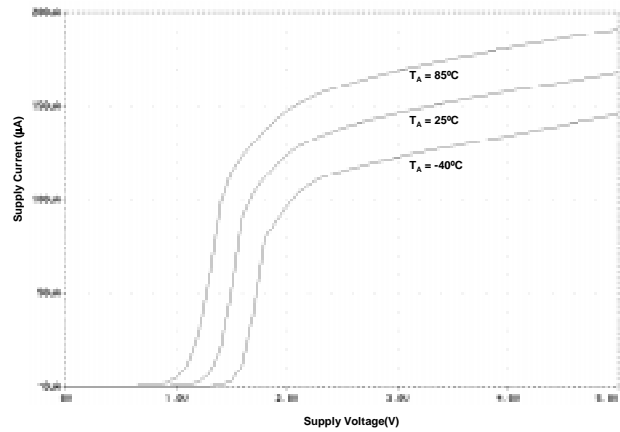
Open Loop Phase Response



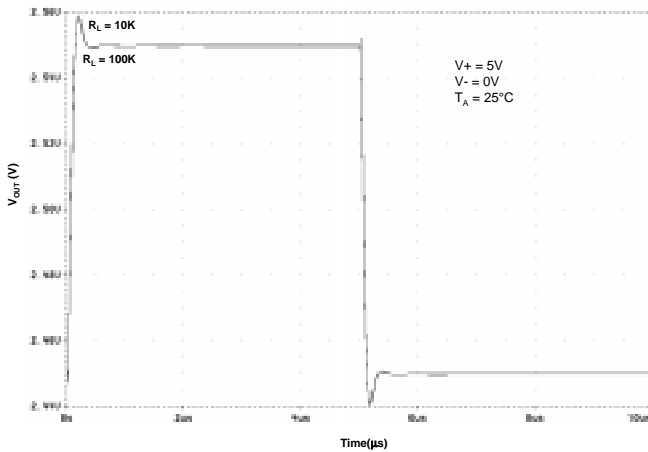
Large Signal Pulse Response



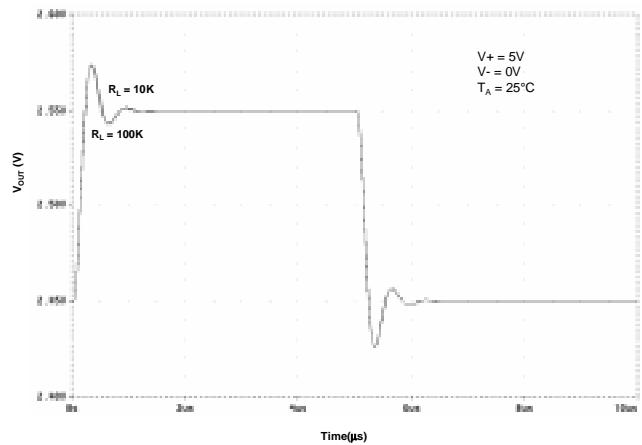
Supply Current Versus Supply Voltage



Non Inverting Small Signal Response

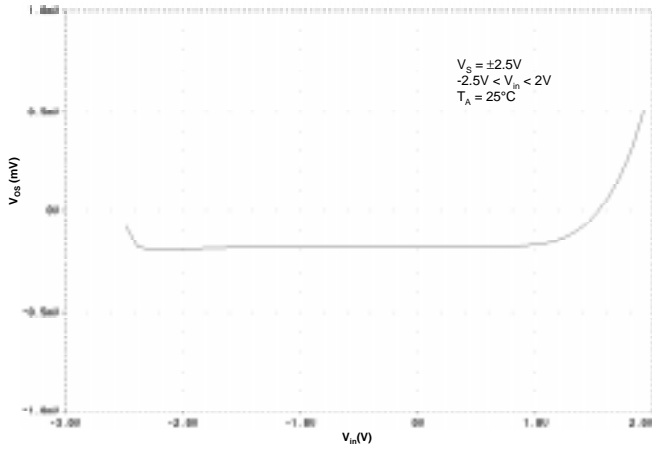


Inverting Small Signal Response

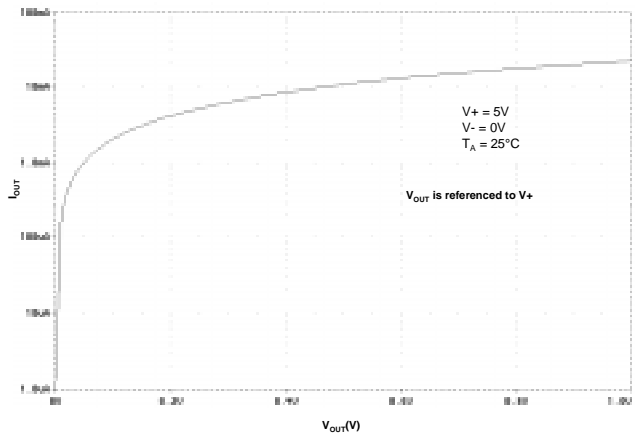




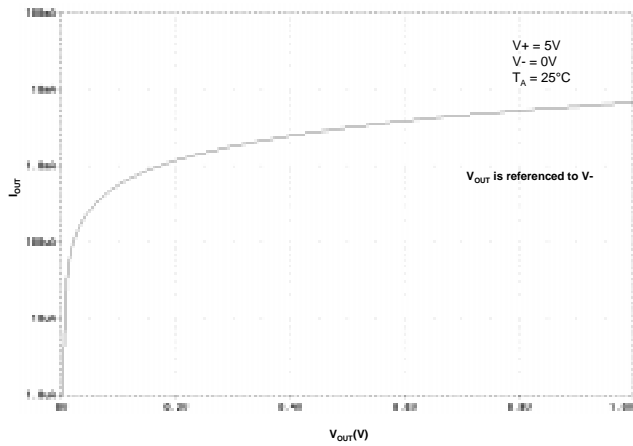
Common Mode Rejection Ratio



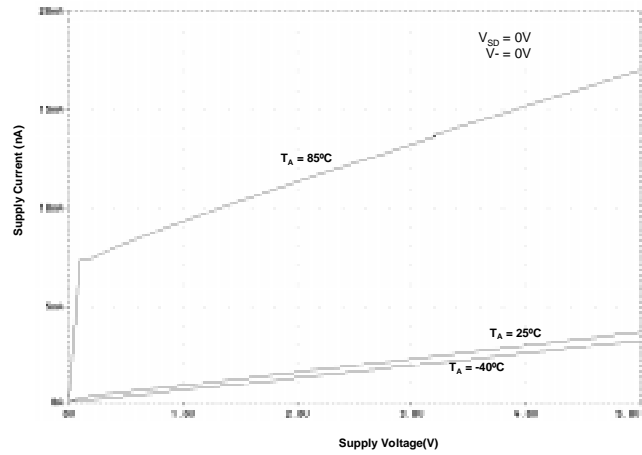
Current Sourcing Versus  $V_{OUT}$



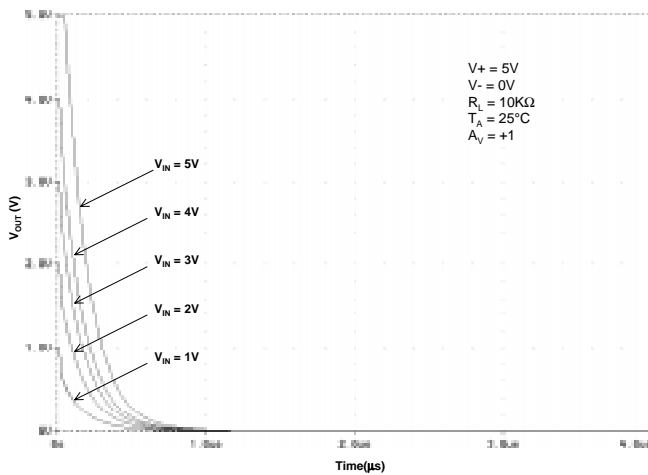
Current Sinking Versus  $V_{OUT}$



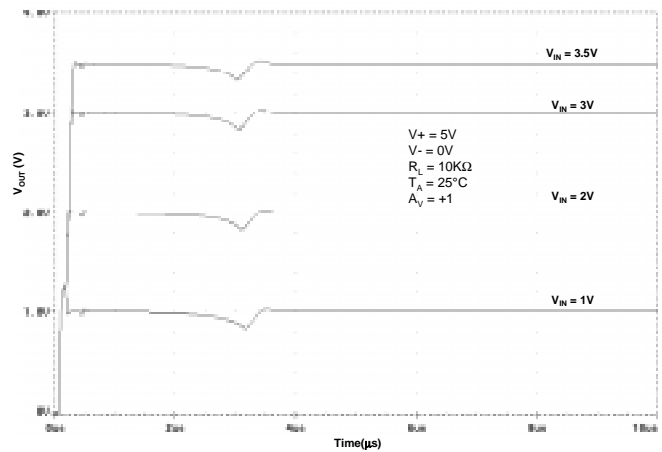
Disabled Supply Current Versus Supply Voltage



5V Disable Response for a family of DC Inputs



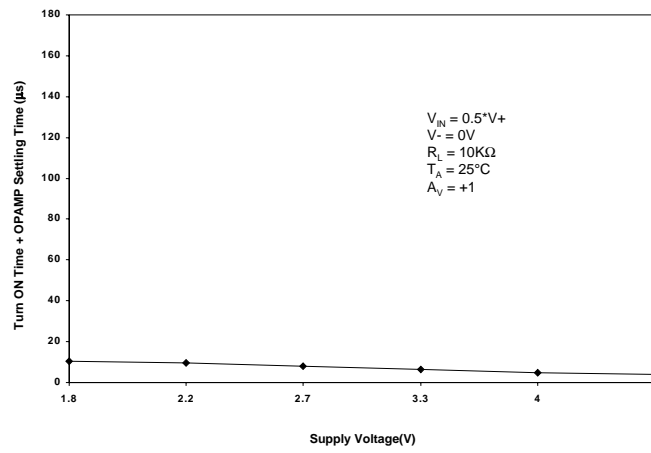
5V Enable Response for a family of DC Inputs







Turn ON Time Versus Supply Voltage





**Applications Information**

**1. Input Common Mode Range and Output Voltage Considerations**

The CMV1036 is capable of accommodating an input common mode voltage equal to one volt below the positive rail and all the way to the negative rail. It is also capable of output voltages equal to both power supply rails. Voltages that exceed the supply voltages will not cause phase inversion of the output, however, ESD diode clamps are provided at the inputs that can be damaged if static currents in excess of  $\pm 5\text{mA}$  are allowed to flow in them. This can occur when the magnitude of input voltage exceeds the rail by more than 0.3 volt. To preclude damage, an applications resistor,  $R_S$ , in series with the input is recommended as illustrated in Figure 1 whose value for  $R_S$  is given by:

$$R_S > \frac{V_{IN} - (V+ + 0.3\text{ V})}{5\text{ mA}}$$

For  $V+$  (or  $V-$ ) equal to 2.2 volts and  $V_{IN}$  equal to 10 volts,  $R_S$  should be chosen for a value of  $2.5\text{K}\Omega$  or greater.

The Shutdown pin also provides ESD clamp diodes that will be damaged if the signal exceeds the rail by 0.3 volts and should also be limited to  $<5\text{mA}$  by inserting the appropriate resistor between the input signal or logic gate and the Shutdown input.

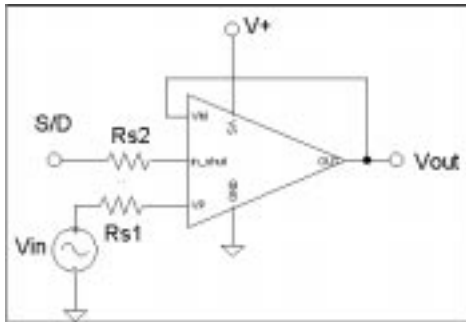


Figure 1.

**2. Output Current and Power Dissipation Considerations**

The CMV1036 is capable of sinking and sourcing output currents in excess of  $7\text{mA}$  ( $V+ = 2.2\text{ volts}$ ) at voltages very nearly equal to the rails. As such, it does not have any internal short circuit protection (which would in any event detract from its rail to rail capability). Although the power dissipation and junction temperature rise are small, a short analysis is worth investigating.

Obviously, the worst case from a power dissipation point of view is when the output is shorted to either ground in a single rail application or to the opposite supply voltage in split rail applications. Since device only draws  $60\mu\text{A}$  supply current ( $100\mu\text{A}$  maximum), its contribution to the junction temperature,  $T_J$ , is negligible. As an example, let us analyze a situation in which the CMV1036 is operated from a 5 volt supply and ground, the output is “programmed” to positive saturation, and the output pin is indefinitely shorted to ground. In general:

$$P_{DISS} = (V+ - V_{OUT}) * I_{OUT} + I_S * V+$$

Where:  $P_{DISS}$  = Power dissipated by the chip  
 $V+$  = Supply voltage  
 $V_{OUT}$  = The output voltage  
 $I_S$  = Supply Current

The contribution to power dissipation due to supply current is  $500\mu\text{W}$  and is indeed negligible as stated above.

The primary contribution to power dissipation occurs in the output stage.  $V+ - V_{OUT}$  would equal  $5\text{V} - 0\text{V} = 5\text{V}$  while the short circuit current would be  $25\text{mA}$ . The power dissipation would be equal to  $125\text{mW}$ .

$$T_J = T_A + \theta_{JA} * P_{diss}$$

Where:  $T_A$  = The ambient temperature  
 $\theta_{JA}$  = The thermal impedance of the package junction to ambient

The SOT23 exhibits a  $\theta_{JA}$  equal to  $325^\circ\text{C/W}$ . Thus for our example the junction rise would be about  $41^\circ\text{C}$  which is clearly not a destructive situation even under an ambient temperature of  $85^\circ\text{C}$ .

**3. Input Impedance Considerations**

The CMV1036 exhibits an input impedance typically in excess of 1 Tera  $\Omega$  ( $1 \times 10^{12}$  ohms) making it very appropriate for applications involving high source impedance such as photodiodes and high output impedance transducers or long time constant integrators. High source impedances usually dictate large feedback resistors. But, the output capacitance of the source in parallel with the input capacitance of the CMV1036 (which is typically  $3\text{pF}$ ) create a parasitic pole with the feedback resistor which erodes the phase margin of the amplifier. The usual fix is to bypass,  $R_F$ , as shown in Figure 2 with a small capacitor to cancel the input pole. The usual formula for calculating  $C_F$  always results in a value larger than that is required:

$$\frac{1}{2 \Pi R_S C_S} \geq \frac{1}{2 \Pi R_F C_F}$$

Since the parasitic capacitance can change between



the breadboard and the production printed circuit board, we favor the use of a "gimmick", a technique perfected by TV technicians in the 1950's. A gimmick is made by taking two lengths (typically about a foot) of small gauge wire such as AWG 24, twisting them together, and then after baring all ends soldering the gimmick across  $R_F$ . With the circuit operating,  $C_F$  is "adjusted" by clipping short lengths of the gimmick off until the compensation is nominal. Then simply remove the gimmick, take it to an impedance bridge, and select the capacitor accordingly.

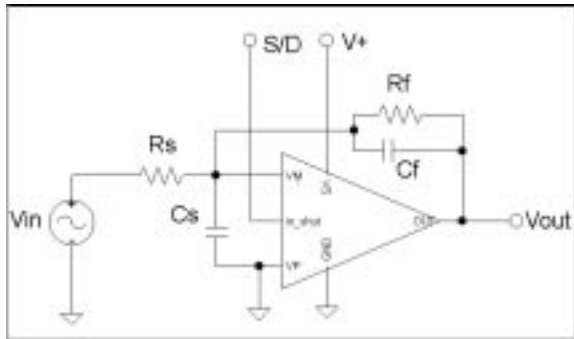


Figure 2.

#### 4. Capacitive Load Considerations

The CMV1036 is capable of driving capacitive loads in excess of 100pF without oscillation. However, significant peaking will result. Probably the easiest way to minimize this problem is to use an isolation resistor as shown in Figure 3.

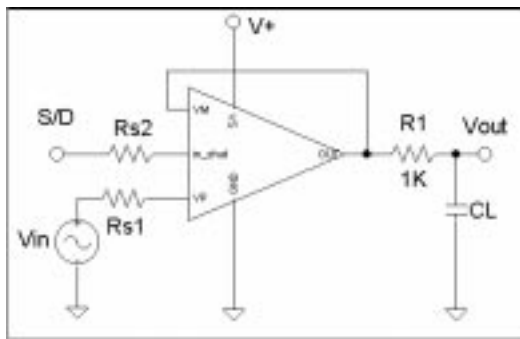


Figure 3

#### 5. Power Supply Decoupling

The CMV1036 is not prone to oscillation without the use of power supply decoupling capacitors, however to minimize hum and noise pick-up, it is recommended that the rails be bypassed with 0.01μF capacitors.

#### 6. Turn On and Turn Off (Shut Down) Characteristics

The turn off delay (Disable Response),  $t_{OFF}$ , is defined as the time between the shut down signal crossing the disable threshold (typically  $V+ - 1$  volt) and the time for the amplifier's output to come within 10% of zero. It is largely governed by a propagation delay within the CMV1036 of few hundred nanoseconds followed by an exponential decay determined by the load resistance in parallel with the load capacitance.

The turn on delay (Enable Response),  $t_{ON}$ , is defined as the time between the shutdown signal crossing the threshold and the time the output reaches to within 10% of its final value.  $t_{ON}$  is largely independent of supply voltage and input level.

#### 7. Typical Applications

Illustrated in Figure 4 is a Sample and Hold Amplifier capable of operating from a single rail, but it will work equally well with split rails. The circuit will accommodate input voltages (common mode) from zero volts to  $V+ - 1$  volt. The Shut Down feature of the CMV1036 is used to disable  $A_1$ , whose output acts like a very high impedance in this mode. The high slew rate of the CMV1036 and large output current minimize Acquisition Time.  $A_2$  presents a very high input impedance and very low bias current. A Logic 1, a voltage  $> V+ - 1$  volt will put the circuit into "Sample" mode. A Logic "0" will put the circuit in "Hold" mode. For the values shown, Acquisition Time to 0.1% is typically 10 mS for a zero to 4 volt input, the hold step is typically 400μV, and the droop rate at 85°C is 0.1μV/μS. Overall accuracy is better than 0.01%. For minimum droop,  $C_1$  should be of polystyrene construction.

#### 7. Typical Applications

Illustrated in Figure 4 is a Sample and Hold Amplifier capable of operating from a single rail, but it will work equally well with split rails. The circuit will accommodate input voltages (common mode) from zero volts to  $V+ - 1$  volt. The Shut Down feature of the CMV1036 is used to disable  $A_1$ , whose output acts like a very high impedance in this mode. The high slew rate of the CMV1036 and large output current minimize Acquisition Time.  $A_2$  presents a very high input impedance and very low bias current. A Logic "1", a voltage  $> V+ - 1$  volt will put the circuit into Sample mode. A Logic "0" will put the circuit in "Hold" mode. For the values shown, Acquisition Time to 0.1% is typically 10μS for a zero to 4 volt input, the hold step is typically 400 μV, and the droop rate at 85°C is 0.1μV/μS. Overall accuracy is better than 0.01%. For minimum droop,  $C_1$  should be of polystyrene construction.

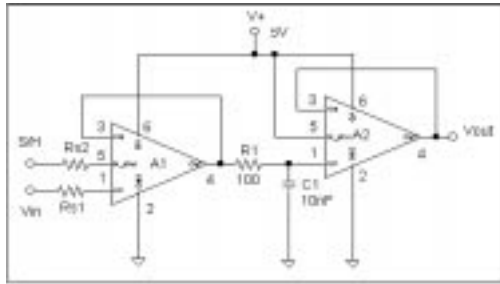


Figure 4

The circuit illustrated in Figure 5 provides a simple analog switch capable of operating from supply voltages as low as 2.2 volts. The circuit takes advantage of the CMV1036's shutdown feature which places

the output stage in a high impedance mode. The outputs are simply "wire OR'd", and as configured, a Logic "1" (Logic In voltage > V+ - 1 volt), V<sub>IN2</sub> is selected.

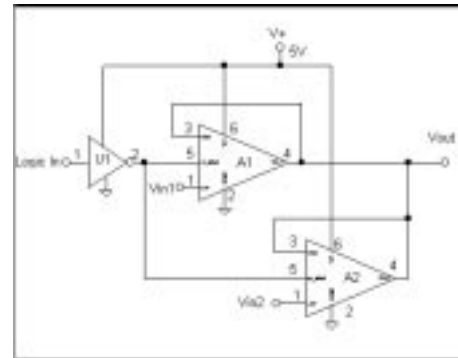


Figure 5