



UT40N04

Preliminary

Power MOSFET

N-CHANNEL LOGIC LEVEL ENHANCEMENT MODE FIDLD EFFECT TRANSISTOR

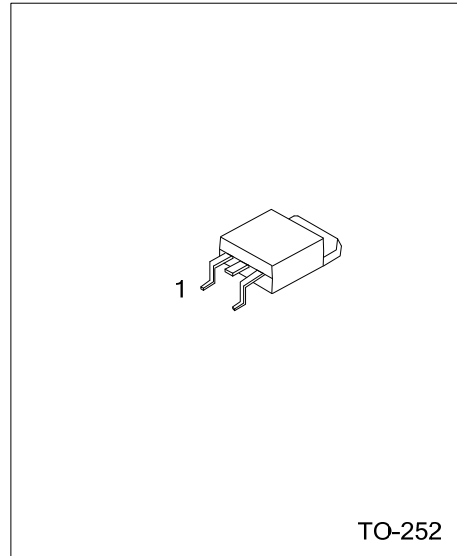
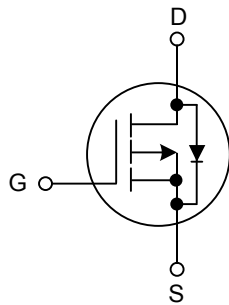
DESCRIPTION

The UTC **40N04** is an N-channel enhancement mode FET using advanced technology to provide fast switching speed, ruggedized device design, low on-resistance and cost-effectiveness.

FEATURES

- * Low on-Resistance
- * Fast Switching Speed
- * Halogen Free

SYMBOL



ORDERING INFORMATION

Ordering Number	Package	Pin Assignment			Packing
		1	2	3	
UT40N04G-TN3-R	TO-252	G	D	S	Tape Reel

Note: G: Gate, D: Drain, S: Source

<p>UT40N04G-TN3-R</p> <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Halogen Free 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) TN3: TO-252 (3) G: Halogen Free
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■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ Unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	25
		$T_C=70^\circ\text{C}$	20
Pulsed Drain Current (Note 1)	I_{DM}	75	A
Avalanche Current	I_{AS}	27	
Avalanche Energy	E_{AS}	37	mJ
Power Dissipation	P_D	$T_C=25^\circ\text{C}$	30
		$T_C=70^\circ\text{C}$	20
Operating Junction Temperature	T_J	-55~150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~150	$^\circ\text{C}$

Note:1. Pulse width limited by maximum junction temperature.

2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	40	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	4.1	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	40			V	
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=32\text{V}, V_{GS}=0\text{V}$			1	μA	
		$V_{DS}=30\text{V}, V_{GS}=0\text{V}, T_J=125^\circ\text{C}$			10		
Gate- Source Leakage Current	I_{GSS}	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			± 250	nA	
On-State Drain Current (Note 1)	$I_{D(ON)}$	$V_{DS}=5\text{V}, V_{GS}=10\text{V}$	75			A	
ON CHARACTERISTICS							
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2	2.4	3	V	
Static Drain-Source On-State Resistance (Note 1)	$R_{DS(ON)}$	$V_{GS}=5\text{V}, I_D=8\text{A}$		26	50	m Ω	
		$V_{GS}=7\text{V}, I_D=8\text{A}$		22	45		
		$V_{GS}=10\text{V}, I_D=10\text{A}$		19	29		
Forward Transconductance (Note 1)	g_{FS}	$V_{DS}=5\text{V}, I_D=10\text{A}$		30		S	
Gate Resistance	R_g	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1.0\text{MHz}$		1.55		Ω	
DYNAMIC PARAMETERS							
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}, V_{DS}=20\text{V}, f=1.0\text{MHz}$		1150		pF	
Output Capacitance	C_{OSS}			157			
Reverse Transfer Capacitance	C_{RSS}			80			
SWITCHING PARAMETERS (Note 2)							
Total Gate Charge	$Q_G (V_{GS}=10\text{V})$	$V_{DS}=0.5V_{(BR)DSS}, I_D=10\text{A}$		19		nC	
	$Q_G (V_{GS}=4.5\text{V})$			9			
Gate to Source Charge	Q_{GS}			4.5			
Gate to Drain Charge	Q_{GD}			3			
Turn-ON Delay Time	$t_{D(ON)}$			10		ns	
Rise Time	t_R		$V_{GS}=10\text{V}, V_{DS}=20\text{V}, I_D \approx -1\text{A}, R_{GS}=6\Omega, R_L=1\Omega$		6		ns
Turn-OFF Delay Time	$t_{D(OFF)}$				26		ns
Fall-Time	t_F			6		ns	
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Continuous Current	I_S				23	A	
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_F=10\text{A}, V_{GS}=0\text{V}$			1.3	V	
Reverse Recovery Time	t_{RR}	$I_F=10\text{A}, dI_F/dt=100\text{A}/\mu\text{s}$		38		ns	
Reverse Recovery Charge	Q_{RR}			29		nC	

Note: 1. Pulsed test: Pulse width $\leq 300\mu\text{sec}$, duty cycle $\leq 2\%$.

2. Independent of Operating Temperature.

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