SYNCHRONOUS SRAM MODULE

32K x 64 SRAM

+3.3V SUPPLY WITH CLOCKED, REGISTERED INPUTS AND BURST COUNTER

FEATURES

- 80 position dual-read-out dual in-line memory module (DIMM) with 160 leads
- Fast access times: 9, 10, 11 and 12ns
- Fast $\overline{OE}$: 5 and 6ns
- Single +3.3V ±5% power supply
- 5V-tolerant common data I/O
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock controlled, registered, address, data and control
- Internally self-timed WRITE cycle
- Burst control pins (interleaved or linear burst)
- Low capacitive bus loading
- High 30pF output drive capability at rated access time

OPTIONS — MARKING

- Timing
  - 9ns access/15ns cycle — -9
  - 10ns access/15ns cycle — -10
  - 11ns access/15ns cycle — -11
  - 12ns access/20ns cycle — -12
- Packages
  - 160-lead DIMM (gold) — G
- Low power (optional) — P
- 2V data retention, low power (optional) — L
- Part Number Example: MT2LSYT3264B2G-9 L

GENERAL DESCRIPTION

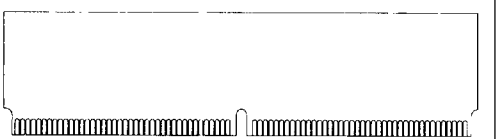
The Micron Synchronous SRAM module family employs high- speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double- layer metal, double-layer polysilicon technology.

The MT2LSYT3264B2 module integrates two 32K x 32 synchronous SRAMs. All synchronous inputs pass through registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, data inputs, active LOW chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion (CE2, $\overline{CE2}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and byte write enables ($\overline{BW0}$ - $\overline{BW7}$, $\overline{BWE}$) and global write ($\overline{GW}$).

Asynchronous inputs include the output enable ($\overline{OE}$) and the clock (CLK) and burst mode (MODE). The Data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to eight bytes wide as controlled by the byte write enables.

PIN ASSIGNMENT (Top View)

160-Lead, Dual Read-out DIMM
(SF-1)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	41	$\overline{GW}$	81	Vss	121	CE2
2	DQ0	42	Vcc2	82	DQ1	122	RSVD
3	Vcc2	43	RSVD	83	RSVD	123	RSVD
4	DQ2	44	A13	84	DQ3	124	A14
5	DQ4	45	MODE	85	DQ5	125	$\overline{ADV}$
6	DQ6	46	A15	86	DQ7	126	A16
7	RSVD	47	A17	87	DQ8	127	NC
8	Vss	48	NC	88	Vss	128	NC
9	DQ9	49	DQ32	89	DQ10	129	DQ33
10	DQ11	50	NC	90	DQ12	130	NC
11	DQ13	51	Vss	91	DQ14	131	Vss
12	Vcc2	52	DQ34	92	RSVD	132	DQ35
13	DQ15	53	DQ36	93	RSVD	133	DQ37
14	DQ16	54	DQ38	94	Vss	134	DQ39
15	Vss	55	DQ40	95	DQ17	135	RSVD
16	DQ18	56	$\overline{BW4}$	96	DQ19	136	$\overline{BW5}$
17	DQ20	57	Vss	97	DQ21	137	Vss
18	$\overline{OE}$	58	$\overline{BW6}$	98	DQ22	138	$\overline{BW7}$
19	Vss	59	DQ41	99	Vss	139	DQ42
20	$\overline{BW0}$	60	DQ43	100	$\overline{BW1}$	140	DQ44
21	DQ23	61	DQ45	101	RSVD	141	DQ46
22	DQ24	62	Vcc2	102	DQ25	142	RSVD
23	Vcc2	63	DQ47	103	RSVD	143	DQ48
24	DQ26	64	RSVD	104	DQ27	144	DQ49
25	DQ28	65	DQ50	105	DQ29	145	DQ51
26	DQ30	66	DQ52	106	DQ31	146	DQ53
27	RSVD	67	DQ54	107	A6	147	DQ55
28	A5	68	Vss	108	A8	148	Vss
29	A7	69	PRD0	109	A10	149	PRD1
30	A9	70	Vcc2	110	A12	150	RSVD
31	$\overline{BW2}$	71	DQ56	111	$\overline{BW3}$	151	RSVD
32	Vss	72	DQ57	112	Vss	152	DQ58
33	$\overline{BWE}$	73	Vss	113	CLK	153	Vss
34	A11	74	DQ59	114	A3	154	DQ60
35	A4	75	DQ61	115	$\overline{CE2}$	155	DQ62
36	RSVD	76	DQ63	116	RSVD	156	RSVD
37	$\overline{ADSC}$	77	PRD2	117	$\overline{ADSP}$	157	PRD3
38	RSVD	78	Vcc2	118	RSVD	158	RSVD
39	$\overline{CE}$	79	NC	119	RSVD	15	NC
40	Vss	80	Vss	120	Vss	160	Vss

GENERAL DESCRIPTION (continued)

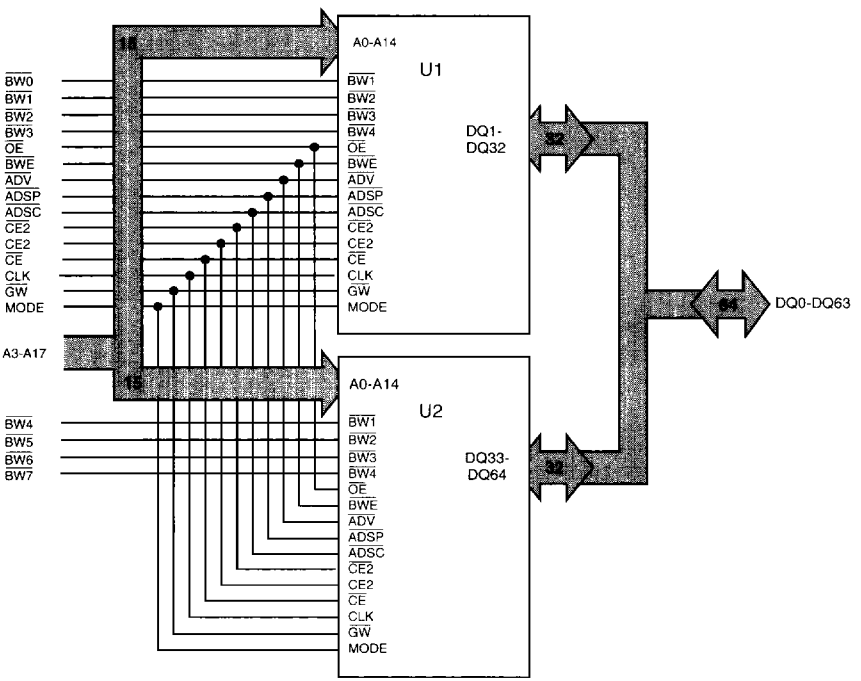
Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{BW0}$ controls DQ0-DQ7, $\overline{BW1}$ controls DQ8-DQ15, $\overline{BW2}$ controls DQ16-DQ23, $\overline{BW3}$ controls DQ24-DQ31 and so forth, conditioned by $\overline{BWE}$ being LOW. $\overline{GW}$ LOW causes all bytes to be written.

The "L" version of this module has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below Vcc MIN (3.1V), it will retain data with a minimum of power dissipation.

The module operates from a +3.3V power supply and all inputs and outputs are TTL compatible and 5V tolerant. This module is ideally suited to Pentium™ and Power PC™ systems and systems that benefit from a very wide data bus. The module is also ideal in generic 32- and 64-bit-wide applications. For additional functional and timing information consult the MT58LC32K32B2 synchronous SRAM data sheet.

FUNCTIONAL BLOCK DIAGRAM
256KB
(32K x 64)



U1-U2 = MT58LC32K32B2LG

NOTE: 1. The Functional Block Diagram illustrates simplified module operation. See MT58LC32K32B2 synchronous SRAM data sheet for more detailed functional information.

PIN DESCRIPTIONS

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
28-30, 34-35, 44, 46-47, 107-110, 114, 124, 126	A3-A17	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
20, 31, 56, 58, 100, 111, 136, 138	$\overline{BW0}$-7	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when $\overline{BWE}$ is LOW and must meet the setup and hold times around the rising edge of CLK. A BYTE WRITE enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW0}$ controls DQ0-DQ7. $\overline{BW1}$ controls DQ8-DQ15. $\overline{BW2}$ controls DQ16-DQ23. $\overline{BW3}$ controls DQ24-DQ31, and so forth. Data I/O are tristated if any of these eight inputs are LOW.
113	CLK	Input	Clock: This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
39	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
121	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to nable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
115	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
18	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
125	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
117	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$, but dependent upon CE2 and $\overline{CE2}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH. Power-down state is entered if CE2 is LOW or $\overline{CE2}$ is HIGH.

PIN DESCRIPTIONS (continued)

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
37	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be registered. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.
7, 27, 36, 38, 43, 64, 83, 92, 93, 101, 103, 116, 118, 119, 122, 123, 135, 142, 150, 151, 156, 158	RSVD	-	No Connect: These pins are reserved.
33	$\overline{BWE}$	Input	Byte Write Enable: This active low input permits byte write operations and must meet the setup and hold times around the rising edge of CLK.
41	$\overline{GW}$	Input	Global Write: This active low input allows a full 32-bit WRITE to occur independent of the $\overline{BWE}$ and $\overline{BW}$n lines and must meet the setup and hold times around the rising edge of CLK.
45	MODE	Input	Mode: This input selects the burst sequence. A low on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST. Do not alter input state while device is operating.
2, 4-6, 9-11, 13-14, 16-17, 21-22, 24-26, 49, 52-55, 59-61, 63, 65-67, 71-72, 74-76, 82, 84-87, 89-91, 95-98, 102, 104-106, 129, 132-134, 139-141, 143-147, 152, 154-155	DQ0-DQ63	Input/ Output	SRAM Data I/O: Byte 1 is DQ0-DQ7; Byte 2 is DQ8-DQ15; Byte 3 is DQ16-DQ23; Byte 4 is DQ24-DQ31 and so forth. Input data must meet setup and hold times around the rising edge of CLK.
3, 12, 23, 42, 62, 70, 78	Vcc2	Supply	Power Supply: +3.3V ±5%
1, 8, 15, 19, 32, 40, 51, 57, 68, 73, 80, 81, 88, 94, 99, 112, 120, 131, 137, 148, 153, 160	Vss	Supply	Ground: GND

PRESENCE-DETECT TABLE

Description	Size	PRD3	PRD2	PRD1	PRD0
None		NC	NC	NC	NC
Synchronous Pipelined	256KB	NC	Vss	NC	NC
Synchronous Pipelined	512KB	NC	Vss	NC	Vss
Synchronous	256KB	NC	Vss	Vss	NC
Synchronous	512KB	NC	Vss	Vss	Vss
Asynchronous	256KB	NC	NC	NC	Vss
Asynchronous	512KB	NC	NC	Vss	NC
Reserved		NC	NC	Vss	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6V
Storage Temperature (plastic) ..... -55°C to +125°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage			V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	$\overline{BW}$0-7	I_{LI1}	-1	1	µA	7
		A3-A17	I_{LI2}	-4	4	µA	7
		All other inputs	I_{LI3}	-2	2	µA	7
Output Leakage Current	Output(s) Disabled, 0V ≤ V_{OUT} ≤ V_{CC}		I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			V_{CC}	3.1	3.5	V	1

					MAX					
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-9	-10	-11	-12	UNITS	NOTES
Power Supply Current: Operating	Device selected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; outputs open	I_{CC1}	ALL	360	540	540	500	450	mA	3, 5, 6
Power Supply Current: Idle	Device selected; V_{CC} = MAX; $\overline{GW}$, $\overline{BW}$, $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; cycle time ≥ ^tKC MIN	I_{CC2}	ALL	56	90	90	90	80	mA	5, 6
CMOS Standby	Device deselected; V_{CC} = MAX; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; all inputs static; CLK frequency = 0	I_{SB1}	STD	1.0	10	10	10	10	mA	5, 6
			P	0.4	4	4	4	4	mA	
TTL Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	I_{SB2}	STD	30	50	50	50	50	mA	5, 6
			P	16	36	36	36	36	mA	
Clock Running	Device deselected; V_{CC} = MAX; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; CLK cycle time ≥ ^tKC MIN	I_{SB3}	ALL	60	100	100	100	90	mA	5, 6

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A3-A17, $\overline{ADSC}$, $\overline{GW}$, MODE	T_A = 25°C; f = 1 MHz	C_{I1}		10	pF	4
Input Capacitance: $\overline{ADSP}$, $\overline{ADV}$, CLK, $\overline{OE}$, $\overline{CE}$, $\overline{BWE}$	V_{CC} = 3.3V	C_{I2}		10	pF	4
Input Capacitance: $\overline{BW0}$-7		C_{I3}		5	pF	4
Input/Output Capacitance: DQ0-63		C_O		8	pF	4

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V
Data Retention Current	$\overline{CE}$, $\overline{CE2}$ ≥ (V_{CC} -0.2V), CE2 ≤ 0.2V V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V V_{CC} = 2V	I_{CCDR}		TBD	µA	8
Chip Deselect to Data Retention Time		^tCDR	^tKC		ns	4, 9
Operation Recovery Time		^tR	^tKC		ns	4

SYNCHRONOUS SRAM MODULE

NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: V_{IH} ≤ +6.0V for t ≤ ^tKC /2.
   Undershoot: V_{IL} ≥ -2.0V for t ≤ ^tKC /2.
   Power-up: V_{IH} ≤ +6.0V and Vcc ≤ 3.1V for t ≤ 200ms
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. "Device deselected" means device is in POWER-DOWN mode as defined in the Truth Table. "Device selected" means device is active (not in POWER-DOWN mode).
6. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
7. MODE pin has an internal pull-up and exhibits an input leakage current of ±10µA.
8. Typical values are measured at 25°C.
9. The device must have a deselect cycle applied at least one clock cycle before data retention mode is entered.