ALPHA
SEMICONDUCTOR
Excellence in Analog Power Products

AS OP-07

Ultra Low Offset Voltage Operational Amplifier

FEATURES

- Low offset Vos .... 25μV Max.
- Low drift vs. temperature:..................................... 0.6μV/°C
- High CMMR ... . 110 dB Min
- Low bias current... ±2nA Max.
- Low noise .... 0.6μV max., 0.1<f<10Hz
- Wide input voltage range .... ±14V
- Direct replacement for 725, 108A/308A, AD510 sockets

APPLICATIONS

- Sampling & Hold Amplifiers
- Integrators
- Medical Instrumentation
- Strain Gauge & Thermocouple

PRODUCT DESCRIPTION

The ALPHA Semiconductor AS OP-07 is an excellent choice for applications that require low offset voltage (25μV Max. for OP-07A), low drift with time and temperature (1.0 mV/Month Max) and very low noise. The OP-07 also offers high open-loop gain, and wide input voltage range. Use of ALPHA Semiconductor's design, processing and testing techniques make our OP-07 superior over similar products.

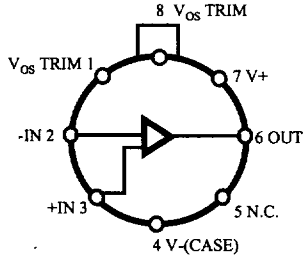
The OP-07 is available in five different grades. The AS OP-07 is available in hermetically sealed TO-99 metal can and 8-pin PDIP and SOIC packages. The operating temperature is 0°C to 70°C and -55°C to +125°C. For improved specification, look for AS OP77.

ORDERING INFORMATION

TO-99 8-PIN	PLASTIC DIP 8-PIN	PLASTIC SOIC 8-PIN	TA=25°C V_{OS} Max (μv)	Oper. Temp. Range
OP07AJ			25	MIL.
OP07EJ	OP07EP	OP07ES	75	COM.
OP07J			75	MIL.
OP07CJ	OP07CP	OP07CS	150	COM.
OP07DJ	OP07DP	OP07DS	150	COM.

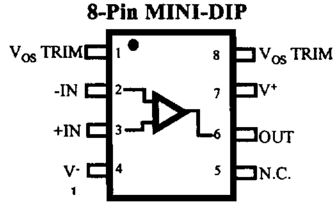
PIN CONNECTIONS

TO-99



Bottom View

8-Pin Surface Mount
8-Pin MINI-DIP



Top View

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage .... ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage .... ±30V
Input Voltage (Note 2) .... ±22V
Output Short-Circuit Duration .... Indefinite
Storage Temperature Range
J Packages .... -65 to +150°C
P Packages .... -65 to +125°C
Operating Temperature Range
OP07A, OP07B, OP07 .... -55 to +125°C
OP07E, OP07C, OP07D .... 0 to +70°C
Dice Junction Temperature(Tj) .... -65 to +150°C
Lead Temperature (Soldering, 60 Sec.) .... 300°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both DICE and packaged parts unless otherwise noted.
3. For Supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99(J)	80°C	7.1 mW/°C
9-Pin Plastic DIP (P)	36°C	5.6 mW/°C

ELECTRICAL CHARACTERISTICS at V_S=±15V, Ta=25°C, unless otherwise specified.

Parameter	Symbol	Conditions	OP-07A Min.	OP-07A Typ.	OP-07A Max.	OP-07 Min.	OP-07 Typ.	OP-07 Max.	Units
Input Offset Voltage	V_{os}	(Note 1)		10	25		30	75	µV
Long-Term Input offset Voltage Stability	V_{OS}/Time	(Note 2)		0.2	1.0		0.2	1.0	µV/M_o
Input Offset Current	I_{os}			0.3	2.0		0.4	2.8	nA
Input Bias Current	I_B			±0.7	±2.0		±1.0	±3.0	nA
Input Noise Voltage	e_{npp}	0.1Hz to10Hz (Note3)		0.35	0.6		0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	f_o=10Hz(Note 3)		10.3	18.0		10.3	18.0	nV/√Hz
Input Noise Voltage Density	e_n	f_o=100Hz(Note 3)		10.0	13.0		10.0	13.0	nV/√Hz
Input Noise Voltage Density	e_n	f_o=1000Hz(Note 3)		9.6	11.0		9.6	11.0	nV/√Hz
Input Noise Current	$i_{np\ p}$	0.1 Hz to 10Hz (Note3)		14	30		14	30	pA_{p-p}
Input Noise Current Density	i_n	f_o=10Hz(Note 3)		0.32	0.80		0.32	0.80	pA/√Hz
Input Noise Current Density	i_n	f_o=100 Hz(Note 3)		0.14	0.23		0.14	0.23	pA/√Hz
Input Noise Current Density	i_n	f_o=1000Hz(Note 3)		0.12	0.17		0.12	0.17	pA/√Hz
Input Resistance-Differential-Mode	R_{in}	(Note 4)	30	80		20	60		MΩ
Input Resistance-Common-Mode	R_{inCM}			200			200		GΩ
Input Voltage Range	IVR		±13	±14		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM}=±13.0	110	126		110	126		dB
Power Supply Rejection Ratio	PSRR	V_S=±3V to ±18		4	10		4	10	µV/V
Large Signal Voltage Gain	AV_O	$R_l \geq 2k\Omega$ V_o=±10V	300	500		200	500		V/mV
Large Signal Voltage Gain	AV_O	Rl ≥500Ω V_o=±0.5 V_s=±3V (Note 4)	150	400		150	400		V/mV
Output Voltage Swing	V_o	Rl ≥10kΩ	± 12.5	± 13.0		± 12.5	± 13.0		V
Output Voltage Swing	V_o	Rl ≥2kΩ	± 12.0	± 12.8		± 12.0	± 12.8		V
Output Voltage Swing	V_o	Rl ≥1kΩ	± 10.5	± 12.0		± 10.5	± 12.0		V
Slew Rate	SR	Rl ≥2kΩ (Note 3)	0.1	0.3		0.1	0.3		V/µs
Closed-Loop Bandwith	BW	A_{vcl}=+1.0(Note 3)	0.4	0.6		0.4	0.6		MHz
Open-Loop Output Resistance	R_o	V_o=0, Io=0		60			60		Ω
Power Consumption	P_d	Vs=±15V, No Load		75	120		75	120	mW
Power Consumption	P_d	V_s=±3V, No load		4	6		4	6	mW
Offset Adjustment Range		R_p=20kΩ		±4			±4		mV

Notes:

1. OP-07 grade Vos is measured approximately one minute after application of power. For all other grades Vos is measured approximately 0.5 seconds after application of power.
2. Long Term input offset voltage stability refers to the averaged trend line of Vos vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days are typically 2.5mV.
3. Sample tested.
4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at V_S=±15V, Ta=25°C, unless otherwise specified.

Parameter	Symbol	Conditions	OP-07E Min.	OP-07E Typ.	OP-07E Max.	OP-07C Min.	OP-07C Typ.	OP-07C Max.	OP-07D Min.	OP-07D Typ.	OP-07D Max	Units
Input Offset Voltage	V_{os}	(Note 1)		30	75		60	150		60	150	µV
Long-Term V_{os} Stability	V_{OS}/Time	(Note 2)		0.3	1.5		0.4	2.0		0.5	3.0	$\mu V/M_o$
Input Offset Current	I_{os}			0.5	3.8		0.8	6.0		0.8	6.0	nA
Input Bias Current	I_B			±1.2	±4.0		±1.8	±7.0		±2.0	±12	nA
Input Noise Voltage	e_{npp}	0.1Hz to10Hz (Note3)		0.35	0.6		0.38	0.65		0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	f_o=10Hz(Note 3)		10.3	18.0		10.5	20.0		10.5	20.0	nV/√Hz
Input Noise Voltage Density	e_n	f_o=100Hz(Note 3)		10.0	13.0		10.2	13.5		10.3	13.5	nV/√Hz
Input Noise Voltage Density	e_n	f_o=1000Hz(Note 3)		9.6	11.0		9.8	11.5		9.8	11.5	nV/√Hz
Input Noise Current	$i_{np\,p}$	0.1 Hz to 10Hz (Note3)		14	30		15	35		15	35	pA_{p-p}
Input Noise Current Density	i_n	f_o=10Hz(Note 3)		0.32	0.80		0.35	0.90		0.35	0.90	pA/√Hz
Input Noise Current Density	i_n	f_o=100 Hz(Note 3)		0.14	0.23		0.15	0.27		0.15	0.27	pA/√Hz
Input Noise Current Density	i_n	f_o=1000Hz(Note 3)		0.12	0.17		0.13	0.18		0.13	0.18	pA/√Hz
Input Resistance-Differential-Mode	R_{in}	(Note 4)	15	50		8	33		7	31		MΩ
Input Resistance-Common-Mode	R_{inCM}			160			120			120		GΩ
Input Voltage Range	IVR		±13	±14		±13	±14		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM}=±13.0	106	123		100	120		94	110		dB
Power Supply Rejection Ratio	PSRR	V_S=±3V to ±18		5	20		7	32		7	32	µV/V
Large Signal Voltage Gain	AV_O	R_l ≥2kΩ V_o=±10V	200	500		120	400		120	400		V/mV
Large Signal Voltage Gain	AV_O	Rl ≥500Ω V_o=±0.5 V_s=±3V (Note 4)	150	400		100	400			400		V/mV
Output Voltage Swing	V_o	Rl ≥10kΩ	±12.5	±13.0		±12.0	±13.0		±12.0	±13.0		V
Output Voltage Swing	V_o	Rl ≥2kΩ	±12.0	±12.8		±11.5	±12.8		±11.5	±12.8		V
Output Voltage Swing	V_o	Rl ≥1kΩ	±10.5	±12.0			±12.0			±12.0		V
Slewing Rate	SR	Rl ≥2kΩ (Note 3)	0.1	0.3		0.1	0.3		0.1	0.3		V/µs
Closed-Loop Bandwith	BW	A_{vcl}=+1.0(Note 3)	0.4	0.6		0.4	0.6		0.4	0.6		MHz
Open-Loop Output Resistance	R_o	V_o=0, Io=0		60			60			60		Ω
Power Consumption	P_d	Vs=±15V, No Load		75	120		80	150		80	150	mW
Power Consumption	P_d	V_s=±3V, No load		4	6		4	8		4	8	mW
Offset Adjustment Range		R_p=20kΩ		±4			±4			±4		mV

ELECTRICAL CHARACTERISTICS at V_S=±15V, -55°C£Ta£+125°C, unless otherwise specified.

Parameter	Symbol	Conditions	OP-07A Min.	OP-07A Typ.	OP-07A Max.	OP-07 Min.	OP-07 Typ.	OP-07 Max.	Units
Input Offset Voltage	V_{OS}	(Note 1)		25	60		60	200	µV
Average Input Offset Voltage Drift Without External Trim With External Trim	 TCV_{OS} TCV_{OS}	 (Note 2) R,=20kΩ (Note 3)		 0.2 0.2	 0.6 0.6		 0.3 0.3	 1.3 1.3	µV/°C µV/°C
Input Offset Current	I_{OS}			0.8	4		1.2	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	Note 2		5	25		8	50	pA/°C
Input Bias Current	I_B			±1	±4		±2	±6	nA
Average Input Bias Current Drift	TCI_B	Note 2		8	25		13	50	pA/°C
Input Voltage Range	IVR		±13	±13.5		±13	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} ±13.0 V	106	123		106	123		dB
Power Supply Rejection Ratio	PSRR	V_s=±3V to ±18V		5	20		5	20	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_l \geq 2k\Omega$, V_o= ±10V	200	400		150	400		V/mV
Output Voltage Swing	V_O	$R_l \geq 2k\Omega$	±12	±12.6		±11	±12.6		V

Notes:

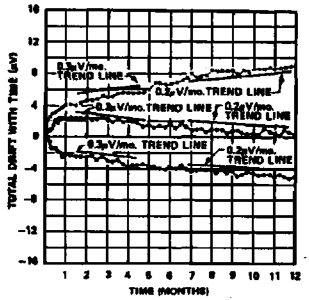
1. OP-07 grade Vos is measured approximatly one minute after application of power. For all other grades Vos is measured approximately 0.5 seconds after application of power
2. Sample tested.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at V_S=±15V, 0°C£Ta£+70°C, unless otherwise specified.

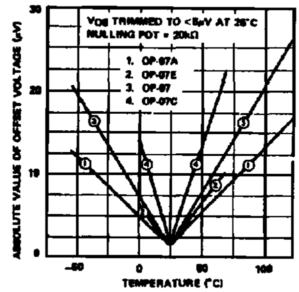
Parameter	Symbol	Conditions	OP-07E Min.	OP-07E Typ.	OP-07E Max.	OP-07C Min.	OP-07C Typ.	OP-07C Max.	OP-07D Min.	OP-07D Typ.	OP-07D Max.	Units
Input Offset Voltage	V_{OS}			45	130		85	250		85	250	µV
Avaeage Input Offset Voltage Drift Without External Trim With External Trim	 TCV_{OS} TCV_{OS}	 (Note 2) R,=20kΩ (Note 3)		 0.3 0.3	 1.3 1.3		 0.5 0.4	 1.8 1.6		 0.7 0.7	 2.5 2.5	µV/°C µV/°C
Input Offset Current	I_{OS}			0.9	5.3		1.6	8.0		1.6	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	Note 2		8	35		12	50		12	50	pA/°C
Input Bias Current	I_B			±1.5	±5.5		±2.2	±9.0		±3.0	±14	nA
Average Input Bias Current Drift	TCI_B	Note 2		13	35		18	50		18	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5		±13.0	±13.5		±13.0	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} ±13.0 V	103	123		97	120		94	106		dB
Power Supply Rejection Ratio	PSRR	V_s=±3V to ±18V		7	32		10	51		10	51	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_l \geq 2k\Omega$, V_o= ± 10V	180	450		100	400		100	400		V/mV
Output Voltage Swing	V_O	$R_l \geq 2k\Omega$	±12	±12.6		±11	±12.6		±11	±12.6		V

TYPICAL CHARACTERISTICS

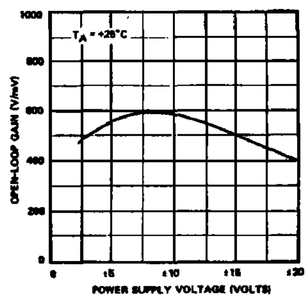
OFFSET VOLTAGE STABILITY vs TIME



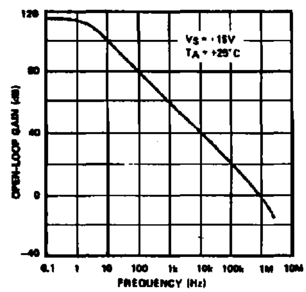
TRIMMED OFFSET VOLTAGE vs TEMPERATURE



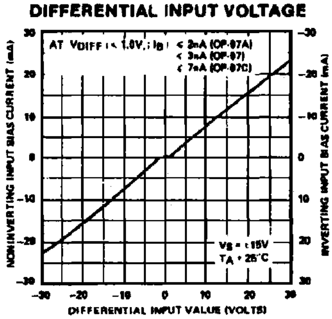
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



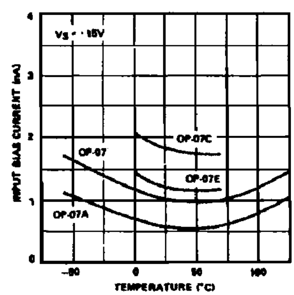
OPEN-LOOP FREQUENCY RESPONSE



INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE

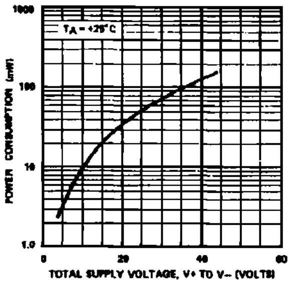


INPUT BIAS CURRENT vs TEMPERATURE

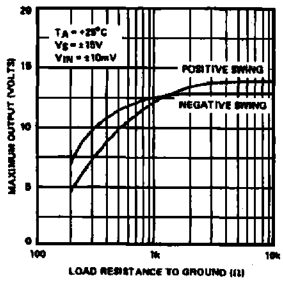


TYPICAL CHARACTERISTICS

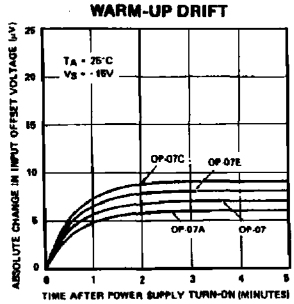
POWER CONSUMPTION vs POWER SUPPLY



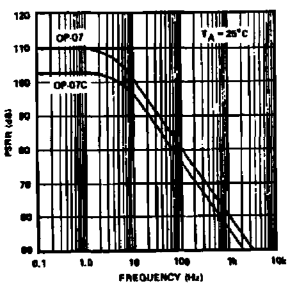
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



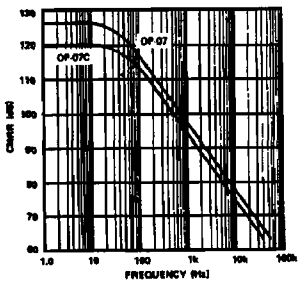
WARM-UP DRIFT



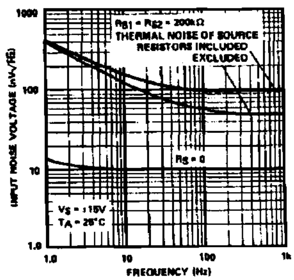
PSRR vs FREQUENCY



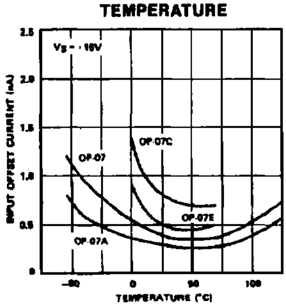
CMRR vs FREQUENCY



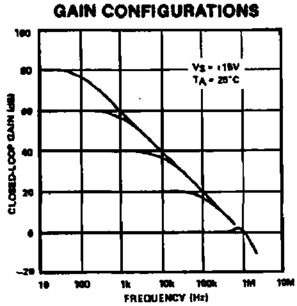
TOTAL INPUT NOISE VOLTAGE vs FREQUENCY



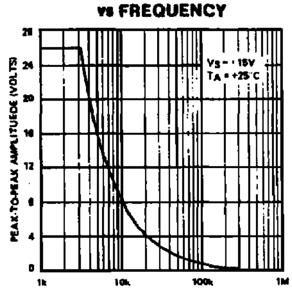
INPUT OFFSET CURRENT vs TEMPERATURE



CLOSED-LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



MAXIMUM OUTPUT SWING vs FREQUENCY

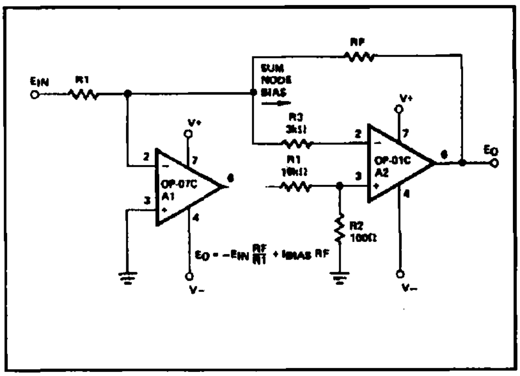


APPLICATION HINTS

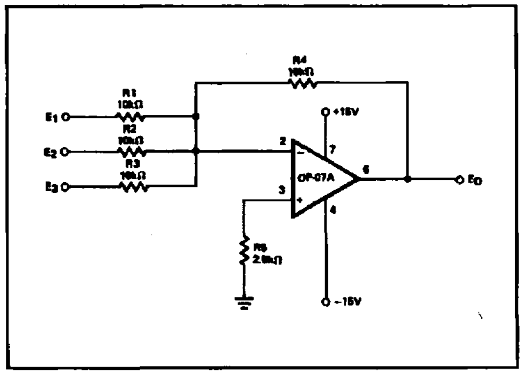
OP-07 series devices can be fitted directly to 725 and 108/108A Series sockets with or without removal of external compensation components. Additionally, the OP-07 may be fitted to unnulled 741 series. However, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-07 operation. The OP-07 provides stable operation with load capacitance of up to 500pF and ±10V swings; larger capacitances should be decoupled with a 50Ω resistor.

Offset stability can be degraded by stray thermoelectric voltages arising from dissimilar metals at the contacts to the input terminals. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

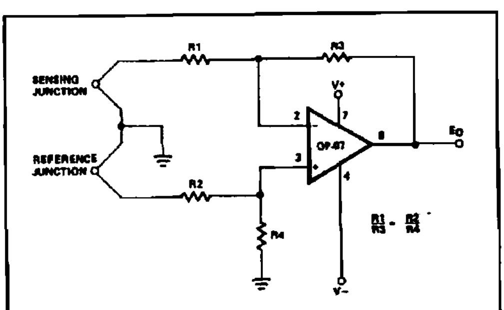
HIGH SPEED, LOW V_{OS}, COMPOSITE AMPLIFIER



ADJUSTMENT-FREE PRECISION SUMMING AMPLIFIER

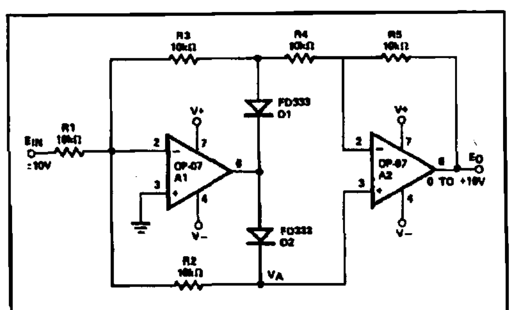


HIGH-STABILITY THERMOCOUPLE AMPLIFIER



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

PRECISION ABSOLUTE-VALUE CIRCUIT



PINOUTS SHOWN FOR J, P, AND Z PACKAGES