T-79-06-20

VA4701

QUAD LOW-NOISE PRECISION OPERATIONAL AMPLIFIER

PRELIMINARY INFORMATION

FEATURES

- Low Noise: 3.0 nV/√Hz at 1KHz
- High Speed: 10 V/μs Slew Rate
  30MHz Gain Bandwidth
- Fast Settling: 10μs to 0.01%
- Low Offset Voltage: 10μV
- Large Output Current: ±50mA
- High Gain: 5 million
- Large Output Swing: ±4V
- Large Input Common Mode Range: ±3.5V

DESCRIPTION

The VA4701 is a quad precision operational version of the VA701. The design architecture is optimized for performance with ±5V supplies. For example, the output voltage swing is typically ±4V while input common mode range is ±3.5V.

The low offset voltage of 250μV and offset current of 50nA maximum makes the amplifier ideal for precision instrumentation applications. In addition, the low noise of 3nV/√Hz insures that amplification accuracy is maintained with low level input signals.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages ..... ±6.5V
Common Mode Input Voltage ..... $\pm V_S$
Differential Input Voltage ..... ±0.7V
Power Dissipation (Note 1, 2) 450mW
Operating Temperature Range:
  Commercial ..... 0° to 70°C
  Military ..... -55° to+125°C
Storage Temperature Range ..... -65° to +150°C
Lead Temperature (Soldering to 60 Sec.) ..... 300°C

Note 1: Power derating above T_A = 70°C to be based on a maximum junction temperature of 150°C and the following thermal resistance factors:

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)
DIP	75	145
SOIC	95	145
LCC	75	145

Note 2: Continuous short circuit protection is allowed to the following case and ambient temperatures:

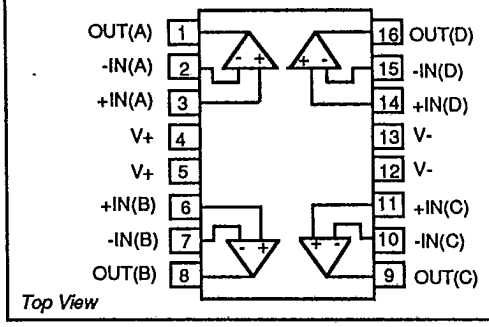
PACKAGE	T_C (°C)	T_A (°C)
DIP	110	70
SOIC	95	70
LCC	110	70

PACKAGE TYPES AVAILABLE

- 14-Pin Plastic DIP
- 14-Pin CERDIP
- 16-Pin SOIC
- 20-Pin LCC

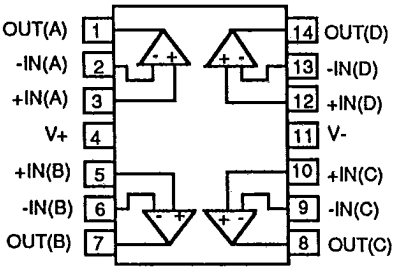
CONNECTION DIAGRAMS

SOIC Package



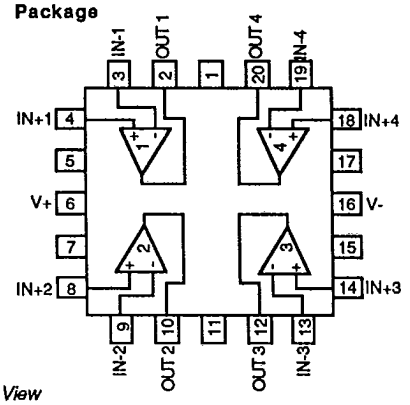
Top View

Dual In-Line Package



Top View

LCC Package



Top View

ELECTRICAL CHARACTERISTICS (V_S = ±5V, T_A = 25°C unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	VA4701J			VA4701S			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			450	500		250		µV
		0°≤T_A ≤70°C		550	800			400	
		-55°≤T_A ≤ +125°C					550	800	
Input Offset Voltage Drift		0°≤T_A ≤70°C			1.0				µV/°C
		-55°≤T_A ≤ +125°C						0.5	
Long Term V_{OS} Stability	V_{OS}/Time	(Notes 1, 2)			3			3	µV/Mo.
Input Offset Current	I_{OS}				150			100	nA
		0°≤T_A ≤70°C			200				
		-55°≤T_A ≤ +125°C						100	
Input Offset Current Drift		0°≤T_A ≤70°C		150					pA/°C
		-55°≤T_A ≤ +125°C					300		
Input Bias Current	I_B			50	200		25	100	nA
		0°≤T_A ≤70°C			200				
		-55°≤T_A ≤ +125°C						200	
Input Differential Resistance (Note 3)	R_{IN}				0.8			1.5	MΩ
Input Common Mode Resistance (Note 3)	R_{INCM}			2			3		GΩ
Large Signal Voltage Gain (Note 3)	A_V	R_L > 2KΩ V_{OUT} = ±3.5V	700	6,000		1,000	6,000		V/mV
Input Common Mode Range	V_{CM}		±3.5			±3.5			V
Output Voltage Swing	V_{OUT}	R_L = 2KΩ	±3.5	±4.0		±3.5	±4.0		V
		R_L = 51Ω	±2.5			±2.5			
Power Supply Current	I_S			32	48		32	48	mA
Positive Current Limit	$+I_{SC}$		60		180	60		180	mA
Negative Current Limit	$-I_{SC}$		60		180	60		180	mA
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5	100			114			dB
Power-Supply Rejection Ratio	PSRR	ΔV_{PS} = ±1.0V	94			100			dB

Notes: 1. Long term input offset voltage stability refers to the average trend line of V_{OS} vs Time over extend periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5µV.

2. Sample tested only.

3. Not tested, guaranteed by design.

AC and NOISE CHARACTERISTCS (V_S = ±5V, T_A = 25°C unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	VA4701J			VA4701S			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Noise Voltage	enp-p	f= 1KHz (Note 1)		0.25	0.75		0.18	0.36	µVp-p
Input Noise Voltage Density	e_n	f = 1KHz (Note 1)		3.8	4.5		3.0	3.8	nV/√Hz
Input Noise Current Density	I_n	f = 1KHz		1.0			1.0		pA/√Hz
Slew Rate	SR		6.0	10		6.0	10		V/µs
Gain Bandwidth Product	GBW	f = 100KHz		30			30		MHz
		f = 16MHz		16			16		
Settling Time	t_s	±3.5V Step		10			10		µs

Note 1: Sample tested only.

SIMPLIFIED SCHEMATIC (One Amplifier)