VTC Incorporated

VA4708

T-79-07-20

QUAD HIGH-SPEED, FAST-SETTLING, HIGH OUTPUT CURRENT OPERATIONAL AMPLIFIER, $A_{CL} \geq 3$

FEATURES

- Fast Settling Time: ±0.1% in 150ns
- High Slew Rate: 90V/µs
- Large Gain Bandwidth: 100MHz
- Full Power Bandwidth: 4.8MHz at 6V p-p
- Ease of Use: Internally Compensated for $A_{CL} \geq 3$ with 50° - 60° phase margin
- Large Output Current: ±50mA
- Low Supply Voltage Operation: ±4V
- Minimal Crosstalk: >90 dB Separation
- Short Circuit Protection
- Available in Commercial Version

DESCRIPTION

The VA4708 offers the high-speed and fast-settling advantages of the VA708 in a quad package configuration. The high slew rate, output drive and open-loop gain allows the amplifier to fit analog amplification and high speed processing applications, capable of driving large capacitance loads at high speeds.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±6V
Differential Input Voltage	±9V
Common Mode Input Voltage	$\|V_S\|$ -0.5V
Power Dissipation (T_A =70°C, Note 1)	550mW
Output Short Circuit Current Duration (Note 2)	Indefinite
Operating Temperature Range:	
Commercial (4708 J)	0° to 70°C
Storage Temperature Range	-65° to +150°C
Lead Temperature (Soldering to 60 Sec.)	300°C

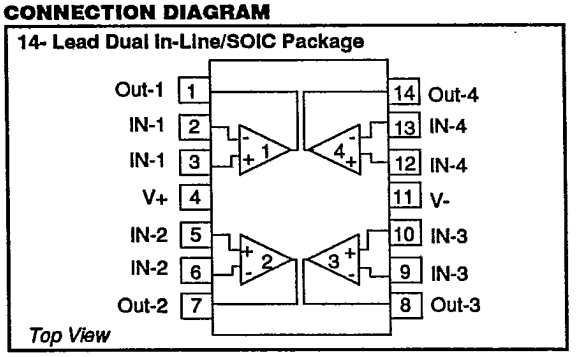
Note 1: Power derating above T_A = 70°C to be based on a maximum junction temperature of 150°C and the thermal resistance factors of θ_{JC} = 75°C/W and θ_{JA} = 145°C/W.
Note 2: Continuous short-circuit protection is allowed on one amplifier per time up to case temperatures of 85°C and ambient temperatures of 30°C.

PACKAGE TYPES AVAILABLE

- 14-Pin Plastic DIP
- 14-Pin SOIC

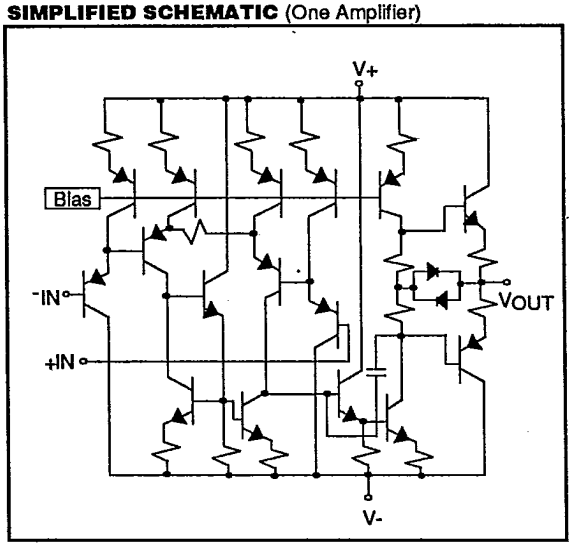
CONNECTION DIAGRAM

14- Lead Dual In-Line/SOIC Package



Top View

SIMPLIFIED SCHEMATIC (One Amplifier)



ELECTRICAL CHARACTERISTICS (V_S= ±5V, T_A = 25° C unless otherwise stated) (each amplifier)

PARAMETER	SYMBOL	CONDITIONS	VA4708J MIN	VA4708J TYP	VA4708J MAX	UNITS
Input Offset Voltage	V_{OS}			5	12	mV
T_{Min} to T_{Max}		0°≤T_A≤70°C		8	16	
		-55≤T_A≤125°C				
Average Offset Voltage Drift	$\frac{\Delta V_{OS}}{\Delta T}$	0°≤T_A≤70°C		20		µV/°C
		-55≤T_A≤125°C				
Input Bias Current	I_B			650	1100	nA
T_{Min} to T_{Max}		0°≤T_A≤70°C			1700	
		-55≤T_A≤125°C				
Input Offset Current	I_{OS}			35	120	nA
Input Common Mode Range	V_{CM}		+3 -4	+3.5 -4.5		V
Differential Input Resistance	R_{IND}	(Note 1)	3	10		MΩ
Common Mode Input Resistance	R_{INC}	(Note 1)	4	8		MΩ
Differential Input Capacitance	C_{IND}	(Note 1)		2		pF
Common Mode Input Capacitance	C_{INC}	(Note 1)		3		pF
Input Voltage Noise	e_N	BW = 10Hz to 100KHz		12		µVRMS
Open Loop Voltage Gain	A_V	V_{OUT}=±3V R_L=2kΩ	2	5		V/mV
Output Voltage Swing	V_{OUT}	R_L=2kΩ	±3.5			V
		R_L=51Ω	±2.0	±2.4		
Power Supply Current (All Four Amplifiers)	I_S			30	40	mA
Common Mode Rejection Ratio	CMRR	V_{CM} =±2V	60	70		dB
Power Supply Rejection Ratio	PSRR	ΔV_{PS} =±0.5V	60	66		dB
Slew Rate	SR	10-90%of Leading Edge (Figure 1)	60	90		V/µs
Settling Time	t_S	To ±0.1%(±4mV) of Final Value (Figure 1, Note 1)		150	200	ns
Gain Bandwidth Product	GBW			100		MHz
Small Signal Rise/Fall Time	t_r / t_f	e_O = ±100mV 10-90% (Figure 1)		7		ns
Full Power Bandwidth	BW_{FP}	R_L= 2kΩ C_L= 50pF V_{OUT}= 6Vp-p		4.8		MHz
Amplifier to Amplifier Crosstalk		Input Referenced f=10KHz (Figure 2)		-96		dB

Notes: 1. Not tested, guaranteed by design.

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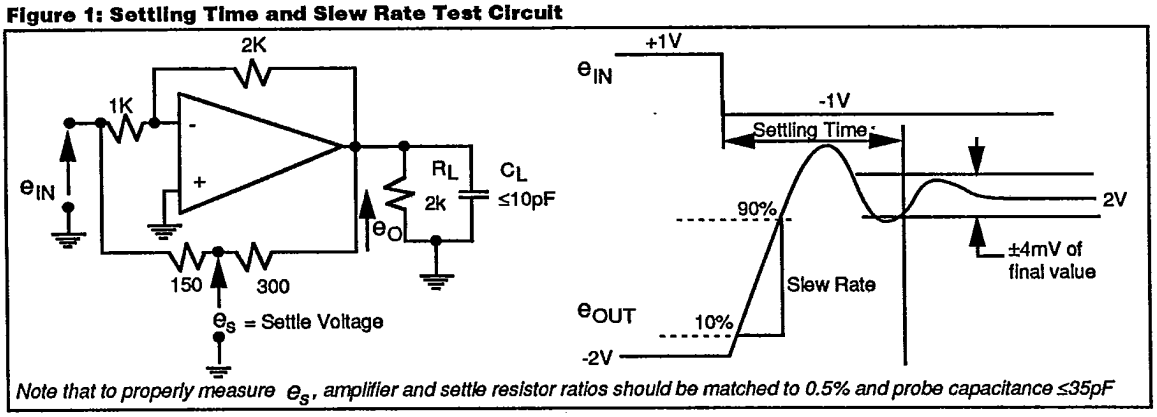
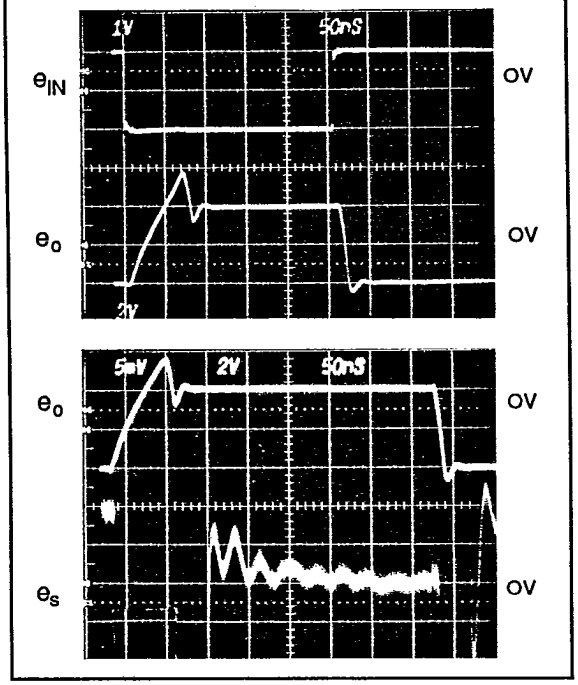
Figure 1: Settling Time and Slew Rate Test Circuit



Note that to properly measure e_S, amplifier and settle resistor ratios should be matched to 0.5% and probe capacitance ≤35pF

Large Signal Response



Small Signal Response

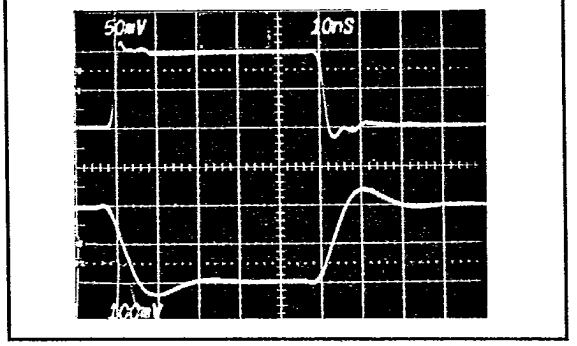
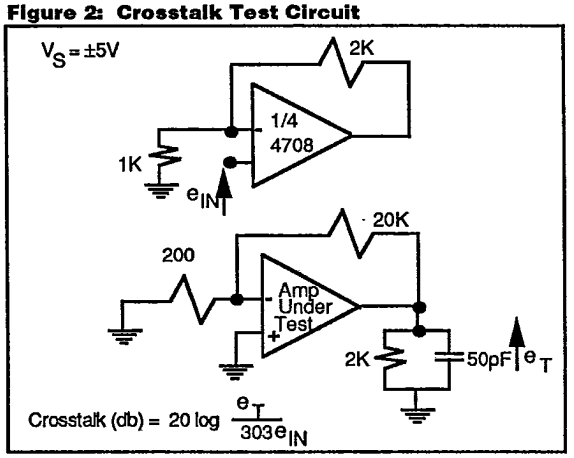


Figure 2: Crosstalk Test Circuit



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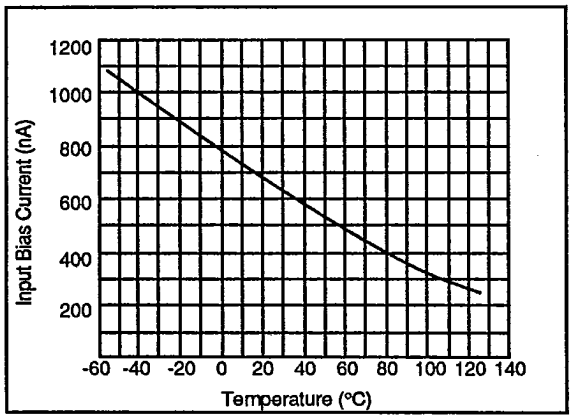
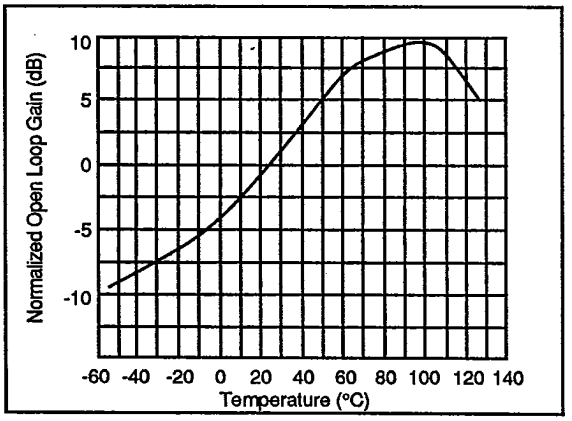
TYPICAL PERFORMANCE CHARACTERISTICS (V_S= ±5V, T_A = 25° C unless otherwise stated)

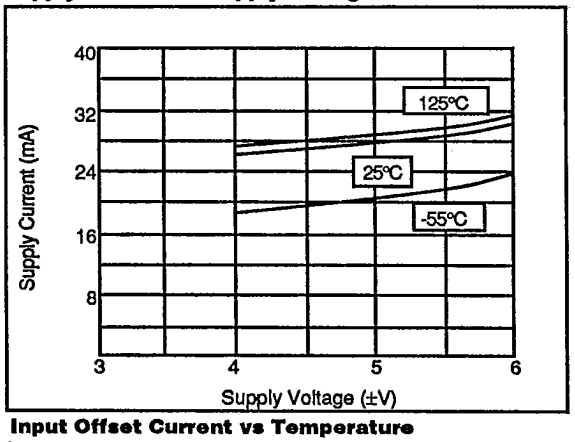
Input Bias Current vs Temperature



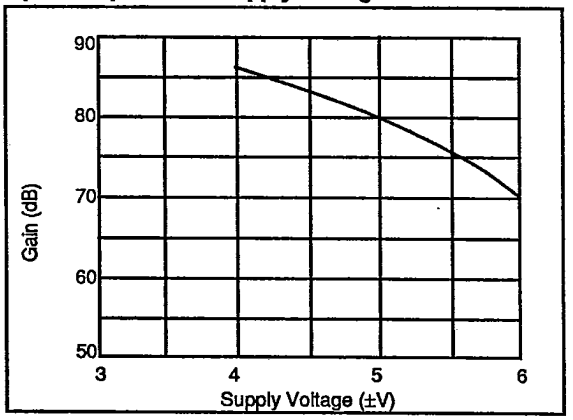
Normalized Open Loop Gain vs Temperature



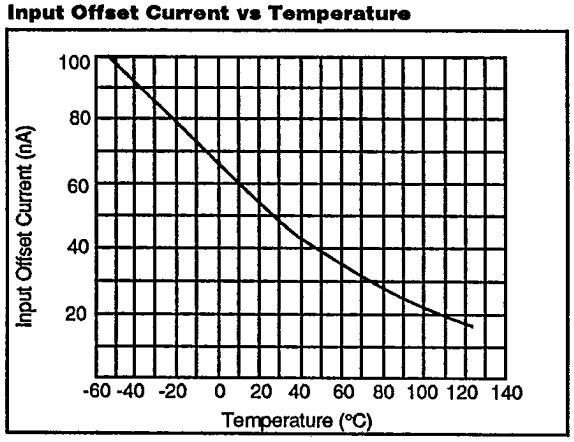
Supply Current vs Supply Voltage



Open Loop Gain vs Supply Voltage



Input Offset Current vs Temperature



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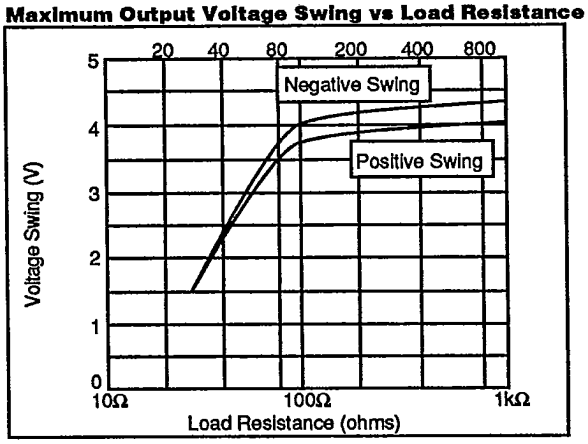
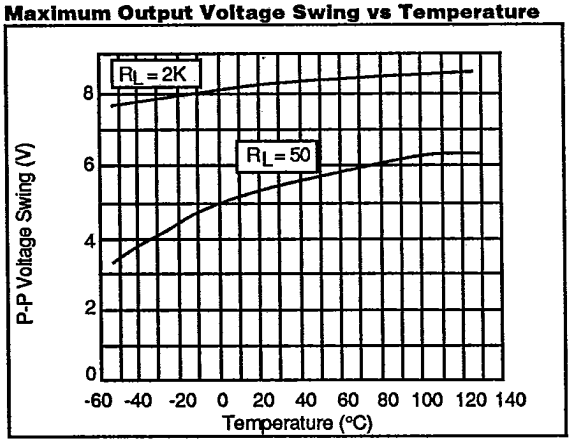
TYPICAL PERFORMANCE CHARACTERISTICS (V_S= ±5V, T_A = 25° C unless otherwise stated)

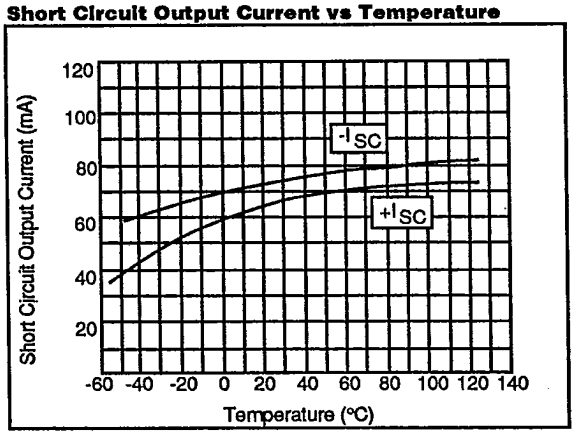
Maximum Output Voltage Swing vs Load Resistance



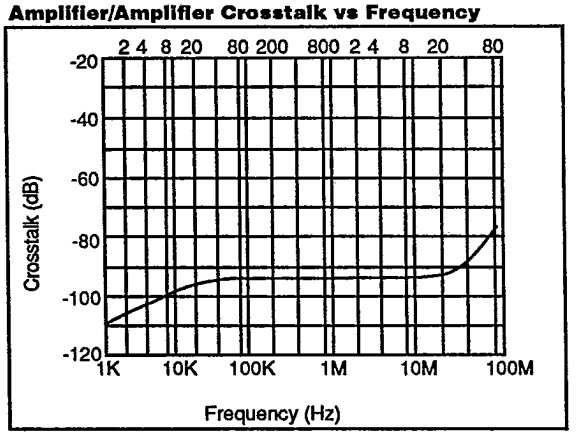
Maximum Output Voltage Swing vs Temperature



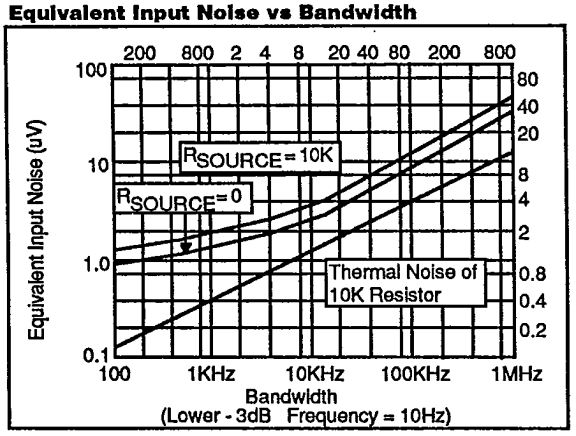
Short Circuit Output Current vs Temperature



Amplifier/Amplifier Crosstalk vs Frequency



Equivalent Input Noise vs Bandwidth



VA4708

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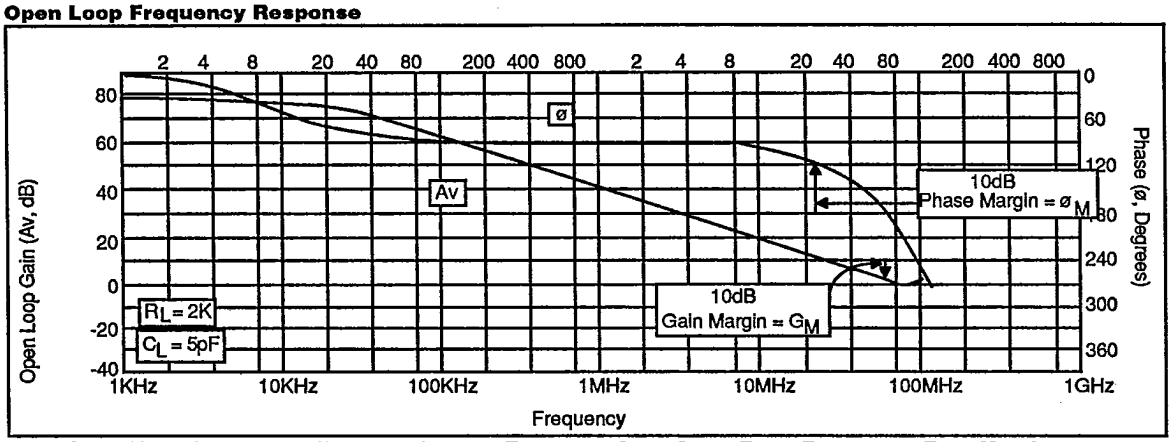
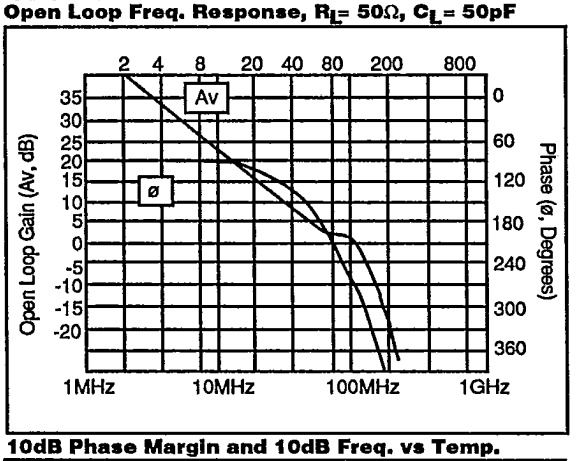
TYPICAL PERFORMANCE CHARACTERISTICS (V_S= ±5V, T_A = 25° C unless otherwise stated)

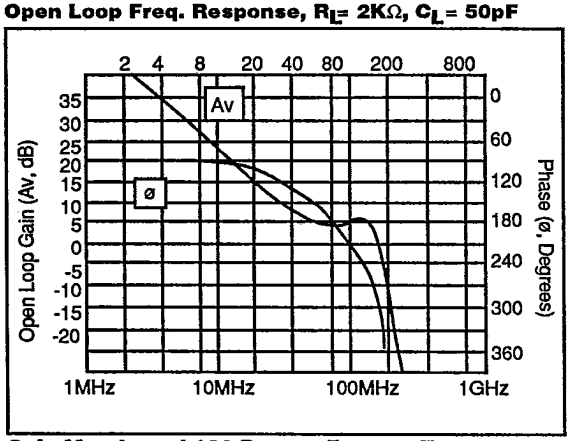
Open Loop Frequency Response



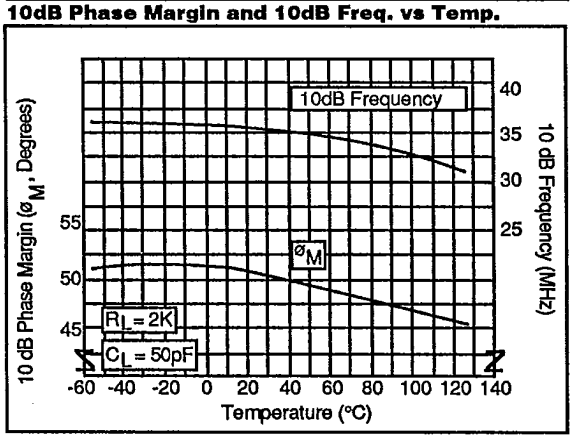
Open Loop Freq. Response, R_L= 50Ω, C_L= 50pF



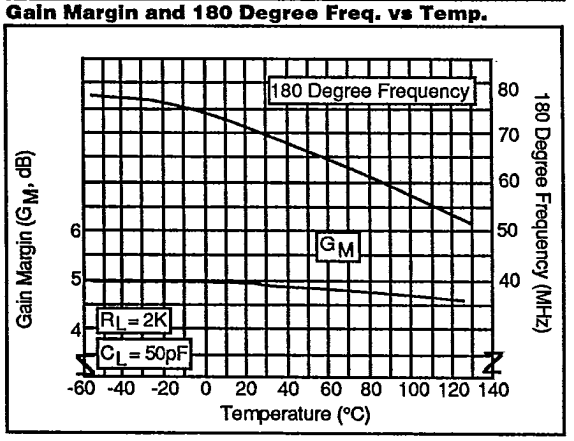
Open Loop Freq. Response, R_L= 2KΩ, C_L= 50pF



10dB Phase Margin and 10dB Freq. vs Temp.



Gain Margin and 180 Degree Freq. vs Temp.



APPLICATION INFORMATION

AC Characteristics

The 35MHz 10dB crossover point of the VA4708 is achieved without feed forward compensation, a technique which can produce long tails in the recovery characteristics. The single pole rolloff follows the classic 20dB/decade slope to frequencies approaching 50MHz. The 10dB (3.2 V/V) phase margin of 50°, even with a capacitive load of 50pF, gives stable and predictable performance down to non-inverting gain configurations of approximately 3 V/V (inverting gains of -2V/V). At frequencies beyond 50MHz, the 20dB/decade slope is disturbed by an output stage zero, the damping factor of which is dependent upon the R_L , C_L load combination. This results in loss of gain margin (gain at loop phase = 360°) at frequencies of 70 to 100MHz which at a gain margin of 5dB (R_L = 2K, C_L = 50pF) results in a peak in the gain of 3 amplifier configurations as shown in Figures 3 and 4.

Figure 3 shows a blow up of the open loop characteristics in the 10MHz to 200MHz frequency range, as well as the corresponding closed loop characteristics for a gain of 3 non-inverting amplifier at similar load conditions. It should be noted that the open loop characteristic does not show the additional phase shift caused by the input capacitance pole — this is why the closed loop peaking at 30 to 40MHz is greater than what would be expected from the 50 to 60 degrees of phase margin indicated by the open loop characteristics. Corresponding small signal step response characteristics show well-behaved pulse waveforms with 16-33% overshoot.

The input capacitive pole can be neutralized by adding a feedback capacitor to R_2 . The value of capacitance is selected according to $R_1 C_{IN} = R_2 C_{FB}$, where C_{IN} is the sum of the common mode and differential input capacitance ≈ 5pF. For $R_2 = 2R_1$, $C_{FB} = C_{IN}/2 \approx 2.5$pF.

Figure 4 shows the results of this feedback capacitor addition. Neutralizing the input capacitance demonstrates the peaking that can result from the loss of gain margin at 70 to 100MHz. As the load time constant ($R_L C_L$) increases the peaking gets progressively worse ≈ 6dB at R_L = 2K, C_L = 50pF. The step response waveforms are as expected with a very strong 88MHz ring being exhibited at R_L = 2K, C_L = 50pF and no overshoot at R_L = 50Ω, C_L = 5pF.

Layout Considerations

As with any high-speed wideband amplifier, certain layout considerations are necessary to ensure stable operation. All connections to the amplifier should be kept as short as possible, and the power supplies bypassed with 0.1μF capacitors to signal ground. It is suggested that a ground plane be considered as the best method for ensuring stability because it minimizes stray inductance and unwanted coupling in the ground signal paths.

To minimize capacitive effects, resistor values should be kept as small as possible, consistent with the application.

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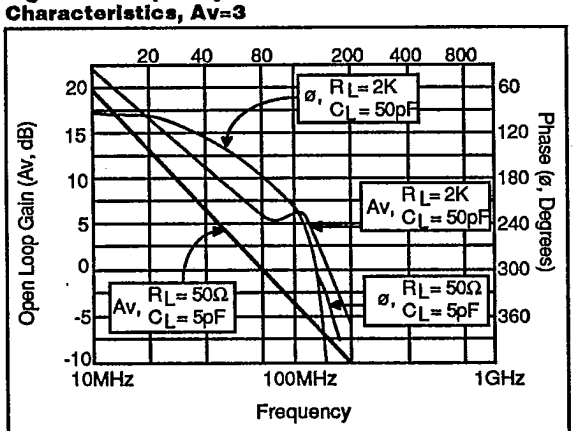
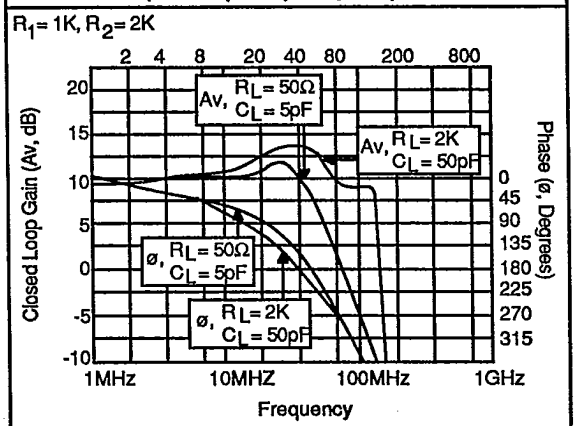
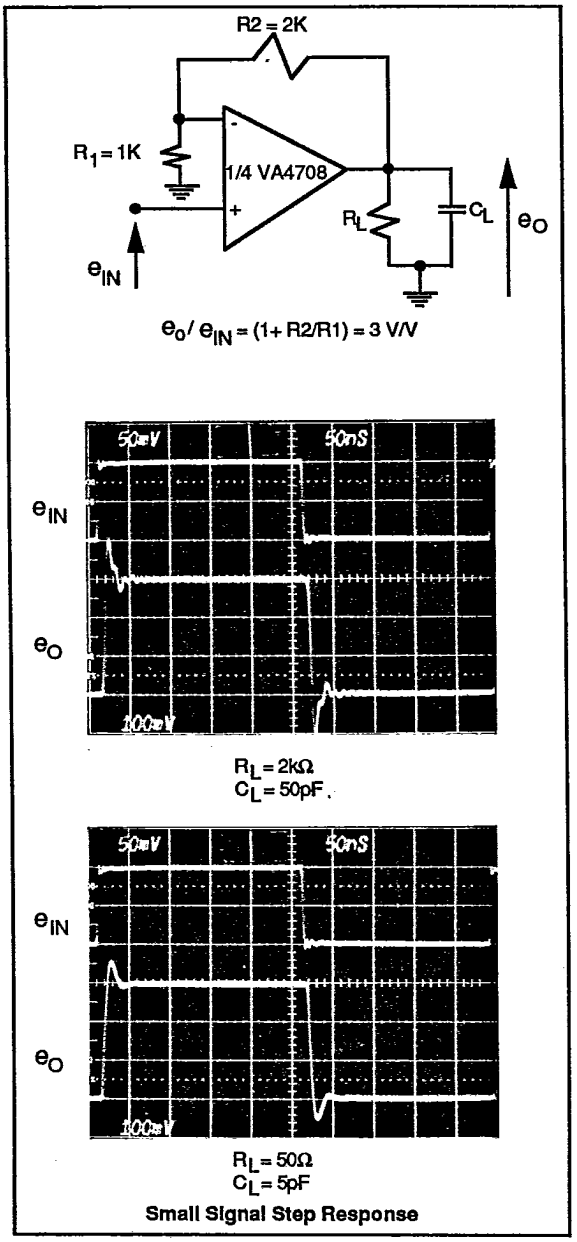
Figure 3: Frequency and Time Domain Response Characteristics, Av=3



Open Loop Frequency Response



Closed Loop Frequency Response



Small Signal Step Response

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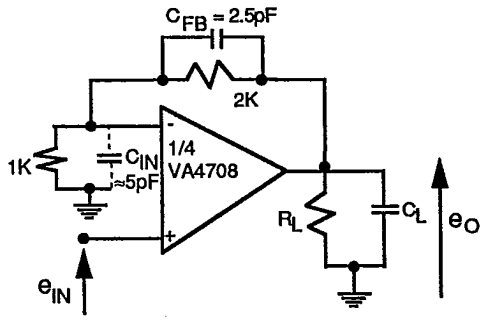
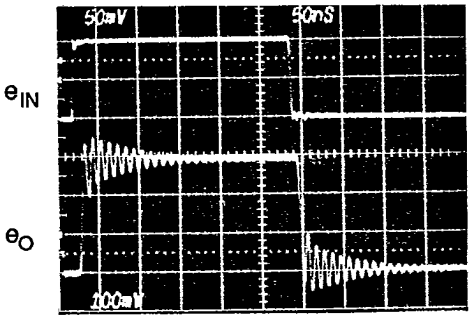
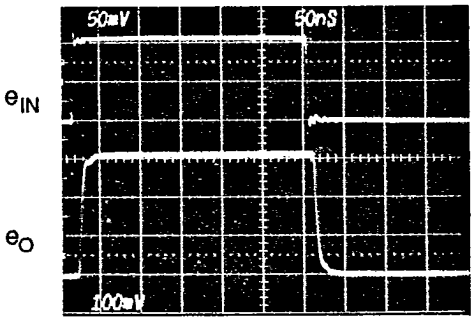
Figure 4: Response Characteristics with Input Pole Cancellation, Av=3



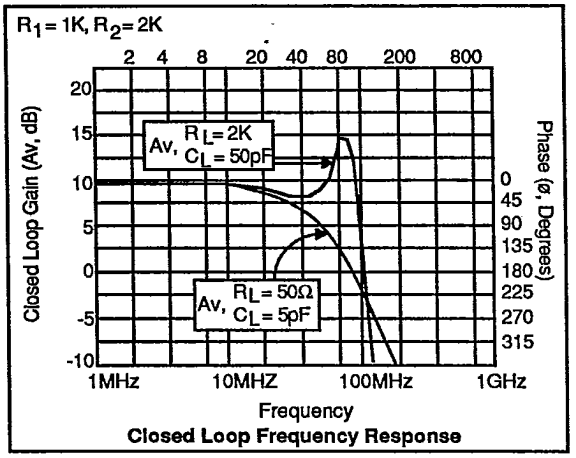


R_L = 2kΩ
C_L = 50pF



R_L = 50Ω
C_L = 5pF

Small Signal Step Response



Closed Loop Frequency Response