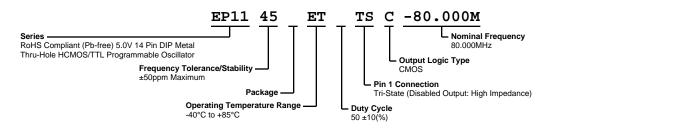


Temperature Cycling

Vibration





Nominal Frequency80.000 Hzirrequency Tolerance/Stability±50ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°Cyging at 25°C±5ppm/year MaximumOperating Temperature Range-40°C to +85°Csupply Voltage5.0Vdc ±10%pupt Current45mA Maximum (Unloaded)Dutput Voltage Logic High (Voh)Vdd-0.4Vdc Minimum (IOH = -16mA)Dutput Voltage Logic Low (Vol)0.4Vdc Maximum (IOL = +16mA)Dutput Logic TypeCMOSDutput Logic TypeCMOSDutput Logic TypeCMOSVin 1 Input Voltage (Vih and Vil)+2.0Vdc Minimum to enable output, +0.8Vdc to disable output, No Connect to enable output.Vin 1 Input Voltage (Vih and Vil)+2.0Vdc Minimum to enable output, +0.8Vdc to disable output, No Connect to enable output.Vin 1 Input Voltage (Vih and Vil)+2.0Vdc Minimum (Pin 1 = Ground)Visable Current30mA Maximum (Pin 1 = Ground)Visable Cur				
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AppendixStoreAppendix45mA Maximum (Unloaded)Output Voltage Logic High (Voh)Vdd-0.4Vdc Minimum (IOH = -16mA)Output Voltage Logic Low (Vol)0.4Vdc Maximum (IOL = +16mA)AnSec Maximum (Measured at 20% to 80% of waveform)Output Cycle50 ±10(%) (Measured at 1.4Vdc with TTL Load; Measured at 50% of waveform with HCMOS Load)Output Logic TypeCMOSVintu Logic TypeCMOSVin 1 Input Voltage (Vih and Vil)+2.0Vdc Minimum to enable output, +0.8Vdc to disable output, No Connect to enable output.Standby Current50µA Maximum (Pin 1 = Ground)Outpate to Peak Jitter (tPK)100pSec Maximum, 50pSec Typical				
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Peak to Peak Jitter (tPK) 100pSec Maximum, 50pSec Typical				
RMS Period Jitter (tRMS) 13pSec Maximum, 8pSec Typical				
Start Up Time 10mSec Maximum				
Storage Temperature Range -55°C to +125°C				
ENVIRONMENTAL & MECHANICAL SPECIFICATIONS				
ine Leak Test MIL-STD-883, Method 1014, Condition A				
Bross Leak Test MIL-STD-883, Method 1014, Condition C				
ead Integrity MIL-STD-883, Method 2004				
MIL-STD-202, Method 213, Condition C				
Resistance to Soldering Heat MIL-STD-202, Method 210				
Resistance to Solvents MIL-STD-202, Method 215				
iolderability MIL-STD-883, Method 2003				

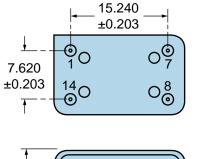
MIL-STD-883, Method 1010

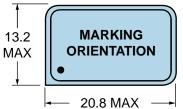
MIL-STD-883, Method 2007, Condition A

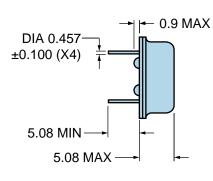
EP1145ETTSC-80.000M



MECHANICAL DIMENSIONS (all dimensions in millimeters)

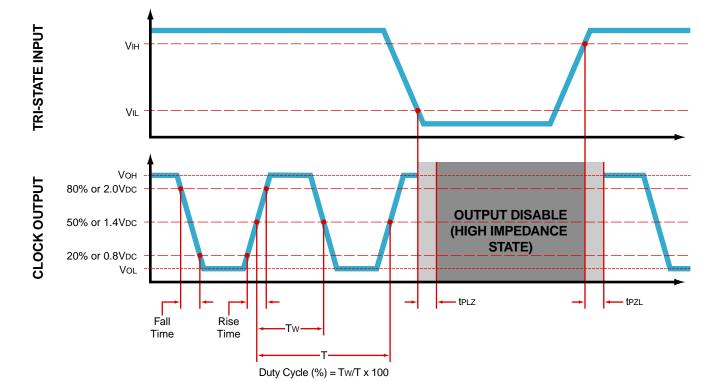






PIN	CONNECTION
1	Tri-State (High Impedance)
7	Ground/Case Ground
8	Output
14	Supply Voltage
LINE	MARKING
1	ECLIPTEK
2	EP11TS EP11=Product Series
3	80.000M
4	XXYZZ XX=Ecliptek Manufacturing Code Y=Last Digit of the Year ZZ=Week of the Year

OUTPUT WAVEFORM & TIMING DIAGRAM



EP1145ETTSC-80.000M



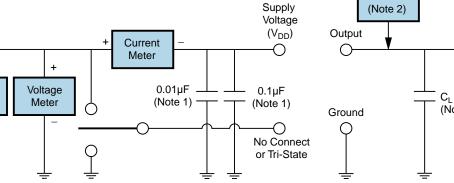
Test Circuit for TTL Output

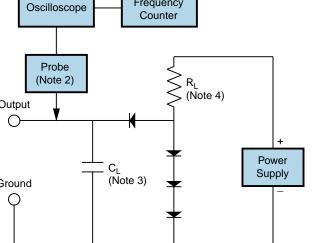
+ Power

Supply

Output Load Drive Capability	R _L Value (Ohms)	C _L Value (pF)
10TTL	390	15
5TTL	780	15
2TTL	1100	6
10LSTTL	2000	15
1TTL	2200	3







Frequency

Note 1: An external 0.1µF low frequency tantalum bypass capacitor in parallel with a 0.01µF high frequency ceramic bypass capacitor close to the package ground and V_{DD} pin is required.

Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.

Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.

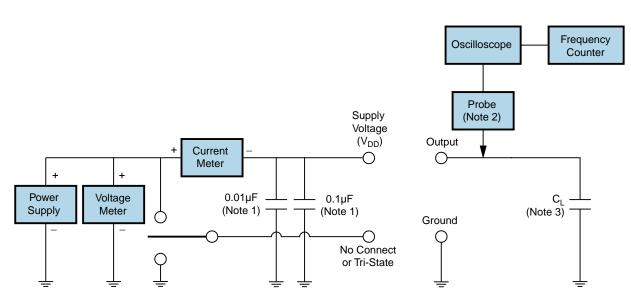
Note 4: Resistance value RL is shown in Table 1. See applicable specification sheet for 'Load Drive Capability'.

Note 5: All diodes are MMBD7000, MMBD914, or equivalent.

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Test Circuit for CMOS Output



Note 1: An external 0.1µF low frequency tantalum bypass capacitor in parallel with a 0.01µF high frequency ceramic bypass capacitor close to the package ground and V_{DD} pin is required.

Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.

Note 3: Capacitance value \dot{C}_L includes sum of all probe and fixture capacitance.



Recommended Solder Reflow Methods

EP1145ETTSC-80.000M



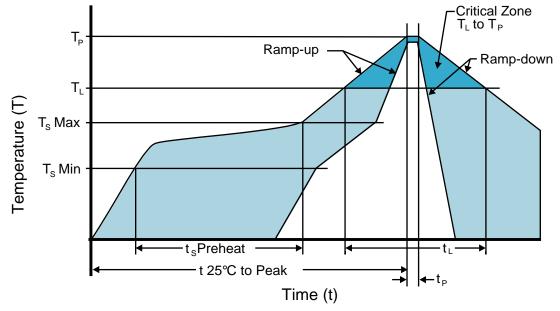
High Temperature Solder Bath (Wave Solder)

T _s MAX to T _L (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum (Ts MIN)	150°C
- Temperature Typical (T _s TYP)	175°C
- Temperature Maximum (T _s MAX)	200°C
- Time (t _s MIN)	60 - 180 Seconds
Ramp-up Rate (T _L to T _P)	3°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	217°C
- Time (t∟)	60 - 150 Seconds
Peak Temperature (T _P)	260°C Maximum for 10 Seconds Maximum
Target Peak Temperature (T _P Target)	250°C +0/-5°C
Time within 5°C of actual peak (t _P)	20 - 40 seconds
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum
Moisture Sensitivity Level	Level 1
Additional Notes	Temperatures shown are applied to back of PCB board and device leads only. Do not use this method for product with the Gull Wing option.



Recommended Solder Reflow Methods

EP1145ETTSC-80.000M



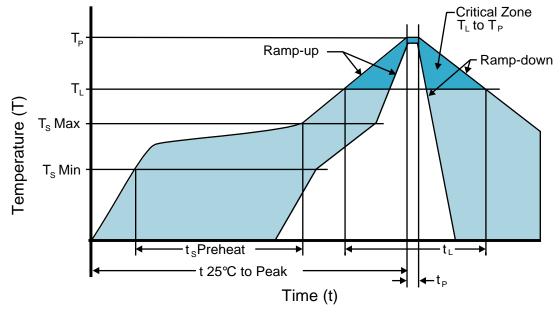
Low Temperature Infrared/Convection 185°C

T _s MAX to T _L (Ramp-up Rate)	5°C/second Maximum
Preheat	
- Temperature Minimum (Ts MIN)	N/A
- Temperature Typical (T _s TYP)	150°C
- Temperature Maximum (T _s MAX)	N/A
- Time (t _s MIN)	60 - 120 Seconds
Ramp-up Rate (T _L to T _P)	5°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	150°C
- Time (t∟)	200 Seconds Maximum
Peak Temperature (T _P)	185°C Maximum
Target Peak Temperature (T _P Target)	185°C Maximum 2 Times
Time within 5°C of actual peak (t _p)	10 seconds Maximum 2 Times
Ramp-down Rate	5°C/second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1
Additional Notes	Temperatures shown are applied to body of device. Use this method only for product with the Gull Wing option.



Recommended Solder Reflow Methods

EP1145ETTSC-80.000M



Low Temperature Solder Bath (Wave Solder)

T _s MAX to T _L (Ramp-up Rate)	5°C/second Maximum
Preheat	
- Temperature Minimum (Ts MIN)	N/A
- Temperature Typical (T _s TYP)	150°C
- Temperature Maximum (T _s MAX)	N/A
- Time (t _s MIN)	30 - 60 Seconds
Ramp-up Rate (T _L to T _P)	5°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	150°C
- Time (t∟)	200 Seconds Maximum
Peak Temperature (T _P)	245°C Maximum
Target Peak Temperature (T _P Target)	245°C Maximum 1 Time / 235°C Maximum 2 Times
Time within 5°C of actual peak (t _P)	5 seconds Maximum 1 Time / 15 seconds Maximum 2 Times
Ramp-down Rate	5°C/second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1
Additional Notes	Temperatures shown are applied to back of PCB board and device leads only. Do not use this method for product with the Gull Wing option.

Low Temperature Manual Soldering

185°C Maximum for 10 seconds Maximum, 2 times Maximum. (Temperatures listed are applied to device leads only. This method can be utilized with both Gull Wing and Non-Gull Wing devices.)

High Temperature Manual Soldering

260°C Maximum for 5 seconds Maximum, 2 times Maximum. (Temperatures listed are applied to device leads only. This method can be utilized with both Gull Wing and Non-Gull Wing devices.)