ASYNCHRONOUS CellularRAM™

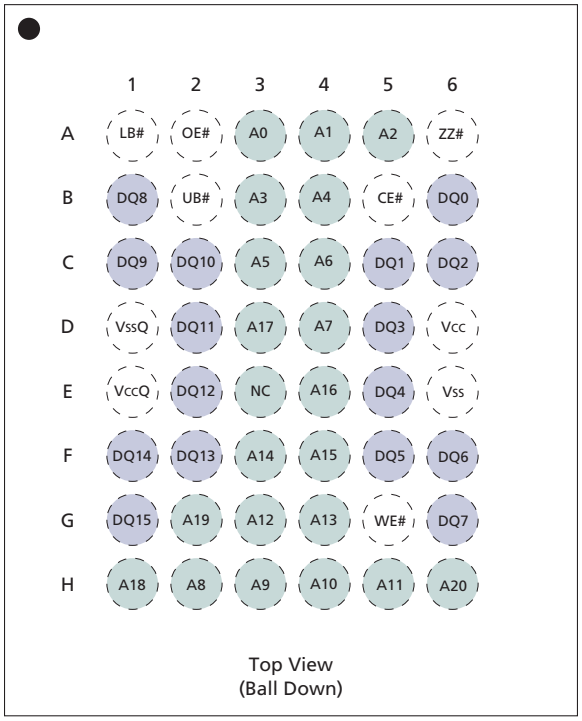
MT45W2MW16PAFA
MT45W1MW16PAFA

Features

- Asynchronous and Page Mode interface
- Random Access Time: 70ns, 85ns
- Page Mode Read Access
  Sixteen-word page size
  Interpage read access: 70ns, 85ns
  Intrapage read access: 20ns, 25ns
- VCC, VCCQ Voltages
  1.70V–1.95V VCC
  1.70V–3.30V VCCQ
- Low Power Consumption
  Asynchronous READ < 20mA
  Intrapage READ < 15mA
  Standby: 110µA (32Mb—standard), 80µA (16Mb)
  90µA (32Mb—low-power option)
  Deep Power-Down < 10µA
- Low-Power Features
  Temperature Compensated Refresh (TCR)
  On-Chip Sensor Control
  Partial Array Refresh (PAR)
  Deep Power-Down (DPD) Mode

Options	Designator
• Configuration	
2 Meg x 16	MT45W2MW16PA
1 Meg x 16	MT45W1MW16PA
Vcc Core Voltage Supply: 1.8V	
VccQ I/O Voltage: 3.0V, 2.5V, 1.8V	
• Package	
48-ball VFBGA	FA
48-ball VFBGA—Lead-free	BA[1]
• Access Time	
60ns	-60[1]
70ns	-70
85ns	-85
• Standby Power	
Standard	None
Low-Power (32Mb)	L

Figure 1: 48-Ball VFBGA



Top View
(Ball Down)

Options (continued)	Designator
• Operating Temperature Range	
Wireless (-30°C to +85°C)	WT[2]
Industrial (-40°C to +85°C)	IT[1]

NOTE:
1. Contact factory.
2. -30°C exceeds the CellularRAM Workgroup 1.0 specification of -25°C.

Part Number Example:

MT45W2MW16PAFA-70LWT

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General Description

Micron® CellularRAM™ products are high-speed, CMOS dynamic random access memories that have been developed for low-power portable applications. The MT45W2MW16PA is a 32Mb device organized as 2 Meg x 16 bits, and the MT45W1MW16PA is a 16Mb device organized as 1 Meg x 16 bits. These devices include the industry-standard, asynchronous memory interface found on other low-power SRAM or Pseudo SRAM offerings.

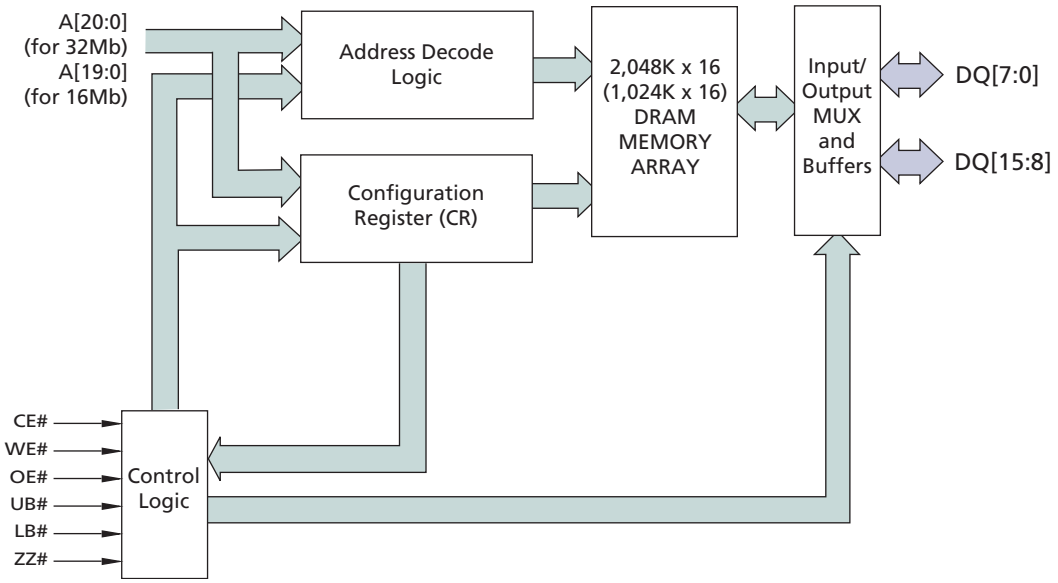
Operating voltages have been reduced in an effort to minimize power consumption. The core voltage has been reduced to a 1.80V operating level. To maintain compatibility with different memory bus interfaces, CellularRAM devices are available with I/O voltages of 3.0V, 2.5V, or 1.8V.

A user-accessible configuration register (CR) defines how the CellularRAM device performs on-chip refresh and whether page mode read accesses are permitted. This register is automatically loaded with a default setting during power-up and can be updated at any time during normal operation.

To operate seamlessly on an asynchronous memory bus, CellularRAM products incorporate a transparent self refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

Special attention has been focused on current consumption during self refresh. CellularRAM products include three system-accessible mechanisms to minimize refresh current. Temperature compensated refresh (TCR) uses an on-chip sensor to adjust the refresh rate to match the device temperature. The refresh rate decreases at lower temperatures to minimize current consumption during standby. TCR can also be set by the system for maximum device temperatures of +85°C, +45°C, and +15°C. Setting sleep enable (ZZ#) to LOW enables one of two low-power modes: partial array refresh (PAR); or deep power-down (DPD). PAR limits refresh to only that part of the DRAM array that contains essential data. DPD halts refresh operation altogether and is used when no vital information is stored in the device. These three refresh mechanisms are accessed through the CR.

Figure 2: Functional Block Diagram 2 Meg x 16 and 1 Meg x 16



NOTE:

Functional block diagrams illustrate simplified device operation. See truth table, ball descriptions, and timing diagrams for detailed information.

Table 1: VFBGA Ball Descriptions

VFBGA BALL ASSIGNMENT	SYMBOL	TYPE	DESCRIPTION
A3, A4, A5, B3, B4, C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4, E4, D3, H1, G2, H6	A[20:0]	Input	Address Inputs: Inputs for the address accessed during READ or WRITE operations. The address lines are also used to define the value to be loaded into the CR. On the 16Mb device, A20 (ball H6) is not internally connected.
A6	ZZ#	Input	Sleep Enable: When ZZ# is LOW, the CR can be loaded or the device can enter one of two low-power modes (DPD or PAR).
B5	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
A2	OE#	Input	Output Enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
G5	WE#	Input	Write Enable: Enables WRITE operations when LOW.
A1	LB#	Input	Lower Byte Enable. DQ[7:0]
B2	UB#	Input	Upper Byte Enable. DQ[15:8]
B6, C5, C6, D5, E5, F5, F6, G6, B1, C1, C2, D2, E2, F2, F1, G1	DQ[15:0]	Input/ Output	Data Inputs/Outputs.
E3	NC	—	Not internally connected.
D6	V_{CC}	Supply	Device Power Supply: (1.70V–1.95V) Power supply for device core operation.
E1	V_{CCQ}	Supply	I/O Power Supply: (1.70V–3.30V) Power supply for input/output buffers.
E6	V_{SS}	Supply	V_{SS} must be connected to ground.
D1	V_{SSQ}	Supply	V_{SSQ} must be connected to ground.

Table 2: Bus Operations

MODE	POWER	CE#	WE#	OE#	LB#/UB#	ZZ#	DQ[15:0][1]	NOTES
Standby	Standby	H	X	X	X	H	High-Z	2, 5
Read	Active	L	H	L	L	H	Data-Out	1, 4
Write	Active	L	L	X	L	H	Data-In	1, 3, 4
No Operation	Idle	L	X	X	X	H	X	4, 5
PAR	Partial Array Refresh	H	X	X	X	L	High-Z	6
DPD	Deep Power-Down	H	X	X	X	L	High-Z	6
Load Configuration Register	Active	L	L	X	X	L	High-Z	

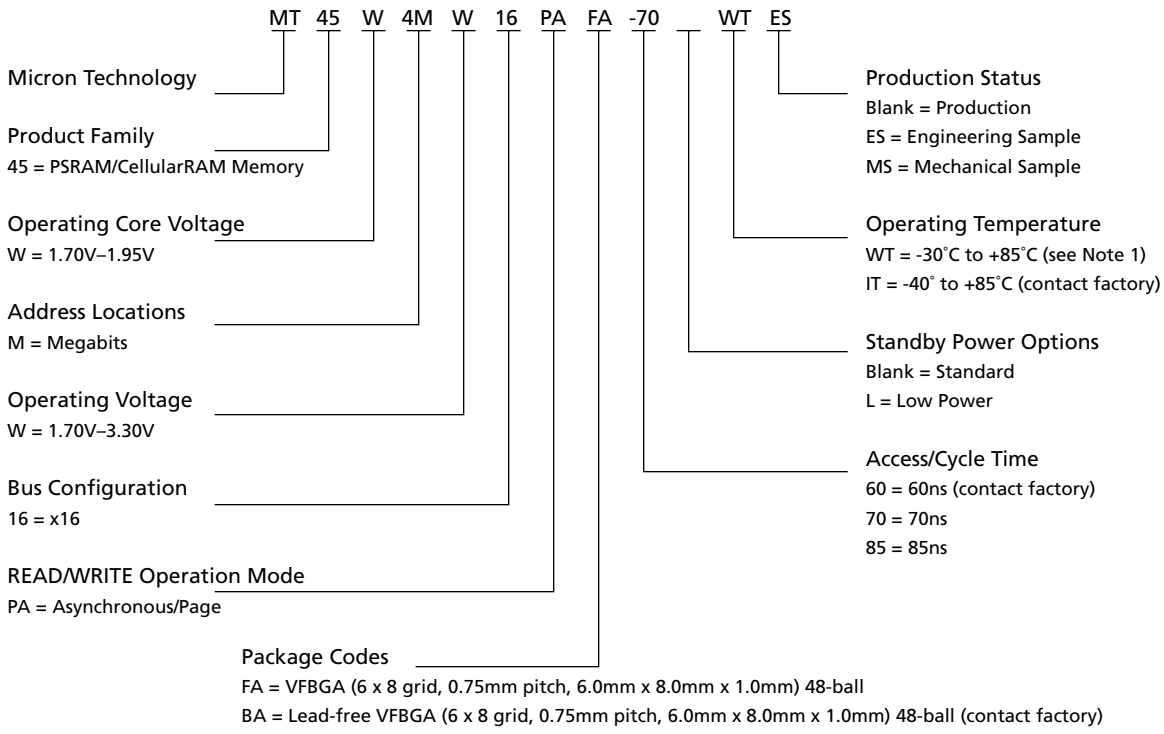
NOTE:

1. When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When LB# only is in select mode, only DQ[7:0] are affected. When UB# only is in the select mode, DQ[15:8] are affected.
2. When the device is in standby mode, control inputs (WE#, OE#), address inputs, and data inputs/outputs are internally isolated from any external influence.
3. When WE# is invoked, the OE# input is internally disabled and has no effect on the I/Os.
4. The device will consume active power in this mode whenever addresses are changed.
5. V_{IN} = V_{CCQ} or 0V; all device balls must be static (unswitched) in order to achieve minimum standby current.
6. DPD is enabled when configuration register bit CR[4] is “0”; otherwise, PAR is enabled.

Part-Numbering Information

Micron CellularRAM devices are available in several different configurations and densities (see Figure 3).

Figure 3: Part Number Chart



NOTE:

1. -30°C exceeds the CellularRAM Workgroup 1.0 specification of -25°C.

Valid Part Number Combinations

After building the part number from the part numbering chart, please go to the Micron Part Marking Decoder Web site at http://www.micron.com/partsearch to verify that the part number is offered and valid. If the device required is not on this list, please contact the factory.

Device Marking

Due to the size of the package, the Micron standard part number is not printed on the top of the device. Instead, an abbreviated device mark comprised of a five-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at http://www.micron.com/partsearch. To view the location of the abbreviated mark on the device, please refer to customer service note, CSN-11, "Product Mark/Label," at http://www.micron.com/csn.

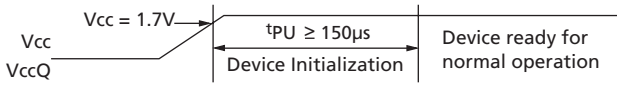
Functional Description

In general, the MT45W2MW16PA device and the MT45W1MW16PA device are high-density alternatives to SRAM and Pseudo SRAM products, popular in low-power, portable applications. The MT45W2MW16PA contains 33,554,432 bits organized as 2,097,152 addresses by 16 bits. The MT45W1MW16PA contains 16,777,216 bits organized as 1,048,576 addresses by 16 bits. These devices include the industry-standard, asynchronous memory interface found on other low-power SRAM or Pseudo SRAM offerings. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous read protocol.

Power-Up Initialization

CellularRAM products include an on-chip voltage sensor that is used to launch the power-up initialization process. Initialization will load the CR with its default setting. VCC and VCCQ must be applied simultaneously, and when they reach a stable level above 1.70V, the device will require 150µs to complete its self-initialization process (see Figure 4). During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

Figure 4: Power-Up Initialization Timing



Bus Operating Modes

The MT45W2MW16PA and the MT45W1MW16PA CellularRAM products incorporate the industry-standard, asynchronous interface found on other low-power SRAM or Pseudo SRAM offerings. This bus interface supports asynchronous READ and WRITE operations as well as the bandwidth-enhancing page mode READ operation. The specific interface that is supported is defined by the value loaded into the CR.

Asynchronous Mode

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry-standard SRAM control interface (CE#, OE#, WE#, LB#/UB#). READ operations (Figure 5) are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH. Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations (Figure 6) occur when CE#, WE#, and LB#/UB# are driven LOW. During WRITE operations, the level of OE# is a "Don't Care"; WE# will override OE#. The data to be written will be latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first). WE# LOW time must be limited to tCEM.

Figure 5: READ Operation

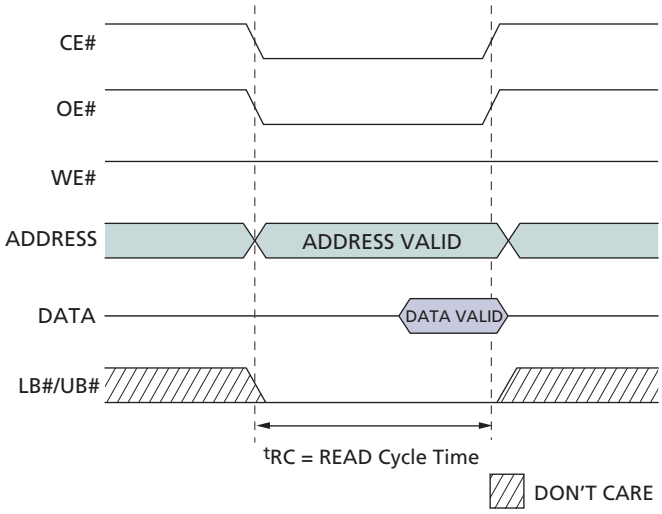
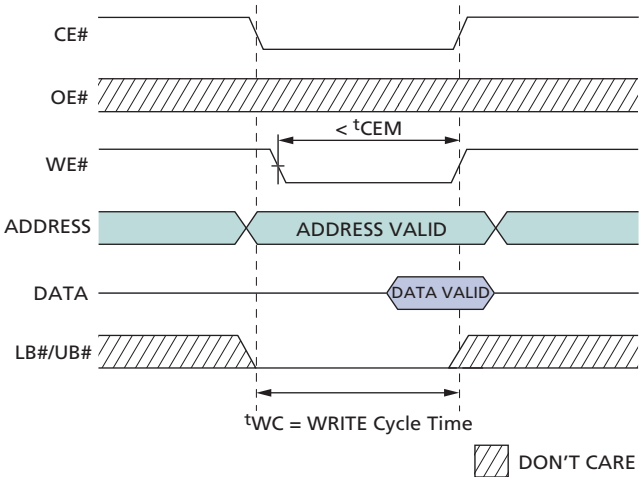


Figure 6: WRITE Operation



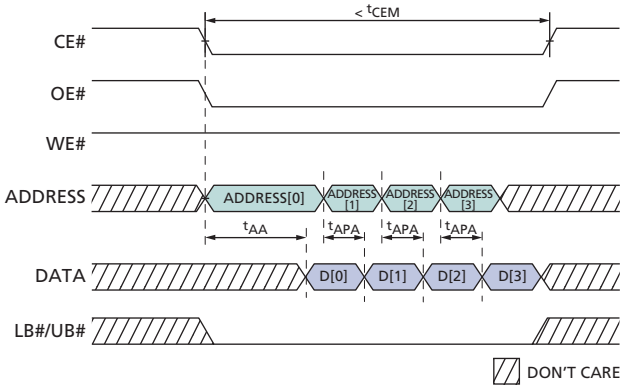
Page Mode READ Operation

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous read access is performed, then adjacent addresses can be quickly read by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Any change in addresses A[4] or higher will initiate a new ^{t}AA access. Figure 7 shows the timing diagram for a page mode access.

Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality.

The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than ^{t}CEM.

Figure 7: Page READ Operation



LB#/UB# Operation

The lower byte (LB#) enable and upper byte (UB#) enable signals allow for byte-wide data transfers. During READ operations, enabled bytes are driven onto the DQs. The DQs associated with a disabled byte are put into a High-Z state during a READ operation. During WRITE operations, any disabled bytes will not be transferred to the memory array and the internal value will remain unchanged. During a WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first.

When both the LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, the device remains in an active mode as long as CE# remains LOW.

Low Power Operation

Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation on the full array. Standby operation occurs when CE# and ZZ# are HIGH.

The device will enter a reduced power state during READ and WRITE operations where the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

Temperature Compensated Refresh

Temperature compensated refresh (TCR) allows for adequate refresh at different temperatures. This CellularRAM device includes an on-chip temperature sensor. When the sensor is enabled, it continually adjusts the refresh rate according to the operating temperature. The on-chip sensor is enabled by default.

Three fixed refresh rates are also available, corresponding to temperature thresholds of +15°C, +45°C, and +85°C. The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. If the case temperature is +35°C, the system can minimize self refresh current consumption by selecting the +45°C setting. The +15°C setting would result in inadequate refreshing and cause data corruption.

Partial Array Refresh

Partial array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the system to reduce refresh current by only refreshing that part of the memory array that is absolutely necessary. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. Data stored in addresses not receiving refresh will become corrupted. The mapping of these partitions can start at either the beginning or the end of the address map (Tables 3 and 4 on page 14). READ and WRITE operations are ignored during PAR operation.

The device only enters PAR mode if the SLEEP bit in the CR has been set HIGH (CR[4] = 1). PAR can be initiated by bring the ZZ# ball to the LOW state for longer than 10µs. Returning ZZ# to HIGH will cause an exit from PAR and the entire array will be immediately available for READ and WRITE operations.

Alternatively, PAR can be initiated using the CR software access sequence (see Software Access to the Configuration Register on page 11). PAR is enabled immediately upon setting CR[4] to "1" using this method. However, using software access to write to the CR alters the function of ZZ# so that ZZ# LOW no longer initiates PAR, although ZZ# continues to enable WRITEs to the CR. This functional change persists until the next time the device is powered up. (See Figure 8.)

Deep Power-Down Operation

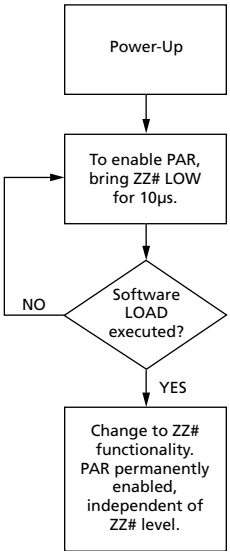
Deep power-down (DPD) operation disables all refresh-related activity. This mode is used when the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is entered. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume. READ and WRITE operations are ignored during DPD operation.

The device can only enter DPD if the SLEEP bit in the CR has been set LOW (CR[4] = 0). DPD is initiated by bringing ZZ# to the LOW state for longer than 10µs. Returning ZZ# to HIGH will cause the device to exit DPD and begin a 150µs initialization process. During this 150µs period, the current consumption will be higher than the specified standby levels but considerably lower than the active current specification.

Driving ZZ# LOW will place the device in the PAR mode if the SLEEP bit in the CR has been set HIGH (CR[4] = 1).

The device should not be put into DPD using CR software access.

Figure 8: Software Access PAR Functionality



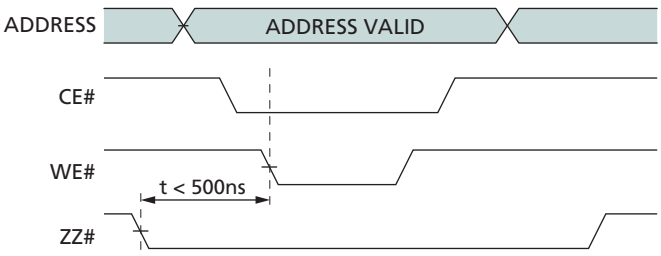
Configuration Register Operation

The configuration register (CR) defines how the CellularRAM device performs its transparent self refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Page mode control is also embedded into the CR. This register can be updated anytime while the device is operating in a standby state. Figure 12 on page 14 describes the control bits used in the CR. At power up, the CR is set to 0010h.

Access Using ZZ#

The CR can be loaded using a WRITE operation immediately after ZZ# makes a HIGH-to-LOW transition (Figure 9). The values placed on addresses A[20:0] are latched into the CR on the rising edge of CE# or WE#, whichever occurs first. LB#/UB# are "Don't Care." Access using ZZ# is WRITE only.

Figure 9: Load Configuration Register Operation



Software Access to the Configuration Register

The contents of the CR can either be read or modified using a software sequence. The nature of this access mechanism may eliminate the need for the ZZ# ball.

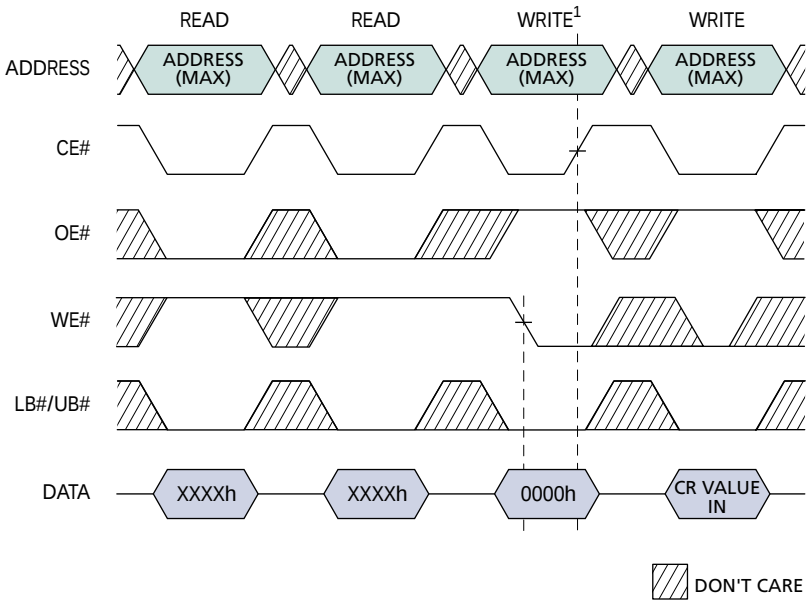
If the software mechanism is used, ZZ# can simply be tied to VCCQ. The port line typically used for ZZ# control purposes will no longer be required. However, ZZ# should not be tied to VCCQ if the system will use DPD; DPD cannot be enabled or disabled using the software access sequence.

The CR is loaded using a four-step sequence consisting of two READ operations followed by two WRITE operations (see Figure 10). The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure 11). Note that a third READ cycle of the highest address will cancel the access sequence until a different address is read.

The address used during all READ and WRITE operations is the highest address of the CellularRAM device being accessed (1FFFFFh for 32Mb and FFFFFh for 16Mb); the content of this address is changed by using this sequence (note that this is a deviation from the CellularRAM specification). The data bus is used to transfer data into or out of bits 15–0 of the CR.

Writing to the CR using the software sequence modifies the function of the ZZ# ball. Once the software sequence loads the CR, the level of the ZZ# ball no longer enables PAR operation. PAR operation will be updated whenever the software sequence loads a new value into the CR. This ZZ# functionality will continue until the next time the device is powered-up. The operation of the ZZ# ball is not affected if the software sequence is only used to read the contents of the CR. The use of the software sequence does not affect the ability to perform the standard (ZZ# controlled) method of loading the CR.

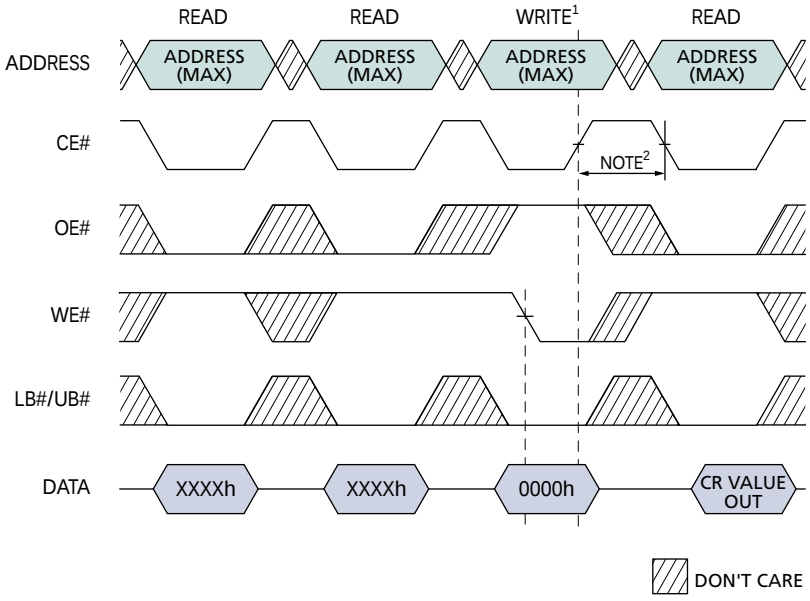
Figure 10: Software Access Load Configuration Register



NOTE:

1. The WRITE on the third cycle must be CE# controlled.

Figure 11: Software Access Read Configuration Register



NOTE:

1. The WRITE on the third cycle must be CE# controlled.
2. CE# must be HIGH for 150ns before performing the cycle that reads the configuration register.

Partial Array Refresh (CR[2:0])
Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the system to reduce current by only refreshing that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Tables Table 3 and Table 4 on page 14).

Sleep Mode (CR[4])
Default = PAR Enabled, DPD Disabled

The sleep mode bit determines which low-power mode is to be entered when ZZ# is driven LOW. If CR[4] = 1, PAR operation is enabled. If CR[4] = 0, DPD operation is enabled. PAR can also be enabled directly by writing to the CR using the software access sequence. Note that this then disables ZZ# initiation of PAR. DPD cannot be enabled or disabled using the software access sequence; this should only be done using ZZ# to access the CR.

DPD operation disables all refresh-related activity. This mode will be used when the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operation can resume. DPD should not be enabled using CR software access.

Temperature Compensated Refresh (CR[6:5])
Default = On-Chip Temperature Sensor

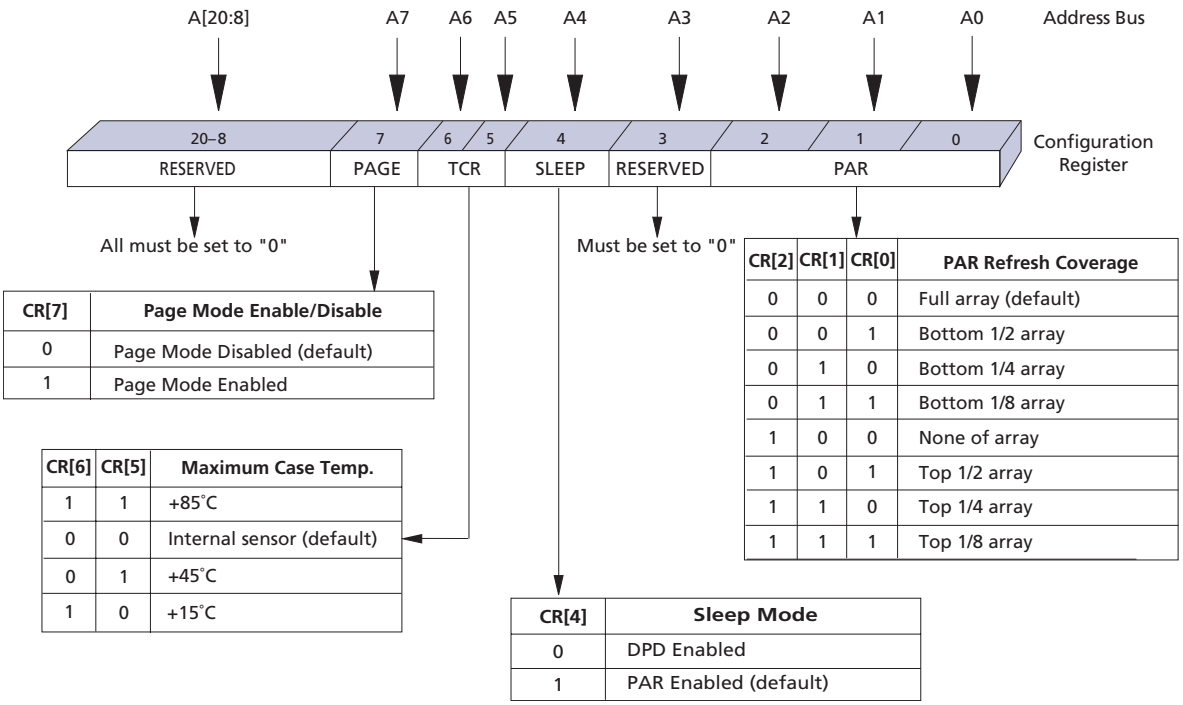
This CellularRAM device includes an on-chip temperature sensor that automatically adjusts the refresh rate according to the operating temperature. The on-chip TCR is enabled by clearing both of the TCR bits in the refresh configuration register (CR[6:5] = 00b). Any other TCR setting enables a fixed refresh rate. When the on-chip temperature sensor is enabled, the device continually adjusts the refresh rate according to the operating temperature.

The TCR bits also allow for adequate fixed-rate refresh at three different temperature thresholds (+15°C, +45°C, and +85°C). The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. If the case temperature is +35°C, the system can minimize self refresh current consumption by selecting the +45°C setting. The +15°C setting would result in inadequate refreshing and cause data corruption.

Page Mode READ Operation (CR[7])
Default = Disabled

The page mode operation bit determines whether page mode READ operations are enabled. In the power-up default state, page mode is disabled.

Figure 12: Configuration Register Bit Mapping



CR[7]	Page Mode Enable/Disable
0	Page Mode Disabled (default)
1	Page Mode Enabled

CR[6]	CR[5]	Maximum Case Temp.
1	1	+85°C
0	0	Internal sensor (default)
0	1	+45°C
1	0	+15°C

CR[4]	Sleep Mode
0	DPD Enabled
1	PAR Enabled (default)

CR[2]	CR[1]	CR[0]	PAR Refresh Coverage
0	0	0	Full array (default)
0	0	1	Bottom 1/2 array
0	1	0	Bottom 1/4 array
0	1	1	Bottom 1/8 array
1	0	0	None of array
1	0	1	Top 1/2 array
1	1	0	Top 1/4 array
1	1	1	Top 1/8 array

Table 3: 32Mb Address Patterns for PAR (CR[4] = 1)

CR[2]	CR[1]	CR[0]	ACTIVE SECTION	ADDRESS SPACE	SIZE	DENSITY
0	0	0	Full die	000000h–1FFFFFh	2 Meg x 16	32Mb
0	0	1	One-half of die	000000h–0FFFFFh	1 Meg x 16	16Mb
0	1	0	One-quarter of die	000000h–07FFFFh	512K x 16	8Mb
0	1	1	One-eighth of die	000000h–03FFFFh	256K x 16	4Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	100000h–1FFFFFh	1 Meg x 16	16Mb
1	1	0	One-quarter of die	180000h–1FFFFFh	512K x 16	8Mb
1	1	1	One-eighth of die	1C0000h–1FFFFFh	256K x 16	4Mb

Table 4: 16Mb Address Patterns for PAR (CR[4] = 1)

CR[2]	CR[1]	CR[0]	ACTIVE SECTION	ADDRESS SPACE	SIZE	DENSITY
0	0	0	Full die	00000h–FFFFFh	1 Meg x 16	16Mb
0	0	1	One-half of die	00000h–7FFFFh	512K x 16	8Mb
0	1	0	One-quarter of die	00000h–3FFFFh	256K x 16	4Mb
0	1	1	One-eighth of die	00000h–1FFFFh	128K x 16	2Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	80000h–FFFFFh	512K x 16	8Mb
1	1	0	One-quarter of die	C0000h–FFFFFh	256K x 16	4Mb
1	1	1	One-eighth of die	E0000h–FFFFFh	128K x 16	2Mb

Absolute Maximum Ratings

Voltage to Any Ball Except V_{CC}, V_{CCQ}
Relative to V_{SS} . . . . . .
-0.50V to (4.0V or VccQ + 0.3V, whichever is less)
Voltage on V_{CC} Supply Relative to V_{SS}. . -0.20V to 2.45V
Voltage on V_{CCQ} Supply Relative to V_{SS} . -0.20V to 4.0V
Storage Temperature . . . . . -55°C to 150°C
Operating Temperature (Case)
Wireless (see Note 1) . . . . . -30°C to 85°C
Industrial . . . . . -40°C to 85°C
Soldering Temperature and Time
10s (solder ball only) . . . . . 260°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

NOTE:

1. -30°C exceeds the CellularRAM Workgroup 1.0 specification of -25°C.

Table 5: Electrical Characteristics and Operating Conditions

Wireless Temperature[1] (-30°C ≤ T_C ≤ +85 °C), Industrial Temperature (-40°C < T_C < +85°C)

DESCRIPTION	CONDITIONS	SYMBOL		MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}		1.70	1.95	V	
I/O Supply Voltage		V_{CCQ}		1.70	3.30	V	
Input High Voltage		V_{IH}		1.4	V_{CCQ} + 0.2	V	2, 3
Input Low Voltage		V_{IL}		-0.2	+0.4	V	4
Output High Voltage	I_{OH} = -0.2mA	V_{OH}		0.80 V_{CCQ}		V	
Output Low Voltage	I_{OL} = 0.2mA	V_{OL}			0.20 V_{CCQ}	V	
Input Leakage Current	V_{IN} = 0 to V_{CCQ}	I_{LI}			1	µA	
Output Leakage Current	OE# = V_{IH} or Chip Disabled	I_{LO}			1	µA	
Operating Current							
Asynchronous Random READ/WRITE	V_{IN} = V_{CCQ} or 0V Chip Enabled, I_{OUT} = 0	I_{CC1}	-70		20	mA	5
			-85		17		
Asynchronous Page READ		I_{CC1P}	-70		15	mA	5
			-85		12		
Standby Current	V_{IN} = V_{CCQ} or 0V CE# = V_{CCQ}	I_{SB}	32Mb—Std		110	µA	6
			32Mb—L		90		
			16Mb		80		

NOTE:

1. -30°C exceeds the CellularRAM Workgroup 1.0 specification of -25°C.
2. Input signals may overshoot to VccQ + 1.0V for periods less than 2ns during transitions.
3. V_{IH} (MIN) value is not aligned with CellularRAM Workgroup 1.0 specification of V_{CCQ} - 0.4V.
4. Input signals may undershoot to Vss - 1.0V for periods less than 2ns during transitions
5. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.
6. I_{SB} (MAX) values measured with PAR set to FULL ARRAY and TCR set to +85°C. In order to achieve low standby current, all inputs must be driven to V_{CCQ} or V_{SS}. I_{SB} might be slightly higher for up to 500ms after power-up, or after changes to the PAR array partition.

Table 6: Temperature Compensated Refresh Specifications and Conditions

DESCRIPTION	CONDITIONS	SYMBOL	POWER	TCR SETTING (CR[6:5])	MAX	UNITS
Temperature Compensated Refresh Standby Current	V_{IN} = V_{CCQ} or 0V, CE# = V_{CCQ}	I_{TCR}	32Mb Standard (no desig.)	+85°C	110	µA
				+45°C	80	µA
				+15°C	70	µA
			32Mb Low-power option (L)	+85°C	90	µA
				+45°C	60	µA
				+15°C	55	µA
			16Mb	+85°C	80	µA
				+45°C	50	µA
				+15°C	40	µA

NOTE:
I_{TCR} (MAX) values measured with FULL ARRAY refresh. MAX values apply across the full temperature range.

Table 7: Partial Array Refresh Specifications and Conditions

DESCRIPTION	CONDITIONS	SYMBOL	POWER	ARRAY PARTITION	MAX	UNITS
Partial Array Refresh Current	V_{IN} = V_{CCQ} or 0V ZZ# = 0V CR[4] = 1	I_{PAR}	32Mb Standard (no desig.)	Full	110	µA
				1/2	105	µA
				1/4	95	µA
				1/8	95	µA
				0	70	µA
			32Mb Low-power option (L)	Full	90	µA
				1/2	85	µA
				1/4	75	µA
				1/8	75	µA
				0	65	µA
			16Mb	Full	80	µA
				1/2	70	µA
				1/4	70	µA
				1/8	70	µA
				0	65	µA

NOTE:
I_{PAR} (MAX) values measured with TCR set to 85°C. I_{PAR} might be slightly higher for up to 500ms after changes to the PAR array partition.

Table 8: Deep Power-Down Specifications and Conditions

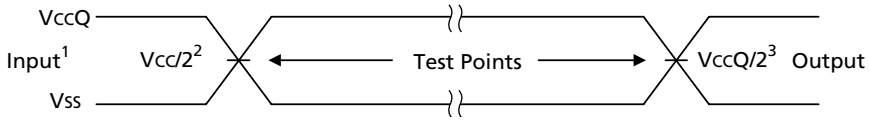
DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS
Deep Power-Down	V_{IN} = V_{CCQ} or 0V; +25°C ZZ# = 0V CR[4] = 0	I_{ZZ}	10	µA

Table 9: Capacitance Specifications and Conditions

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_C = +25°C; f = 1 MHz;	C_{IN}	2.0	6.5	pF	1
Input/Output Capacitance (DQ)	V_{IN} = 0V	C_{IO}	3.0	6.5	pF	1

NOTE:
1. These parameters are verified in device characterization and are not 100% tested.

Figure 13: AC Input/Output Reference Waveform



NOTE:
1. AC test inputs are driven at VccQ for a logic 1 and Vss for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.
2. Input timing begins at Vcc/2. Due to the possibility of a difference between Vcc and VccQ, the input test point may not be shown to scale.
3. Output timing ends at VccQ/2.

Figure 14: Output Load Circuit

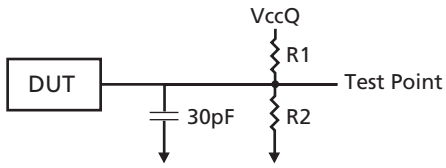


Table 10: Output Load Circuit

VccQ	R1/R2
1.8V	2.7KΩ
2.5V	3.7KΩ
3.0V	4.5KΩ

Table 11: READ Cycle Timing Requirements

PARAMETER	SYMBOL	-70		-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Address Access Time	^{t}AA		70		85	ns	
Page Access Time	^{t}APA		20		25	ns	
LB#/UB# Access Time	^{t}BA		70		85	ns	
LB#/UB# Disable to High-Z Output	^{t}BHZ		8		8	ns	2
LB#/UB# Enable to Low-Z Output	^{t}BLZ	10		10		ns	1
Maximum CE# Pulse Width	^{t}CEM		8		8	µs	3
Chip Select Access Time	^{t}CO		70		85	ns	
Chip Disable to High-Z Output	^{t}HZ		8		8	ns	2
Chip Enable to Low-Z Output	^{t}LZ	10		10		ns	1
Output Enable to Valid Output	^{t}OE		20		20	ns	
Output Hold from Address Change	^{t}OH	5		5		ns	
Output Disable to High-Z Output	^{t}OHZ		8		8	ns	2
Output Enable to Low-Z Output	^{t}OLZ	5		5		ns	1
Page Cycle Time	^{t}PC	20		25		ns	
Read Cycle Time	^{t}RC	70		85		ns	

Table 12: WRITE Cycle Timing Requirements

PARAMETER	SYMBOL	-70		-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Address Setup Time	^{t}AS	0		0		ns	
Address Valid to End of Write	^{t}AW	70		85		ns	
Byte Select to End of Write	^{t}BW	70		85		ns	
CE# HIGH Time During Write	^{t}CPH	5		5		ns	
Chip Enable to End of Write	^{t}CW	70		85		ns	
Data Hold from Write Time	^{t}DH	0		0		ns	
Data Write Setup Time	^{t}DW	23		25		ns	
Chip Enable to Low-Z Output	^{t}LZ	10		10		ns	1
End Write to Low-Z Output	^{t}OW	5		5		ns	1
Write Cycle Time	^{t}WC	70		85		ns	
Write to High-Z Output	^{t}WHZ		8		8	ns	2
Write Pulse Width	^{t}WP	46		50		ns	4
Write Pulse Width HIGH	^{t}WPH	10		10		ns	
Write Recovery Time	^{t}WR	0		0		ns	

NOTE:

1. High-Z to Low-Z timings are tested with the circuit shown in Figure 14 on page 17. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.
2. Low-Z to High-Z timings are tested with the circuit shown in Figure 14 on page 17. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.
3. Page mode enabled only.
4. WE# LOW time must be limited to ^{t}CEM (8µs).

Table 13: Load Configuration Register Timing Requirements

DESCRIPTION	SYMBOL	-70		-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Address Setup Time	^{t}AS	0		0		ns	
Address Valid to End of Write	^{t}AW	70		85		ns	
Chip Deselect to ZZ# LOW	$^{t}CDZZ$	5		5		ns	
Chip Enable to End of Write	^{t}CW	70		85		ns	
Write Cycle Time	^{t}WC	70		85		ns	
Write Pulse Width	^{t}WP	40		40		ns	
Write Recovery Time	^{t}WR	0		0		ns	
ZZ# LOW to WE# LOW	$^{t}ZZWE$	10	500	10	500	ns	

Table 14: Deep Power-Down Timing Requirements

DESCRIPTION	SYMBOL	-70		-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Chip Deselect to ZZ# LOW	$^{t}CDZZ$	5		5		ns	
Deep Power-Down Recovery	^{t}R	150		150		µs	
Minimum ZZ# Pulse Width	$^{t}ZZMIN$	10		10		µs	

Timing Diagrams

Figure 15: Power-Up Initialization Period

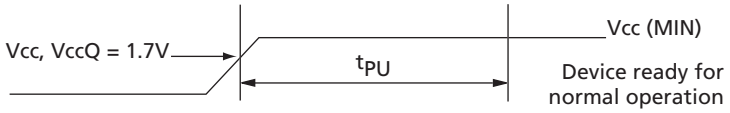


Table 15: Power-Up Initialization Timing Requirements

PARAMETER	SYMBOL	-70		-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Power-Up Initialization Period	^{t}PU	150		150		µs	

Figure 16: Load Configuration Register

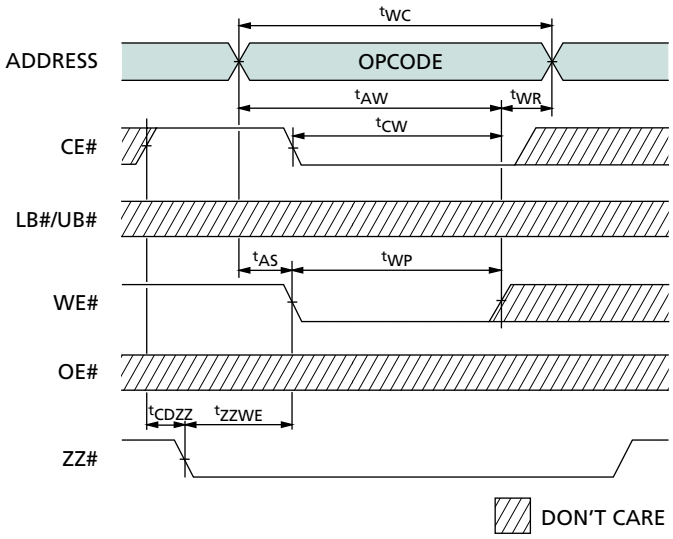


Table 16: Load Configuration Register Timing Requirements

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
^{t}AS	0		0		ns
^{t}AW	70		85		ns
$^{t}CDZZ$	5		5		ns
^{t}CW	70		85		ns

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
^{t}WC	70		85		ns
^{t}WP	40		40		ns
^{t}WR	0		0		ns
$^{t}ZZWE$	10	500	10	500	ns

Figure 17: Deep Power-Down—Entry/Exit

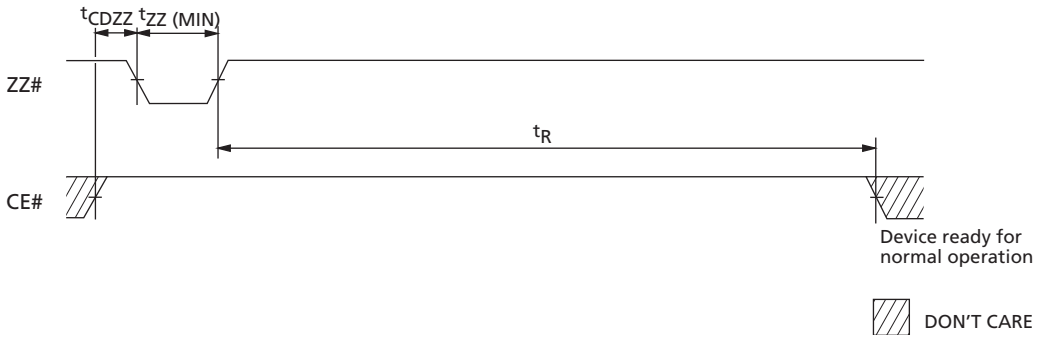


Table 17: Deep Power-Down Timing Parameters

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
^{t}CDZZ	5		5		ns
^{t}R	150		150		µs
^{t}ZZ (MIN)	10		10		µs

Figure 18: Single READ Operation (WE# = VIH)

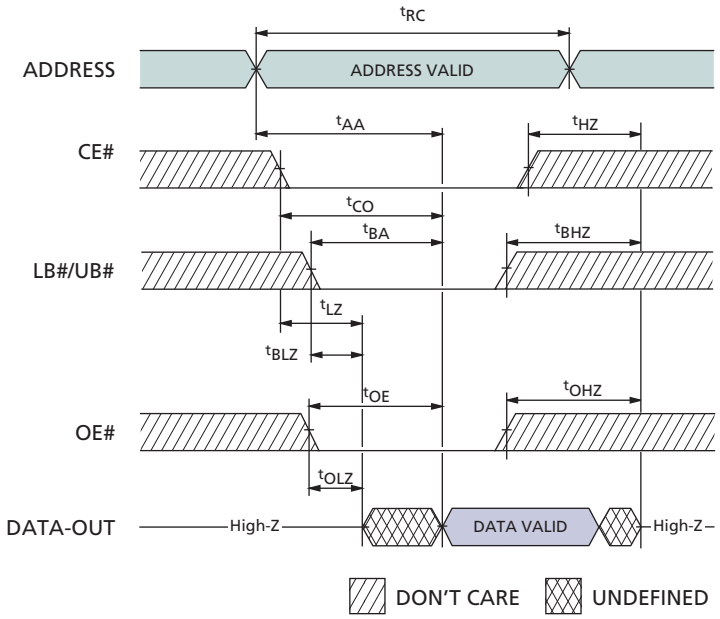


Table 18: READ Timing Parameters

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
tAA		70		85	ns
tBA		70		85	ns
tBHZ		8		8	ns
tBLZ	10		10		ns
tCO		70		85	ns
tHZ		8		8	ns

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
tLZ	10		10		ns
tOE		20		20	ns
tOHZ		8		8	ns
tOLZ	5		5		ns
tRC	70		85		ns

Figure 19: Page Mode READ Operation (WE# = VIH)

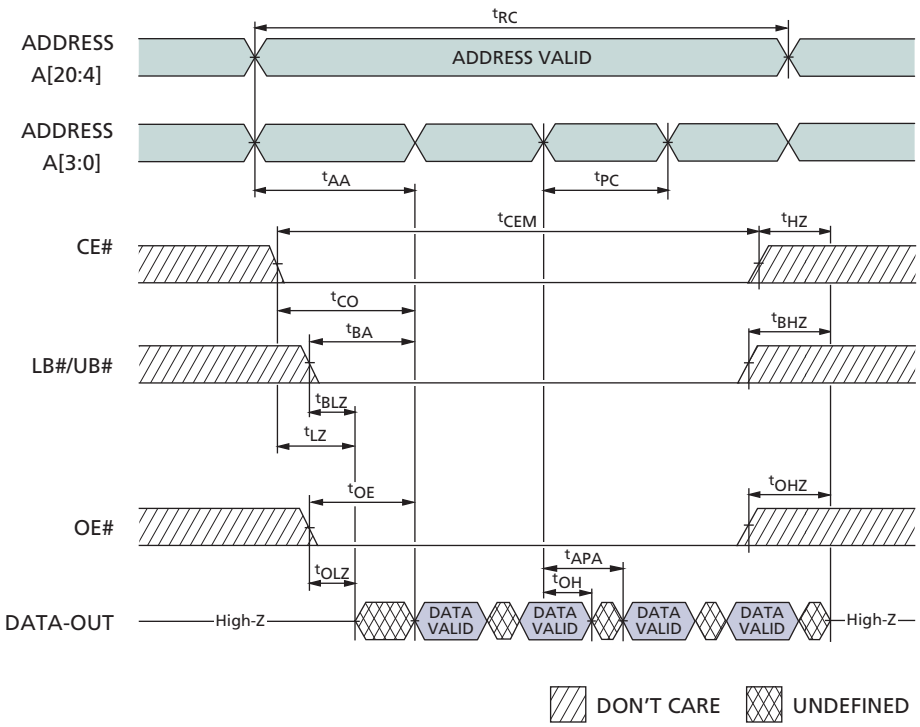


Table 19: Page Mode READ Timing Parameters

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
tAA		70		85	ns
tAPA		20		25	ns
tBA		70		85	ns
tBHZ		8		8	ns
tBLZ	10		10		ns
tCEM		8		8	µs
tCO		70		85	ns
tHZ		8		8	ns

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
tLZ	10		10		ns
tOE		20		20	ns
tOH	5		5		ns
tOHZ		8		8	ns
tOLZ	5		5		ns
tPC	20		25		ns
tRC	70		85		ns

Figure 20: WRITE Cycle (WE# Control)

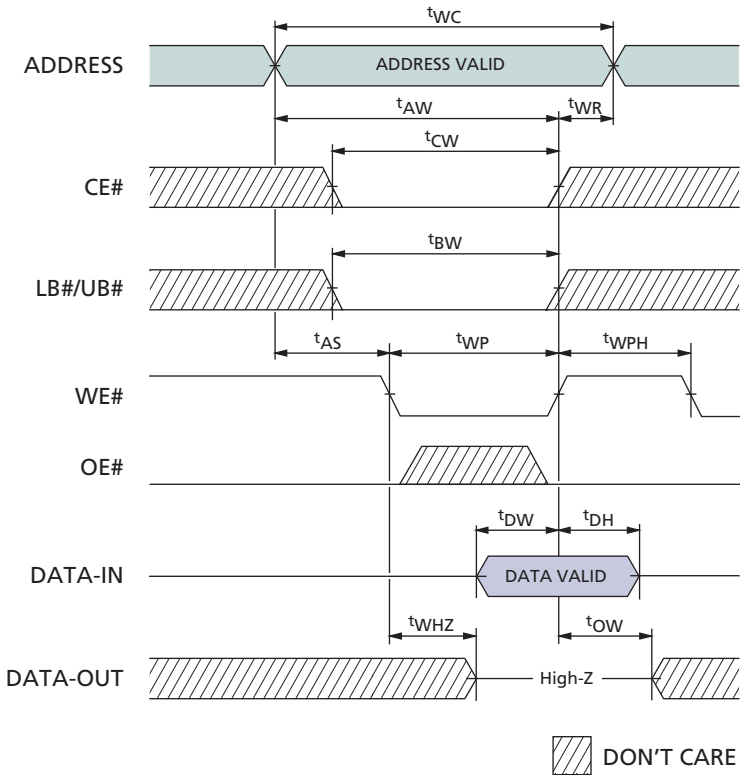


Table 20: WRITE Timing Parameters

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
t_{AS}	0		0		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns
t_{DW}	23		25		ns

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
t_{OW}	5		5		ns
t_{WC}	70		85		ns
t_{WHZ}		8		8	ns
t_{WP}	46		50		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns

Figure 21: WRITE Cycle (CE# Control)

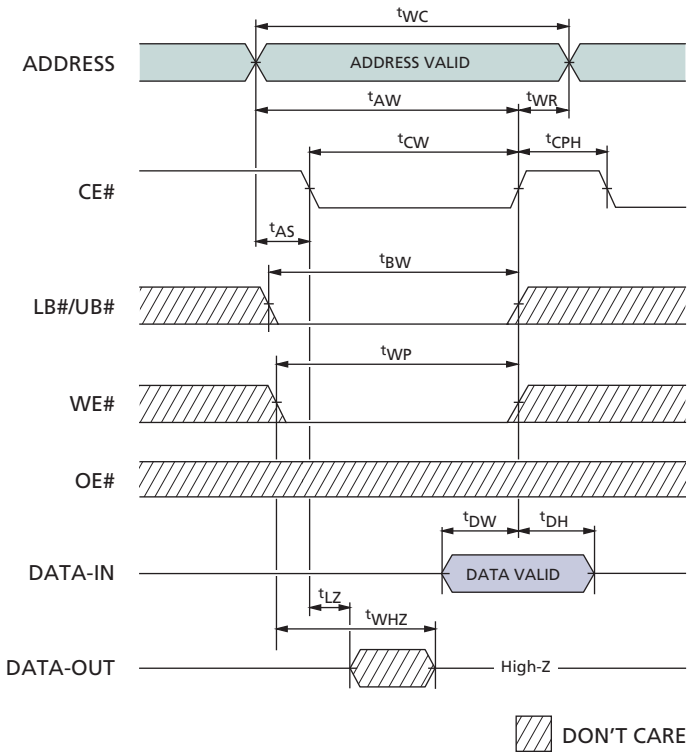


Table 21: WRITE Timing Parameters

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
t_{AS}	0		0		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CPH}	5		5		ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
t_{DW}	23		25		ns
t_{LZ}	10		10		ns
t_{WC}	70		85		ns
t_{WHZ}		8		8	ns
t_{WP}	46		50		ns
t_{WR}	0		0		ns

Figure 22: WRITE Cycle (LB#/UB# Control)

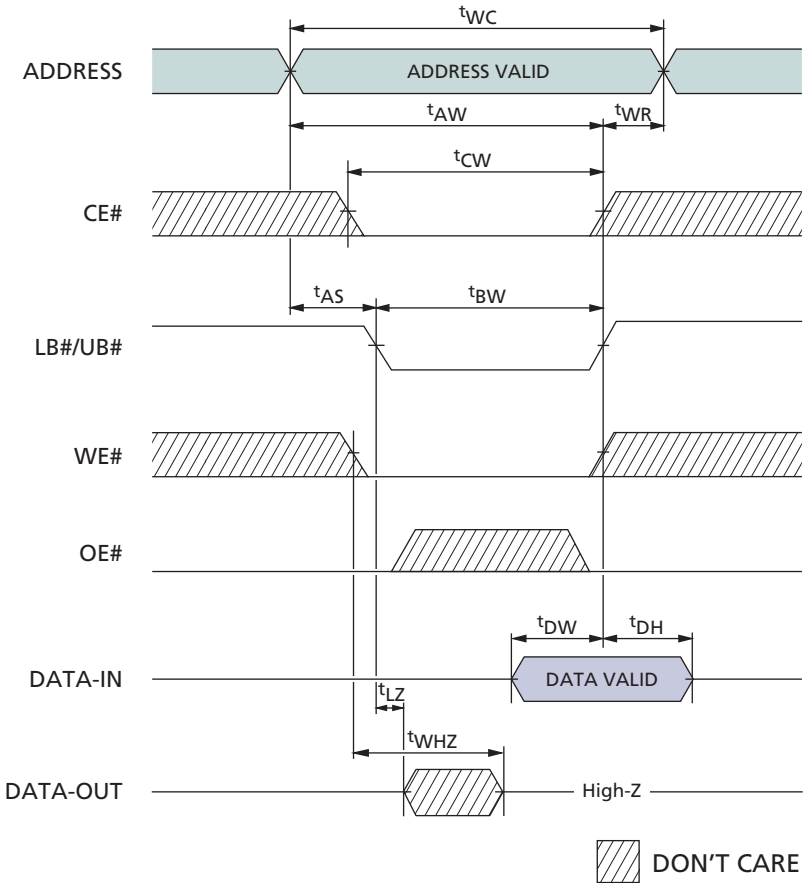
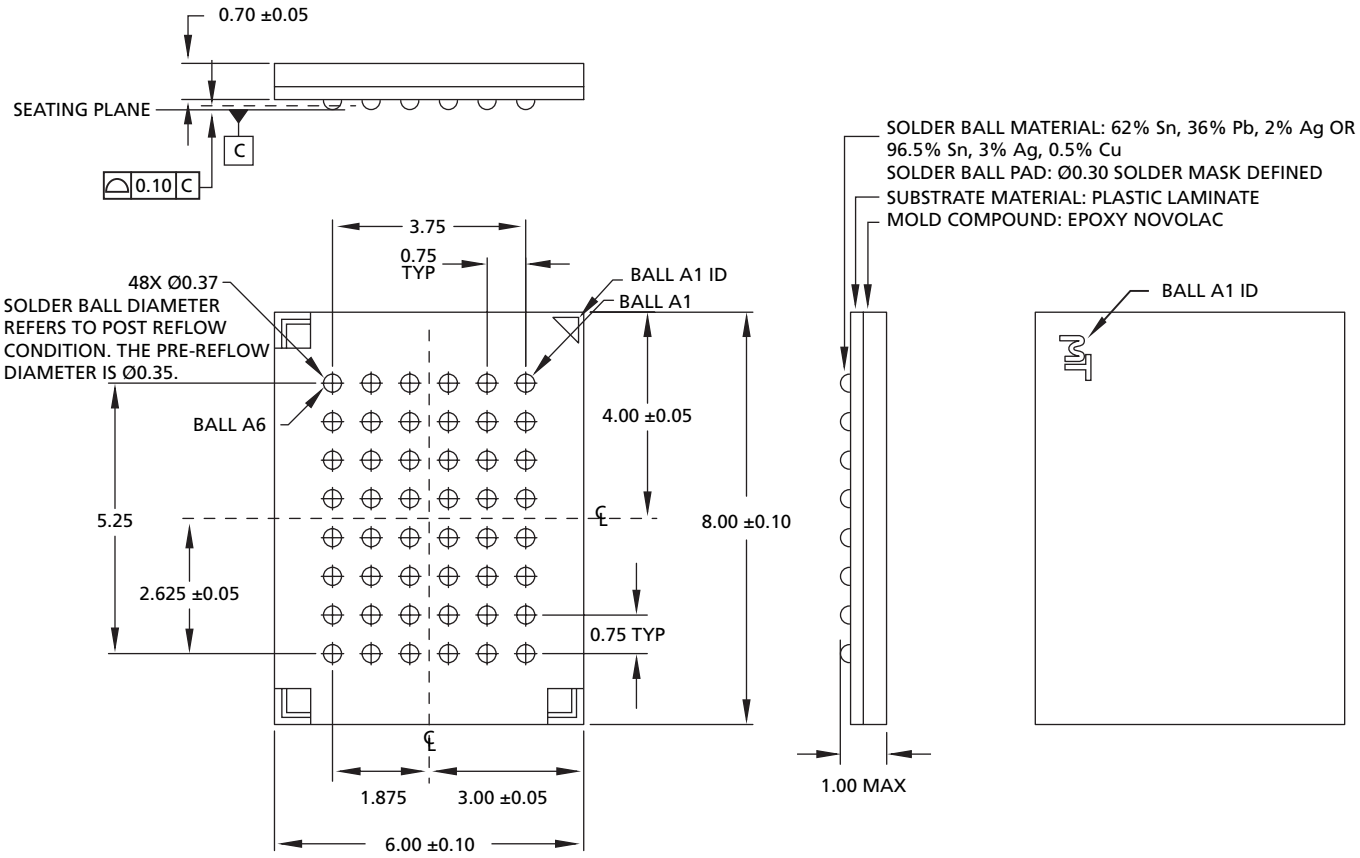


Table 22: WRITE Timing Parameters

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
^{t}AS	0		0		ns
^{t}AW	70		85		ns
^{t}BW	70		85		ns
^{t}CW	70		85		ns
^{t}DH	0		0		ns

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
^{t}DW	23		25		ns
^{t}LZ	10		10		ns
^{t}WC	70		85		ns
^{t}WHZ		8		8	ns
^{t}WR	0		0		ns

Figure 23: 48-Ball VFBGA



NOTE:

1. All dimensions in millimeters, MAX/MIN or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

Data Sheet Designation

Release (No Marking): This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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Revision History

Rev. B 9/04

- Clarified CE# LOW time limited by refresh—must not stay LOW longer than ^{t}CEM.
- Changed PAR options to full, one-half, one-quarter, one-eighth, or none.
- Clarified address A[4] and higher in page mode.
- Clarified ICC and updated values and symbols.
- Updated ICC values.
- Changed CIN and CIO MAX values to 6.5pF.
- Changed CIN and CIO MIN values.
- Changed ^{t}CEM MAX to 8.
- Deleted Appendix A (extended timings and all references).
- Changed doc status to “production.”
- Replaced abbreviated component marks with part numbering chart.
- Corrected package nomenclature to VFBGA.
- Added measurement time clarification to ISB and IPAR notes.
- Updated ISB, ITCR, and IPAR to production values.
- Renamed ^{t}CEH to ^{t}CPH.
- Noted software access third cycle must be CE#-controlled WRITE.
- Last address changed by software sequence.
- WE# LOW limited to ^{t}CEM.
- Clarified TCR temperatures and setting in Table 6.
- Changed VCCQ Option W to 1.7–3.3V.
- Changed wireless temperature to -30°C.
- Clarified software access.
- Noted input HIGH voltage not aligned with the workgroup specification of VccQ - 0.4.
- Noted wireless temp (MIN) exceeds the workgroup spec.

Rev. A, Advance 2/04

- Corrected typographic error in software access description.
- Last address not changed by software access sequence.
- Added on-chip sensor to TCR.
  Clarified software access description.