Military CMOS Programmable Gate Array Logic Cell™ Array M2064/M2018

Conforms to MIL-STD-883, Class B*

Features

CMOS
- Low power
- TTL or CMOS input threshold levels

PROGRAMABLE
- Programmable Logic functions
- Programmable I/O blocks
- Programmable interconnects

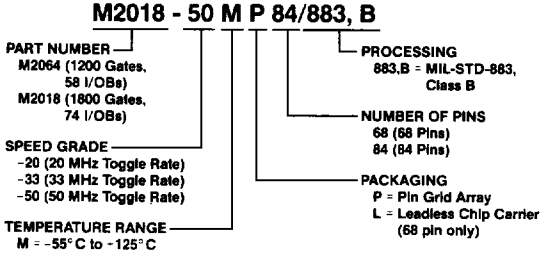
STATIC RAM BASED
- Reprogrammable
- Reconfigurable

SECURITY
- User selectable Security Mode
- Verification feature

Benefits

- Reduced power supply
- Higher board densities
- Complete user control of design
- Instant prototyping
- Replaces SSI and MSI devices
- Easy design modification
- Selectable configuration modes
- 100% testable
- Protects proprietary designs
- Eases design debug

Ordering Information



Description

The Military CMOS Logic Cell Array bridges the gap between Programmable Logic Devices (PLDs) and gate arrays. This high-density, low-power Logic Cell Array device provides designers with both the density benefits of gate arrays and the programmability benefits of user-configurable devices.

The flexible architecture of the LCA is similar to that of a gate array, with an interior matrix of programmable logic blocks called Configurable Logic Blocks (CLBs), a surrounding ring of programmable I/O blocks (IOBs) and programmable interconnects used to define the overall device structure. Unlike gate arrays, LCA functionality is user defined by loading the internal writable storage cells with the configuration data. The reprogrammability of the SRAM-based LCA allows instant design modification on the bench and on the board. Due to the SRAM-based architecture of the LCA, the radiation tolerance data for the M2064 is similar to industry SRAMs which display Total Dose levels from 10^4 to 10^6 rads (Si).

Applications for the LCA cover a wide spectrum of uses. With its high gate density and low-power CMOS technology, the LCA is an ideal low-cost gate array good for prototyping as well as production. The LCA's SRAM-based architecture allows it to be used in applications that take advantage of its reconfigurability. Ground systems (radar) can use the LCA as reconfigurable hardware replacing several devices and saving board space. The SRAM-based logic of the LCA allows for pattern security of sensitive designs when the device is removed from its board. When a different mode backup device is needed the LCA provides excellent redundancy. In short, the LCA offers the total ASIC solution.

Silicon Menu

MMI PART	ORGANIZATION	EQUIVALENT GATE COUNT	CONFIGURABLE LOGIC BLOCKS	USER I/Os	CONFIGURATION PROGRAM BITS	MAX STANDBY CURRENT (CMOS INPUTS)	MAX STANDBY CURRENT (TTL INPUTS)	PACKAGES	MAX TOGGLE RATE BETWEEN CLBs
M2064-20	8x8	1200	64	58	12040	5 mA	10 mA	68LCC, 68PGA	20 MHz
M2064-33	8x8	1200	64	58	12040	5 mA	10 mA	68LCC, 68PGA	33 MHz
M2064-50	8x8	1200	64	58	12040	5 mA	10 mA	68LCC, 68PGA	50 MHz

* Latest revision.

10331A
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Software/Hardware Menu

MMI PARTS	
LCA-MDS21	LCA Development System
LCA-MSC21	LCA Development System Annual Support Agreement
LCA-MDS22	LCA Simulator (P-SILOS™)
LCA-MDS23	LCA Automatic Placement and Routing Program
LCA-MDS24	LCA In-Circuit Emulator

MMI PARTS	
LCA-MDS28	LCA Universal Pod
LCA-MDS27XX	LCA Package Specific Pod Headers
LCA-MDS31	LCA Futurenet® Interface
LCA-MDS33	LCA Daisy Interface
LCA-MDS34	LCA Mentor Interface
LCA-MDSXX	LCA/OrCAD™ Package
LCA-MEK01	LCA Evaluation Kit

Absolute Maximum Ratings

Supply voltage, V_{CC} ..... -0.5 V to 7.0 V
Power down, V_{CC} ..... 2.0 V to 7.0 V
Input voltage range ..... -1.5 V to 5.5 V
Voltage applied to three-state output ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C
Terminal temperature, Leadless Chip Carrier package (Soldering, 10 seconds) ..... 240°C
Thermal resistance, junction to case, θ_{jcmax}, and junction to ambient, θ_{jamax}

Package	θ_{jcmax}	θ_{jamax} (Still air)
(L) Leadless Chip Carrier	1.5°C/W	32°C/W
(P) Pin Grid Array	3°C/W	45°C/W

Maximum power dissipation ..... See Table 2
Maximum junction temperature ..... 175°C
Maximum current density ..... Contact factory

Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage relative to GND	4.5		5.5	V
V_{IHT}	High level input voltage—TTL configuration	2.0		V_{CC}	V
V_{IHC}	High level input voltage—CMOS configuration	0.7 V_{CC}		V_{CC}	V
V_{ILT}	Low level input voltage—TTL configuration	0		0.8	V
V_{ILC}	Low level input voltage—CMOS configuration	0		0.2 V_{CC}	V
I_{IT}	Input leakage current—TTL configuration	±1			µA
I_{IC}	Input leakage current—CMOS configuration	±1			µA
I_{OZ}	Three-state output off current (V_{CC} = 5.5 V)	±10			µA
t_{OP}	Operating free-air temperature	-55		+125	°C

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Electrical Characteristics Over Operating Conditions

Conforms to MIL-STD-883 Group A
Subgroups 1, 2 and 3

SYMBOL	PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage		V_{CC} = MIN	I_{OH} = -4.0 mA	3.7			V
V_{OL}	Low level output voltage		V_{CC} = MIN	I_{OL} = 4.0 mA			0.4	V
I_{CCO}	Quiescent operating power supply current	CMOS inputs	V_{CC} = 5.0 V				5	mA
		TTL inputs	V_{CC} = 5.0 V				10	mA
I_{CCPD}	Power down supply current		V_{CC} = 2.0 V				0.5	mA

Power On Timing

The LCAs contain on-chip reset timing logic for power-up operation. To insure proper master mode system operation, VCC must rise from 2.0 V to minimum specification level in 10 ms or less. For other modes, initiation of configuration must be delayed for 60 ms after VCC reaches the minimum specified level.

Test Conditions

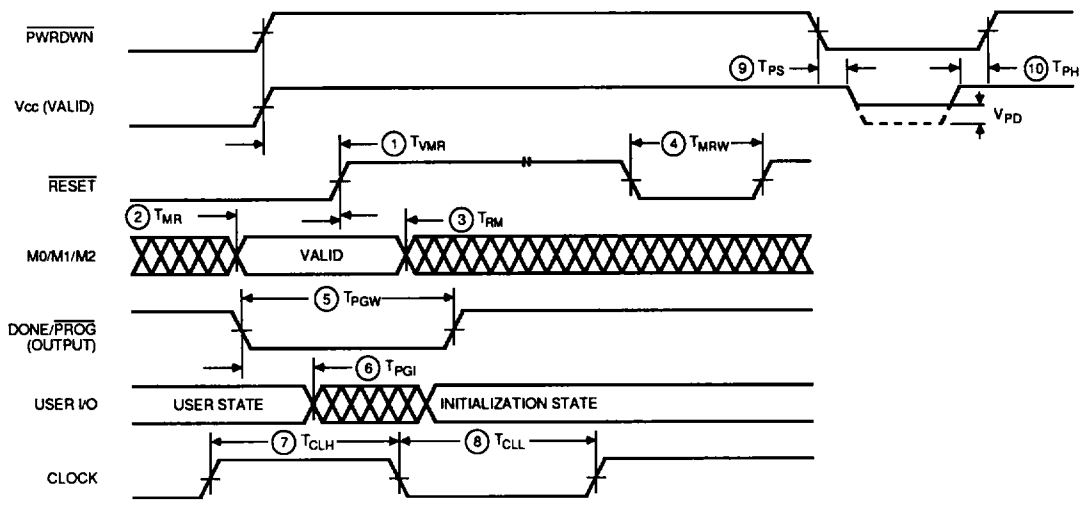
Outputs loaded with rated DC current and 50-pF capacitance to GND.

Switching Characteristics — General

Conforms to MIL-STD-883 Group A Subgroups 9, 10 and 11*

SYMBOL	DESCRIPTION		-20		-33		-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{VMR} ①	$\overline{RESET}$[2]	V_{CC} setup (2.0 V)	250		150		150		ns
t_{MR} ②		M2, M1, M0 setup	100		60		60		ns
t_{RM} ③		M2, M1, M0 hold	100		60		60		ns
t_{MRW} ④		Width (LOW)	250		150		150		ns
t_{PGW} ⑤	DONE/$\overline{PROG}$	Program width (LOW)	6		6		6		µs
t_{PGI} ⑥		Initialization		7		7		7	µs
t_{CLH} ⑦	CLOCK	Clock (HIGH)	20		12		8		ns
t_{CLL} ⑧		Clock (LOW)	20		12		8		ns
t_{PS} ⑨	$\overline{PWR}$ $\overline{DWN}$	Setup to V_{CC}	0		0		0		ns
t_{PH} ⑩		Hold from V_{CC}	0		0		0		ns
V_{PD}		Power Down	2.0		2.0		2.0		V

Notes: 1. V_{CC} must rise from 2.0 Volts to V_{CC} minimum in lest than 10 ms for master mode
2. $\overline{RESET}$ timing relative to power-on and valid mode lines (M0, M1, M2) is relevant only when $\overline{RESET}$ is used to delay configuration.
3. Minimum CLOCK widths for the auxiliary buffer are 1.25 times the t_{CLH}, t_{CLL}.
* Contact factory for test macros.



Switching Characteristics — CLB

SYMBOL	DESCRIPTION		-20		-33		-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{ILO} ①	Logic input to output	Combinatorial		35		20		15	ns
t_{ITO} ②		Transparent latch		45		25		20	ns
t_{QLO}		Additional for Q through F or G to out		30		13		8	ns
t_{CKO} ⑨	K Clock	To output		35		20		15	ns
t_{ICK} ③		Logic-input setup	22		12		8		ns
t_{CKI} ④		Logic-input hold	0		0		0		ns
t_{CCO} ⑩	C Clock	To output		45		25		19	ns
t_{ICC} ⑤		Logic-input setup	18		12		9		ns
t_{CCI} ⑥		Logic-input hold	10		6		0		ns
t_{CIO} ⑪	Logic input to G Clock	To output		65		37		27	ns
t_{ICI} ⑦		Logic-input setup	10		6		4		ns
t_{CII} ⑧		Logic-input hold	15		9		5		ns
t_{RIO} ⑫	Set/reset direct	Input A or D to out		45		25		22	ns
t_{RLO} ⑬		Through F or G to out		65		37		28	ns
t_{MRQ}		Master Reset pin to out		60		35		25	ns
t_{RS}		Separation of set/reset	30		17		9		ns
t_{RPW}		Set/reset pulse-width	20		12		9		ns
F_{CLK}	Flip-flop toggle rate	Q through F to flip-flop	20		33		50		MHz
t_{CH} ⑭	Clock	Clock HIGH	20		12		8		ns
t_{CL} ⑮		Clock LOW	20		12		8		ns

Note: All switching characteristics apply to all valid combinations of process, temperature and supply

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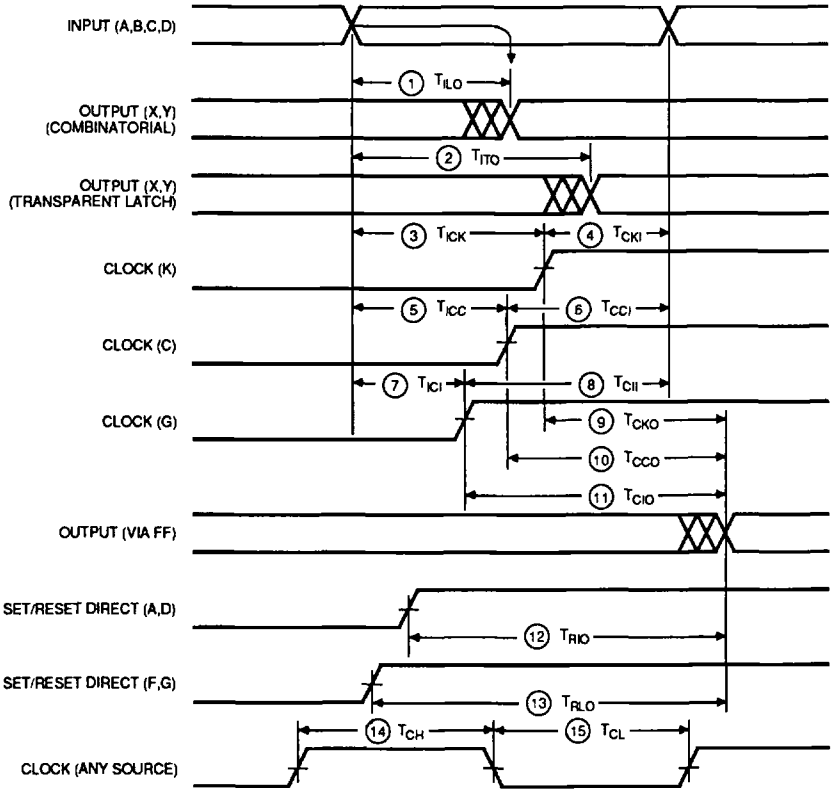
Military Case Outlines*

PACKAGE OUTLINE LETTER	CONFORMS TO MIL-M-38510 APPENDIX C CASE
L	C-7
P	P-BC

* Refer to MIL-M-38510, Appendix C for the appropriate package drawings

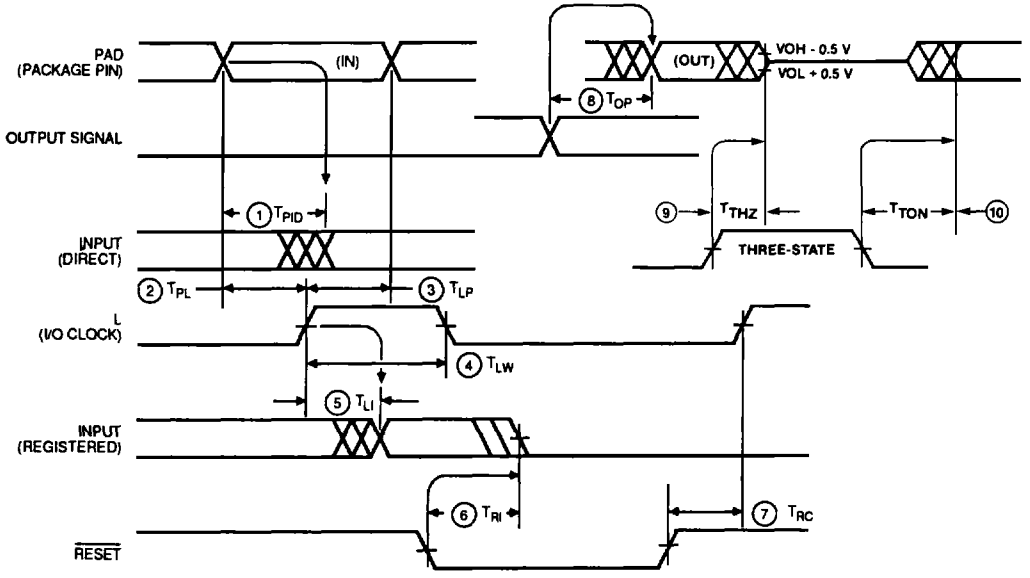
Switching Characteristics CLB



Switching Characteristics — IOB

SYMBOL	DESCRIPTION	-20		-33		-50		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PID} ①	Pad (package pin) to input (direct)		20		12		8	ns
t_{LI} ⑤	I/O Clock to input (storage)		30		20		15	ns
t_{PL} ②	/O Clock to pad-input setup	20		12		8		ns
t_{LP} ③	I/O Clock to pad-input hold	0		0		0		ns
t_{LW} ④	I/O Clock pulse width	20		12		9		nsp
	I/O Clock frequency		20		33		50	MHz
t_{OP} ⑧	Output to pad (output enabled)		25		15		12	ns
t_{THZ} ⑨	Three-state to pad begin hi-Z		35		25		20	ns
t_{TON} ⑩	Three-state to pad end hi-Z		40		25		20	ns
t_{RI} ⑥	$\overline{RESET}$ to input (storage)		50		40		30	ns
t_{RC} ⑦	$\overline{RESET}$ to input clock		35		35		25	ns

Note Timing is measured at 0.5 V_{CC} levels with 50-pF output load.



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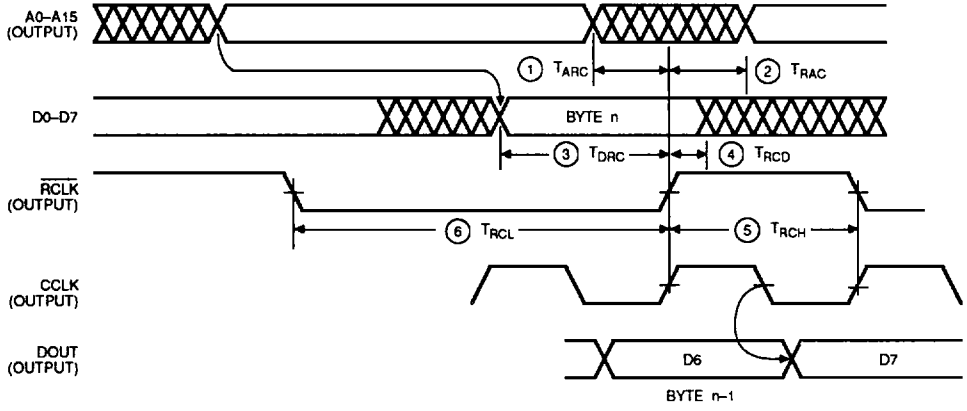
Switching Characteristics — Programming — Master Mode

SYMBOL	DESCRIPTION		-20		-33		-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{ARC} ①	RCLK	From address invalid		0		0		0	ns
t_{RAC} ②		To address valid		300		200		200	ns
t_{DRC} ③		To data setup	100		60		60		ns
t_{RCD} ④		To data hold	0		0		0		ns
t_{RCH} ⑤		$\overline{\text{RCLK}}$ HIGH	600		600		600		ns
t_{RCL} ⑥		$\overline{\text{RCLK}}$ LOW	4.0		4.0		4.0		μs

Notes 1. CCLK and DOUT timing are the same as for slave mode

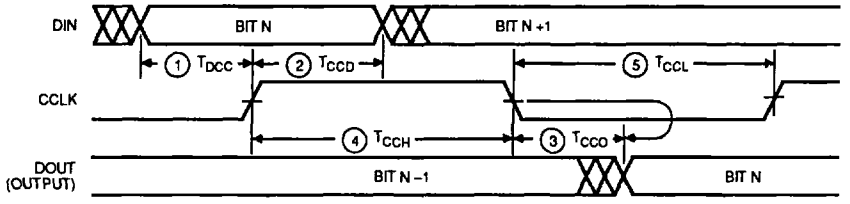
2 At power up, V_{CC} must rise from 2.0 V to V_{CC} minimum in less than 10 ms



Switching Characteristics — Programming — Slave Mode

SYMBOL	DESCRIPTION	-20		-33		-50		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CCO} ③	CCLK to DOUT		100		65		65	ns
t_{DCC} ①	CCLK DIN setup	50		25		0		ns
t_{CCD} ②	CCLK DIN hold	75			40		40	ns
t_{CCH} ④	CCLK HIGH time	0.50		0.30		0.25		μs
t_{CCL} ⑤	CCLK LOW time	0.30	10.0	0.25	5.0	0.25	5.0	μs
F_{CC}	CCLK frequency		1		2		2	MHz

Note Configuration must be delayed at least 40 ms after V_{CC} minimum.



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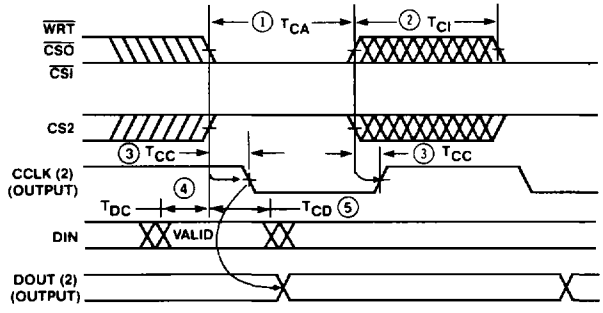
Switching Characteristics — Programming — Peripheral Mode

SYMBOL	DESCRIPTION		-20		-33		-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CA} ①	Controls[1] ($\overline{CS0}$, $\overline{CS1}$, CS2, $\overline{WRT}$)	Active (last active input to first inactive)	0.30	10.0	0.25	5.0	0.25	5.0	μs
t_{CI} ②		Inactive (first inactive input to last active)	0.25		0.25		0.25		μs
t_{CCC} ③		CCLK[2]		100		75		75	ns
t_{DC} ④		DIN setup	50		35		35		ns
t_{CD} ⑤		DIN hold	10		5		5		ns

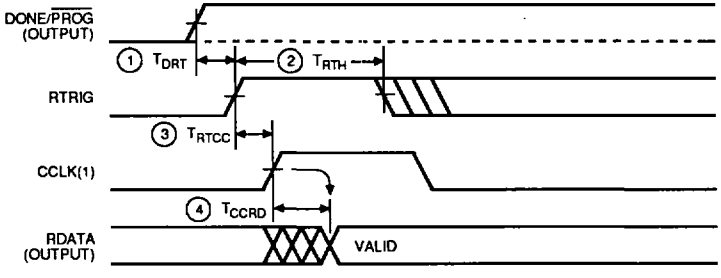
Notes: 1. Peripheral mode timing determined from last control signal of the logical AND of ($\overline{CS0}$, $\overline{CS1}$, CS2, $\overline{WRT}$) to transition to active or inactive state
2. CCLK and DOUT timing are the same as for slave mode
3. Configuration must be delayed at least 40 ms after V_{CC} minimum.



Switching Characteristics — Program Readback

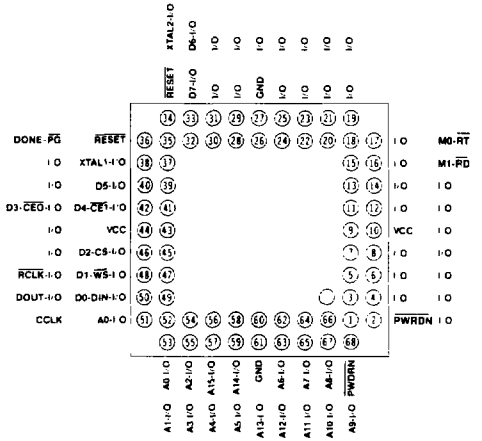
SYMBOL	DESCRIPTION		-20		-33		-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{DRT} ①	RTRIG	PROG setup	300		300		300		ns
t_{RTH} ②		RTRIG HIGH	250		250		250		ns
t_{RTCC} ③	CCLK	RTRIG setup	100		100		100		ns
t_{CCRD} ④		RDATA delay		100		100		100	ns

Notes: 1. CCLK and DOUT timing are the same as for slave mode.
2. DONE/PROG output/input must be HIGH (device programmed) prior to a positive transition of RTRIG (M0).

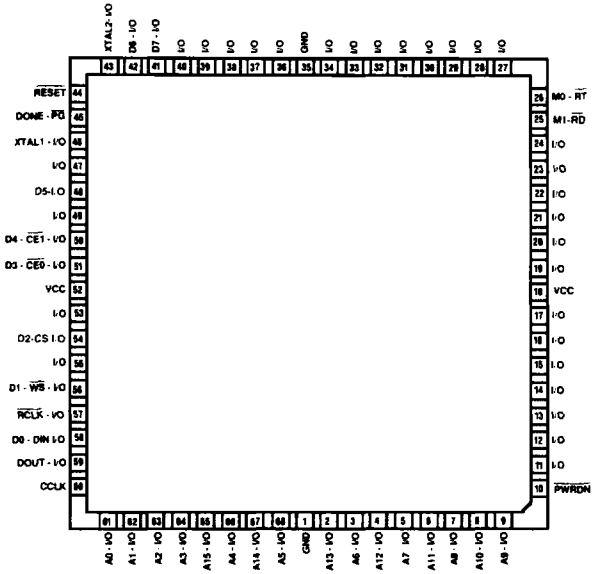


Device Pinouts*

M2064
Logic Cell Array
68 Pin Grid Array
Top View

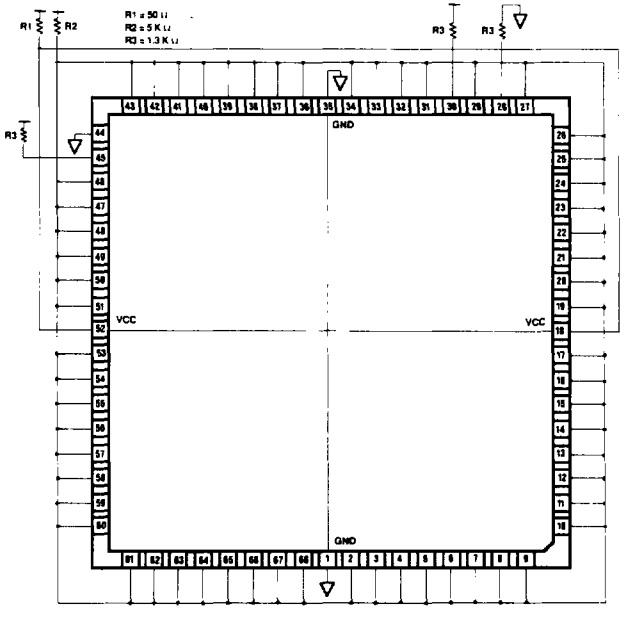


M2064
Logic Cell Array
68 Pin
Leadless Chip Carrier



Burn-In Circuitry*

Condition C
Static Burn-In



Condition D
Dynamic Burn-In
Contact factory

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Configuration Pin Assignments*

68-PIN LCC	68-PIN PGA	CONFIGURATION MODE: ≪M2: M1: M0≫				USER OPERATION
		SLAVE <1:1:1>	PERIPHERAL <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>	
1	B6	GND				
2	A6	≪HIGH≫		A13 (O)		I/O
3	B5			A6 (O)		
4	A5			A12 (O)		
5	B4			A7 (O)		
6	A4			A11 (O)		
7	B3			A8 (O)		
8	A3			A10 (O)		
9	A2			A9 (O)		
10	B2	$\overline{\text{PWRDWN}}$ (I)				
11	B1	≪HIGH≫				I/O
12	C2					
13	C1					
14	D2					
15	D1					
16	E2					
17	E1					
18	F2	VCC				
19	F1	≪HIGH≫				I/O
20	G2					
21	G1					
22	H2					
23	H1					
24	J2					
25	J1	M1 (HIGH)	M1 (LOW)	M1 (HIGH)	M1 (LOW)	$\overline{\text{RDATA}}$ (O)
26	K1	M0 (HIGH)	M0 (HIGH)	M0 (LOW)	M0 (LOW)	RTRIG (I)
27	K2	M2 (HIGH)				I/O
28	L2	HDC (HIGH)				
29	K3	≪HIGH≫				
30	L3	LDC (LOW)				
31	K4	≪HIGH≫				
32	L4					
33	K5					
34	L5					

≪HIGH≫ is high impedance with a 20 to 50-KΩ internal pull-up resistor during configuration

Table 1. M2064 Pin Assignments
(continued on next page)

Configuration Pin Assignments*

68-PIN LCC	68-PIN PGA	CONFIGURATION MODE: ≪M2: M1: M0≫				USER OPERATION
		SLAVE <1:1:1>	PERIPHERAL <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>	
35	K6	GND				
36	L6	≪HIGH≫				I/O
37	K7					
38	L7					
39	K8					
40	L8					
41	K9			D7 (I)		
42	L9			D6 (I)		
43	L10					XTL2 or I/O
44	K10	$\overline{\text{RESET}}$ (I)				
45	K11	DONE (O)				PROG (I)
46	J10	≪HIGH≫				XTL1 or I/O
47	J11					I/O
48	H10			D5 (I)		
49	H11					
50	G10		$\overline{\text{CS0}}$ (I)	D4 (I)		
51	G11		$\overline{\text{CS1}}$ (I)	D3 (I)		
52	F10	VCC				
53	F11	≪HIGH≫				I/O
54	E10		$\overline{\text{CS2}}$ (I)	D2 (I)		
55	E11					
56	D10		$\overline{\text{WRT}}$ (I)	D1 (I)		
57	D11			$\overline{\text{RCLK}}$		
58	C10	DIN (I)		D0 (I)		
59	C11	DOUT (O)				
60	B11	CCLK (I)	CCLK (O)			CCLK (I)
61	B10	≪HIGH≫		A0 (O)		I/O
62	A10			A1 (O)		
63	B9			A2 (O)		
64	A9			A3 (O)		
65	B8			A15 (O)		
66	A8			A4 (O)		
67	B7			A14 (O)		
68	A7			A5 (O)		

≪HIGH≫ is high impedance with a 20 to 50-KΩ internal pull-up resistor during configuration

Table 1. M2064 Pin Assignments

* Contact factory for M2018 pinout, burn in circuitry and pin assignments.

Pin Description

$\overline{\text{PWRDWN}}$

An active low power-down input stops all internal activity to minimize VCC power and puts all output buffers in a high-impedance state. Configuration is retained, however, internal storage elements are Reset. When the $\overline{\text{PWRDWN}}$ pin returns HIGH, the device returns to operation with the same sequence of reset, buffer enable and DONE, $\overline{\text{PROGRAM}}$ as at the completion of configuration.

M0, RTRIG

As Mode 0, this input and M1, M2 are sampled before the start of configuration to establish the configuration mode to be used.

As a read trigger, an input transition to a HIGH, after configuration is complete, will initiate a readback of configuration and storage element data. This operation may be limited to a single request, or be inhibited altogether, by selecting the appropriate readback option when generating the bit stream.

M1, $\overline{\text{RDATA}}$

As Mode 1, this input and M0, M2 are sampled before the start of configuration to establish the configuration mode to be used.

As an active-low read data; after configuration is complete, this pin is the output of the readback data.

M2

As Mode 2, this input and M0, M1 are sampled before the start of configuration to establish the configuration, mode to be used. After configuration, this pin becomes a user-programmable I/O.

HDC

High during configuration is held at a HIGH level by the LCA until after configuration. It is intended to be available as a control indication that configuration is not complete. After configuration, this pin is a user I/O.

$\overline{\text{LDC}}$

Low during configuration is held at a LOW level by the LCA until after configuration. It is intended to be available as a control indication that configuration is not completed. It is particularly useful in master mode as a LOW enable for an EPROM. After configuration, this pin is a user I/O. If used as a LOW EPROM enable, it should be programmed as a HIGH after configuration.

$\overline{\text{RESET}}$

This is an active-low input which has three functions. Prior to the start of configuration, a LOW input will delay the start of the configuration process. An internal circuit senses the application of power and begins a minimal time-out cycle on the order of 100 ms. When the time-out and $\overline{\text{RESET}}$ are complete, the levels of the "M" mode lines are sampled and configuration begins. If $\overline{\text{RESET}}$ is asserted during a configuration, the LCA is reinitialized and will restart the configuration at the termination of RESET. If $\overline{\text{RESET}}$ is asserted after configuration is complete, it will provide an asynchronous reset of all IOB and CLB storage elements of the LCA.

DONE, $\overline{\text{PROG}}$

The DONE open drain output is configurable with or without a pull-up resistor of about 3 KΩ. At the completion of configuration, the circuitry of the LCA becomes active in a synchronous order and one configuration clock cycle later DONE is asserted. Once configuration is done, a HIGH-to-LOW transition of this program pin will cause an initialization of the LCA and start a reconfiguration if that mode is selected in the current configuration.

XTL1

This user I/O pin may be configured to operate as the output of an amplifier usable with an external crystal and bias circuitry to form an oscillator.

XTL2

This user I/O pin may be configured to operate as the input of an amplifier usable with an external crystal and bias circuitry to form an oscillator.

CCLK

During configuration, configuration clock is an output of an LCA in either master or peripheral mode. LCAs in slave mode use it as a clock input. During a readback operation, it is an input clock for the configuration data being output.

DOUT

This user I/O pin is used during configuration to output serial configuration data out for daisy-chained slaves' data in.

DIN

This user I/O pin is used as serial data in during slave or peripheral configuration. This pin is D0 in master configuration mode.

$\overline{\text{CS0}}$, $\overline{\text{CS1}}$, CS2, $\overline{\text{WRT}}$

These four inputs represent a set of signals, three active low and one active high, which are used in the peripheral mode to control configuration data entry. The assertion of all four generates a LOW CCLK and shifts DOUT data. The removal of any assertion clocks in the DIN data present and causes a HIGH CCLK. In master mode, these pins become part of the parallel configuration byte (D4, D3, D2, D1). After configuration is complete, they are user-programmed I/O.

$\overline{\text{RCLK}}$

During master mode configuration, this pin represents a read clock of an external memory device. After configuration is complete, this pin becomes a user-programmed I/O.

D0-D7

This set of eight pins represents the parallel configuration data byte for the master mode. After configuration is complete, they are user-programmed I/O.

A0-A15

This set of sixteen pins presents an address output for an external configuration memory during master mode. After configuration is complete, they are user-programmed I/O. A12 through A15 are not available in packages with less than sixty-eight pins.

I/O

A pin which may be programmed by the user to be input and/or output following configuration. Some of these pins present a high-impedance pull-up or perform other functions before configuration is complete.