8. ELECTRICAL SPECIFICATIONS

This section contains electrical specifications and associated timing information for the TMP68303.

8.1 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	Vcc	-0.3~ + 7.0	V
Input Voltage	Vin	-0.3~ + 7.0	V
Operating Temperature Range	Ta	0~ + 70	°C
Storage Temperature	Tstg	-55~ + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or Vcc).

8.2 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C)

Item		Symbol	TMP68303 Min	TMP68303 Max	Unit
Input High Voltage (except P0, P1 Port)		V_{IH}	2.0	V_{CC}	V
Input High Voltage (P0, P1 Port)		V_{IHP}	V_{CC} × 0.7	V_{CC} + 0.3	V
Input Low Voltage (except P0, P1 Port)		V_{IL}	GND − 0.3	0.8	V
Input Low Voltage (P0, P1 Port)		V_{IHL}	−0.3	V_{CC} × 0.3	V
Input Leakage Curren (5.25V)	$\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, $\overline{HALT}$, $\overline{RESET}$, CLK, NOR / $\overline{EMU}$, TIN, INT0~INT2, RxD0, RxD1, $\overline{DREQ0}$~$\overline{DREQ2}$, $\overline{DTEND}$, P00~P03, P10~P13, P20, P21	I_{IN}	− − −	2.5 2.5 20	μA μA
3-state (off state) Input Current	(2.4V/0.4V) $\overline{AS}$, A1~A23, D0~D15,FC0~FC2, $\overline{LDS}$, $\overline{UDS}$, R / $\overline{W}$	I_{TSI}	− −	20 20	μA μA
Output High Voltage (I_{OH} = -400μA)	$\overline{AS}$, A1~A23, D0~D15, FC0~FC2,$\overline{LDS}$, $\overline{UDS}$, R / $\overline{W}$, $\overline{BG}$, P00~P03, P10~P13, P20, P21 Tout1, Tout2, $\overline{RAS}$, $\overline{CAS}$, INT0~INT2, TxD0, TxD1, $\overline{DACK0}$~$\overline{DACK2}$, $\overline{IACK0}$~$\overline{IACK2}$ $\overline{IPL0}$~$\overline{IPL2}$	V_{OH}	− V_{CC} − 0.75	−	V
Output Low Voltage (I_{OL} = 1.6mA) (I_{OL} = 3.2mA) (I_{OL} = 5.3mA)	$\overline{HALT}$, $\overline{RESET}$ A1~A23, $\overline{BG}$, FC0~FC2 $\overline{AS}$, D0~D15, $\overline{LDS}$, $\overline{UDS}$, R / $\overline{W}$, P00~P03, P10~P13, P20, P21, Tout1, Tout2, $\overline{RAS}$, $\overline{CAS}$, $\overline{DTACK}$ $\overline{BERR}$, TxD0, TxD1, $\overline{DACK0}$~$\overline{DACK2}$, $\overline{IACK0}$~$\overline{IACK2}$ $\overline{DTEND}$, $\overline{BR}$, $\overline{BGACK}$, $\overline{IPL0}$~$\overline{IPL2}$	V_{OL}	− − −	0.5 0.5 0.5	V
Current Dissipation	f = 12.5MHz f = 16.67MHz	I_D	− −	90 100	mA
Power Dissipation	f = 12.5MHz f = 16.67MHz	P_D	− −	0.473 0.525	W
Capacitance (Vin = 0V, Ta = 25°C ; Frequency = 1MHz)*		C_{IN}	−	20.0	pF
Load Capacitance	$\overline{HALT}$ All other	C_L	− −	70 130	pF

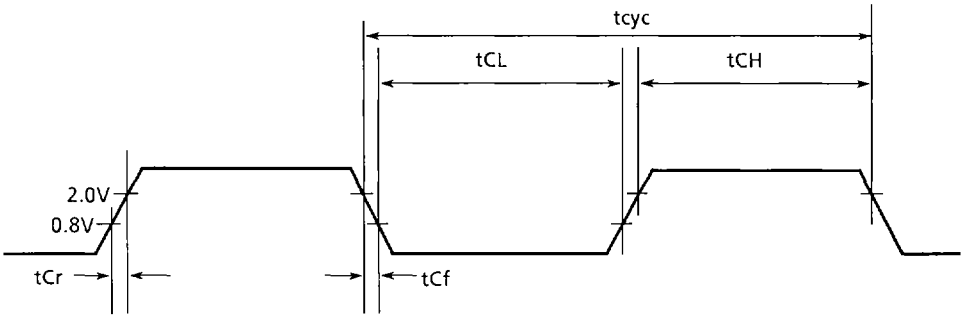
281189

* : Capacitance is periodically sampled rather then 100% test

8.3 AC Electrical Specifications – Clock Timing

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figure 8.1)

Characteristic	Symbol	8MHz		10MHz		12.5MHz		16.67MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Frequency of Operation	f	4.0	8.0	4.0	10.0	4.0	12.5	8.0	16.67	MHz
Cycle Time	tcyc	125	250	100	250	80	250	60	125	ns
Clock Pulse Width	tCL tCH	55 55	125 125	45 45	125 125	35 35	125 125	27 27	62.5 62.5	ns
Rise and Fall Times	tCr tCf	– –	10 10	– –	10 10	– –	5 5	– –	5 5	ns



Note : Timing measurements are referenced to and from a low voltage of 0.8 volt and high a voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 8.1 Clock Input Timing Diagram

8.4 AC Electrical Specifications – Read and Write Cycles (1/4)

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figures 8.2 and 8.3)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		16.67MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
1	Clock Period	tCYC	125	250	100	250	80	250	60	125	ns
2	Clock Width Low	tCL	55	125	45	125	35	125	27	62.5	ns
3	Clock Width High	tCH	55	125	45	125	35	125	27	62.5	ns
4	Clock Fall Time	tCf	–	10	–	10	–	5	–	5	ns
5	Clock Rise Time	tCr	–	10	–	10	–	5	–	5	ns
6	Clock Low to Address Valid	tCLAV	–	62	–	50	–	50	–	50	ns
6A	Clock High to FC Valid	tCHFCV	–	62	–	50	–	45	0	45	ns
7	Clock High to Address, Data Bus High Impedance (Maximum)	tCHADZ	–	80	–	70	–	60	–	50	ns
8	Clock High to Address, FC Invalid (Minimum)	tCHAFI	0	–	0	–	0	–	0	–	ns
9[1]	Clock High to $\overline{AS}$, $\overline{DS}$ Low	tCHSL	3	60	3	50	3	40	3	30	ns
11[2]	Address Valid to $\overline{AS}$, $\overline{DS}$ Low (Read) / $\overline{AS}$ Low (Write)	tAVSL	30	–	20	–	15	–	15	–	ns
11A[2]	FC Valid to $\overline{AS}$, $\overline{DS}$ Low (Read) / $\overline{AS}$ Low (Write)	tFCVSL	90	–	70	–	60	–	30	–	ns
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ High	tCLSH	–	62	–	50	–	40	3	30	ns
13[2]	$\overline{AS}$, $\overline{DS}$ High to Address / FC Invalid	tSHAFI	40	–	30	–	20	–	10	–	ns
14[2]	$\overline{AS}$, $\overline{DS}$ Width Low (Read) / $\overline{AS}$ Low (Write)	tSL	270	–	195	–	160	–	120	–	ns
14A[2]	$\overline{DS}$ Width Low (Write)	tDSL	140	–	95	–	80	–	60	–	ns
15[2]	$\overline{AS}$, $\overline{DS}$ Width High	tSH	150	–	105	–	65	–	60	–	ns

8.4 AC Electrical Specifications – Read and Write Cycles (2/4)

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figures 8.2 and 8.3)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		16.67MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
16	Clock High to Control Bus High Impedance	tCHCZ	–	80	–	70	–	60	–	50	ns
17[2]	$\overline{AS}$, $\overline{DS}$, High to R / $\overline{W}$ High (Read)	tSHRH	40	–	30	–	20	–	10	–	ns
18[1]	Clock High to R / $\overline{W}$ High	tCHRH	0	55	0	45	0	40	0	40	ns
20[1]	Clock High to R / $\overline{W}$ Low (Write)	tCHRL	0	55	0	45	0	40	0	40	ns
20A[2,8]	$\overline{AS}$ Low to R / $\overline{W}$ Valid (Write)	tASRV	–	10	–	10	–	10	–	10	ns
21[2]	Address Valid to R / $\overline{W}$ Low (Write)	tAVRL	20	–	0	–	0	–	0	–	ns
21A[2]	FC Valid to R / $\overline{W}$ Low (Write)	tFCVRL	60	–	50	–	30	–	20	–	ns
22[2]	R / $\overline{W}$ Low to $\overline{DS}$ Low (Write)	tRLSL	80	–	50	–	30	–	20	–	ns
23	CLock Low to Data Out Valid (Write)	tCLDO	–	62	–	50	–	50	–	50	ns
25[2]	$\overline{AS}$, $\overline{DS}$ High to Data Out Invalid (Write)	tSHDOI	40	–	30	–	20	–	15	–	ns
26[2]	Data Out Valid to $\overline{DS}$ Low (Write)	tDOSL	40	–	30	–	20	–	15	–	ns
27[6]	Data in to Clock Low (Setup Time on Read)	tDICL	10	–	10	–	10	–	7	–	ns
28[2]	$\overline{AS}$, $\overline{DS}$ High to Data in Invalid (Hot Time on Read)	tSHDAH	0	240	0	190	0	150	0	110	ns
29	($\overline{AS}$, $\overline{DS}$ High to BERR High	tSHDII	0	–	0	–	0	–	0	–	ns

8.4 AC Electrical Specifications – Read and Write Cycles (3/4)

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figures 8.2 and 8.3)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		16.67MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
30	$\overline{AS}$, $\overline{DS}$ High to $\overline{BERR}$ High	tSHBEH	0	–	0	–	0	–	0	–	ns
31[2,6]	$\overline{DTACK}$ Low to Data In (Setup Time)	tDALDI	–	90	–	65	–	50	–	40	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition	tRHr, f	0	200	0	200	0	200	0	150	ns
33	Clock High to $\overline{BG}$ Low	tCHGL	–	62	–	50	–	40	–	40	ns
34	CLock High to $\overline{BG}$ High	tCHGH	–	62	–	50	–	40	0	40	ns
35	$\overline{BR}$ Low to $\overline{BG}$ Low	tBRLGL	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
36[9]	$\overline{BR}$ High to $\overline{BG}$ High	tBRHGH	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37	$\overline{BGACK}$ Low to $\overline{BG}$ High	tGALGH	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37A[10]	$\overline{BGACK}$ Low to $\overline{BR}$ High	tGALBRH	20	1.5 Clocks	20	1.5 Clocks	20	1.5 Clocks	10	1.5 Clocks	ns
38	$\overline{BG}$ Low to Control, Address, Data Bus High Impedance ($\overline{AS}$ High)	tGLZ	–	80	–	70	–	60	–	50	ns
39	$\overline{BG}$ Width High	tGH	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.

8.4 AC Electrical Specifications – Read and Write Cycles (4/4)

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figures 8.2 and 8.3)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		16.67MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
46	$\overline{BGACK}$ Width Low	tGAL	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.
47[6]	Asynchronous Input Setup Time	tASI	10	–	10	–	10	–	10	–	ns
48[2,3]	$\overline{BERR}$ Low to $\overline{DTACK}$ Low	tBELDAL	20	–	20	–	20	–	10	–	ns
53	Clock High to Data Out Invalid	tCHDOI	0	–	0	–	0	–	0	–	ns
55	R / $\overline{W}$ to Data Bus Driven	tRLDBD	30	–	20	–	10	–	0	–	ns
56[4]	$\overline{HALT}$ / $\overline{RESET}$ Pulse Width	tHRPW	12	–	12	–	12	–	12	–	Clk. Per.
57	$\overline{BGACK}$ High to Control Bus Driven	tGASD	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.
58[9]	$\overline{BG}$ High to Control Bus Driven	tRHSD	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.

Note : 1. For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the value given in the maximum columns.

2. Actual value depends on clock period.

3. If #47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, #48 may be ignored. In the absence of $\overline{DTACK}$, $\overline{BERR}$ is an asynchronous input using the asynchronous input setup time (#47).

4. For power-up, the MPU must be held in the reset state for 100 milliseconds to allow stabilization of on-chip circuitry. After the system is powered up, #56 refers to the minimum pulse width required to reset the processor.

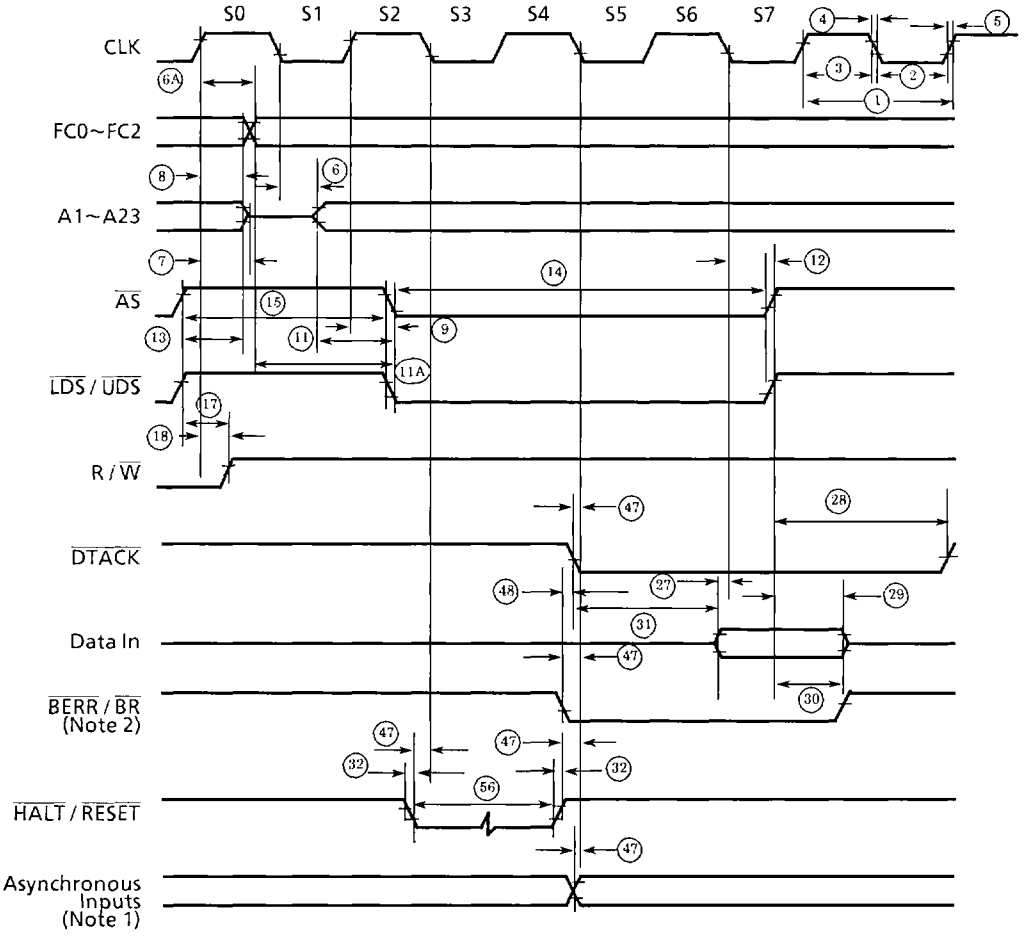
6. If the asynchronous input setup time (#47) requirement is satisfied for $\overline{DTACK}$, the $\overline{DTACK}$-asserted to data setup time (#31) requirement can be ignored. The data must only satisfy the data-in to clock low setup time (#27) for the following clock cycle.

8. When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (±20%), subtract 5 nanoseconds from the values given is these columns.

9. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.

10. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{BG}$ may be re-asserted.

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional descriptions of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



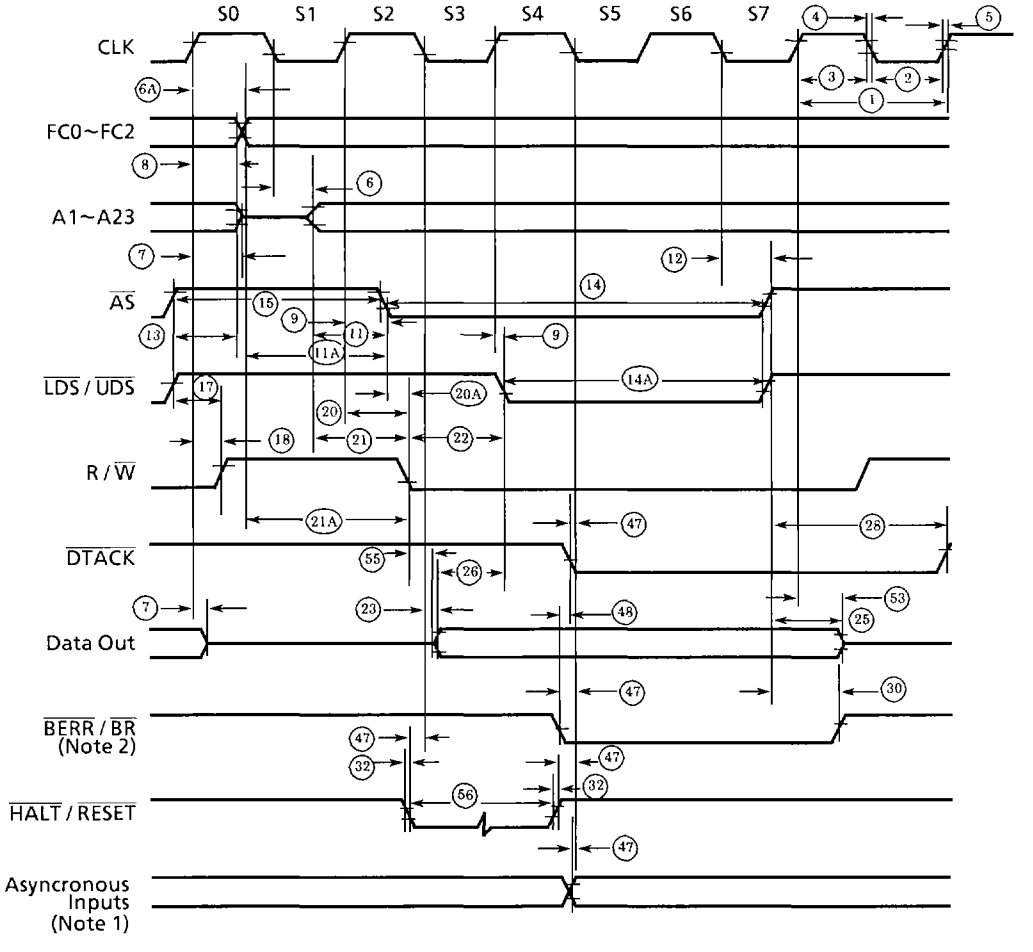
Note : 1. Setup time for the asynchronous inputs $\overline{BGACK}$, $\overline{IPL0}$~$\overline{IPL2}$ guarantees their recognitions at the next falling edge of the clock.

2. $\overline{BR}$ need fall at this time only in order to insure being recognized at the end of this bus cycle.

3. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 8.2 Read Cycle Timing Diagram

These waveforms should onluy be referenced in regard to the edge-to-edge reasurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions andf their related diagrams for device operation.



Note : 1. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.
The voltage swing through this range should start outside and pass through the range such that the rise of fall will be linear between 0.8 volt and 2.0 volt.

2. Because of loading variation, R/$\overline{W}$ may be valid after $\overline{AS}$ even through both are initiated by the rising edge of S2 (Specification 20A).

Figure 8.3 Write Cycle Timing Diagram

8.5 AC Electrical Specifications – Bus Arbitration

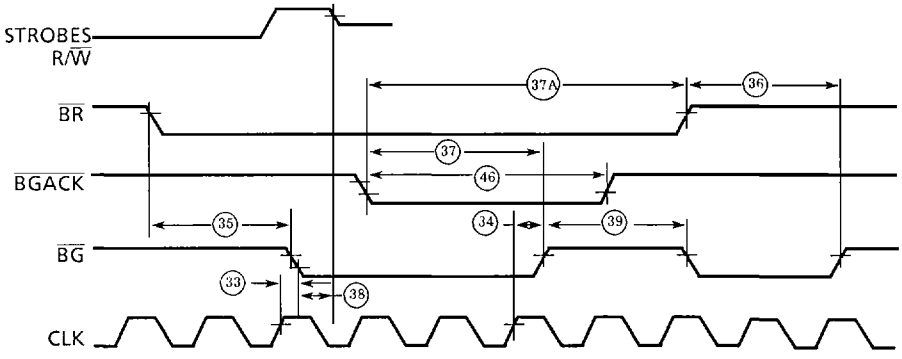
(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figures 8.4, 8.5 and 8.6)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		16.67MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
7	Clock High to Address, Data Bus High Impedance	tCHADZ	–	80	–	70	–	60	–	50	ns
16	Clock High to Control Bus High Impedance	tCHCZ	–	80	–	70	–	60	–	50	ns
33	Clock High to $\overline{BG}$ Low	tCHGL	–	62	–	50	–	40	0	40	ns
34	Clock High to $\overline{BG}$ High	tCHGH	–	62	–	50	–	40	0	40	ns
35	$\overline{BR}$ Low to $\overline{BG}$ Low	tBRLGL	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
36[1]	$\overline{BR}$ High to $\overline{BG}$ High	tBKHGH	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37	$\overline{BGACK}$ Low to $\overline{BG}$ High	tGALGH	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37A[2]	$\overline{BGACK}$ Low to $\overline{BR}$ High	tGALBRH	20	1.5 Clocks	20	1.5 Clocks	20	1.5 Clocks	10	1.5 Clocks	ns
38	$\overline{BG}$ Low to Control, Address, Data Bus High Impedance ($\overline{AS}$ High)	tGLZ	–	80	–	70	–	60	–	50	ns
39	$\overline{BG}$ Width High	tGH	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.
46	$\overline{BGACK}$ Width Low	tGAL	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.
47	Asynchronous Input Setup Time	tASI	10	–	10	–	10	–	5	–	ns
57	$\overline{BGACK}$ High to Control Bus Driven	tGABD	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.
58[1]	$\overline{BG}$ High to Control Bus Driven	tGHBD	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.

Note: 1. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.

2. The minimum value must to guarantee proper operation. If the maximum value is exceeded, $\overline{BG}$ may be reasserted.

These waveforms (Figures 8.4, 8.5 and 8.6) should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



Note : Setup time to the clock (#47) for the asynchronous inputs $\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, $\overline{IPL0}$-$\overline{IPL2}$ guarantees their recognition at the next falling edge of the clock.

Figure 8.4 Bus Arbitration Timing Diagram

8.6 AC Electrical Specifications – Peripheral

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figure 8.5~8.13)

Num.	Item	Symbol	12.5MHz		16.67MHz		Unit
			MIN	MAX	MIN	MAX	
47	Asynchronous Input setup Time	tASI	10	–	10	–	ns
101	Delay Time from $\overline{AS}$	tDAS	–	50	–	50	ns
102	Clock Low to TOUT High	tCLTO	–	70	–	70	ns
103	BCLK Peviod	tBCYC	125	–	125	–	ns
104	BClk Width (Low)	tBCL	55	–	55	–	ns
105	BCLK Width (High)	tBCH	55	–	55	–	ns
106	BCLK Rise Time	tBCr	–	10	–	10	ns
107	BCLK Fall Time	tBCf	–	10	–	10	ns
108	$\overline{LDS}$ (High) to $\overline{RTS0}$ (Low)	tDSMC	–	140	–	140	ns
109	$\overline{CTS0}$ (Low) to $\overline{LDS}$ (Low)	tMCDS	50	–	50	–	ns
113	Clock (Low) to $\overline{RAS}$, $\overline{CAS}$ Assert	tCLNRC	–	40	–	30	ns
114	$\overline{AS}$, $\overline{DS}$ (High) to $\overline{RAS}$, $\overline{CAS}$ Negated	tADSRC	–	40	–	30	ns
115	$\overline{RAS}$ Precharge Time	tRP	1.5	–	1.5	–	Clk. Per.
117	Clock (High) to Column Address Valid	tCLCO	–	40	–	30	ns
118	$\overline{RAS}$-$\overline{CAS}$ Delay Time	tRCD	1.0	–	1.0	–	Clk. Per.
119	$\overline{RAS}$ Pulse Width (Read / Write)	tRAS	2.0	–	2.0	–	Clk. Per.
120	$\overline{DTACK}$ (Low) to $\overline{CAS}$ Assert	tDTCCA	–	10	–	10	ns
121	Clock (High) to $\overline{RAS}$, $\overline{CAS}$ Assert	tCLRCA	–	10	–	10	ns
122	Clock (High) to $\overline{RAS}$, $\overline{CAS}$ Negate	tCLRCN	–	10	–	10	ns
123	$\overline{CAS}$ Setup Time	tCSR	1.0	–	1.0	–	Clk. Per.

201289

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figure 8.14~8.18)

Num.	Item	Symbol	12.5MHz		16.67MHz		Unit
			MIN	MAX	MIN	MAX	
124	LDS (High) to P0, P1 Output	tDPW1	40	—	40	—	ns
125	P0, P1 Input Setup Time	tPRD1	1.5	—	1.5	—	Clk. Per.
126	P0, P1 Input Hold Time	tPHD1	0	—	0	—	ns
127	$\overline{LDS}$ (Low) to P2 Output	tDPW2	40	—	30	—	ns
128	P2 Input Setup Time	tPRD2	10	—	10	—	ns
129	P2 Input Hold Time	tPHD2	40	—	30	—	ns
130	$\overline{DREQ}$ Input Setup Time	tDASI	40	—	30	—	ns
131	$\overline{DREQ}$ Input Hold Time	tDCH	40	—	30	—	ns
132	$\overline{BGACK}$ (Low) to $\overline{DREQ}$ (High)	tGALRQH	0	—	0	—	ns
133	Clock to $\overline{BR}$ (Low)	tCHBRL	—	10	—	10	ns
134	Clock (Low) to Bus Drive	tGALDBD	—	40	—	30	ns
135	$\overline{BGACK}$ (High) to Bus Hz	tGAHZ	—	40	—	30	ns
136	CPU Bus Hz to $\overline{BGACK}$ (Low)	tZGAL	—	1.0	—	1.0	Clk. Per.
137	Clock (High) to $\overline{BGACK}$ (Low)	tCHGAL	—	40	—	30	ns
138	Clock (High) to $\overline{BGACK}$ (High)	tCHGAH	—	40	—	30	ns
139	$\overline{AS}$ (Low) to $\overline{DTEND}$ Input Setup Time	tASLEDL	0	—	0	—	ns
140	$\overline{DTEND}$ (Low) Width	tEDW	1.0	—	1.0	—	Clk. Per.
141	Clock (High) to $\overline{DTEND}$ (Low)	tCHEDL	—	10	—	10	ns
142	Clock (High) to $\overline{DTEND}$ (High)	tCHEDH	—	10	—	10	ns
143	Clock (Low) to FC0-2 Valid	tGALFC	—	40	—	30	ns
144	$\overline{BGACK}$ (High) to FC 0-2 Hz	tDFCZ	—	20	—	20	ns
145	Clock (Low) to Control Bus Valid	tGALCSV	—	40	—	30	ns
146	$\overline{BGACK}$ (High) to Control Bus Hz	tGAHCSZ	—	20	—	20	ns

051289

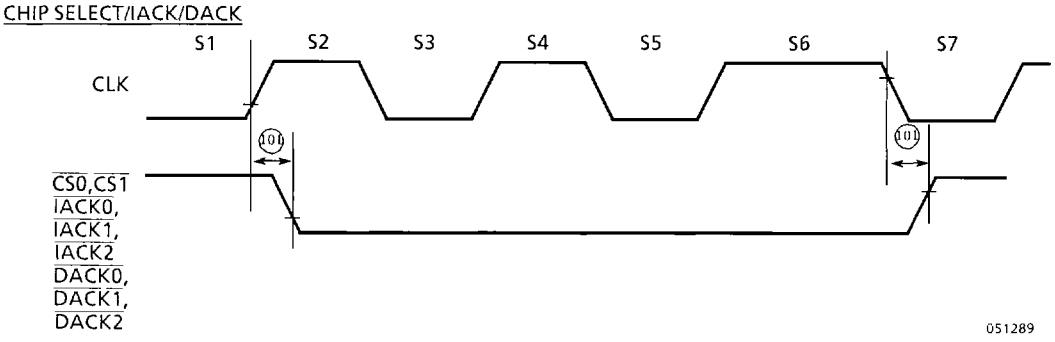


Figure 8.5 $\overline{CS}$, $\overline{IACK}$ Timming

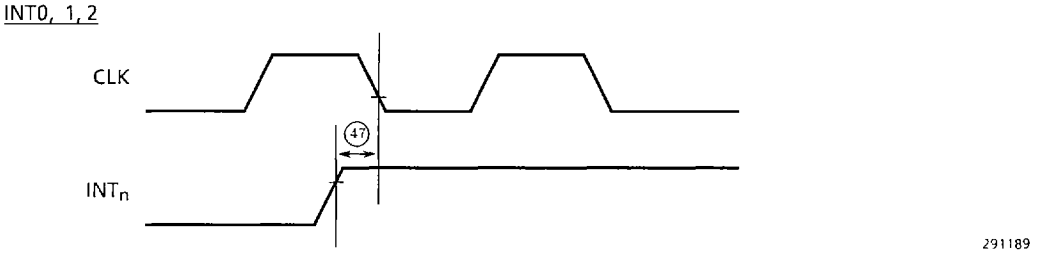


Figure 8.6 Interrupt Request Timming

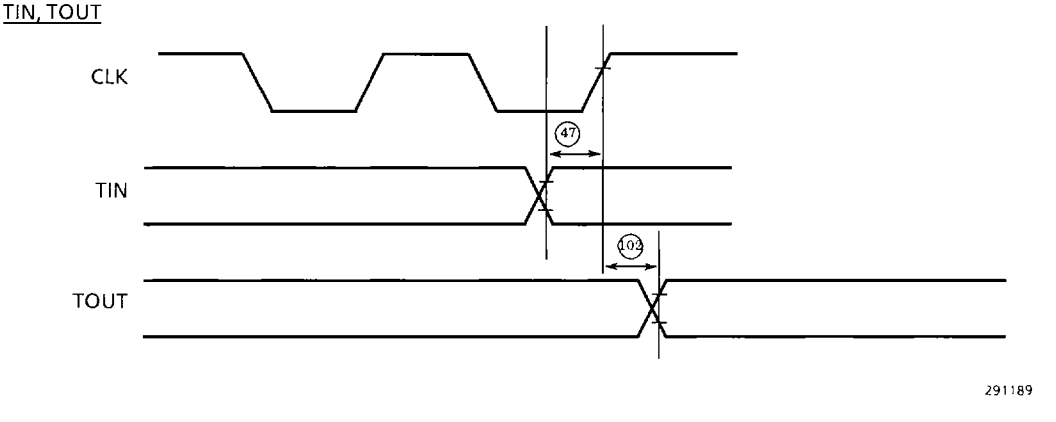


Figure 8.7 Timer Input / Output Timming

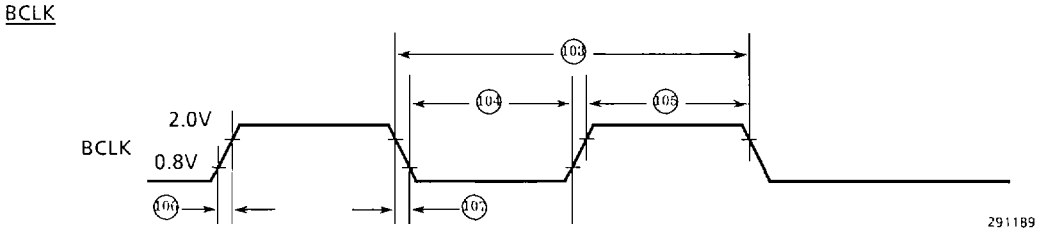


Figure 8.8 Baud Rate Clock Timming

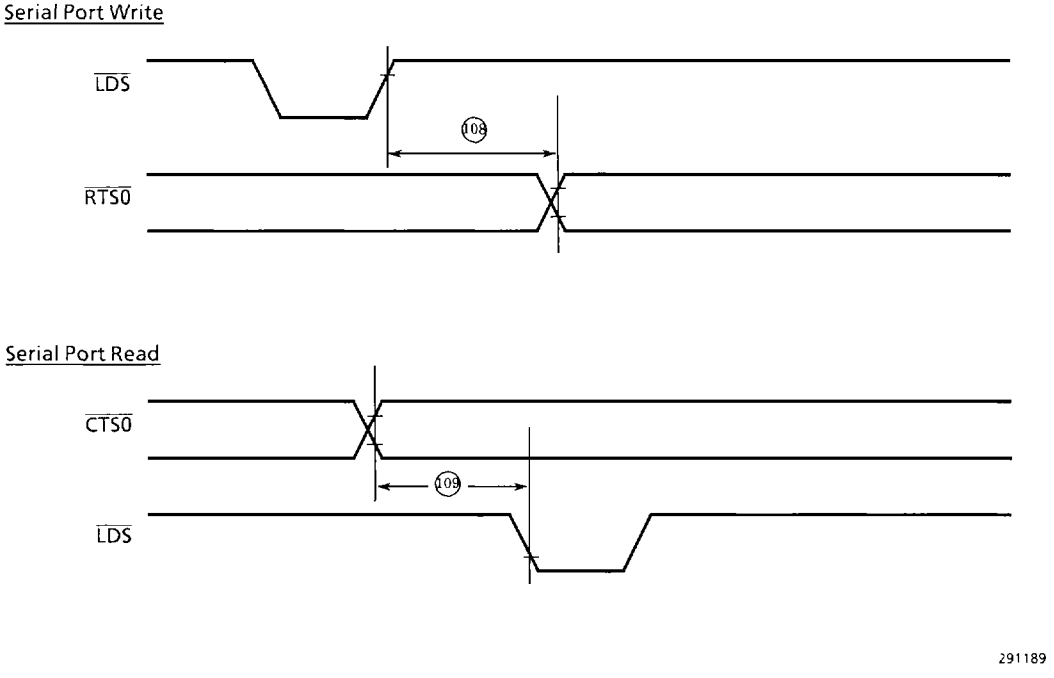


Figure 8.9 Serial Port Timming

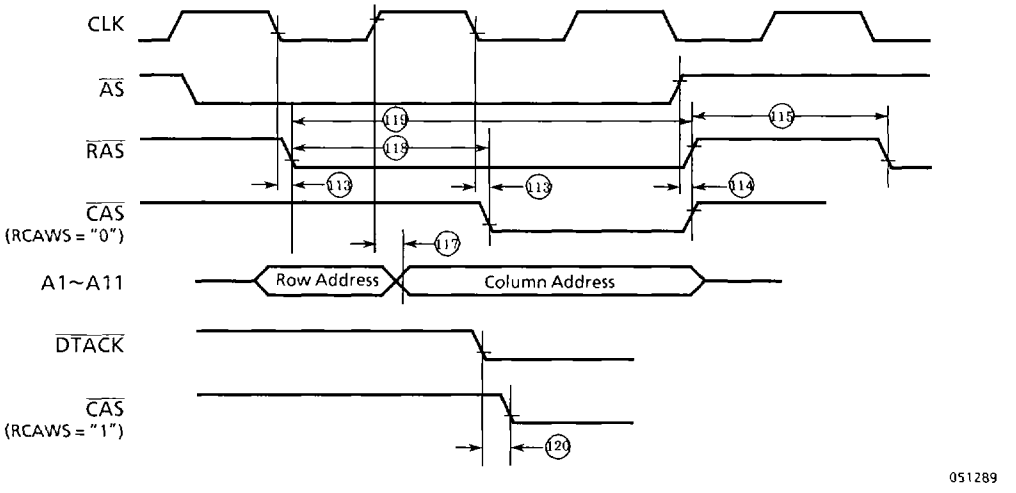


Figure 8.10 DRAM Read / Write

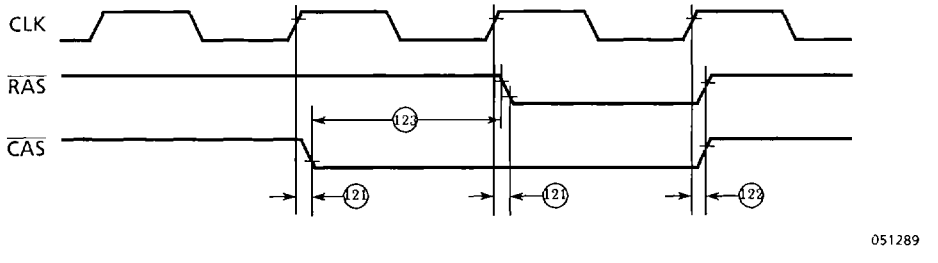


Figure 8.11 DRAM Refresh

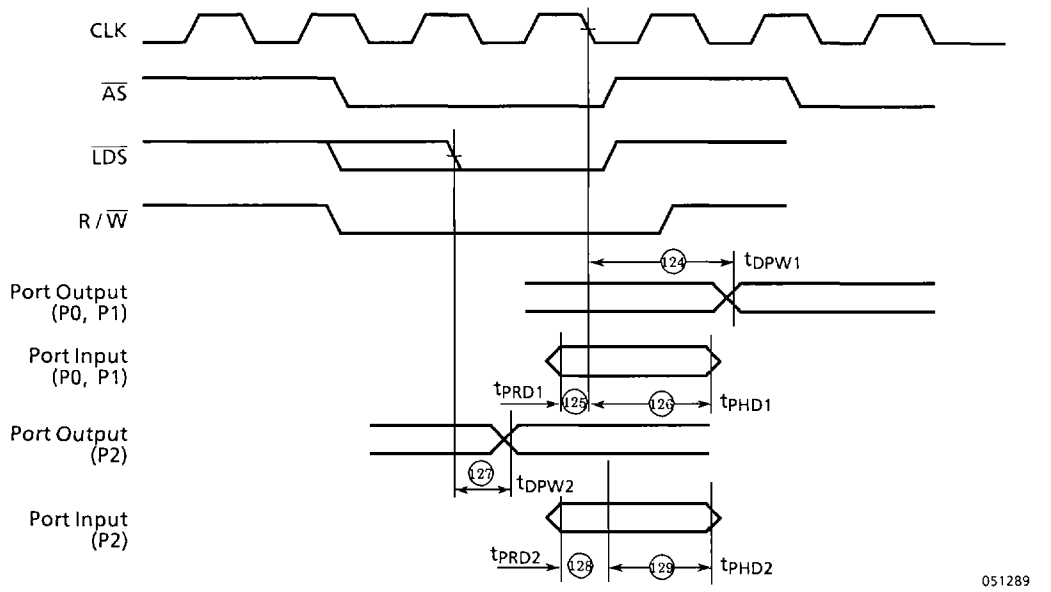


Figure 8.12 P0-2 Port Timming

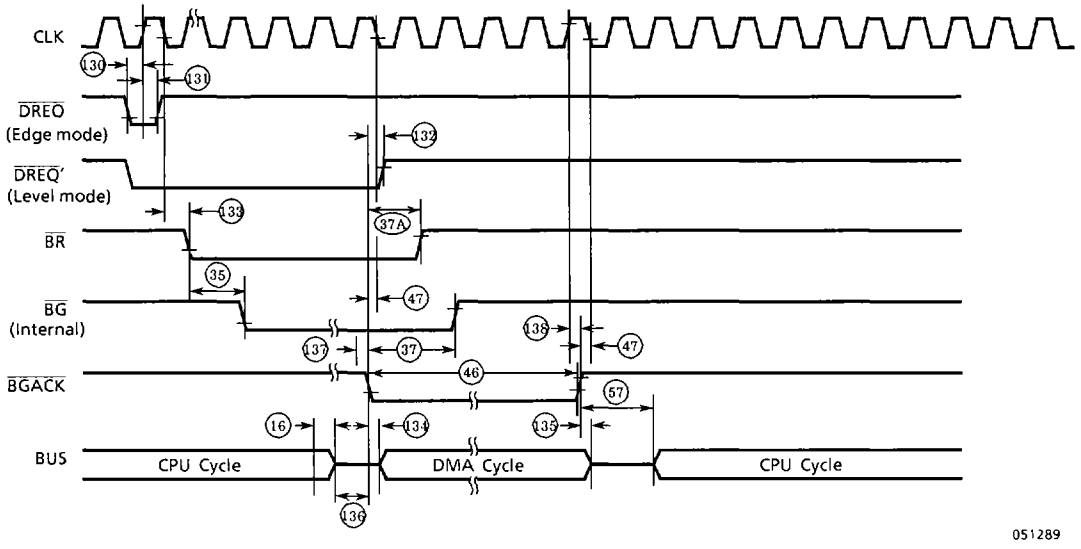


Figure 8.13 Active Bus Case Timming

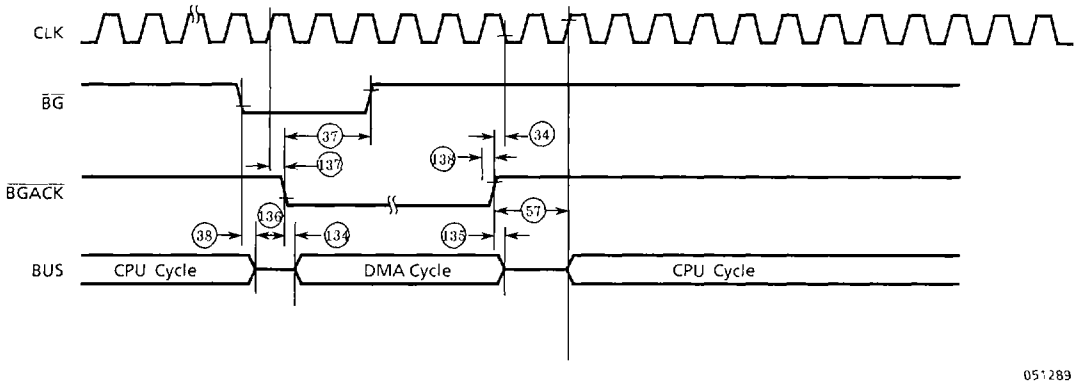


Figure 8.14 Idle Bus Case Timming

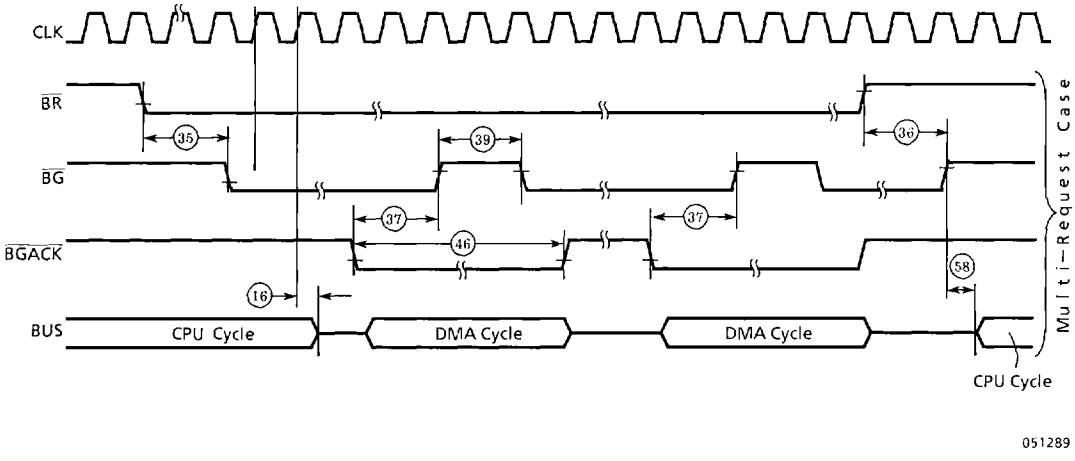


Figure 8.15 Multiple Bus Requests Case Timming

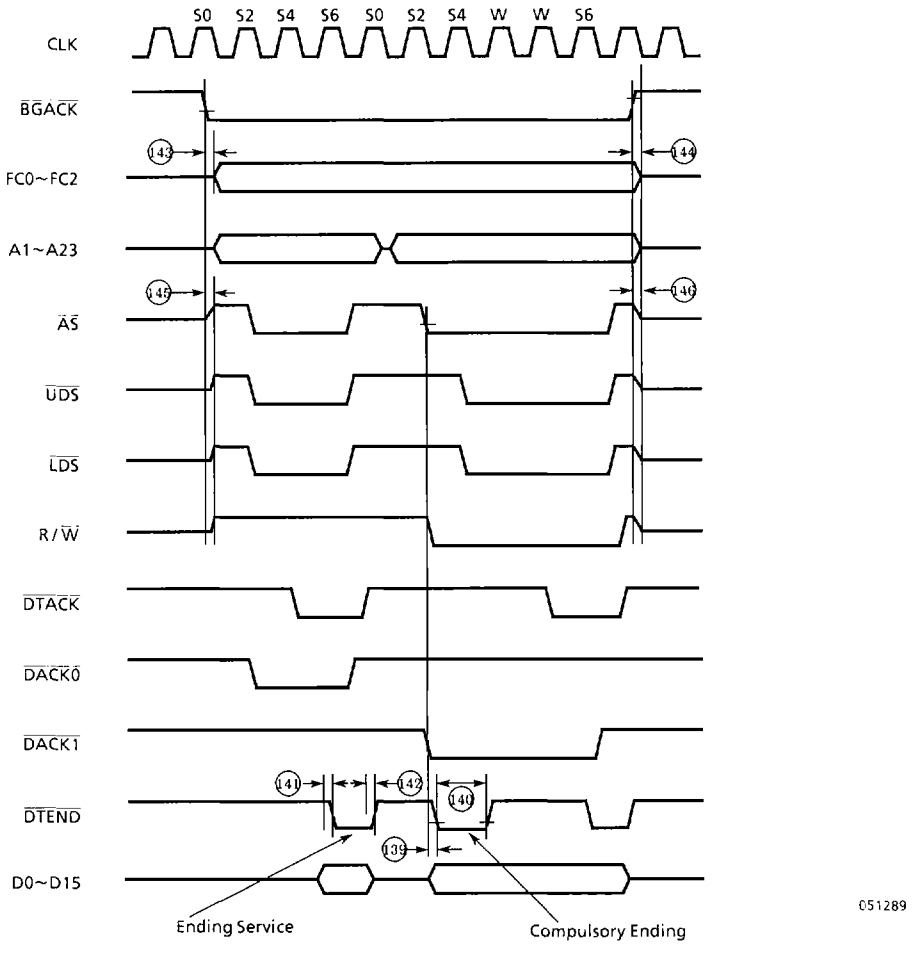

S0 S2 S4 S6 S0 S2 S4 W W S6
CLK
BGACK
143
144
FC0~FC2
A1~A23
145
146
AS
UDS
LDS
R/W
DTACK
DACK0
DACK1
141
142
140
DTEND
139
D0~D15
Ending Service
Compulsory Ending
051289

Figure 8.16