SANYO **SANYO Semiconductors**

DATA SHEET

CMOS IC

LC74950BG — Silicon gate 40/30MSPS Analog Display I/F LSI

Overview

The LC74950BG is an analog display I/F IC that converts analog video signals into equivalent digital video signals. It incorporates 3 channels of ADC and a PLL circuit.

Features

- Maximum sampling frequency: 40MSPS
- 8-bit output
- Supports self-clamp (bottom/center switching) and digital clamp
- Input signal: 1.0Vp-p maximum
- External clock input
- Low jitter PLL
- Power down mode
- Low power consumption
- Input format: Supports RGB and YCbCr
- Built-in I^2C bus interface

LSI Specifications

- Supply voltage Core: 1.5±10%
  I/O: 3.3V±0.3V (40MHz) or 2.4V to 3.6V (30MHz)
- Maximum operating frequency: 40MHz
- Package: FBGA96

Principal Applications

- Small-size monitors

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Functions & Overview

1. Input

All the inputs listed below can be connected to the analog ports. It is also possible to switch between the inputs of two systems and use the one selected.

YCbCr/YPbPr input (480I/576I, 480P/576P): Component input

RGB: RGB input

External clock supported

2. Output

Digital 8-bit/channel output

3. Clamp

Analog clamping and digital clamping supported

4. Gain

Digital gain adjustment

5. PLL circuit

This circuit can be used as the H lock or frequency-multiplied clock. It is also possible to use the PLL circuit and analog-digital converter (ADC) independently.

H lock PLL circuit: This makes it possible to generate a clock synchronized with the external H sync signal.

Frequency-multiplier PLL circuit: This makes it possible to generate clocks synchronized with an external clock.

6. External interface

I^2C: This supports the 100kHz mode. It is possible to select slave addresses by establishing pin settings.

Slave addresses: 0x98, 0x9A

7. PDOWN

Power-down of the whole system can be controlled using the PDOWN pin. Alternatively, the ADC, PLL and other circuits can be powered down separately using register settings. This makes it possible to limit the power as required.

Specifications

Absolute Maximum Ratings at Ta = 25°C, DV_{SS} = 0V, AV_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage (I/O)	$DV_{DD}33$ $AV_{DD}33$		-0.3 to +3.95	V
Maximum supply voltage (core)	$DV_{DD}15$ $AV_{DD}15$		-0.3 to +1.8	V
Digital input voltage	V_I		-0.3 to +5.5	V
	V_I (when in low voltage)		-0.3 to $DV_{DD}33$+0.3	V
Digital output voltage	V_O		-0.3 to $DV_{DD}33$+0.3	V
Operating temperature	Topr		-30 to +70	°C
Storage temperature	Tstg		-55 to +125	°C

Allowable Operating Ranges at Ta = -30 to +70°C

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Supply voltage (I/O)	$AV_{DD}33$		3.00	3.3	3.60	V
	$DV_{DD}33$	Max 40MHz	3.00	3.3	3.60	V
		Max 30MHz	2.40	3.3	3.60	V
Supply voltage (I/O)	$DV_{DD}15$ $AV_{DD}15$		1.35	1.5	1.65	V
Input voltage range (5V withstand voltage pin)	$V_{IN}5$		0		5.5	V
Input voltage range (non-5V withstand voltage pin)	V_{IN}		0		3.9	V

DC Characteristics at Ta = -30 to +70°C, $DV_{DD}33$ = 3.3V±0.3V (other than low-voltage support models),
$DV_{DD}15$= 1.5±10%

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Input high-level voltage	V_{IH}	CMOS level inputs (5V withstand voltage pin)	$0.8DV_{DD}33$		5.5	V
		CMOS level inputs (2.4V to 3.6V or non-5V withstand voltage pin)	$0.8DV_{DD}33$		$DV_{DD}33$	V
		CMOS level Schmitt inputs (5V withstand voltage pin)	2.0		5.5	V
		CMOS level Schmitt inputs (2.4V to 3.6V or non-5V withstand voltage pin)	$0.8DV_{DD}33$		$DV_{DD}33$	V
Input low-level voltage	V_{IL}	CMOS level inputs	0		$0.2V_{DD}33$	V
		CMOS level Schmitt inputs	0		$0.2V_{DD}33$	V
Input high-level current	I_{IH}	$V_I=DV_{DD}$			10	μA
		$V_I=DV_{DD}$, with pull-down resistance		100		μA
Input low-level current	I_{IL}	$V_I=V_{SS}$	-10			μA
Output high-level voltage	V_{OH}	CMOS (Pin G/I: I_{OH}=-4mA, Pin F: when set to -6mA)	DV_{DD}-0.6			V
Output low-level voltage	V_{OL}	CMOS			0.4	V
Output leak current	I_{OZ}	At output of high-impedance	-10		10	μA
Pull-down resistor	R_{DN}	3.0V to 3.6V		58		kΩ
		2.4V to 3.6V		70		kΩ
Dynamic supply current ($DV_{DD}33$)	I_{DDOP}	Outputs open, tck=27MHz natural image, Ta=25°C		13		mA
Dynamic supply current ($DV_{DD}15$)		tck=27MHz: natural image, Ta=25°C		7		mA
Dynamic supply current ($AV_{DD}33$)		tck=27MHz: natural image, Ta=25°C		52		mA
Dynamic supply current ($AV_{DD}15$)		tck=27MHz: natural image, Ta=25°C		0.1		mA
Static supply current: *1	I_{DDST}	Outputs open, $V_I=V_{SS}$, Ta=25°C		10		μA

*1: There is an input terminal which builds in pull down resistance. Please note that there is no guarantee about static consumption current depending on circuit composition.

A/D Convertor Characteristics at Ta = 25°C, DV_{SS} = 0V, AV_{SS} = 0V

Parameter	Symbol/pin	min	typ	max	Unit
ADC resolution				9	bit
Clock frequency	Fclk	5		40	MHz
SNR			48		dB
DNL			±0.5		LSB
INL			±1.0		LSB
External capacitance					
Analog input coupling capacitance	Analog video pin		0.1		μF
Top level reference fixed capacitance	VRTx pin		0.01		μF
Bottom level reference capacitance	VRBx pin		0.01		μF
Analog input frequency	FAIN			10	MHz
Analog input amplitude			1.0		V
ADC stabilization time (time required to restore from standby mode)				500	ms
PLL lock time				3	ms

Package Dimensions: FBGA96

unit: mm (typ)

3387
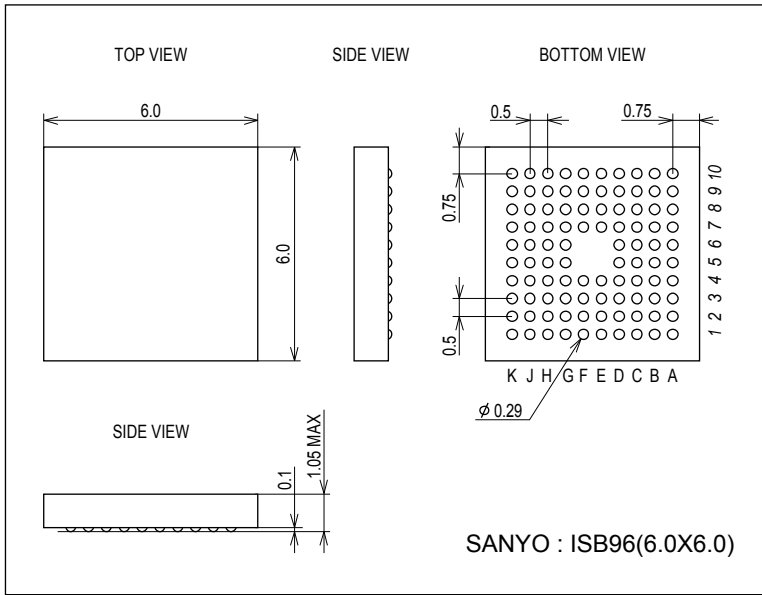
Pin Assignment

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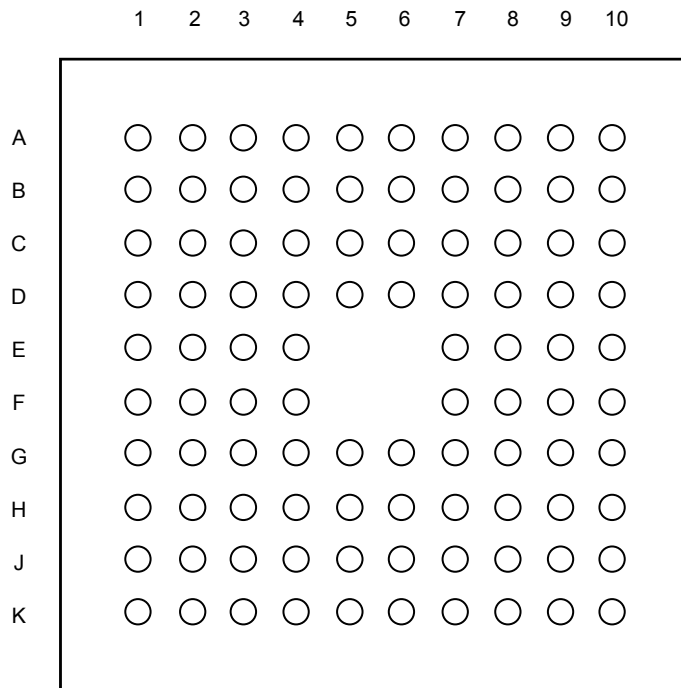
Top view

Block Diagram

LC74950BG
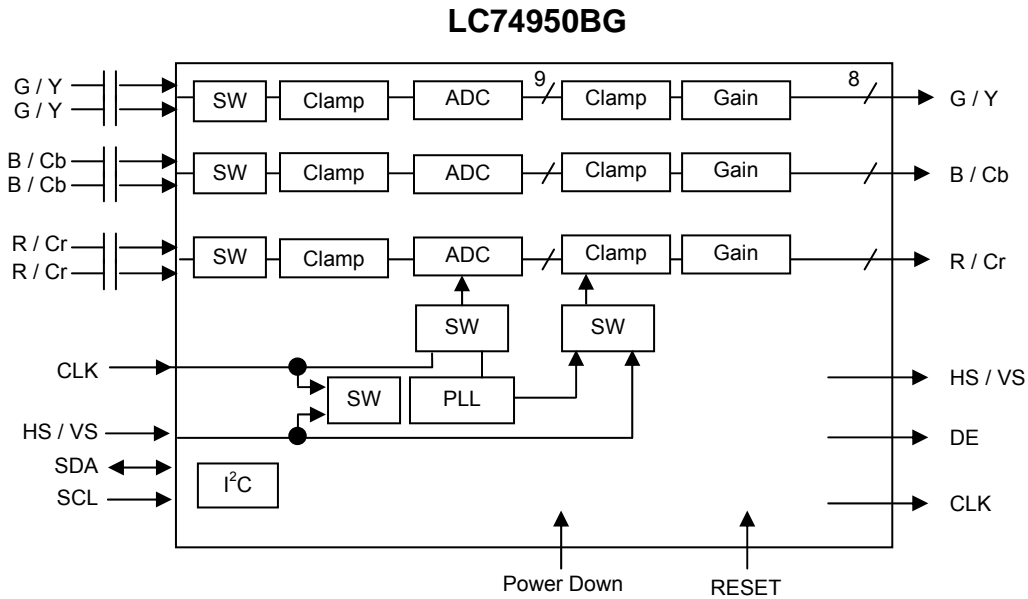
Pin Functions

Pin No.	Pin symbol	In/output format		Connecting destination		Remarks
		I/O	Format			
A1	ADC2AV$_{SS}$33	P		GND	Analog	It must be treated in the same way as an NC pin.
A2	CBOUT0	I/O	I	3.3V CMOS	Digital	Video signal output Cb or B (LSB)
A3	CBOUT2	I/O	I	3.3V CMOS	Digital	Video signal output Cb or B
A4	CBOUT4	I/O	I	3.3V CMOS	Digital	Video signal output Cb or B
A5	CBOUT6	I/O	I	3.3V CMOS	Digital	Video signal output Cb or B
A6	PDWN	I	B	3.3V CMOS	Digital	Power DOWN "L" Power DOWN
A7	AV$_{SS}$33_PLL	P		GND	Analog	
A8	CHRGPMP	O	A		Analog	Filter input
A9	AV$_{DD}$33_PLL	P		3.3V	Analog	PLL power supply
A10	DV$_{DD}$15	P		1.5V	Digital	
B1	VRT2	I	A		Analog	Top level reference voltage connection pin for ADC2
B2	ADC2AV$_{SS}$33	P		GND	Analog	
B3	CBOUT1	I/O	I	3.3V CMOS	Digital	Video signal output Cb or B
B4	CBOUT3	I/O	I	3.3V CMOS	Digital	Video signal output Cb or B
B5	CBOUT5	I/O	I	3.3V CMOS	Digital	Video signal output Cb or B
B6	CBOUT7	I/O	I	3.3V CMOS	Digital	Video signal output Cb or G (MSB)
B7	DV$_{SS}$	P		GND	Digital	
B8	AV$_{SS}$33_PLL	P		GND	Analog	
B9	DV$_{DD}$15	P		1.5V	Digital	It must be treated in the same way as an NC pin.
B10	HSIN	I	B	3.3V CMOS	Digital	Horizontal synchronizing signal
C1	CRIN1	I	A	to 1.0Vp-p	Analog	Analog CR or R input (ADC2)
C2	VRB2	I	A		Analog	Bottom level reference voltage connection pin for ADC2
C3	ADC2AV$_{DD}$33A	P		3.3V	Analog	
C4	DV$_{SS}$	P		GND	Digital	
C5	DV$_{SS}$	P		GND	Digital	
C6	DV$_{SS}$	P		GND	Digital	
C7	DV$_{DD}$15	P		1.5V	Digital	
C8	DV$_{DD}$15	P		1.5V	Digital	
C9	VSIN	I	B	3.3V CMOS	Digital	Vertical synchronizing signal
C10	RESET	I	B	3.3V CMOS	Digital	System reset "L" reset

LC74950BG

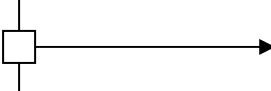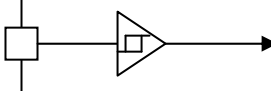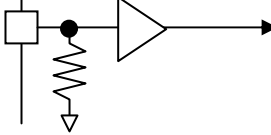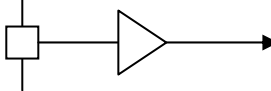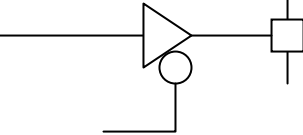| Pin No.	Pin symbol	In/output format		Connecting destination		Remarks
		I/O	Format			
D1	VRT1	I	A			Top level reference voltage connection pin for ADC1
D2	CRIN0	I	A	to 1.0Vp-p	Analog	Analog CR or R input (ADC2)
D3	ADC1AV$_{SS}$33	P		GND	Analog	
D4	DV$_{SS}$	P		GND	Digital	
D5	DV$_{SS}$	P		GND	Digital	
D6	DV$_{SS}$	P		GND	Digital	
D7	DV$_{DD}$15	P		1.5V	Digital	
D8	DV$_{DD}$15	P		1.5V	Digital	
D9	CLKOUT2	O	F	3.3V CMOS	Digital	CLKOUT1×2 output or PLL output
D10	CLKOUT1	O	F	3.3V CMOS	Digital	Datasynchronization clock output
E1	CBIN1	I	A	to 1.0Vp-p	Analog	Analog CB or B input (ADC1)
E2	VRB1	I	A			Bottom level reference voltage connection pin for ADC1
E3	ADC1AV$_{DD}$33A	P		3.3V	Analog	
E4	DV$_{SS}$	P		GND	Digital	
E7	DV$_{DD}$15	P		1.5V	Digital	
E8	I^{2}CSEL	I	C	3.3V CMOS		I^{2}C slave addresses L=0×98, H=0×9A
E9	SCL	I	D		Digital	
E10	COAST	I	B	3.3V CMOS	Digital	Connected to GND
F1	VRT0	I	A		Analog	Top level reference voltage connection pin for ADC0
F2	CBIN0	I	A	to 1.0Vp-p	Analog	Analog CB or B input (ADC1)
F3	ADC0AV$_{SS}$33	P		GND	Analog	
F4	DV$_{SS}$	P		GND	Digital	
F7	DV$_{DD}$15	P		1.5V	Digital	
F8	TEST	I	H	3.3V CMOS	Digital	Test pin (normally fixed low)
F9	SDA	I/O	G		Digital	
F10	CLKIN	I	D	3.3V CMOS	Digital	System clock (Must be connected to GND when not to be used)
G1	YGIN1	I	A	to 1.0Vp-p	Analog	Analog Y or G input (ADC0)
G2	VRB0	I	A		Analog	Bottom level reference voltage connection pin for ADC0
G3	ADC0AV$_{DD}$33	P		3.3V	Analog	
G4	SCANEN	I	H	3.3V CMOS	Digital	Test pin (normally, Lo)
G5	DV$_{DD}$33	P		3.3V	Digital	
G6	DV$_{DD}$33	P		3.3V	Digital	
G7	DV$_{DD}$33	P		3.3V	Digital	
G8	DV$_{DD}$33	P		3.3V	Digital	
G9	HSOUT	I/O	I	3.3V CMOS	Digital	Horizontal synchronizing signal
G10	VSOUT	I/O	I	3.3V CMOS	Digital	Vertical synchronizing signal
H1	ATB	O	A			Analog output for testing the ADC. It must be held open when not to be used.
H2	YGIN0	I	A	to 1.0Vp-p	Analog	Analog Y or G input (ADC0)
H3	AV$_{DD}$15_OSC	P		1.5V	Analog	Power supply for the RC oscillator
H4	SCANMOD	I	H	3.3V CMOS	Digital	Test pin (normally, Lo)
H5	DV$_{DD}$33	P		3.3V	Digital	
H6	DV$_{DD}$33	P		3.3V	Digital	
H7	DV$_{DD}$33	P		3.3V	Digital	
H8	DV$_{DD}$33	P		3.3V	Digital	
H9	CROUT7	I/O	I	3.3V CMOS	Digital	Video signal output Cr or R (MSB)
H10	DEOUT	I/O	I	3.3V CMOS	Digital	Data enable. It must be held open when not to be used.
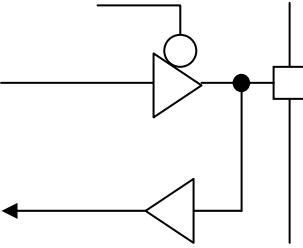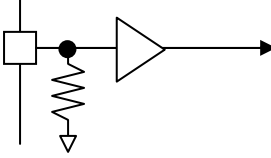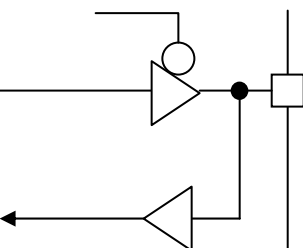
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Pin No.	Pin symbol	In/output format		Connecting destination		Remarks
		I/O	Format			
J1	SVO	O	A	to 1.0Vp-p	Analog	Test pin. It must be held open when not to be used.
J2	AV$_{SS}$_OSC	P		GND	Analog	
J3	YGOUT1	I/O	I	3.3V CMOS	Digital	Video signal output Y or G
J4	YGOUT7	I/O	I	3.3V CMOS	Digital	Video signal output Y or G (MSB)
J5	YGOUT4	I/O	I	3.3V CMOS	Digital	Video signal output Y or G
J6	CROUT0	I/O	I	3.3V CMOS		Video signal output Cr or R (LSB)
J7	CROUT3	I/O	I	3.3V CMOS	Digital	Video signal output Cr or R
J8	CROUT5	I/O	I	3.3V CMOS	Digital	Video signal output Cr or R
J9	DV$_{DD}$33	P		3.3V	Digital	
J10	CROUT6	I/O	I	3.3V CMOS	Digital	Video signal output Cr or R
K1	AV$_{SS}$_OSC	P		GND	Analog	It must be treated in the same way as an NC pin.
K2	YGOUT0	I/O	I	3.3V CMOS	Digital	Video signal output Y or G (LSB)
K3	YGOUT2	I/O	I	3.3V CMOS	Digital	Video signal output Y or G
K4	YGOUT3	I/O	I	3.3V CMOS	Digital	Video signal output Y or G
K5	YGOUT5	I/O	I	3.3V CMOS	Digital	Video signal output Y or G
K6	YGOUT6	I/O	I	3.3V CMOS	Digital	Video signal output Y or G
K7	CROUT1	I/O	I	3.3V CMOS		Video signal output Cr or R
K8	CROUT2	I/O	I	3.3V CMOS	Digital	Video signal output Cr or R
K9	CROUT4	I/O	I	3.3V CMOS	Digital	Video signal output Cr or R
K10	DV$_{DD}$33	P		3.3V	Digital	It must be treated in the same way as an NC pin.

Pin No.	Pin symbol	In/output format		Connecting destination		Remarks
		I/O	Format			

Pin Type

| In/Output form	Function	Equivalent circuit	Application Terminal
A	Analog input/output		CHRGPMP, CRIN0, CRIN1, VRT2, VRB2, CBIN0, CBIN1, VRT1, VRB1, YGIN0, YGIN1, VRT0, VRB0, SVO, ATB
B	5V withstand Schmitt trigger CMOS input *		HSIN, PDWN, VSIN, COAST, RESET
C	5V withstand CMOS input with built-in pull-down resistor *		I²CSEL
D	5V withstand CMOS input *		CLKIN, SCL
F	12mA switching 3-STATE drive CMOS output		CKOUT1, CKOUT2
G	8mA 3-STATE drive CMOS input/output * (5V withstand)		SDA
H	CMOS input with built-in pull-down resistor		TEST, SCANEN, SCANMOD
I	8mA 3-STATE drive CMOS input/output		HSOUT, VSOUT, DEOUT, CROUT0, CROUT1, CROUT2, CROUT3, CROUT4, CROUT5, CROUT6, CROUT7, CBOUT4, CBOUT5, CBOUT6, CBOUT7, CBOUT0, CBOUT1, CBOUT2, CBOUT3, YGOUT0, YGOUT1, YGOUT2, YGOUT3, YGOUT4, YGOUT5, YGOUT6, YGOUT7

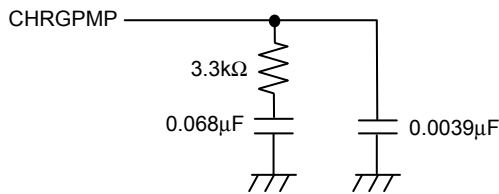*: 5V Tolerant

Pin Connection

1) ADC and its peripherals

VRTx   VRBx

0.1μF

10μF   0.1μF   0.1μF   10μF
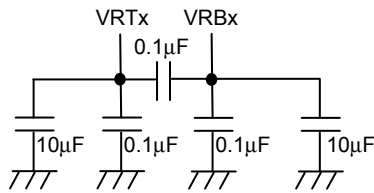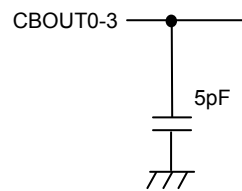
VRTx: VRT0, VRT1, VRT2
VRBx: VRB0, VRB1, VRB2

0.1μF

xINx

Terminal
resistor
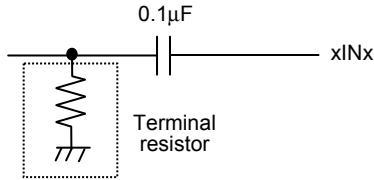
YGIN0, YGIN1
CRIN0, CRIN1
CBIN0, CBIN1

2) PLL and its pereipherals

CHRGPMP

3.3kΩ

0.068μF   0.0039μF

3) Output pin (recommended)

CBOUT0-3

5pF

4) Power supplies

The analog A** and digital D** power supplies must be supplied separately without fail. In addition, the power supply for the PLL circuit must also be provided separately as it will affect the jitter characteristics of the PLL circuit. For ADC power supply, it is desirable to provide separate power for eachof the ADC channel.

$AV_{DD}33\_PLL$: Must be separated by L components, etc.
$ADC2AV_{DD}33A$: Separating by L components, etc. recommended
$ADC1AV_{DD}33A$: Separating by L components, etc. recommended
$ADC0AV_{DD}33A$: Separating by L components, etc. recommended

5) Unused pin treatment

YGIN0, 1/CBIN0, 1/CRIN0, 1: Open
PDWN: Pull up
CHRGPMP: Open (when PLL is not in use)
***OUT* (e.g., YGOUT0): Open
HSIN/VSIN: Must always be configured for input.
RESET: Must always be configured for input.
COAST: Must be connected to DV_{SS}.
TEST, SCANEN, SCANMOD: DV_{SS}
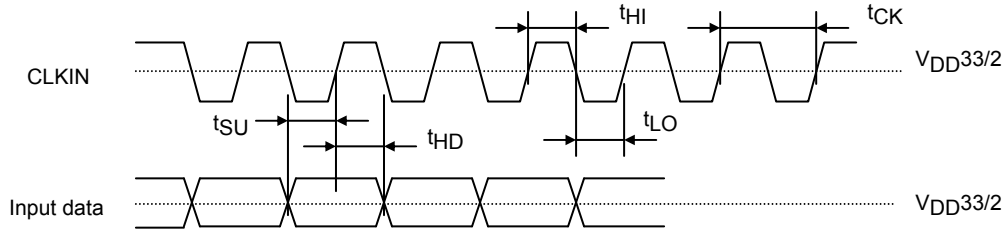CLKIN: DV_{SS}
HSOUT, VSOUT, DEOUT: Open
SVO, ATB: Open
* The specified voltage of power must be applied to each of the power supply pin even if it is not to be used
  (PLL is not to be used, for example).

I/O Data Timing

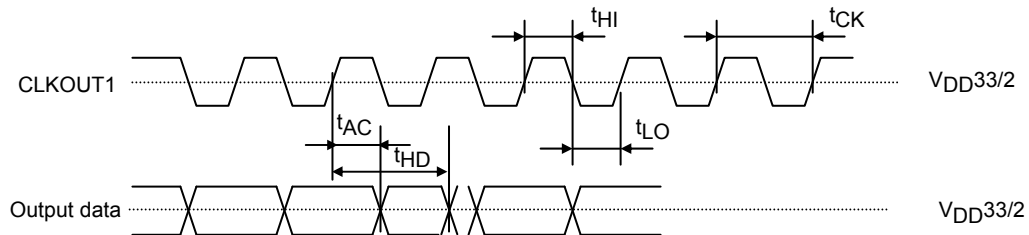(1) Input data timing

Pin name	Parameter	Symbol	min	typ	max	unit
CLKIN	Clock cycle	t_{CK}	25			ns
	Duty			50		%
HSIN, VSIN	Input data setup time (DV$_{DD}$33=3.0 to 3.6V)	t_{SU}	3.0			ns
	Input data setup time (DV$_{DD}$33=2.4 to 3.6V)	t_{SU}	3.0			ns
	Input data hold time (DV$_{DD}$33=3.0 to 3.6V)	t_{HD}	3.0			ns
	Input data hold time (DV$_{DD}$33=2.4 to 3.6V)	t_{HD}	3.0			ns

*: The recommended duty cycle of input clock is 50%

(2) Output data timing

Pin name	Parameter	Symbol	min	typ	max	unit
CLKOUT1	Clock cycle	t_{CK}	25			ns
	Duty			50		%
YGOUT*, CBOUT*, CROUT*, HSOUT ,VSOUT, DEOUT	Output data delay time (3.0 to 3.6V)	t_{AC}	0		2.0	ns
	Output data delay time (2.4 to 3.6V)	t_{AC}	0		3.0	ns
	Output data hold time (3.0 to 3.6V)	t_{HD}	3.0			ns
	Output data hold time (2.4 to 3.6V)	t_{HD}	3.0			ns

* When CLKOUT1 is set to the forward rotation output.

Timing Chart
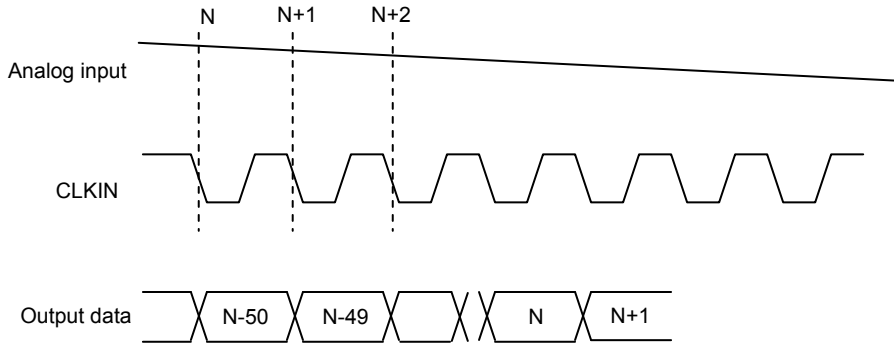
Note: For the initial setting of the registers

Details of the functions

1. Selection of input pins

Registers related to the selection of input pins

Name	Functions	Sub address	bit width
AINSEL	Video input select control Analog video input select 0: YGIN0/CBIN0/CRIN0 1: YGIN1/CBIN1/CRIN1	0x22	1

- Video input selector function
  The video input signal used for actual processing can be selected out of the two systems of video input.
  AINSEL=0: YGIN0/CBIN0/CRIN0
  AINSEL=1: YGIN1/CBIN1/CRIN1

2. Input format

Registers related to the selection of the input format

Name	Functions	Sub address	bit width
SELYCRGB	This register switches between the YCbCr input and RGB input. 0: YCbCr, 1: RGB	0x14	1
SYNCON	For YCbCr input, this register, by cutting off the digitally clamped sync component of the Y video signal, sets the applicable gain adjustment function to ON or OFF. This must be set to 0 for the RGB input (SELYCRGB=1). 0: ON, 1: OFF	0x1B	1

All the inputs listed below can be connected to the analog ports. It is also possible to switch between the inputs of two systems and use the one selected.
YCbCr/YPbPr input (480I/576I, 480P/576P): Component input
RGB: RGB input

3. Operating modes

Register related to the selection of operating mode

Name	Functions	Sub address	bit width
CLKSEL	Operating mode selection 000: External clock mode (PLL not used) 001: External clock mode (PLL used) 010: H lock PLL mode 011: Panel PLL mode <1> 100: Panel PLL mode <2>	0x00	3

LC74950BG

1) External clock mode (PLL not used: CLKOUT1=CLKIN/2, CLKOUT2=CLKIN)
   Example: Component input (NTSC) (down sample)
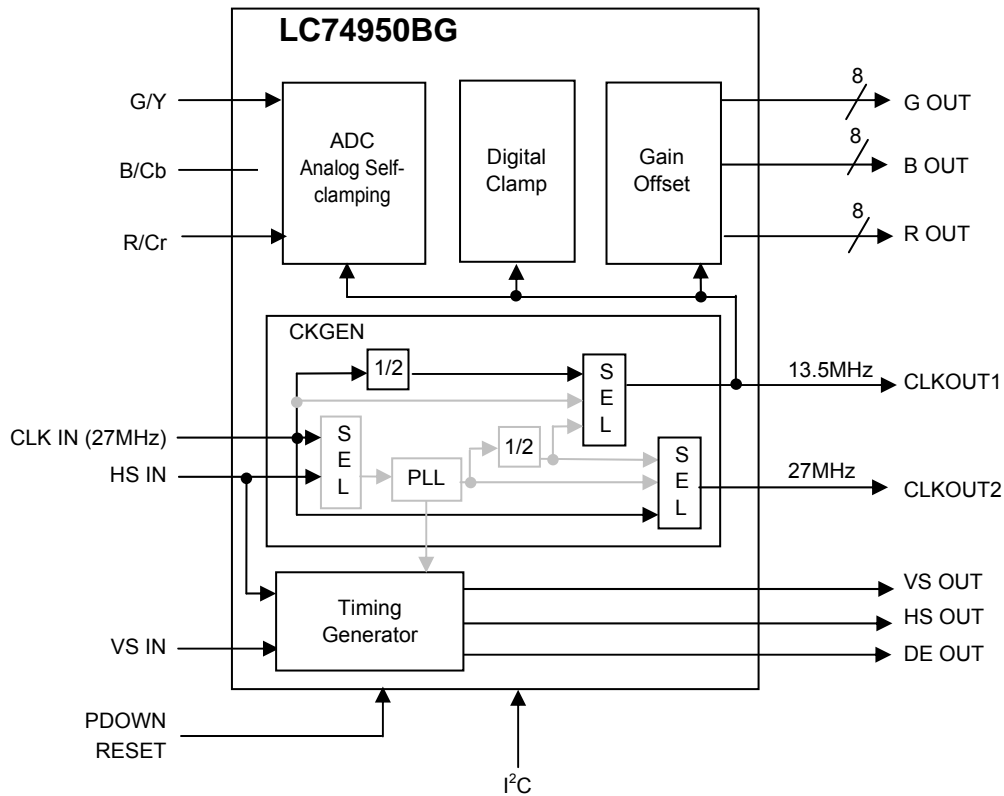
2) External clock mode (PLL used: CLKOUT1=CLKIN, CLKOUT2=CLKIN*2)
   Example: Component input (NTSC) (2× clock generation)

3) H-lock PLL mode (PLL used: CLKOUT1=HS/Divide, CLKOUT2=CLKOUT1*2)
   Example: Component input (NTSC) (2× clock generation)
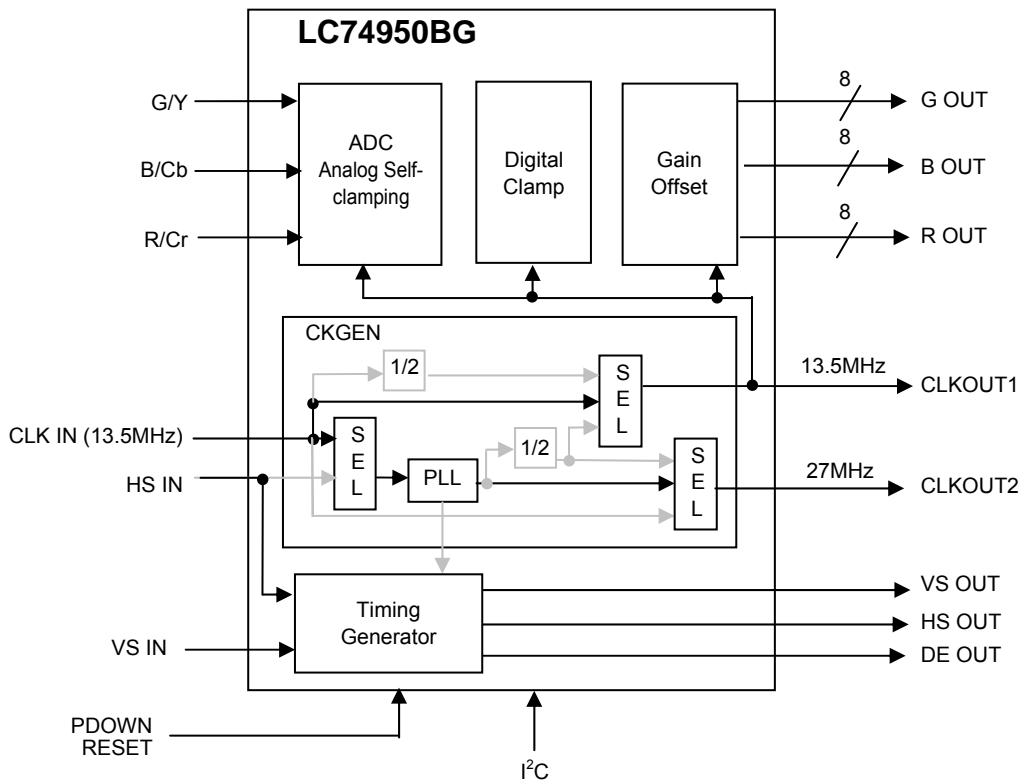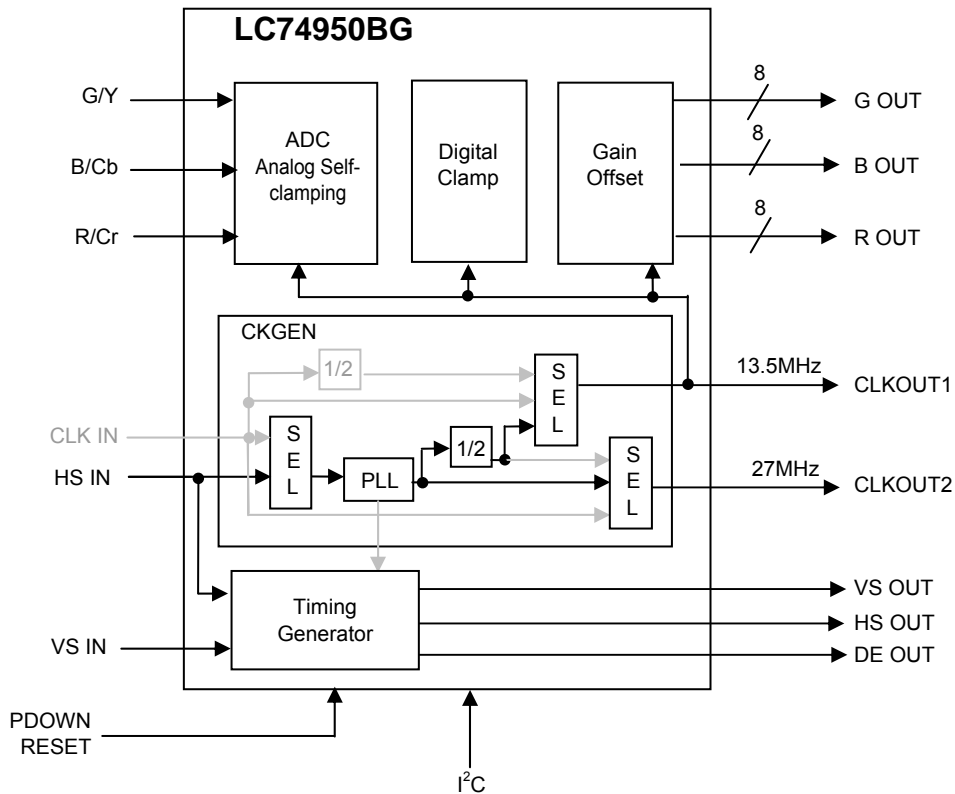
LC74950BG

G/Y

B/Cb

R/Cr

ADC
Analog Self-
clamping

Digital
Clamp

Gain
Offset

8 → G OUT
8 → B OUT
8 → R OUT

CKGEN

1/2

S E L

CLK IN

HS IN

S E L

PLL

1/2

S E L

S E L

13.5MHz CLKOUT1

27MHz CLKOUT2

Timing
Generator

VS IN

VS OUT
HS OUT
DE OUT

PDOWN
RESET

I²C

4) ADC/PLL independent mode <1>
   (External clock input, PLL configured independently: CLKOUT1=CLKIN/2, CLKOUT2=CLKIN/In-Divide*Out-
   Divide)
   Example: Component (ADC down sample), PLL: Generation of separate system clock

LC74950BG

G/Y

B/Cb

R/Cr

ADC
Analog Self-
clamping

Digital
Clamp

Gain
Offset

8 → G OUT
8 → B OUT
8 → R OUT

CKGEN

1/2

S E L

CLK IN (27MHz)

HS IN

S E L

PLL

1/2

S E L

S E L

13.5MHz CLKOUT1

33MHz CLKOUT2

Timing
Generator

VS IN

VS OUT
HS OUT
DE OUT

PDOWN
RESET

I²C
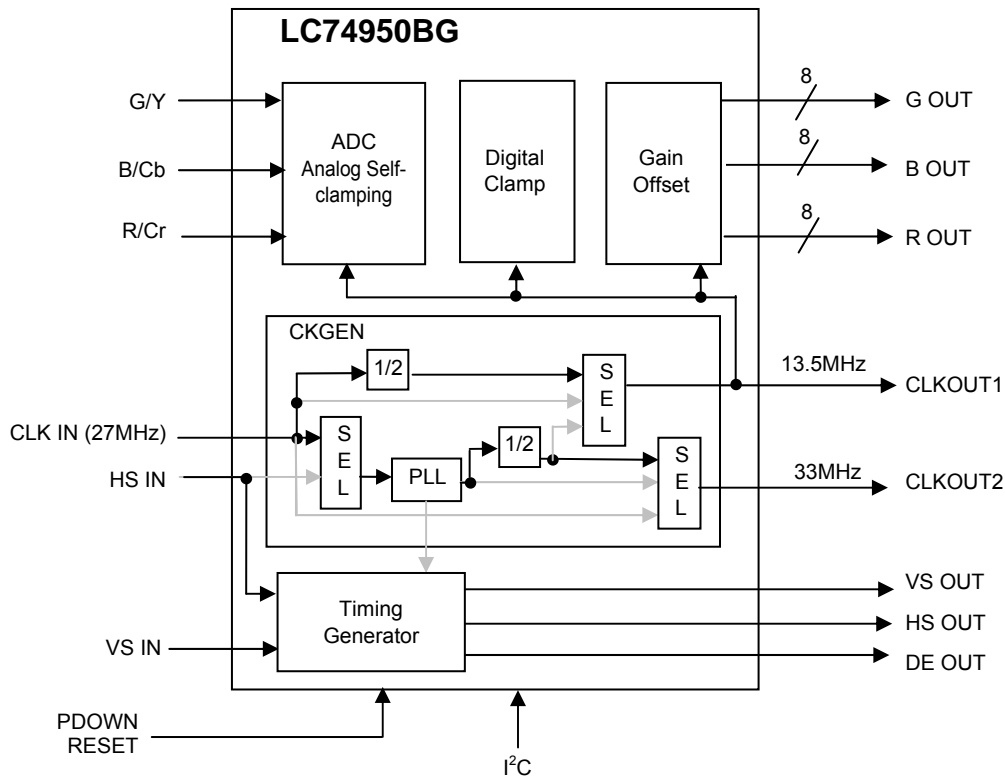
5) ADC/PLL independent mode <2>

(External clock input, PLL configured separately: CLKOUT1=CLKIN, CLKOUT2=CLKIN/In-Divide*Out-Divide)

Example: Component (ADC down sample), PLL: Generation of separate system clock

4. Clock system

1) Clock system diagram
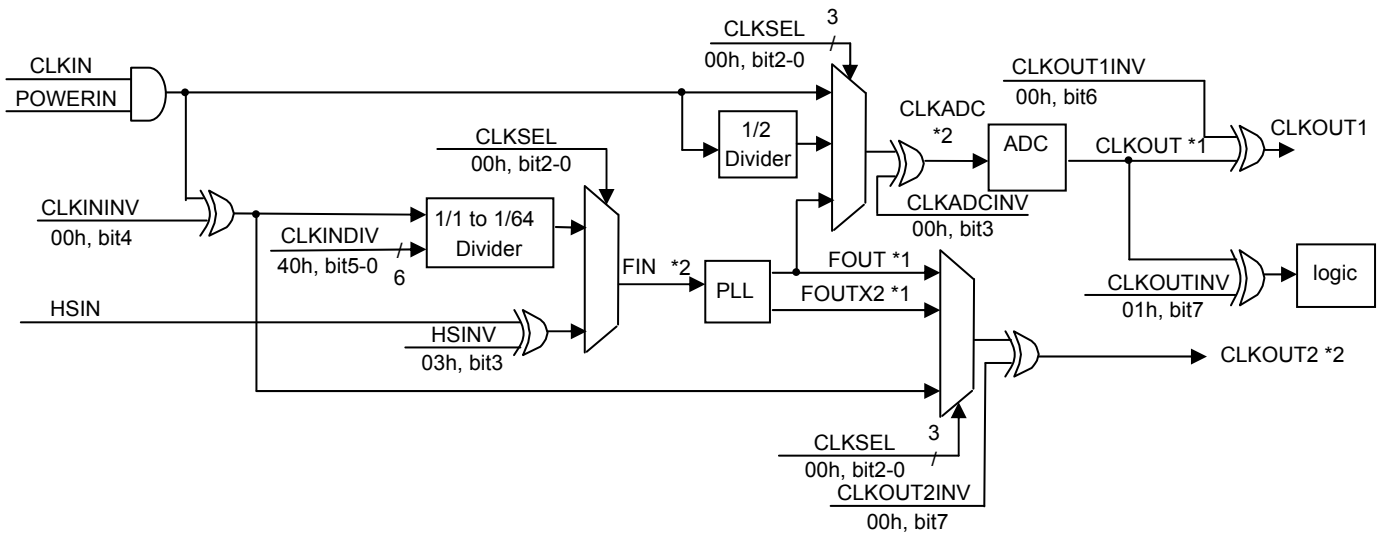
*1 Explanation of signals

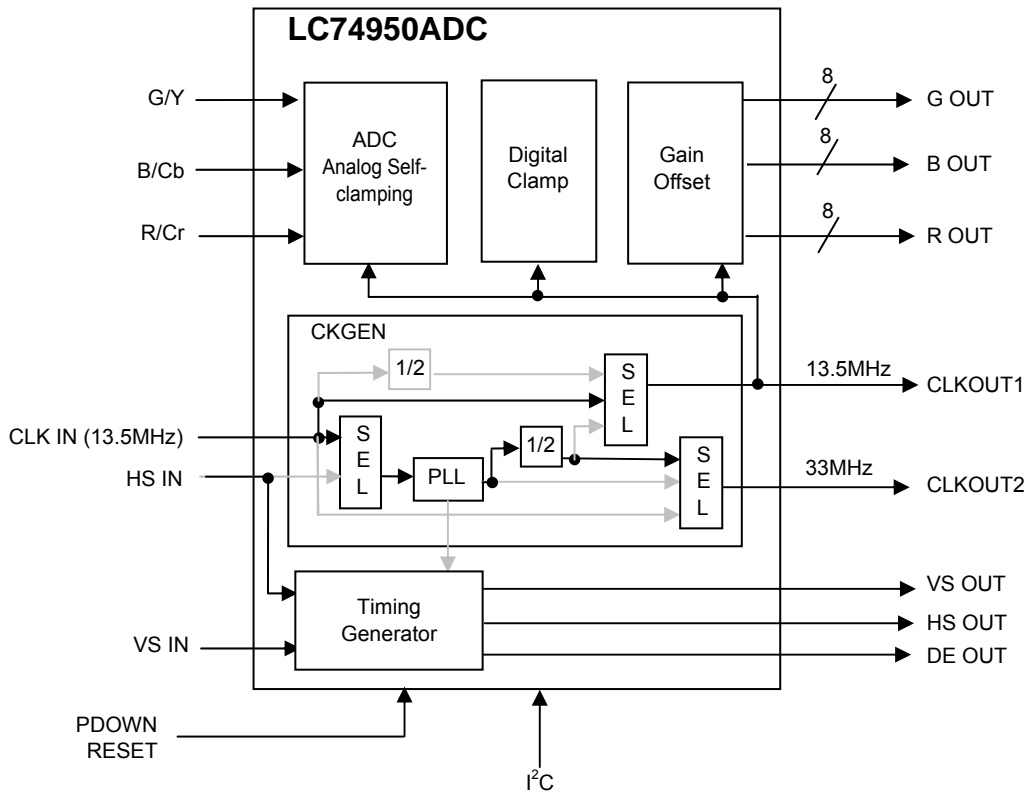FOUT: A clock generated in the PLL circuit and synchronized with the reference signal (FIN). The frequency of FIN and PLL divider value (HPLDIV, 28h-29h, bits 15-0) determine the frequency of FOUT.

FOUTX2: A clock generated in the PLL circuit and synchronized with the reference signal (FIN). The frequency of FOUTX2 is two times of the frequency of FOUT.

CLKOUT: A clock generated in the ADC. To output the clock it is necessary to adjust the phase of the sampling clock (CLKADC) in order that the rising edge of the clock does not occur near the change point of the ADC sampled data.

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Registers related to the control of clock

Name	Functions	Sub address	bit width
CLKININV	This register controls the inversion of CLKIN when the CLKIN input is used as a reference clock to PLL. 0: Uses CLKIN in its original form 1: Uses CLKIN in its inverted form	0x00	2
HSINV	This register controls the inversion of HSIN input. The HSIN must be used in its inverted form when the polarity of HSIN input is negative. 0: Original form (when HSIN is positive) 1: Inverted form (when HSIN is negative)	0x02	1
CLKINDIV	This register sets the frequency division ratio of CLKIN to an arbitrary value (1/1 to1/64) when the CLKIN is used as a reference clock to PLL. 1/(CLKINDIV[5:0]+1) division	0x40	6
CLKSEL	This register selects the operating mode. 000: (External clock mode (PLL not used) 001: (External clock mode (PLL used) 010: H-lock PLL mode 011: Panel PLL mode <1> 100: Panel PLL mode <2>	0x00	3
CLKADCINV	This register controls the inversion of the ADC sampling clock (CLKADC). 0: Uses CLKADC in its original form 1: Uses CLKADC in its inverted form	0x00	1
CLKOUTINV	This register controls the inversion of the ADC-generated clock. (CLKOUT). 0: Uses CLKOUT in its original form 1: Uses CLKOUT in its inverted form	0x01	1
CLKOUT1INV	This register controls the inversion of CLKOUT (video clock output). 0: Original form 1: Inverted form	0x00	1
CLKOUT2INV	This register controls the inversion of CLKOUT2 (panel clock output). 0: Original form 1: Inverted form	0x00	1

*2 Clock control register (CLKSEL, 00h, bits 2-0) specifications

| CLKSEL (bit2-0)	CLKADC*3 (ADC sampling clock)	FIN (PLL reference)	CLKOUT2 (Clock output)	Remarks
000	CLKIN/2 (13.5MHz)	L fixed (PLL not used)	CLKIN(27MHz)	External clock mode (PLL not used)
001	FOUT (PLL output)	CLKIN *4	FOUTX2 (PLL output X2)	External clock mode (PLL used)
010	FOUT (PLL output)	HSIN *5	FOUTX2 (PLL output X2)	H-lock PLL mode
011	CLKIN/2	CLKIN *4	FOUT (PLL output)	Panel PLL mode <1>
100	CLKIN	CLKIN *4	FOUT (PLL output)	Panel PLL mode <2>

*3: Register CLKADCINV (00h, bit 3) allows for clock inversion.

*4: Register CLKINDIV (40h, bits 5-0) allows for division of clock frequency (1/1 to 1/64).

*5: Register HSINV (03h, bit 3) allows for HSIN inversion.
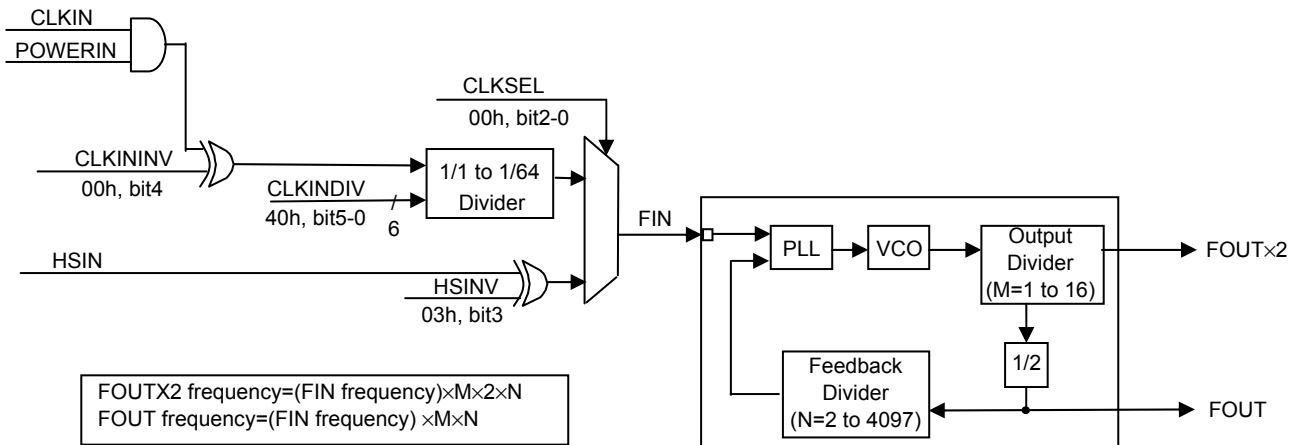
2) PLL circuit

FOUTX2 frequency=(FIN frequency)×M×2×N
FOUT frequency=(FIN frequency) ×M×N

This circuit can be used as the H lock or frequency-multiplied clock. It is also possible to use the PLL circuit and analog-digital converter (ADC) independently.

H lock PLL circuit: This makes it possible to generate a clock that is synchronized with the external H sync signal.

Frequency-multiplier PLL circuit: This makes it possible to generate clocks that are synchronized with an external clock.

Registers related to the setting of PLL circuit

Name	Functions	Sub address	bit width
CLKININV	This register controls the inversion of CLKIN when the CLKIN input is used as a reference clock to PLL. 0: Uses CLKIN in its original form 1: Uses CLKIN in its inverted form	0x00	2
HSINV	This register controls the inversion of HSIN input. The HSIN must be used in its inverted form when the polarity of HSIN input is negative. 0: Original form (when HSIN is positive) 1: Inverted form (when HSIN is negative)	0x02	1
CLKINDIV	This register sets the frequency division ratio of CLKIN to an arbitrary value (1/1 to 1/64) when the CLKIN is used as a reference clock to PLL. 1/(CLKINDIV[5:0] 1) division	0x40	6
CLKSEL	This register selects the PLL reference input. 000: L fixed (PLL not used) 001: External clock input (CLKIN) 010: External Hsync input (HSIN) 011: External clock input (CLKIN) 100: External clock input (CLKIN)	0x00	3
HPLDIV15-12	This register sets the output divider (M-1, NTSC, 480i=3).	0x28	4
HPLDIV11-0	This register sets the feedback divider (N-2, NTSC, 480i=856). H-lock PLL output frequency (1x)=Hsync frequency×N H-lock PLL output frequency (2x)=Hsync frequency×N×2 * After changing the setting, an interval of 3.0ms is required for the H-lock PLL to get stabilized.	0x28 0x29	12

Continued from preceding page.

Name	Functions	Sub address	bit width
PLLGAIN	This register switches the setting of Fmin, Fmax, and Gain of the H-lock PLL VCO. 000: Fmin=60MHz, Fmax=240MHz, Gain=120MHz/V←Standard setting 001: Fmin=Standard, Fmax=Standard-20%, Gain=Standard-22.5% 010: Fmin=Standard-20%, Fmax=Standard, Gain=Standard+2.5% 011: Fmin=Standard-20%, Fmax=Standard-20%, Gain=Standard-20.0% 100: Fmin=Standard+20%, Fmax=Standard+10%, Gain=Standard+8.75% 101: Fmin=Standard+20%, Fmax=Standard-10%, Gain=Standard-13.75% 110: Fmin=Standard, Fmax=Standard+10%, Gain=Standard+11.25% 111: Fmin=Standard, Fmax=Standard-10%, Gain=Standard-11.25% * After changing the setting, an interval of 3.0ms is required for the H-lock PLL to get stabilized.	0x27	3
PLLCTL2	H-lock PLL power down mode 0: Normal operation 1: H-lock PLL power OFF	0x27	1
PLLCTL1	H-lock PLL Normal Mode FOUT Disable 0: Normal operation 1: H-lock PLL output= L fixed	0x27	1
CPIS_COAST CPIS_ORG	These registers set the PLL charge pump constant current (make sure that CPIS_COAST=CPIS_ORG) 0000: 40μA 0001: 60μA 0010: 120μA 0011: 180μA 0100: 200μA 0110: 280μA 0101: 300μA 1000: 360μA 0111: 420μA 1010: 440μA ←Standard setting 1100: 520μA 1001: 540μA 1110: 600μA 1011: 660μA 1101: 780μA 1111: 900μA * After changing the setting, an interval of 3.0ms is required for the H-lock PLL to get stabilized.	0x2A	4

PLL setting example (when using as H-lock PLL)

|	Ref [kHz]	CLKSEL [2:0]	PLLDIV 15-12	PLLDIV 11-0	FVCO* [MHz]	FOUTX2 [MHz]	FOUT [MHz]	CPIS [3:0]	PLLGAIN [2:0]
NTSC	15.734	2h	3h	6B2h	216	(54)	27	Ch	0h
NTSC	15.734	2h	7h	358h	216	27	13.5	Ch	0h
PAL	15.630	2h	3h	6BEh	216	(54)	27	Ch	0h
PAL	15.630	2h	7h	35Eh	216	27	13.5	Ch	0h
PAL-N	15.630	2h	7h	35Eh	216	27	13.5	Ch	0h
PAL-M	15.734	2h	7h	358h	216	27	13.5	Ch	0h
QVGA	15.70	2h	Fh	1A6h	213	13.3	6.68	Ch	0h
VGA	31.5	2h	3h	31Eh	201	(50.4)	25.2	Ch	0h
WVGA	31.0	2h	3h	41Eh	262	(65.4)	32.7	Dh	0h

*20MHz < FVCO < 340MHz

5. Timing control

1) DEOUT (enable output) setting

Registers related to the setting of enable

Name	Functions	Sub address	bit width
HBLKS	This register specifies the 1H start position of DEOUT in dot units.	0x04	12
	Set value smaller than HBLKE.	0x05	
HBLKE	This register specifies the 1H end position of DEOUT in dot units.	0x04	12
	Set the value that is larger than HBLKS and does not overlap the next Hsync.	0x06	
VBLKS	This register specifies the 1V start position of DEOUT in line units.	0x07	11
	Set the value smaller than VBLKE.	0x08	
VBLKE	This register specifies the 1V end position of DEOUT in line units.	0x07	11
	Set the value that is larger than VBLKS and does not overlap the next Vsync.	0x09	

• Setting of horizontal enable
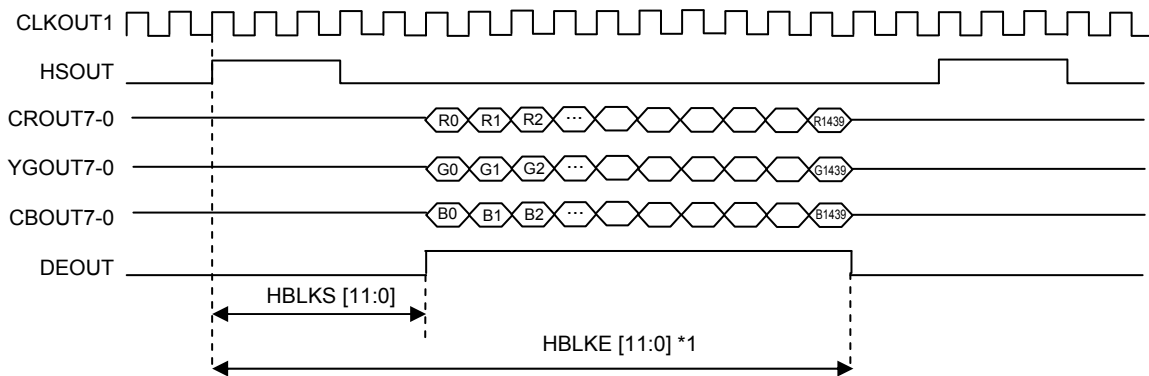
*1: DEOUT is forcibly disabled at the leading edge of the next HSOUT even if HBLKE[11:0] is set with a value larger than the total pixel count of 1H.

• Setting of vertical enable
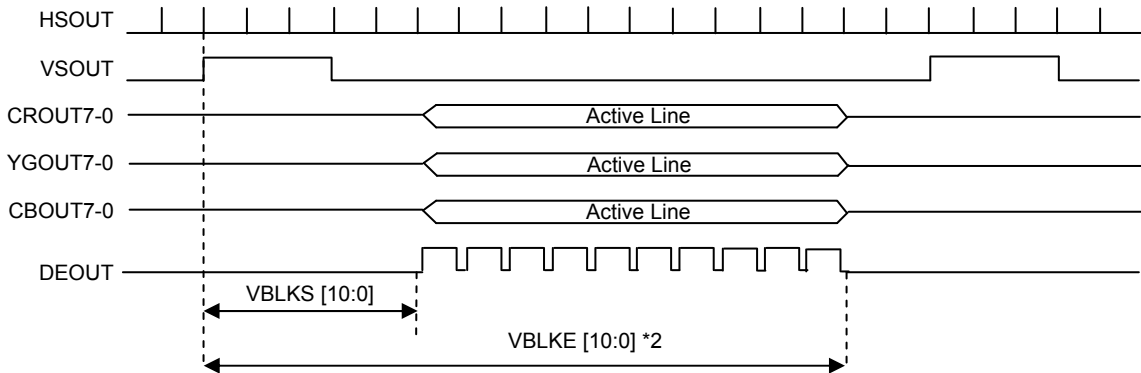
*2: DEOUT is forced disabled at the leading edge of the next VSOUT even if VBLKE[10:0] is set with a value larger than the total line count of 1V.

2) SYNC width adjustment (H-lock PLL mode only) of horizontal sync output (HSOUT)

Registers related to SYNC width adjustment of HSOUT

Name	Functions	Sub address	bit width
HSPLLSEL	This register selects the horizontal sync signal (SHOUT) in the H-lock PLL mode. 0: HSIN 1: This is the signal that is fed back to the phase detector after dividing the VCO output of the PLL. *: SYNC width adjustment for HSOUT must be turned on when HSPLLSEL is set to 1.	0x01	1
CORREN	This register turns on and off the SYNC width adjustment for HSOUT. 0: OFF, 1: ON	0x27	1
CORRHSS	SYNC width adjustment register for HSOUT (to be described below)	0x2B 0x2C	12
CORRHSE	SYNC width adjustment register for HSOUT (to be described below)	0x2B 0x2D	12

When "1" is set for HSPLLSEL in the H lock PLL mode, the horizontal sync output signal is not HSIN but the signal that is fed back to the phase detector after dividing the VCO output of the PLL. The duty ratio of this signal is 50%, which means when it is to be used as the horizontal sync signal, the sync width must be determined. Furthermore, if "0" is set for HSPLLSEL, the horizontal sync input (HSIN) signal can be output in its original form even in the H lock PLL mode.
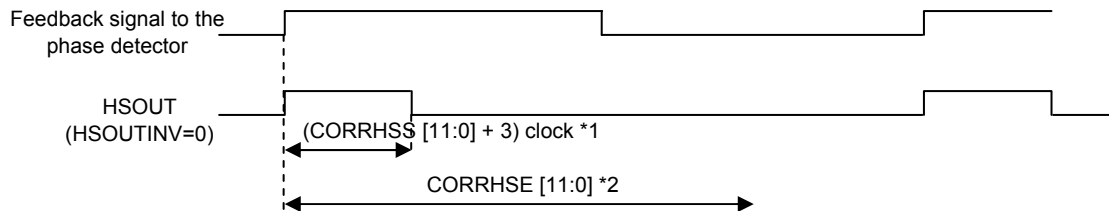
*1: Clock is expressed in units of CLKOUT1.
*2: A value equivalent to about three-fourths of one HSOUT period (640 or so with the NTSC system) must be set as the CORRHSE[11:0] value.

3) Offset adjustment of video output

Registers related to video output offset adjustment

Name	Functions	Sub address	bit width
ASYG	This register adjusts the offset for the Y/G video signal. It is used when the timing between the video signal and sync signals is off. The Y/G video signal can be shifted by an amount equivalent to (ASYG + 1) locks.	0x01	3
ASCRR	This register adjusts the offset for the CR/R video signal. It is used when the timing between the video signal and sync signals is off. The CR/R video signal can be shifted by an amount equivalent to (ASCRR + 1) clocks.	0x02	3
ASCBB	This register adjusts the offset for the CB/B video signal. It is used when the timing between the video signal and sync signals is off. The CB/B video signal can be shifted by an amount equivalent to (ASVBBYG + 1) clocks.	0x02	3
ASVS	This register adjusts the offset for the VSOUT video signal. It is used when the timing between the video signal and sync signals is off. The vertical sync signal can be shifted by an amount equivalent to (ASVS + 1) clocks.	0x03	3
ASHS	This register adjusts the offset for the HSOUT. It is used when the timing between the video signal and sync signals is off. The horizontal sync signal can be shifted by an amount equivalent to (ASHS + 1) clocks.	0x03	3

• Offset adjustment method

If the following fluctuations are present between the video outputs when ASYG[2:0] = 000b, ASCRR[2:0] = 000b and ASCBB[2:0] = 000b:
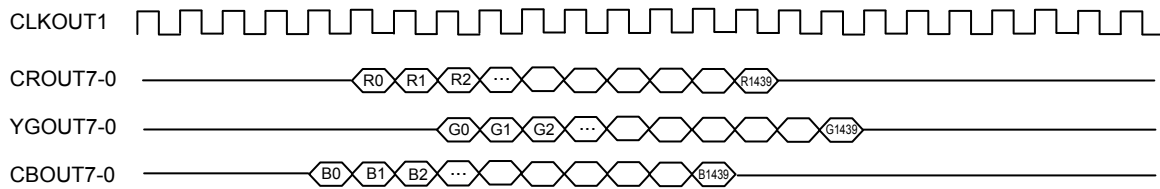
Then, by setting ASYG[2:0] = 010b, ASCRR[2:0] = 000b and ASCBB[2:0] = 011b, the video outputs can be aligned as shown below. The maximum shift width of the video signals is 8 clocks. If the ASVS[2:0] and ASHS[2:0] registers are used in line with the video signal shift, the sync signals (VSOUT and HSOUT) can also be shifted in line with the video signals. (DEOUT is also shifted following HSOUT.)
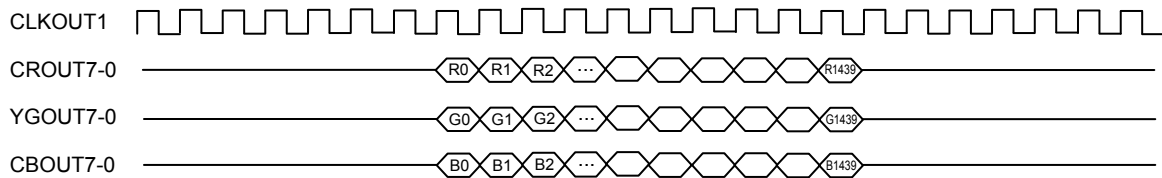
6. ADC

1) Analog clamp

Registers related to analog clamp control

Name	Functions	Sub address	bit width
STBB	This register controls the band gap VREF circuit. 0: Band gap VREF circuit enters standby mode. 1: Band gap VREF circuit enters normal operating mode. * This must be set in line with the operation mode of ADC.	0x21	1
STBB_Y STBB_B STBB_R	These registers control the AFE standby mode (Y: STBB_Y, B: STBB_B, R: STBB_R) 0: AFE standby mode 1: AFE normal operating mode * This must be set in line with the operation mode of ADC.	0x21 0x23 0x25	1
SELFCLPSTBB_Y SELFCLPSTBB_B SELFCLPSTBB_R	These registers control self-clamp. (Y: SELFCLPSTBB_Y, B: SELFCLPSTBB_B, R: SELFCLPSTBB_R) 0: Self-clamp function is OFF 1: Self-clamp function is ON *1: This is disabled when STBB_x=0 (self-clamp function is OFF). *2: The clamp level is set to MAINCLPLVCNT_x[1:0].	0x21 0x23 0x25	1
MAINCLPLVCNT_Y MAINCLPLVCNT_B MAINCLPLVCNT_R	These registers control the clamp level. (Y: MAINCLPLVCNT_Y, B: MAINCLPLVCNT_B, R: MAINCLPLVCNT_R) 00: 0.35V (sink tip clamp) 01: 0.50V (pedestal clamp) 10: 0.85V (center clamp) 11: Inhibited. *: This is enabled when the self-clamp is ON. (STBB_x=1, SELFCLPSTBB_x=1)	0x22 0x24 0x26	2
HPFCLPON_Y HPFCLPON_B HPFCLPON_R	These registers control HPF center clamp. (Y: HPFCLPON_Y, B: HPFCLPON_B, R: HPFCLPON_R) 0: HPF center clamp is OFF 1: HPF center clamp is ON *: This must be set OFF unless the center clamp is selected. (MAINCLPLVCNT_x[1:0]=10).	0x22 0x24 0x26	1
CLPLPFON_Y CLPLPFON_B CLPLPFON_R	These registers control clamp LPF. (Y: CLPLPFON_Y, B: CLPLPFON_B, R: CLPLPFON_R) 0: LPF function is OFF 1: LPF function is ON *: This is appropriate for rejecting high-frequency noises in a weak electric field (cut-off frequency is 1MHz). This must be set OFF when the video signals equivalent to HD specifications is input.	0x22 0x24 0x26	1

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- Analog clamp function

  This function performs sync tip clamping and pedestal clamping to the video input selected by AINSEL. When the analog clamp function is not used, it can be placed in the standby status using the SELFCLPSTBB_x setting.

STBB_x	SELFCLPSTBB_x	State	Clamping Voltage
0	*	Analog clamp function OFF	-
1	0	Analog clamp function OFF	-
1	1	Analog clamp function ON	Subjected to the clamp level control

- Analog clamp level control

  When the analog clamp function is ON, sync tip clamp, pedestal clamp and center clamp can be selected using the settings below.
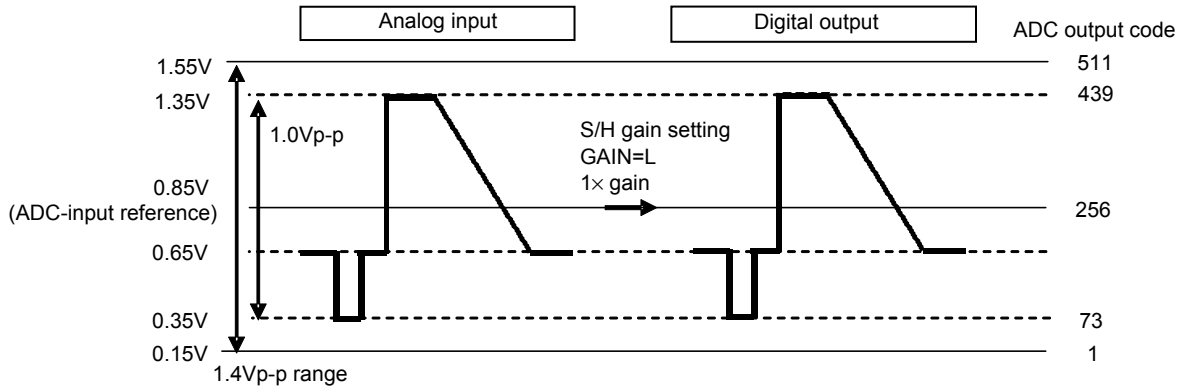
MAINCLPLVCNT[1:0]	Clamp Level	State/Use
00	0.35V	Sync tip clamp
01	0.50V	Pedestal clamp
10	0.85V	Center clamp
11	-	Inhibited

The clamp levels applied to the YCbCr and RGB inputs are given below.

AFE CH	YCbCr	RGB
Y	Sync chip clamp	Pedestal clamp
B	Center clamp	Pedestal clamp
R	Center clamp	Pedestal clamp

• Sync tip clamp specifications

Analog input		Digital output	ADC output code

1.55V — 511
1.35V — 439
1.0Vp-p

S/H gain setting
GAIN=L
1× gain →

0.85V
(ADC-input reference) — 256

0.65V

0.35V — 73
0.15V — 1
1.4Vp-p range

The figures represent the set values set under ideal conditions.

Clamp settings

Self-clamp setting
SELFCLPSTBB   H: Self-clamp ON

Main clamp level setting
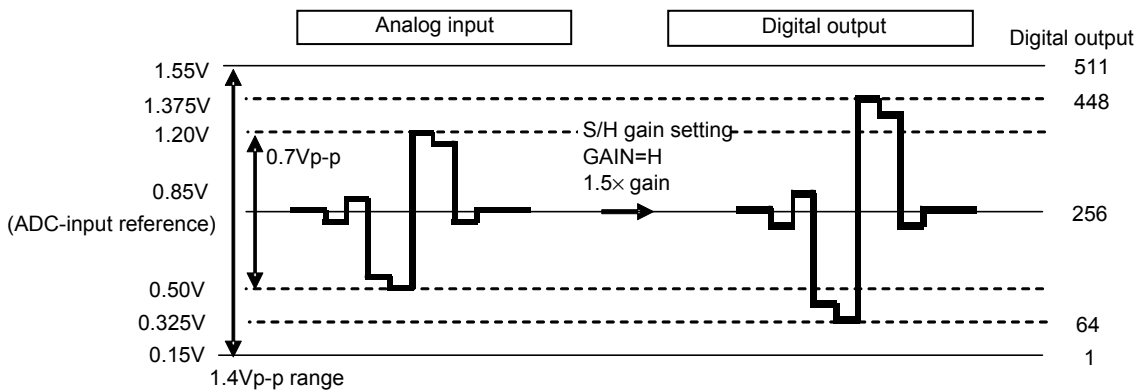MAINCLPLVCNT [1:0]   00: Main clamp level set to 0.35V

HPF center clamp setting
HPFCLPON   L: HPF clamp OFF

S/H gain setting
GAIN   L: 1× gain

• Center clamp specifications

Analog input		Digital output	Digital output

1.55V — 511
1.375V — 448
1.20V
0.7Vp-p

S/H gain setting
GAIN=H
1.5× gain →

0.85V
(ADC-input reference) — 256

0.50V
0.325V — 64
0.15V — 1
1.4Vp-p range

*The figures represent the set values set under ideal conditions.

Clamp settings

Main clamp level setting
MAINCLPLVCNT [1:0]   10: Main clamp level set to 0.85V

Self-clamp setting
SELFCLPSTBB   L: Self-clamp OFF
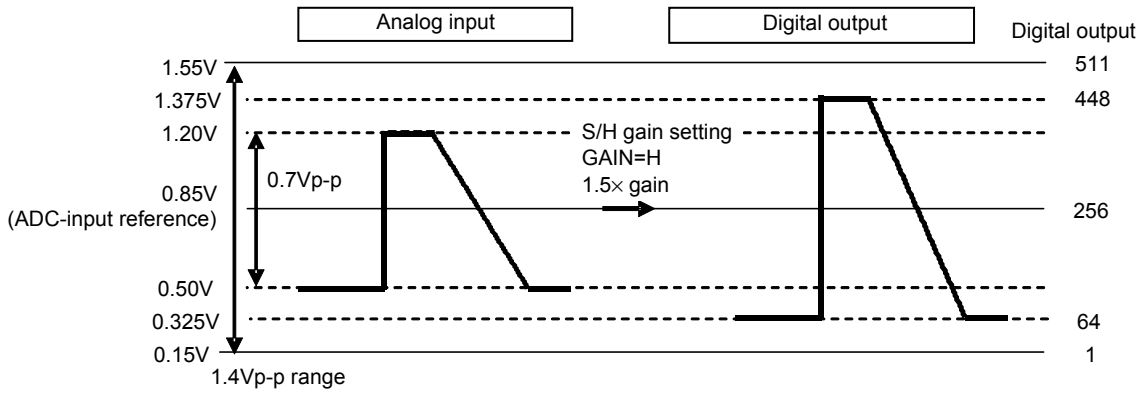
HPF center clamp setting
HPFCLPON   H: HPF clamp ON

S/H gain setting
GAIN   H: 1.5× gain

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• Pedestal clamp specifications

| Analog input | | Digital output | | Digital output |

```
1.55V ┬                                                              511
1.375V ┤ - - - - - - - - - - - - - - - - - - - - - - - ┌──┐ - - - -   448
1.20V ┤        ┌────┐         S/H gain setting  - - - - │  │
                              GAIN=H
  0.7Vp-p                     1.5× gain
0.85V ┤        │    │           ──────►                 │  │          256
(ADC-input reference)
0.50V ┤ - ┌────┘    └────┐ - - - - - - - - - - - - - - -┘  │
0.325V ┤               - - - - - - - - - - - - ┌──────┘    └──── - -  64
0.15V ┴                                                               1
```
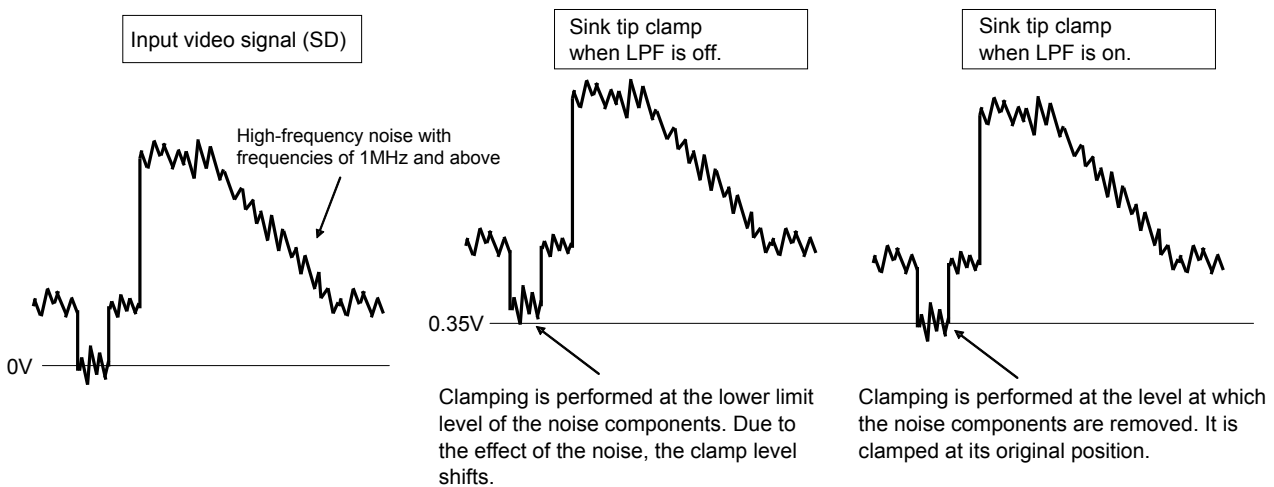1.4Vp-p range

* The figures represent the set values set under ideal conditions.

Clamp settings

Self-clamp setting
SELFCLPSTBB   H: Self-clamp ON

Main clamp level setting
MAINCLPLVCNT [1:0]   01: Main clamp level set to 0.50V

HPF center clamp setting
HPFCLPON   L: HPF clamp OFF

S/H gain setting
GAIN   H: 1.5× gain

• Clamp LPF function
A primary LPF with a 1MHz cutoff frequency has been inserted in the stage before the self-clamp circuit as a measure to deal with the high-frequency noise that is present in weak electrical fields. The clamp LPF function is for minimizing shifts in the clamp levels of the self-clamp and sub-clamp when high-frequency noise components are present in the video signals. The LPF can be set to ON or OFF using the CLPLPFON setting. It must be set to ON when SD standard signals are input, and set to OFF when HD standard signals are input. The cutoff frequency of the LPF is 1MHz. Care must therefore be taken when the LPF is set to ON since the clamp level will drop when HD standard signals are input because it is not possible to track frequencies corresponding to the sync width.

| Input video signal (SD) | Sink tip clamp when LPF is off. | Sink tip clamp when LPF is on. |

High-frequency noise with frequencies of 1MHz and above

0.35V

0V

Clamping is performed at the lower limit level of the noise components. Due to the effect of the noise, the clamp level shifts.

Clamping is performed at the level at which the noise components are removed. It is clamped at its original position.

No.A1647-24/37

2) ADC

Registers related to ADC control

Name	Functions	Sub address	bit width
STBL_Y STBL_B STBL_R	These registers control the ADC standby mode (Y: STBL_Y, B: STBL_B, R: STBL_R). 0000: ADC standby mode 1111: ADC normal operating mode *1: Any other settings than above inhibited. *2: This must be set in line with the operating mode of ADC.	0x21 0x23 0x25	4
ICNT_Y ICNT_B ICNT_R	These registers control the internal bias current of ADC (Y: ICNT_Y, B: ICNT_B, R: ICNT_R). Bias current generating resistor values: 000: 600Ω (recommended) 001: 540Ω 010: 480Ω 011: 420Ω 100: 360Ω 101: 300Ω 110: 240Ω 111: 180Ω	0x39 0x3A 0x3B	3

7. Digital Clamp

1) Digital clamp pulses

Registers related to digital clamp pulse control

| Name	Functions	Sub address	bit width
OSEL	This register sets the digital clamp pulse output to ON or OFF. It is used to adjust the position of the digital clamp pulses. 000: Normal operation 101: The Y digital clamp pulse is output from the YGOUT7 pin and the C digital clamp pulse is output from the CBOUT7 pin.	0x2E	3
DCLPYON DCLPCON	These registers set the digital clamp pulse to ON and OFF (Y: DCLPYON, C: DCLPCON). 0: OFF, 1: ON	0x0A 0x0F	1
DCPYSET DCPCSET	These registers set the digital clamp pulse positions (Y: DCPYSET, C: DCPCSET). They are set in 4-clock increments using the trailing edge of Hsync as a reference. Setting range: -32 (00h) to +31 (3Fh), default value: +/-0 (20h)	0x0A 0x0F	6
DCLPYW DCLPCW	These set the digital clamp pulse width. It can be set in 1 clock increments. 0 specifies a pulse width of 0. (Y: DCLPYW, C: DCLPCW)	0x0B 0x10	6
DCLPYV DCLPCV	These registers set the disable function of the digital clamp pulses during the vertical blanking period to ON or OFF. (Y: DCLPYV, C: DCLPCV) 0: OFF, 1: ON	0x0B 0x10	1
DCPYVMS DCPCVMS	These specify the start line at which the digital clamp pulses are enabled within 1V. As a basic rule, the same values as the V-enable start line (VBLKS[10:0]) are set.	0x0C-0x0D 0x11-0x12	11
DCPYVME DCPCVME	These specify the end line at which the digital clamp pulses are enabled within 1V. As a basic rule, the same values as the V-enable end line (VBLKS[10:0]) are set.	0x0C-0x0E 0x11-0x13	11

Digital clamp pulse settings (how to output the clamp pulses)

OSEL[2:0] *1	YGOUT7	CBOUT7
101	Digital clamp pulse (Y)	Digital clamp pulse (C)

*1: The "000" setting must be used during normal operation.

• Digital clamp pulse settings (how to establish settings in the horizontal direction)
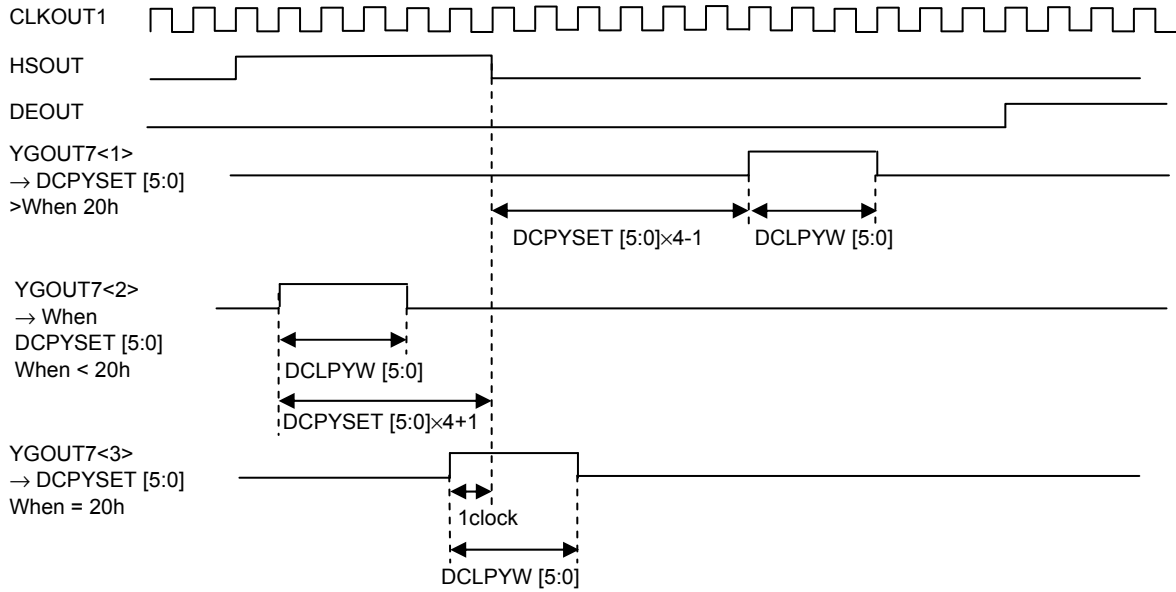
*2: The digital clamp pulse positions must be set so that they come within the horizontal blanking period (DEOUT = L).

*3: The digital clamp pulse (C) setting method is the same as that described above. However, DCPCSET[5:0] (0Fh, bit5-0) must be used for the pulse position setting, and DCLPCW[5:0] (10h, bit5-0) must be used for the pulse width setting.

• Digital clamp pulse settings (how to establish settings in the vertical direction)
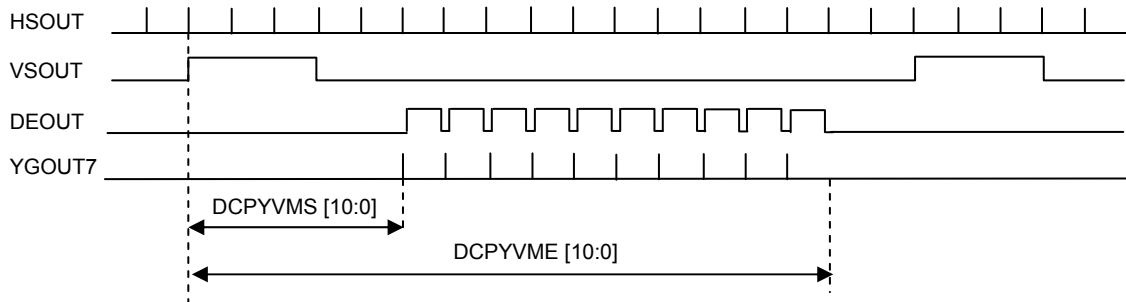
*4: By using the digital clamp pulse disable function (Y: DCLPYV = 1, C: DCLPCV = 1), the digital clamp pulse in the vertical blanking period can be set to OFF. The same values as the vertical enable settings (VBLKS[10:0], VBLKE[10:0]) must be used for the mask period settings (DCPYVMS[10:0], DCPYVME[10:0]).

*5: The digital clamp pulse (C) setting method is the same as that described above. However, DCPCVMS[10:0] and DCPVME[10:0] must be used for the mask period settings.

2) Digital clamp

Registers related to digital clamp control

Name	Functions	Sub address	bit width
SELYCRGB	This register switches between the YCbCr input and RGB input. 0: YCbCr, 1: RGB	0x14	1
STDLEVY	YG digital clamp levels (SELYCRGB=0: Y, SELYCRGB=1: G) The 9-bit (0-511) YG video signals are clamped by the values determined assuming the pedestal levels (Y: STDLEVY[5:0] + 118, G: STDLEVY[5:0]). Setting range: Y (118-181), G (0-63)	0x14	6
STDLEVCB	CBB digital clamp levels (SELYCRGB=0: CB, SELYCRGB=1: B) The 9-bit (0-511) CBB video signals are clamped by the value determined assuming the center level (STDLEVCB[5:0] + 225) for CB and the pedestal level (STDLEVCB[5:0]) for B. Setting range: CB (225-288), B (0-63)	0x15	6
STDLEVCR	CRR digital clamp levels (SELYCRGB=0: CR, SELYCRGB=1: R) The 9-bit (0-511) CRR video signals are clamped by the value determined assuming the center level (STDLEVCR[5:0] + 225) for CR and the pedestal level (STDLEVCR[5:0]) for R. Setting range: CR (225-288), R (0-63)	0x16	6
DCLINE	This sets the digital clamp update unit. 0: 1V, 1: 1H (used for testing)	0x15	1
FRAMEDC	[When the digital clamp update unit is 1V (DCLINE=0)] This register sets the number of update frames (FRAMEDC[4:0] + 1). Setting range: 0-31 (1 to 32 frames)	0x17	5
TCDIGCLP	This register sets the digital clamp time constant. 000: 1/1　　001: 1/2 010: 1/4　　011: 1/8 100: 1/16　　101: 1/32 110: 1/64　　111: 1/128	0x17	3

• Digital clamp specifications

The 9-bit (0-511) video signals output from the ADC are clamped at the set digital clamp pulse position to the set digital clamp level.
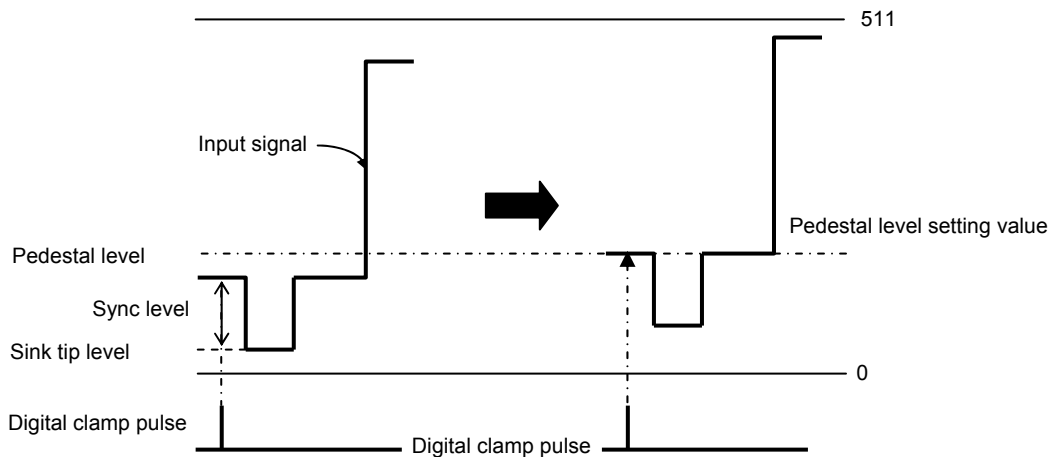
The digital clamp level setting values are given below.

Y=118+STDLEVY[5:0]

Cb/Cr=225+(STDLEVCB[5:0]/STDLEVCR[5:0])

R, G, B=STDLEVY[5:0]/STDLEVCB[5:0]/STDLEVCR[5:0]

• Concerning the time constant setting

A difference between the pedestal level of the 9-bit (0-511) video signals and set digital clamp level is obtained through digital clamp processing as shown in the figure below. The result of multiplying this difference by the 1/X time constant is added to the input signals and output. In this way, the level is changed gradually to the set digital clamp level. The time constant is set using TCDIGCLP[2:0].
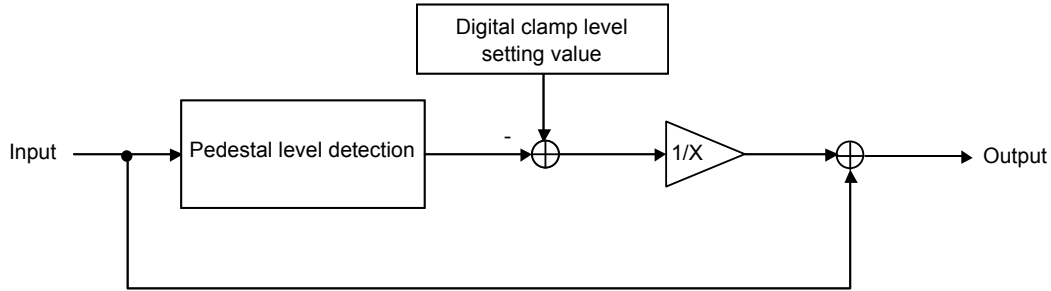
8. Gain

1) Gain adjustments

Registers related to gain adjustments

Name	Functions	Sub address	bit width
SELYCRGB	This register switches between YCbCr input and RGB input. 0: YCbCr, 1: RGB	0x14	1
SYNCON	This register turns ON and OFF the function to adjust the gain by cutting off the sync component of the digitally clamped Y video signal for YCbCr input. This must be set to 0 for the RGB input (SELYCRGB=1). 0: ON, 1: OFF	0x1B	1
CNLINE	This register sets the nonlinear gain adjustment to ON or OFF. 0: OFF (linear gain adjustment) 1: ON (nonlinear gain adjustment)	0x19	1
COFFSET	This register adjusts the nonlinear gain region when the nonlinear gain adjustment is ON (CNLINE=1).	0x1C	5
GAINY	Linear gain adjustment (YG) The multipliers for linear gain adjustment are given below. Y (SELYCRGB=0): (32+GAINY[6:0])/64 G (SELYCRGB=1): (48+GAINY[6:0])/64	0x19	7
GAINCB	Linear gain adjustment (CBB) The multiplier is set to (48+GAINCB[6:0])/64 for linear gain adjustment.	0x1A	7
GAINCR	Linear gain adjustment (CRR) The multiplier is set to (48+GAINCR[6:0])/64 for linear gain adjustment.	0x1B	7

• Gain adjustment specifications

The digitally clamped 9-bit video signals are converted into 8-bit video signals as shown in the figure below. In this case, the digital clamp level is shifted to the LSB of the 8 bits, and gain is adjusted in such a way that the components (video signals) above the digital clamp level fit in the 8-bit range.

- Non-linear gain adjustment

When CNLINE = 1, the output obtained in response to the input near the saturation region is made non-linear. When the non-linear gain adjustment parameter (CONPARA), obtained from the formula below, is less than the multiplier (RGB: $(32 + GAIN\_x[6:0])/64$, YCbCr: $(48 + 12A\_GAIN\_x[6:0])/64$) that is used when the non-linear gain is adjusted, the input is multiplied by the non-linear gain adjustment parameter, resulting in a non-linear output. The non-linear start position and maximum non-linear output value can be adjusted using COFFSET[4:0].

$$CONPARA = (1023 - \text{9-bit video signals}) \times (64 + COFFSET[4:0])/64$$

The figure below shows the gain adjustment output when the input is Y and GAIN_Y[6:0] = 63.

GAIN_Y=63 (AMP=1.73)
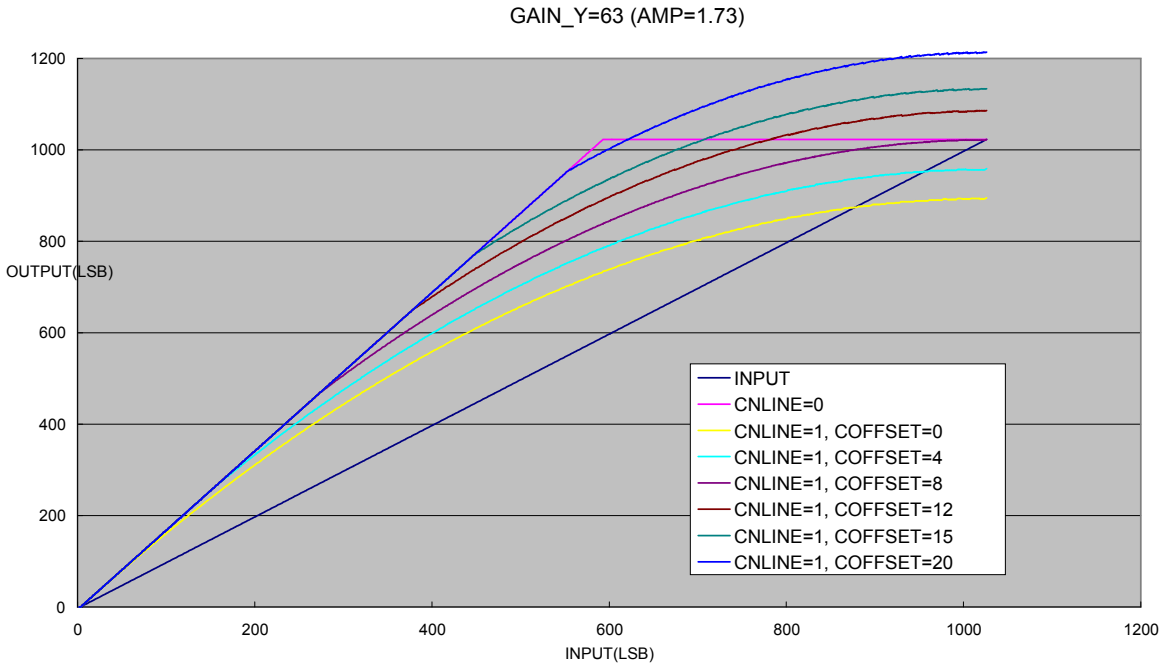
2) DC level adjustment
Registers related to DC level adjustment

Name	Functions	Sub address	bit width
SELYCRGB	This register switches between the YCbCr input and RGB input. 0: YCbCr, 1: RGB	0x14	1
BRADJ	This register adjusts the DC level. When the gain adjustment + DC level adjustment output is linear (BNLINE = 0), BRADJ is offset from the video signals produced after the gain adjustment (the Y signal is further offset by 64). Setting range: -64 to +63, default value: ±0 (40h)	0x1D	7
CNLINE	This register sets the applicable non-linear gain adjustment, when the gain adjustment + DC level adjustment is used (BRADJ<40h), to ON or OFF. 0: OFF (linear gain adjustment) 1: ON (non-linear gain adjustment)	0x19	1
BNLINE	This register sets the applicable non-linear gain adjustment, when the gain adjustment + DC level adjustment is used (BRADJ>40h), to ON or OFF. 0: OFF (linear gain adjustment) 1: ON (nonlinear gain adjustment)	0x1A	1
COFFSET	This register adjusts the non-linear gain region when the non-linear gain adjustment is ON (BNLINE = 1)	0x1C	5

- DC level adjustment specifications
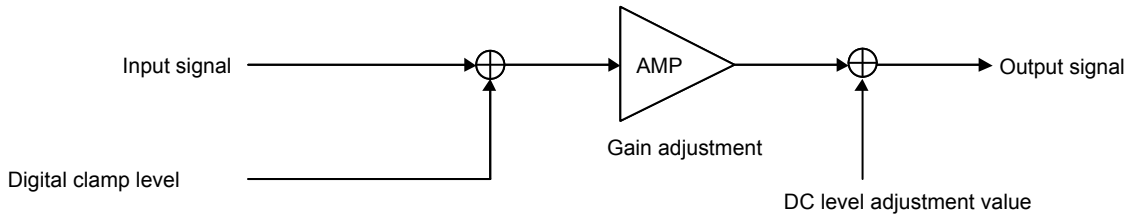
The DC level is adjusted by adding BRADJ[6:0] to the Y signal or RGB signals subjected to gain adjustment processing.

- Non-linear gain adjustment + DC level adjustment
When CNLINE = 1 and BRADJ[6:0]<0x40 (minus), the output corresponding to the input near the saturation region is made non-linear. When the non-linear gain adjustment parameter (CONPARA) obtained from the formula below is less than the multiplier (RGB: (32 + GAIN_x[6:0])/64, YCbCr: (48 + GAIN_x[6:0])/64) that is used when the linear gain is adjusted, the input is multiplied by the non-linear gain adjustment parameter, resulting in a non-linear output. The non-linear start position and maximum non-linear output value can be adjusted using COFFSET[4:0].

$$CONPARA = (1023 - 9\text{-bit video signal}) \times (64 + COFFSET[4:0])/64 - BRADJ[6:0]/2$$

Similarly, when BNLINE = 1 and BRADJ[6:0]>0x40 (plus), the output corresponding to the input near the saturation region is made non-linear. When the DC adjustment parameter (BRPARA), obtained from the formula below, is less than BRADJ[6:0], the extent to which the output is to be non-linear is adjusted by adding the DC adjustment parameter to the Y signal or RGB signals subjected to non-linear gain adjustment processing.

$$BRPARA = (127 - \text{non-linear gain output}/16) \times (64 + COFFSET[4:0])/64$$

The figure below shows the output obtained when the gain adjustment and DC level adjustment have been performed (when GAIN_Y[6:0] = 63, COFFSET[4:0] = 8).
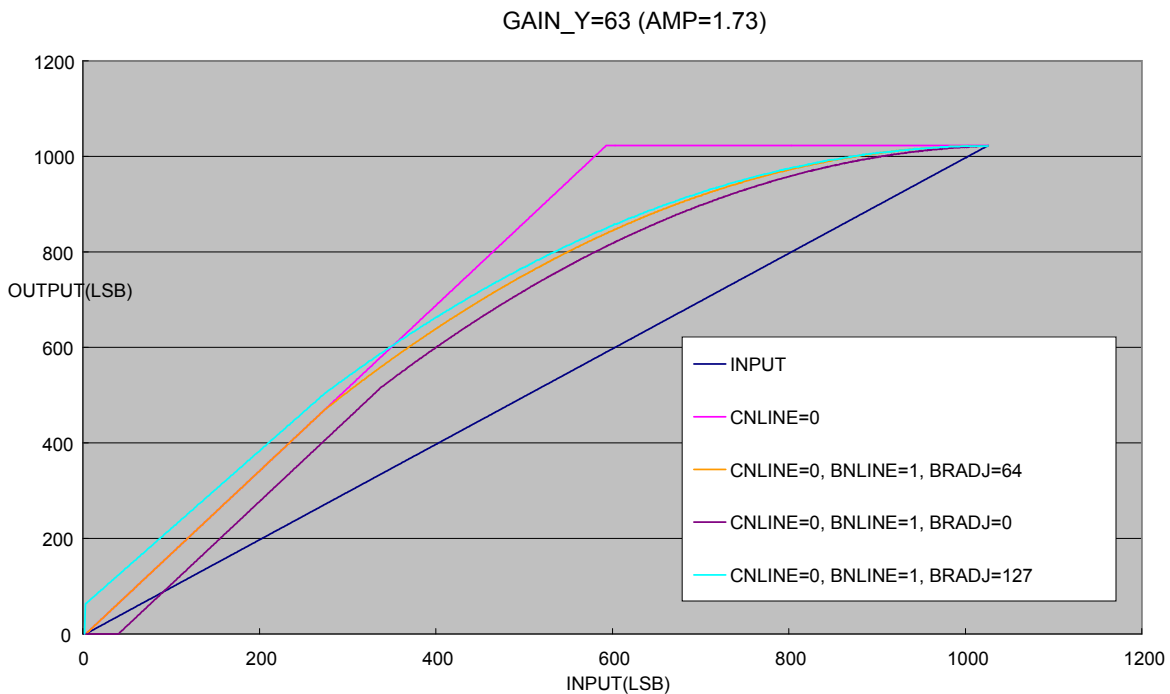
9. External interface

I^2C: 100kHz mode is supported. The slave address can be selected using the pin settings.

Slave address: 0x98, 0x9A

1) Control specifications

Slave operations in the standard mode (100kHz) are supported.

These must be used for setting the internal registers and setting the internal status output and γ correction characteristics. The slave addresses are listed in the table below. Two addresses can be selected using the I^2CSEL pin.

Slave address: ($I^2CSEL=0$)

1	0	0	1	1	0	0	R/W

Slave address: ($I^2CSEL=1$)

1	0	0	1	1	0	1	R/W

2) Control and timing specifications

(1) Receive mode

As shown below, the slave address W, sub-address and input data must be set in this sequence after the start condition. The data of each sub-address can be input in auto address increments consecutively from the data of the sub-address specified. The data must be set consecutively with ACK between one data and the next. The stop condition must be set last.
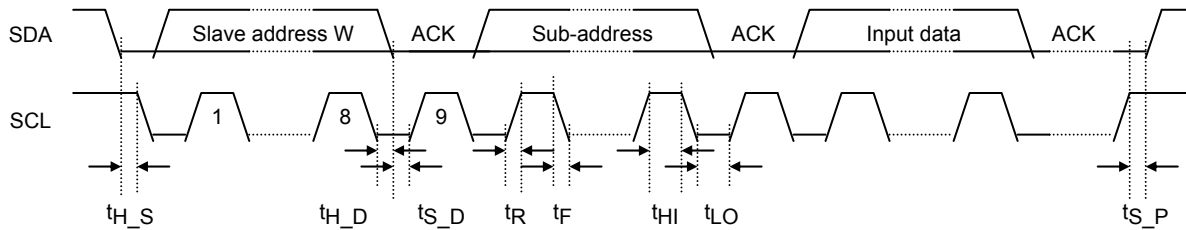

Parameter	Symbol	min	max	unit
SCL clock frequency	fSCL	0	100	kHz
Start condition hold time	tH_S	4.0		μs
Data hold time	tH_D	0		μs
Data setup time	tS_D	250		ns
SDA and SCL rise time	tR		1000	ns
SDA and SCL fall time	tF		300	ns
SCL high level hold time	tHI	4.0		μs
SCL low level hold time	tLO	4.7		μs
Stop condition setup time	tS_P	4.7		μs

(2) Send mode

As shown below, slave address W and the sub-address must be set after the start condition. The stop condition must be set last.

SDA   Slave address W   ACK   Sub-address   ACK

SCL
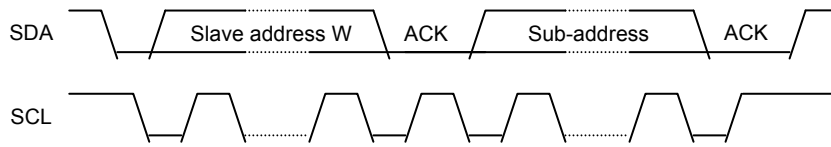
Slave address R must then be set after the start condition. The data of each sub-address is output in auto address increments consecutively from the data of the specified sub-address. The stop condition must be set last.

SDA   Slave address R   ACK   Input data   ACK   Input data   ACK

SCL
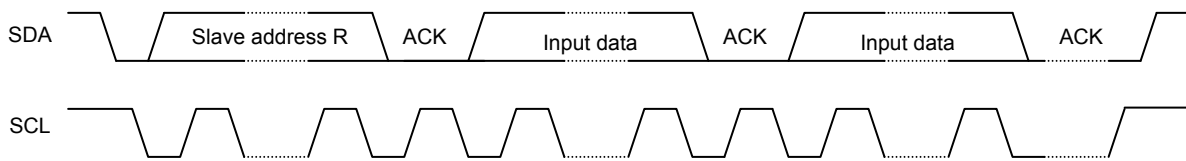
(3) Register settings

The registers can be broadly divided into receive and send registers. Receive registers are setting registers for internal control; send registers are for outputting the internal statuses to an external destination. The receive register settings can also be output to an external destination.

3) Register map

Sub Address		bit7 (MSB)	bit6	bit5	bit4	bit3	bit2	bit1	bit0 (LSB)	Initial Value
Clock I/O control										
00H	R/W	CLKOUT2INV	CLKOUT1INV	CLKHSYIINV	CLKININIINV	CLKADCIINV	CLKSEL[2:0]			08h
Synchronous I/O control/offset adjustment control										
01H	R/W	CLKOUTINV	-	-	-	HSPLLSEL	ASYG[2:0]			88h
02H	R/W	VSOUTINV	ASCRR[2:0]			VSINV	ASCBB[2:0]			08h
03H	R/W	HOUTINV	ASVS[2:0]			HSINV	ASHS[2:0]			08h
H/V enable control										
04H	R/W	HBLKS[11: 8]				HBLKE[11: 8]				03h
05H	R/W	HBLKS[7:0]								7Ah
06H	R/W	HBLKE[7:0]								4Ah
07H	R/W	-	VBLKS[10: 8]			-	VBLKE[10: 8]			01h
08H	R/W	VBLKS[7:0]								11h
09H	R/W	VBLKE[7:0]								02h
Digital clamp										
0AH	R/W	DCLPYON	-	DCPYSET[5:0]						A7h
0BH	R/W	DCLPYV	DIGCLPON	DCLPYW[5:0]						C4h
0CH	R/W	-	DCPYVMS[10: 8]			-	DCPYVME[10: 8]			01h
0DH	R/W	DCPYVMS[7:0]								11h
0EH	R/W	DCPYVME[7:0]								02h
0FH	R/W	DCLPCON	-	DCPCSET[5:0]						A7h
10H	R/W	DCLPCV	-	DCLPCW[5:0]						84h
11H	R/W	-	DCPCVMS[10: 8]			-	DCPCVME[10: 8]			01h
12H	R/W	DCPCVMS[7:0]								11h
13H	R/W	DCPCVME[7:0]								02h
14H	R/W	SELYCRGB	-	STDLEVY[5:0]						A0h
15H	R/W	DCLINE	-	STDLEVCB[5:0]						20h
16H	R/W	EXSYNCON	-	STDLEVCR[5:0]						20h
17H	R/W	TCDIGCLP[2:0]			FRAMEDC[4:0]					40h
18H	R/W	-	-	-						20h
Sub-contrast/brightness										
19H	R/W	CNLINE	GAINY[6:0]							20h
1AH	R/W	BNLINE	GAINCB[6:0]							20h
1BH	R/W	SYNCON	GAINCR[6:0]							20h
1CH	R/W	-	-	-	COFFSET[4:0]					08h
1DH	R/W	-	BRADJ[6:0]							40h
1EH	R/W	-	-							40h
1FH	R/W	-		-		-		-		00h
20H	R/W	-								00h
AFE/ADC										
21H	R/W	STBB	-	SELFCLPSTBB_Y	STBB_Y	STBL_Y[3:0]				BFh
22H	R/W	AINSEL	-	MAINCLPLVCNT_Y[1:0]		-	HPFCLPON_Y	CLPLPFON_Y	GAIN_Y	12h
23H	R/W	-	-	SELFCLPSTBB_B	STBB_B	STBL_B[3:0]				3Fh
24H	R/W	-	-	MAINCLPLVCNT_B[1:0]		-	HPFCLPON_B	CLPLPFON_B	GAIN_B	12h
25H	R/W	-	-	SELFCLPSTBB_R	STBB_R	STBL_R[3:0]				3Fh
26H	R/W	-	-	MAINCLPLVCNT_R[1:0]		-	HPFCLPON_R	CLPLPFON_R	GAIN_R	12h

Continued on next page.

Continued from preceding page.

Sub Address		bit7 (MSB)	bit6	bit5	bit4	bit3	bit2	bit1	bit0 (LSB)	Initial Value
PLL										
27H	R/W	CORREN	-		PLLGAIN[2:0]			PLLCTL2	PLLCTL1	C0h
28H	R/W	HPLDIV15	HPLDIV14	HPLDIV13	HPLDIV12	HPLDIV11	HPLDIV10	HPLDIV9	HPLDIV8	73h
29H	R/W	HPLDIV7	HPLDIV6	HPLDIV5	HPLDIV4	HPLDIV3	HPLDIV2	HPLDIV1	HPLDIV0	58h
2AH	R/W	CPIS_COAST[3:0]				CPIS_ORG[3:0]				AAh
2BH	R/W	CORRHSS[11: 8]				CORRHSE[11: 8]				02h
2CH	R/W	CORRHSS[7:0]								35h
2DH	R/W	CORRHSE[7:0]								1Ch
2EH	R/W	OSEL[2:0]			-	-			-	01h
2FH	R/W	-	-	-		-	-	-	-	06h
30H	R/W	-								00h
31H	R/W	-	-	-	-	-				80h
32H	R/W	-				-				08h
33H	R/W	-	-	-						20h
34H	R	-	-	-	-	-		-		00h
35H	R	-								00h
36H	R	-								00h
37H	R/W	-		-						01h
38H	R/W	-	-	-	-	-			-	00h
39H	R/W	-	-	-		-	ICNT_Y[2:0]			0Ch
3AH	R/W	-	-	-		-	ICNT_B[2:0]			0Ch
3BH	R/W	-	-	-		-	ICNT_R[2:0]			0Ch
3CH	R/W	-	-	-	-	-	-	-	-	00h
3DH	R/W	-	-	-	-	-	-	-	-	00h
3EH	R/W	-	-	-	-	-	-	-	-	00h
3FH	R/W	-	-	-	-	-	-	-	-	92h
PLL and others										
40H	R/W	-	-	CLKINDIV[5:0]						1Fh
FEH	R/W	-	-	-	-	-	-	-	-	80h

PDOWN

Complete power-down can be controlled using the PDWN pin. ADC, PLL and other items can be powered down individually by means of register settings. This makes it possible to limit the power consumption as required.

Internal states based on the PDWN pin setting

PDWN	ADC	PLL	Logic	Communication	Remarks
0	PowerDown	PowerDown	Clocks stopped	Stopped	Registers reset state
1	Operating	Operating	Operating	Operating	

Power Down control by controlling registers

Item	
ADC	Power-down can be controlled using dedicated registers. See below for the relevant registers.
PLL	Power-down can be controlled using dedicated registers. See below for the relevant registers.
Logic	External input is selected and the external clock is stopped. Similarly, the clock is stopped by selecting the PLL mode and power down the PLL circuit.
Output pin	Output-enable (Hi-Z) can be set by using the dedicated registers.
Communication	Cannot be stopped.

Name	Functions	Sub address	bit width
STBL_Y STBL_B STBL_R	These registers control the ADC standby mode (Y: STBL_Y, B: STBL_B, R: STBL_R). 0000: ADC standby mode 1111: ADC normal operating mode *1: Any other setting than above inhibited. *2: These must be set in accordance with the operating mode of AEC.	0x21 0x23 0x25	4
STBB	This register controls the band gap VREF circuit. 0: Places the band gap VREF circuit into the standby mode. 1: Places the band gap VREF circuit into the normal operating mode. *: This must be set in accordance with the operating mode of ADC.	0x21	1
STBB_Y STBB_B STBB_R	These registers control the AFE standby mode (Y: STBB_Y, B: STBB_B, R: STBB_R). 0: AFE standby mode 1: AFE normal operating mode *: These must be set in accordance with the operating mode of ADC.	0x21 0x23 0x25	1
PLLCTL2	This register controls the H-lock PLL power down mode 0: Normal operating mode 1: H-lock PLL power off	0x27	1

Other (usage precautions)

1. Precaution when turning on the power

As shown in the figure below, start the transfer of the I^{2}C bus command after factoring in the power-on time (A), PDWN operation time (B), RESET operation time (C) and command transfer start time (D).
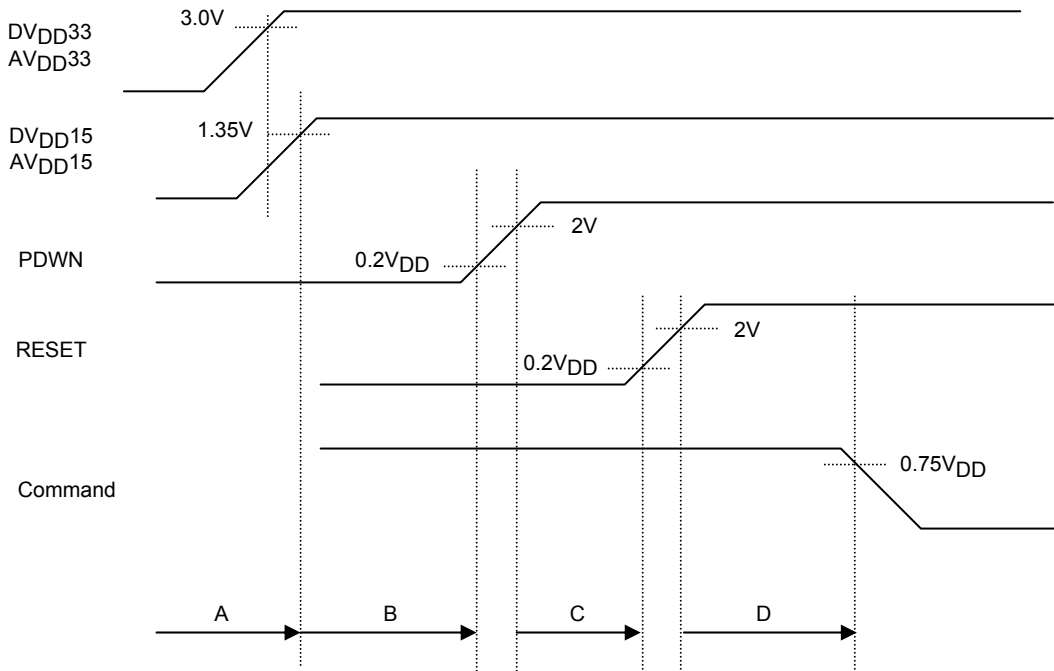
A: Power-on time

This is the time taken from power-on to when the *V$_{DD}$15 operating supply voltage has reached the lowest level (1.35V) and operation has stabilized. The power-on-time depends on the characteristics of the power ICs and other components, so it must be checked separately. With regard to *V$_{DD}$33 and *V$_{DD}$15, *V$_{DD}$15 must be turned on after *V$_{DD}$33 has turned on.

B: PDWN operation time

This is the time during which the "L" level must be applied continuously for a period of 10ms or more to the PDWN pin after the lowest level (1.35V) of the *V$_{DD}$15 operating supply voltage has been reached and operation has stabilized.

C: RESET operation time

This is the time during which the "L" level must be applied continuously for a period of 10ms or more to the RESET pin after the PDWN is released ("H" level).

D: Command transfer start time

At least an interval of 10ms is required from the time the RESET pin is released ("H" level) to the start of command transfer.

2. Precaution when turning off the power
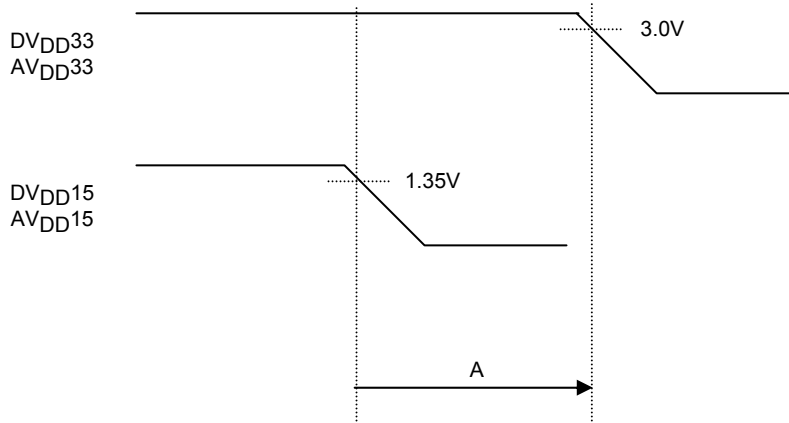
As a basic rule, power-off must be performed in the reverse sequence of power-on. However, no problems are posed if there is no wait time.

A: Power-off time

This is the time it takes to reach the I_O supply voltage and for operation to stabilize from the lowest level (1.35V) of the $*V_{DD}15$ operating supply voltage. With regard to $*V_{DD}33$ and $*V_{DD}15$, $*V_{DD}33$ must be turned off after $*V_{DD}15$ has been turned off or they must be turned off at the same time.