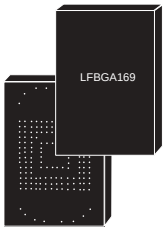
NAND16GAH0P
NAND32GAH0P NAND64GAH0P

2-Gbyte, 4-Gbyte, 8-Gbyte, 1.8 V/3.3 V supply, NAND flash memories with MultiMediaCard™ interface

Preliminary Data

Features

- Packaged NAND flash memory with MultiMediaCard interface
- 2, 4 and 8 Gbytes of formatted data storage
- eMMC/MultiMediaCard system specification, compliant with V4.3
- Full backward compatibility with previous MultiMediaCard system specification
- Bus mode
  - High-speed MultiMediaCard protocol
  - Three different data bus widths:1 bit, 4 bits, 8 bits
  - Data transfer rate: up to 52 Mbyte/s
- Operating voltage range:
  - V_{CCQ} =1.8 V/3.3 V
  - V_{CC} = 3.3 V
- Multiple block read (x8 at 52 MHz): up to 29 Mbyte/s
- Multiple block write (x8 at 52 MHz): up to 19 Mbyte/s
- Power dissipation
  - Standby current: down to 100 µA (typ)
  - Read current: down to 70 mA (typ)
  - Write current: down to 100 mA (typ)
- Trim for data management optimization
- Simple boot sequence method
- Enhanced power saving method by introducing sleep functionality



LFBGA169 12 x 16 x 1.4 mm (ZA)

- Error free memory access
  - Internal error correction code
  - Internal enhanced data management algorithm (wear levelling, bad block management, garbage collection)
  - Possibility for the host to make sudden power failure safe-update operations for data content
- Security
  - Secure erase, secure trim and secure bad block erase commands
  - Disable protection modes (lock/unlock by password and device's permanent write protection)
  - Password protection of data
  - Built-in write protection

Table 1. Device summary

Root part number	Density	Package	Operating voltage
NAND16GAH0P	2 Gbytes	LFBGA169	V_{CC} = 3.3 V, V_{CCQ} = 1.8 V/3.3 V
NAND32GAH0P	4 Gbytes		
NAND64GAH0P	8 Gbytes		

Contents

1 Description 6

1.1 eMMC Standard Specification 7

2 Product specification 8

2.1 System performance 8

3 Device physical description 9

3.1 Package connections 10

3.2 Form factor 10

4 Memory array partitioning 11

5 MultiMediaCard interface 12

5.1 **Signals description 12**

5.1.1 **Clock (CLK) 12**

5.1.2 **Command (CMD) 12**

5.1.3 **Input/outputs (DAT0-DAT7) 12**

5.1.4 V_{CC} core supply voltage 12

5.1.5 V_{SS} ground 12

5.1.6 V_{CCQ} input/output supply voltage 13

5.1.7 V_{SSQ} supply voltage 13

5.2 Bus topology 14

5.3 Power-up 14

5.4 Power cycling 14

5.5 Bus operating conditions 16

5.6 Bus signal levels 16

5.7 Bus timing 16

6 High speed MultiMediaCard operation 17

6.1 Boot mode 17

6.2 Write protect management 17

6.3 Secure erase 17

6.4 Secure trim 18

6.5 Trim 18
6.6 Secure Bad Block management 19
6.7 Identification mode 19
6.8 Data transfer mode 20
6.9 Clock control 20
6.10 Error conditions 20
6.11 Commands 20
6.12 State transition 20
6.13 Response 20
6.14 Timing diagrams and values 20
6.15 Minimum performance 20

7 Device registers 21
7.1 Operation conditions register (OCR) 21
7.2 Card identification (CID) register 22
7.3 Card specific data register (CSD) 22
7.4 Extended CSD register 24
7.5 RCA (relative card address) register 27
7.6 DSR (driver stage register) register 27
7.7 Status register 27

8 Package mechanical 28

9 Ordering information 30

10 Revision history 31

List of tables

Table 1. Device summary . . . 1
Table 2. System performance . . . 8
Table 3. Current consumption . . . 8
Table 4. Communication channel performance . . . 8
Table 5. Signal names . . . 13
Table 6. OCR register definition . . . 21
Table 7. Card identification (CID) register . . . 22
Table 8. Card specific data register . . . 23
Table 9. Extended CSD . . . 24
Table 10. LFBGA169 12 x 16 x 1.4 mm 132+21+16 3R14 0.50 mm, mechanical data . . . 29
Table 11. Ordering information scheme . . . 30
Table 12. Document revision history . . . 31

List of figures

Figure 1. Device block diagram 9
Figure 2. LFBGA169 package connections (top view through package) 10
Figure 3. Form factor 10
Figure 4. Memory array structure 11
Figure 5. Power-up 15
Figure 6. Power cycling 15
Figure 7. LFBGA169 12 x 16 x 1.4 mm 132+21+16 3R14 0.50 mm, package outline 28

1 Description

The NANDxxGAH0P is an embedded flash memory storage solution with MultiMediaCard™ interface (eMMC™). The eMMC™ was developed for universal low-cost data storage and communication media. The NANDxxGAH0P is fully compatible with MMC bus and hosts.

The NANDxxGAH0P communications are made through an advanced 13-pin bus. The bus can be either 1-bit, 4-bit, or 8-bit in width. The device operates in high-speed mode at clock frequencies equal to or higher than 20 MHz, which is the MMC standard. The communication protocol is defined as a part of this MMC standard and referred to as MultiMediaCard mode.

The device is designed to cover a wide area of applications such as smart phones, cameras, organizers, PDA, digital recorders, MP3 players, pagers, electronic toys, etc. They feature high performance, low power consumption, low cost and high density.

To meet the requirements of embedded high density storage media and mobile applications, the NANDxxGAH0P supports both 3.3 V supply voltage (V_{CC}), and 1.8 V/3.3 V input/output voltage (V_{CCQ}).

The address argument for the NAND16GAH0P is the byte address, while the address argument for the NAND32GAH0P and NAND64GAH0P is the sector address (512-byte sectors). This means that the NAND32GAH0P and NAND64GAH0P are not backward compatible with devices of density lower than 2 Gbytes. If the host does not indicate its capability of handling sector type of addressing to the memory, the NAND32GAH0P and NAND64GAH0P change their state to inactive.

The device has a built-in intelligent controller which manages interface protocols, data storage and retrieval, wear leveling, bad block management, garbage collection, and internal ECC.

The NANDxxGAH0P makes available to the host sudden power failure safe-update operations for the data content, by supporting reliable write features.

The device supports boot operation and sleep/awake commands. In particular, during the sleep state the host power regulator for V_{CC} can be switched off, thus minimizing the power consumption of the NANDxxGAH0P.

The password protection feature can be disabled permanently by setting the permanent password disable bit in the extended CSD (PERM_PSWD_DIS bit in the EXT_CSD byte [171], see *Section 7.4: Extended CSD register*). It is recommended to disable the password protection feature on the card, if it is not required. In this way the protection feature can not be set unintentionally or maliciously.

In addition to the standard Erase command, the NANDxxGAH0P devices feature optional Secure Erase command, trim operation, and secure trim operation.

The Secure Erase command allows the applications with tight security constraints, to request that the device performs secure operations even though a negative impact on the erase time performance is possible.

The trim operation is similar to the standard erase operation, but it applies to write blocks instead of erase groups. The secure trim operation is similar to the secure erase operation, but it performs a secure purge operation on write blocks instead of erase groups.

The system performance and characteristics are given in *Table 2*, *Table 3*, and *Table 4*.

1.1 eMMC Standard Specification

The NANDxxGAH0P device is fully compatible with the JEDEC Standard Specification No. JESD84-A43.

This datasheet describes the key and specific features of the NANDxxGAH0P device. Any additional information required to interface the device to a host system and all the practical methods for card detection and access can be found in the proper sections of the JEDEC Standard Specification.

2 Product specification

2.1 System performance

Table 2. System performance

System performance	Typical value(1)			Unit
	NAND16GAH0P	NAND32GAH0P	NAND64GAH0P	
Multiple block read sequential	15	29	29	Mbyte/s
Multiple block write sequential	8.5	19.3	19.3	Mbyte/s

1. Values given for an 8-bit bus width, a clock frequency of 52 MHz, V_{CC} = 3.3 V and V_{CCQ} = 3.3 V.

Table 3. Current consumption

Operation	Test conditions	Current consumption(1)						Unit
		NAND16GAH0P		NAND32GAH0P		NAND64GAH0P		
		Typ	Max	Typ	Max	Typ	Max	
Read	V_{CC}= 3.3 V ± 5% V_{CCQ} = 1.8 V ± 5%	60	70	65	70	65	70	mA
Write		68	80	80	90	80	90	
Standby	V_{CC} = 3.3 V ± 5%	30	50	50	80	70	135	µA
	V_{CCQ} = 1.8 V ± 5%	40	170	40	230	40	230	

1. Values given for an 8-bit bus width and a clock frequency of 52 MHz.

Table 4. Communication channel performance

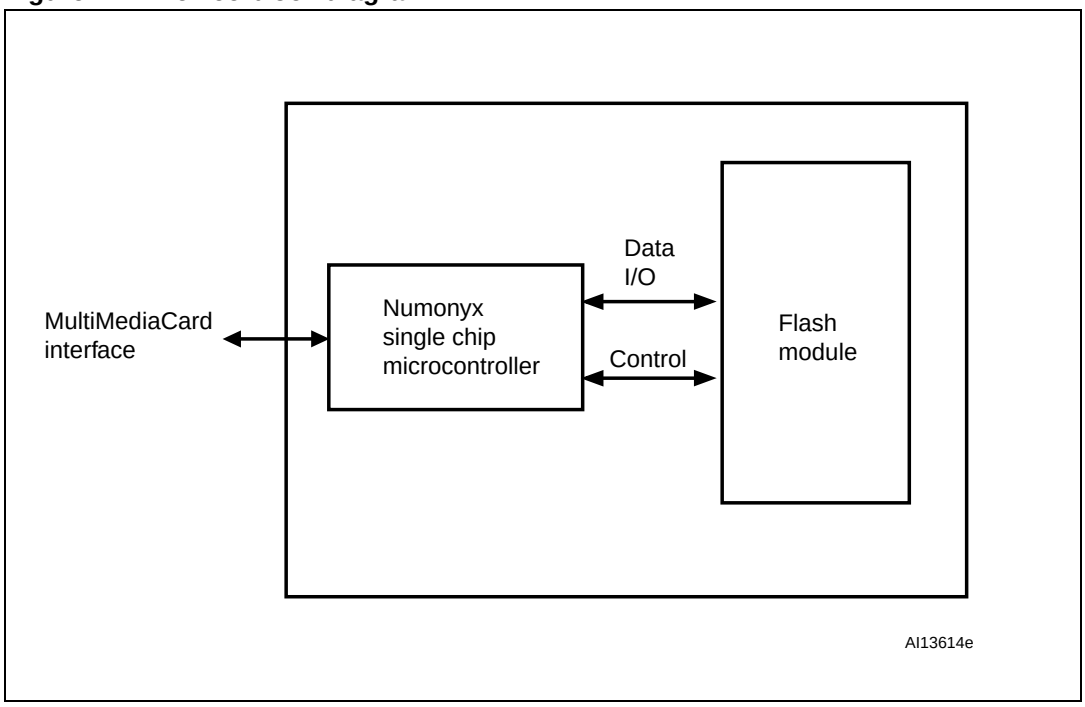
MultiMediaCard communication channel performance
Three-wire serial data bus (clock, command, data)
Variable clock rate 0, 26, 52 MHz
Easy card identification
Error protected data transfer
Sequential and single/multiple block oriented data transfer

3 Device physical description

The NANDxxGAH0P contains a single chip controller and flash memory module, see *Figure 1: Device block diagram*. The microcontroller interfaces with a host system allowing data to be written to and read from the flash memory module. The controller allows the host to be independent from details of erasing and programming the flash memory.

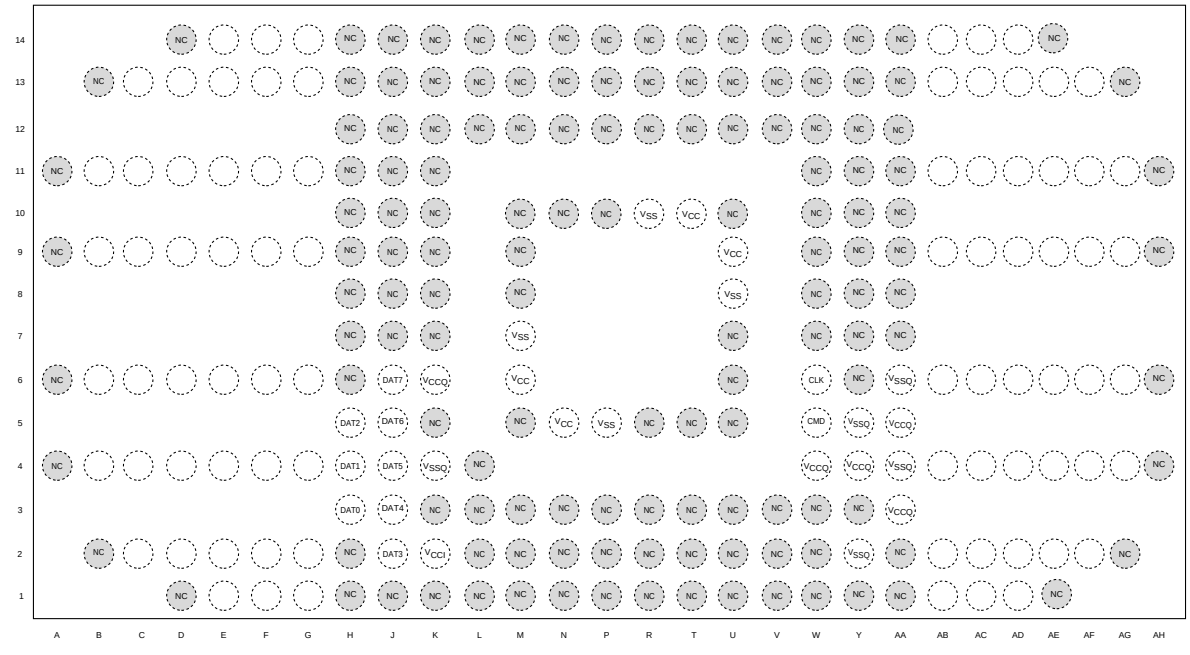
Figure 2 shows the package connections. See *Table 5: Signal names* for the description of the signals corresponding to the balls.

Figure 1. Device block diagram



3.1 Package connections

Figure 2. LFBGA169 package connections (top view through package)



1. The ball corresponding to V_{CCI} must be decoupled with an external capacitance.

3.2 Form factor

The ball diameter, d, and the ball pitch, p, for the LFBGA169 package are:

- d = 0.30 mm (solder ball diameter)
- p = 0.5 mm (ball pitch)

Figure 3. Form factor

4 Memory array partitioning

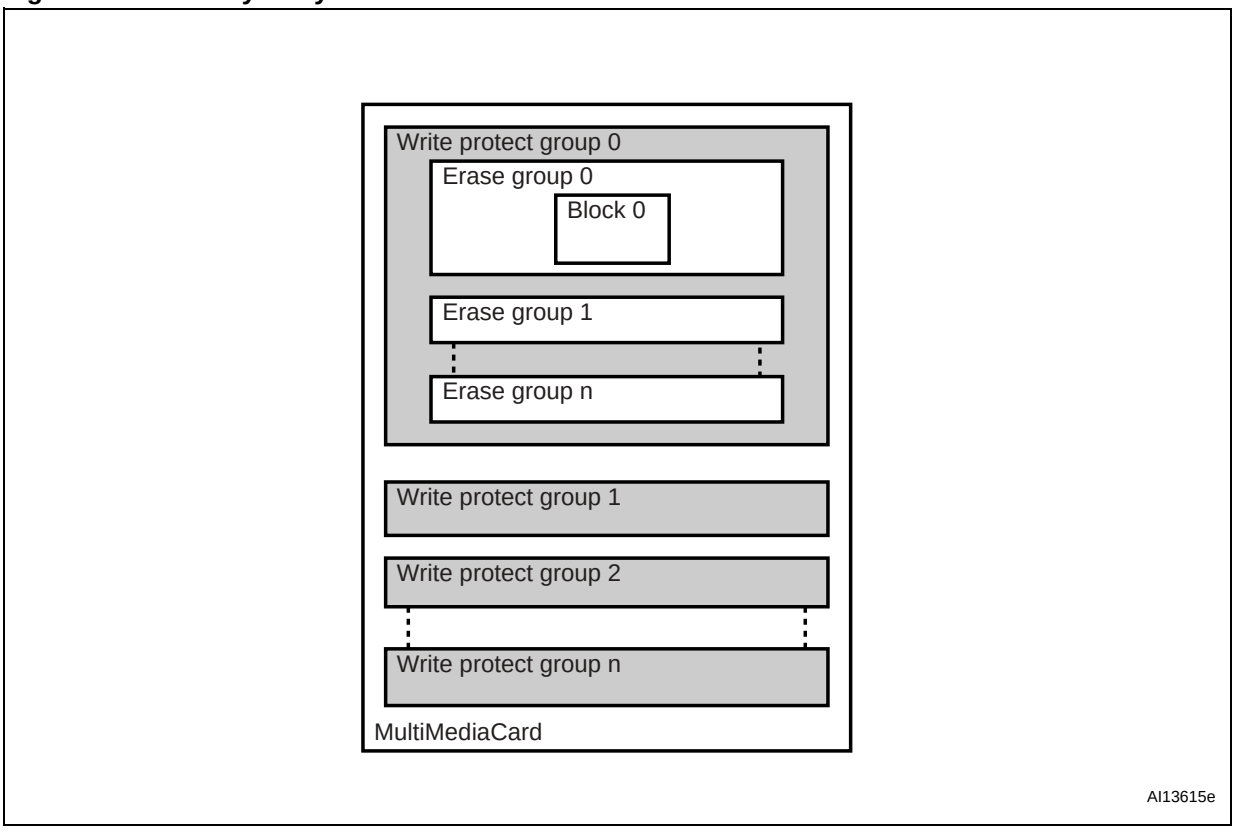
The basic unit of data transfer to/from the device is one byte. All data transfer operations which require a block size always define block lengths as integer multiples of bytes. Some special functions need other partition granularity.

For block oriented commands, the following definitions are used:

- **Block**: the unit which is related to the block oriented read and write commands. Its size is the number of bytes which are transferred when one block command is issued by the host. The size of a block is either programmable or fixed. The information about allowed block sizes and the programmability is stored in the CSD register.
- **Erase group**: the unit which is related to special erase and write commands defined for R/W cards. Its size is the smallest number of consecutive write blocks which can be addressed for erase. The size of the erase group depends on each device and is stored in the CSD.
- **Write protect group**: the smallest unit that may be individually write protected. Its size is defined in units of erase groups. The size of a WP-group depends on each device and is stored in the CSD.

Figure 4 shows the NANDxxGAH0P memory array organization.

Figure 4. Memory array structure



1. n = number of last erase group or last write protect group.

5 MultiMediaCard interface

The signal/pin assignments are listed in *Table 5*. Refer to this table in conjunction with *Figure 2* and *Figure 3: Form factor*.

5.1 Signals description

5.1.1 Clock (CLK)

The Clock input, CLK, is used to synchronize the memory to the host during command and data transfers. Each clock cycle gates one bit on the command and on all the data lines. The Clock frequency, f_{PP}, may vary between zero and the maximum clock frequency.

5.1.2 Command (CMD)

The CMD signal is a bidirectional command channel used for device initialization and command transfer. The CMD signal has two operating modes: open-drain and push-pull. The open-drain mode is used for initialization, while the push-pull mode is used for fast command transfer. Commands are sent by the MultiMediaCard bus master (or host) to the device who responds by sending back responses.

5.1.3 Input/outputs (DAT0-DAT7)

DAT0 to DAT7 are bidirectional data channels. The signals operate in push-pull mode. The NANDxxGAH0P includes internal pull ups for all data lines. These signals cannot be driven simultaneously by the host and the NANDxxGAH0P device. Right after entering the 4-bit mode, the card disconnects the internal pull ups of lines DAT1 and DAT2. Correspondingly right after entering the 8-bit mode, the card disconnects the internal pull ups of lines DAT1, DAT2 and DAT4-DAT7.

By default, after power-up or hardware reset, only DAT0 is used for data transfers. The host can configure the device to use a wider data bus, DAT0, DAT0-DAT3 or DAT0-DAT7, for data transfer.

5.1.4 V_{CC} core supply voltage

V_{CC} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase). The core voltage (V_{CC}) can be within 2.7 V and 3.6 V.

5.1.5 V_{SS} ground

Ground, V_{SS}, is the reference for the power supply. It must be connected to the system ground.

5.1.6 V_{CCQ} input/output supply voltage

V_{CCQ} provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}.

The input/output voltage (V_{CCQ}) can be either within 1.65/1.7 V and 1.95 V (low voltage range) or 2.7 V and 3.6 V (high voltage range).

5.1.7 V_{SSQ} supply voltage

V_{SSQ} ground is the reference for the input/output circuitry driven by V_{CCQ}.

Table 5. Signal names

Name	Type(1)	Description
DAT0	I/O (PP)	Data
DAT1	I/O (PP)	Data
DAT2	I/O (PP)	Data
DAT3	I/O (PP)	Data
DAT4	I/O (PP)	Data
DAT5	I/O (PP)	Data
DAT6	I/O (PP)	Data
DAT7	I/O (PP)	Data
CMD	I/O (OD or PP)	Command
CLK	I (PP)	Clock
V_{CCQ}		Input/output power supply
V_{CC}		Core power supply
V_{SSQ}		Input/output ground
V_{CCI}	I	Must be decoupled with an external capacitance
V_{SS}		Ground
NC	NC	Not connected(2)

1. I: input; O: output, OD: open drain, PP: push-pull.
2. NC pins can be connected to ground or left floating.

5.2 Bus topology

The NANDxxGAH0P device supports the MMC protocol. For more details, refer to section 6.4 of the JEDEC Standard Specification No. JESD84-A43. The section 12 of the JEDEC Standard Specification contains a bus circuitry diagram for reference.

5.3 Power-up

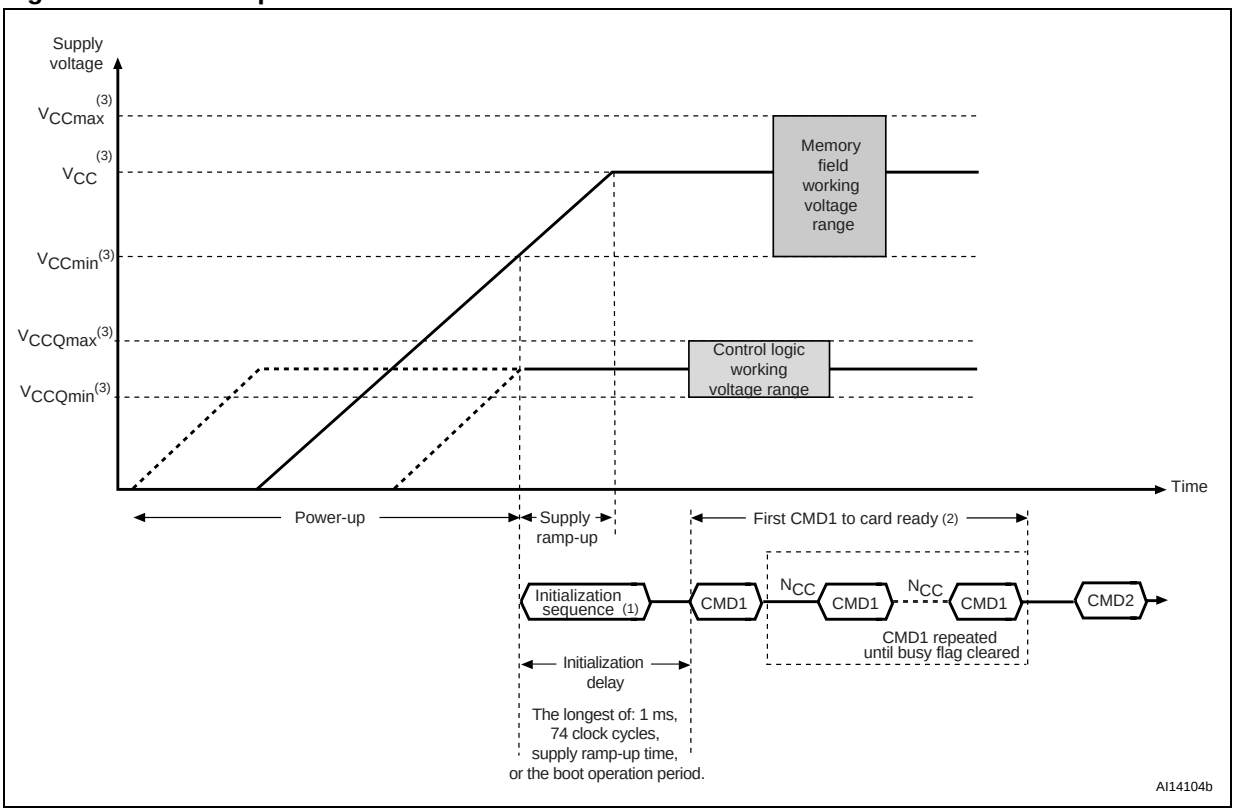
The power-up is handled locally in each device and in the bus master. *Figure 5: Power-up* shows the power-up sequence. Refer to section 12.3 of the JEDEC Standard Specification No. JESD84-A43 for specific instructions regarding the power-up sequence.

After power-up, the maximum initial load the NANDxxGAH0P can present on the V_{CC} line is C4, in parallel with a minimum of R4. During operation, device capacitance on the V_{CC} line must not exceed 10 µF.

5.4 Power cycling

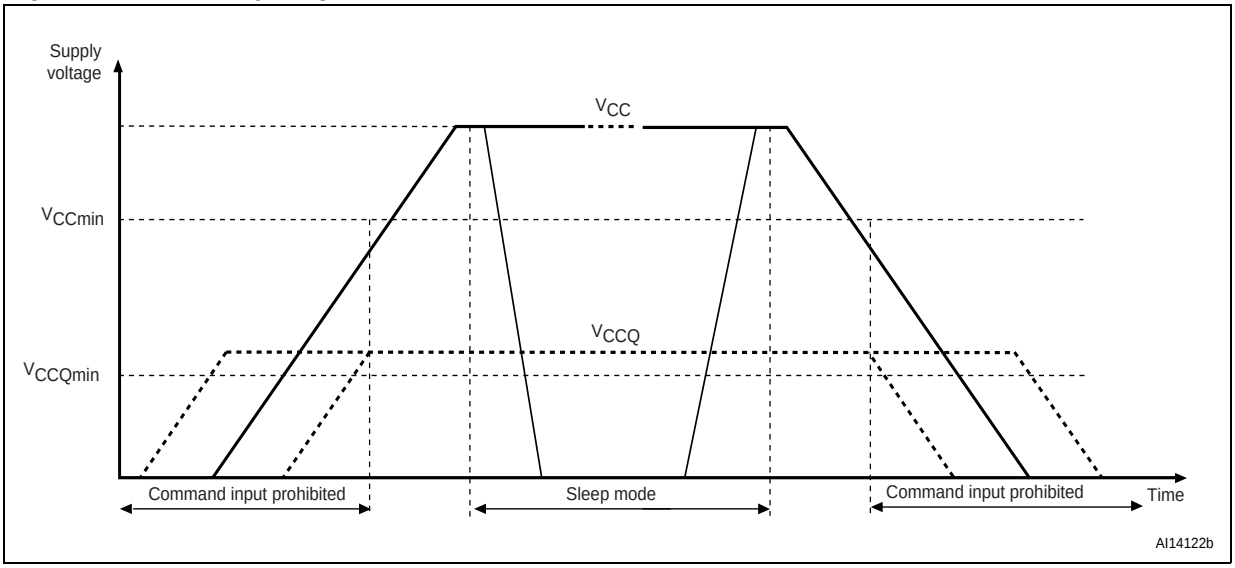
The bus master can execute any sequences of V_{CC} and V_{CCQ} power-up/power down. However, the master must not issue any commands until V_{CC} and V_{CCQ} are stable within each operating voltage range. For more information about power cycling see Section 12.3.3 of the JEDEC Standard Specification No. JESD84-A43 and *Figure 6: Power cycling*.

Figure 5. Power-up



1. The initialization sequence is a contiguous stream of logic 1's. Its length is either 1 ms, 74 clocks or the supply ramp up time, whichever is the longest. The device shall complete its initialization within 1 second from the first CMD1 with a valid V range.
2. N_{CC} is the number of clock cycles.
3. Refer to *Section 7.1: Operation conditions register (OCR)* for details on voltage ranges.

Figure 6. Power cycling



5.5 Bus operating conditions

Refer to section 12.6 of the JEDEC Standard Specification No. JESD84-A43.

5.6 Bus signal levels

Refer to section 12.6 of the JEDEC Standard Specification No. JESD84-A43.

5.7 Bus timing

Refer to section 12.7 of the JEDEC Standard Specification No. JESD84-A43.

6 High speed MultiMediaCard operation

All communication between the host and the device is controlled by the host (master).

The following section provides an overview of the identification and data transfer modes, commands, dependencies, various operation modes and restrictions for controlling the clock signal. For detailed information, refer to section 7 of the JEDEC Standard Specification No. JESD84-A43.

6.1 Boot mode

The host can read boot data from NANDxxGAH0P by keeping CMD line Low after power-on or sending CMD0 with argument + 0xFFFFFFFA (optional for slave), before issuing CMD1. The data can be read from either boot area or user area depending on the register setting. Refer to section 7.2 of the JEDEC Standard Specification No. JESD84-A43.

6.2 Write protect management

To allow the host to protect data against erase or write operations, the NANDxxGAH0P supports two levels of write protect commands:

- The whole NANDxxGAH0P is write-protected by setting the permanent or temporary write protect bits in the CSD register.
- Specific segments of the NANDxxGAH0P are write-protected. ERASE_GROUP_DEF in EXT_CSD defines the segment size.
  When set to ‘0’, the segment size is defined in units of WP_GRP_SIZE erase groups as specified in the CSD register.
  When set to ‘1’, the segment size is defined in units of HC_WP_GRP_SIZE erase groups as specified in the EXT_CSD.

The SET_WRITE_PROT command sets the write protection of the addressed write protect group, and the CLR_WRITE_PROT command clears the write protection of the addressed write protect group. The SEND_WRITE_PROT command is similar to a single block read command.

The card sends a data block containing 32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits. The address field in the write protect commands is a group address in byte units, for NAND16GAH0P, and in sector units for NAND32GAH0P and NAND64GAH0P. Both permanent and temporary write protection applies not only to user data area but also to boot partitions.

6.3 Secure erase

In addition to the standard Erase command the NANDxxGAH0P devices feature also an optional Secure Erase command. The Secure Erase command differs from the standard Erase command since it requires the card to execute the erase operation on the memory array when the command is issued and requires the card and host to wait until the operation is complete before moving to the next card operation. Also, the secure erase command requires the card to do a secure purge operation on the erase groups, and that any copies of items in those erase groups must be identified for erase.

The Secure Erase command is executed in the same way as the erase command outlined in section 7.5.8 of JEDEC Standard Specification No. JESD84-A43, except that the Erase command (CMD38) is executed with argument bit 31 set to ‘1’ and the other argument bits set to ‘0’.

The host has to excute the Secure Erase command with caution to avoid unintentional data loss. A card resetting (using CMD0, CMD15) or a power failure terminates any pending or active Secure Erase command. This may leave the data involved in the operation in an unknown state.

6.4 Secure trim

The Secure Trim command is very similar to the Secure Erase command. The Secure Trim command performs a secure purge operation on write blocks instead of erase groups. To minimize the impact on the card's performance and reliability, the secure trim operation is completed by executing two distinct steps:

- In the Secure Trim step 1 the host defines the range of write blocks to be marked for the secure purge operation. This step does not perform the actual purge operation. The blocks are marked by defining the start address of the range using the ERASE_GROUP_START command (CMD35), followed by defining the last address of the range using the ERASE_GROUP_END command (CMD36). In the case of Secure Trim, both the ERASE_GROUP_START and ERASE_GROUP_END arguments identify write block addresses. Once the range of blocks has been identified, the ERASE (CMD 38) with argument bit 31and 0 set to ‘1’ and the remainder of the argument bits set to ‘0’ is applied. This completes the step 1, which can be repeated several times, with other commands being allowed in between, until all the write blocks that need to be purged have been identified. It is recommended that the Secure Trim Step 1 is done on as many blocks as possible to improve the efficiency of the secure trim operation.
- The Secure Trim step 2 issues the ERASE_GROUP_START (CMD35) and ERASE_GROUP_END (CMD36) with addresses that are in range. Note that the arguments used with these commands are ignored. Then the ERASE (CMD 38), with bit 31 and 15 set to ‘1’ and the remainder of the argument bits set to ‘0’, is sent. This step actually performs the secure purge on all the write blocks, as well as any copies of those blocks, that were marked during Secure Trim Step 1 and completes the secure trim operation.

Once a write block is marked for erase using Secure Trim Step 1, it is recommended that the host consider this block as erased. However, if the host does write to a block after it has been marked for erase, then the last copy of the block, which occurred as a result of the modification, will not be marked for erase. All previous copies of the block will remain marked for erase.

6.5 Trim

The trim operation is similar to the standard erase operation described in section 7.5.8 of JEDEC Standard Specification No. JESD84-A43. The trim function applies the erase operation to write blocks instead of erase groups. The trim function allows the host to identify data that is no longer required so that the card can erase the data, if necessary, during background erase events. The contents of a write block where the trim function has

been applied is '0' or '1' depending on the memory technology. This value is defined in the EXT_CSD.

The trim process consists of a three-steps sequence:

- First the host defines the start address of the range using the ERASE_GROUP_START command (CMD35)
- Next it defines the last address of the range using the ERASE_GROUP_END command (CMD36)
- Finally it starts the erase process by issuing the ERASE command (CMD38) with argument bit 0 set to ‘1’ and the remainder of the arguments set to ‘0’.

In the case of a trim operation both CMD35 and CMD36 identify the addresses of write blocks rather than erase groups.

If an element of the Trim command (either CMD35, CMD36, CMD38) is received out of the defined erase sequence, the card sets the ERASE_SEQ_ERROR bit in the status register and resets the whole sequence.

If the host provides an out-of-range address as an argument to CMD35 or CMD36, the card rejects the command, responds with the ADDRESS_OUT_OF_RANGE bit set and resets the whole erase sequence.

If a non erase command (neither of CMD35, CMD36, CMD38 or CMD13) is received, the card responds with the ERASE_RESET bit set, resets the erase sequence and executes the last command. Commands not addressed to the selected card do not abort the erase sequence.

If the trim range includes write protected blocks, they shall be left intact and only the non protected blocks shall be erased. The WP_ERASE_SKIP status bit in the status register shall be set.

As described above for block write, the card indicates that a Trim command is in progress by holding DAT0 Low. The actual erase time may be quite long, and the host may issue CMD7 to deselect the card.

The host must excute the Trim command with caution to avoid unintentional data loss.

A card reset or a power failure terminates any pending or active Trim command. This may leave the data involved in the operation in an unknown state.

6.6 Secure Bad Block management

The memory array can become defective with use. The NANDxxGAH0P will recover the information from the defective portion of the memory array before it retires the block. If the register bit SEC_BAD_BLK_MGMNT [134] of the EXT_CSD is set, the NANDxxGAH0P performs a secure purge on the contents of the defective region before it is retired. This feature requires only those bits that are not defective in the region to be purged.

6.7 Identification mode

When in card identification mode, the host resets the NANDxxGAH0P, validates the operating voltage range and the access mode, identifies the device and assigns a relative address (RCA) to it. For more information see section 7.3 of the JEDEC Standard Specification No. JESD84-A43.

6.8 Data transfer mode

The device enters data transfer mode once an RCA is assigned to it. When the device is in standby mode, issuing the CMD7 command along with the RCA, selects the device and puts it into the transfer state. The host enters data transfer mode after identifying the NANDxxGAH0P on the bus. When the device is in standby state, communication over the CMD and DAT lines is in push-pull mode.

The section 7.5 of the JEDEC Standard Specification No. JESD84-A43 contains more detailed information about data read and write, erase, write protect management, lock/unlock operations, the switch function command, high speed mode selection, and bus testing procedure. Moreover section 7.5.7 contains a detailed description of the reliable write features supported by the NANDxxGAH0P.

6.9 Clock control

Refer to section 7.6 of the JEDEC Standard Specification No. JESD84-A43.

6.10 Error conditions

Refer to section 7.7 of the JEDEC Standard Specification No. JESD84-A43.

6.11 Commands

Refer to section 7.9 of the JEDEC Standard Specification No. JESD84-A43.

6.12 State transition

Refer to section 7.10 and 7.12 of the JEDEC Standard Specification No. JESD84-A43.

6.13 Response

Refer to section 7.11 of the JEDEC Standard Specification No. JESD84-A43.

6.14 Timing diagrams and values

Refer to section 7.14 of the JEDEC Standard Specification No. JESD84-A43.

6.15 Minimum performance

Refer to section 7.8 of the JEDEC Standard Specification No. JESD84-A43.

7 Device registers

There are five different registers within the device interface:

- Operation conditions register (OCR)
- Card identification register (CID)
- Card specific data register (CSD)
- Relative card address register (RCA)
- DSR (driver stage register)
- Extended card specific data register (EXT_CSD).

These registers are used for the serial data communication and can be accessed only using the corresponding commands (refer to section 7.9 of the JEDEC Standard Specification No. JESD84-A43. The device does not implement the DSR register.

The NANDxxGAH0P has a status register to provide information about the device current state and completion codes for the last host command.

7.1 Operation conditions register (OCR)

The 32-bit operation conditions register stores the V_{CCQ}, the input/output voltage of the flash memory component. The device is capable of communicating (identification procedure and data transfer) with any MultiMediaCard host using any operating voltage within 1.7 V and 1.95 V (low-voltage range) or 2.7 V and 3.6 V (high-voltage range) depending on the voltage range supported by the host. For further details, refer to section 8.1 of the JEDEC Standard Specification No. JESD84-A43.

If the host tries to change the OCR values during an initialization procedure the changes in the OCR content will be ignored.

The level coding of the OCR register is as follows:

- Restricted voltage windows = Low
- Device busy = Low

Table 6. OCR register definition

OCR bit	Description	MultiMediaCard
6 to 0	Reserved	000 0000b
7	Low V_{CCQ}	1b
14 to 8	2.0 - 2.6	000 0000b
23 to 15	2.7 - 3.6 (High V_{CCQ} range)	1 1111 1111b
28 to 24	Reserved	000 0000b
30 to 29	Access mode	00b (byte mode for 2-Gbyte devices)
		01b (sector mode for 4- and 8-Gbyte devices)
31	Power-up status bit (busy)(1)	

1. This bit is set to Low if the device has not finished the power-up routine.

7.2 Card identification (CID) register

The CID register is 16-byte long and contains a unique card identification number used during the card identification procedure. It is a 128-bit wide register with the content as defined in *Table 7*. It is programmed during device manufacturing and can not be changed by MultiMediaCard hosts. For details, refer to section 8.2 of the JEDEC Standard Specification No. JESD84-A43.

Table 7. Card identification (CID) register

Name	Field	Width	CID - slice	CID - value	Note
Manufacturer ID	MID	8	[127:120]	0xFE	
Reserved		6	[119:114]		
Card/BGA	CBX	2	[113:112]	0x01	BGA
OEM/application ID	OID	8	[111:104]	0x4E	
Product name	PNM	48	[103:56]	MMC02, MMC04, MMC08	
Product revision	PRV	8	[55:48]	TBD	
Product serial number	PSN	32	[47:16]	TBD	
Manufacturing date	MDT	8	[15:8]	TBD	
CRC7 checksum	CRC	7	[7:1]	TBD	
Not used, always ‘1’	–	1	[0:0]	1	

7.3 Card specific data register (CSD)

All the configuration information required to access the device data is stored in the CSD register. The MSB bytes of the register contain the manufacturer data and the two least significant bytes contains the host controlled data (the device copy, write protection and the user ECC register).

The host can read the CSD register and alter the host controlled data bytes using the SEND_CSD and PROGRAM_CSD commands.

In *Table 8*, the cell type column defines the CSD field as read only (R), one time programmable (R/W) or erasable (R/W/E). The programmable part of the register (entries marked by W or E) can be changed by command CMD27.

The copy bit in the CSD can be used to mark the device as an original or a copy. Once set it cannot be cleared. The device can be purchased with the copy bit set (copy) or cleared, indicating the device is a master.

The one time programmable (OTP) characteristic of the copy bit is implemented in the MultiMediaCard controller firmware and not with a physical OTP cell.

For details, refer to section 8.3 of the JEDEC Standard Specification No. JESD84-A43.

Table 8. Card specific data register

Name	Field	Width [bits]	Cell type	CSD-slice	CSD-value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x02
MultiMediaCard protocol version	SPEC_VERS	4	R	[125:122]	0x04
Reserved		2	R	[121:120]	TBD
Data read access-time-1	TAAC	8	R	[119:112]	0x4F
Data read access-time-2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	0x01
Max. data transfer rate	TRAN_SPEED	8	R	[103:96]	0x32
Command classes	CCC	12	R	[95:84]	0xF5
Max. read data block length	READ_BL_LEN	4	R	[83:80]	10 for 2-Gbyte devices 9 for 4- and 8-Gbyte devices
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x01
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x00
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x00
DSR implemented	DSR_IMP	1	R	[76:76]	0x00
Reserved		2	R	[75:74]	TBD
Device size	C_SIZE	12	R	[73:62]	1976320 blocks for 2-Gbyte devices Refer to the extended CSD for 4- and 8-Gbyte devices
Max. read current at V_{CC}(min)	VDD_R_CURR_MIN	3	R	[61:59]	0x07
Max. read current at V_{CC}(max)	VDD_R_CURR_MAX	3	R	[58:56]	0x07
Max. write current at V_{CC}(min)	VDD_W_CURR_MIN	3	R	[55:53]	0x07
Max. write current at V_{CC}(max)	VDD_W_CURR_MAX	3	R	[52:50]	0x07
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	0x07
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0x0F
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	0x01
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	TBD
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x02
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	10 for 2-Gbyte devices 9 for 4- and 8-Gbyte devices
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x00

Table 8. Card specific data register (continued)

Name	Field	Width [bits]	Cell type	CSD-slice	CSD-value
Reserved				[20:20]	TBD
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0x00
File format group	FILE_FORMAT_GROUP	1	R/W	[15:15]	0x00
Copy flag (OTP)	COPY	1	R/W	[14:14]	0x00
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x00
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x00
File format	FILE_FORMAT	2	R/W	[11:10]	Hard disk like file system with partition table
ECC code 2 R/W/E none 0	ECC	2	R/W/E	[9:8]	0x00
CRC	CRC	7	R/W/E	[7:1]	TBD
Not used, always ‘1’		1	–	[0:0]	TBD

7.4 Extended CSD register

The extended CSD register defines the device properties and selected modes. It is 512-byte long. The 320 most significant bytes are the properties segment that defines the device capabilities and cannot be modified by the host. The 192 lower bytes are the modes segment that defines the configuration the device is working in. For details, refer to section 8.4 of the JEDEC Standard Specification No. JESD84-A43.

These modes can be changed by the host by means of the Switch command.

Table 9. Extended CSD(1)(2)

Name	Field	Size (bytes)	Cell type	CSD-slice	CSD-slice value
Properties segment					
Reserved(3)		7		[511:505]	TBD
Supported command sets	S_CMD_SET	1	R	[504]	0x01
Reserved(3)		272	TBD	[503:233]	TBD
TRIM multiplier	TRIM_MULT	1	R	[232]	0x03
Secure feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x15
Secure erase multiple	SEC_ERASE_MULT	1	R	[230]	0x01
Secure trim multiple	SEC_TRIM_MULT	1	R	[229]	0x01
Boot information	BOOT_INFO	1	R	[228]	0x01
Reserved(3)		1	TBD	[227]	TBD
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	0x02

Table 9. Extended CSD(1)(2) (continued)

Name	Field	Size (bytes)	Cell type	CSD-slice	CSD-slice value
Access size	ACC_SIZE	1	R	[225]	0x00
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x00
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x03
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x01
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x00
Sleep current (V_{CC})	S_C_VCC	1	R	[220]	0x04
Sleep current (V_{CCQ})	S_C_VCCQ	1	R	[219]	0x08
Reserved(3)		1	TBD	[218]	TBD
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x0B
Reserved(3)		1	TBD	[216]	TBD
Sector count	SEC_COUNT	4	R	[215:212]	0x0040F100 for 8-Gbyte devices 0x00A07800 for 4-Gbyte devices
Reserved(3)		1		[211]	TBD
Minimum write performance for 8 bit at 52 MHz	MIN_PERF_W_8_52	1	R	[210]	0x08
Minimum read performance for 8 bit at 52 MHz	MIN_PERF_R_8_52	1	R	[209]	0x08
Minimum write performance for 8 bit at 26 MHz, for 4 bit at 52 MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x08
Minimum read performance for 8 bit at 26 MHz, for 4 bit at 52 MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x08
Minimum write performance for 4 bit at 26 MHz	MIN_PERF_W_4_26	1	R	[206]	0x08
Minimum read performance for 4 bit at 26 MHz	MIN_PERF_R_4_26	1	R	[205]	0x08
Reserved(3)		1		[204]	TBD
Power class for 26 MHz at 3.6 V	PWR_CL_26_360	1	R	[203]	0x00
Power class for 52 MHz at 3.6 V	PWR_CL_52_360	1	R	[202]	0x00
Power class for 26 MHz at 1.95 V	PWR_CL_26_195	1	R	[201]	0x00
Power class for 52 MHz at 1.95 V	PWR_CL_52_195	1	R	[200]	0x00
Reserved(3)		3		[199:197]	TBD
Card type	CARD_TYPE	1	R	[196]	0x03

Table 9. Extended CSD(1)(2) (continued)

Name	Field	Size (bytes)	Cell type	CSD-slice	CSD-slice value
Reserved(3)		1		[195]	TBD
CSD structure version	CSD_STRUCTURE	1	R	[194]	0x02
Reserved(3)		1		[193]	TBD
Extended CSD revision	EXT_CSD_REV	1	R	[192]	0x03
Modes segment					
Command set	CMD_SET	1	R/W	[191]	0x00
Reserved(3)		1		[190]	TBD
Command set revision	CMD_SET_REV	1	RO	[189]	0x00
Reserved(3)		1		[188]	TBD
Power class	POWER_CLASS	1	R/W	[187]	0x00
Reserved(3)		1		[186]	TBD
High speed interface timing	HS_TIMING	1	R/W	[185]	0x00
Reserved(3)		1		[184]	TBD
Bus width mode	BUS_WIDTH	1	WO	[183]	0x00
Reserved(3)		1		[182]	TBD
Erased memory content	ERASED_MEM_CONT	1	RO	[181]	0x00
Reserved(3)		1		[180]	TBD
Boot configuration	BOOT_CONFIG	1	R/W	[179]	0x00
Reserved(3)		1		[178]	TBD
Boot bus width 1	BOOT_BUS_WIDTH	1	R/W	[177]	0x00
Reserved(3)		1		[176]	TBD
High-density erase group definition	ERASE_GROUP_DEF	1	R/W	[175]	0x00
Reserved(3)		3	TBD	[174:172]	TBD
User Write Protect	USER_WP	1	R/W, R/W/C_P, R/W/E_P	[171]	0x00
Reserved(3)		37	TBD	[174:134]	TBD
Secure bad block management	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x00
Reserved(3)		133	TBD	[132:0]	TBD

1. TBD stands for ‘to be defined’.
2. CSD-slices are added to manage secure erase and secure trim functionalities which are not available in JEDEC Standard Specification No. JESD84-A43.
3. Reserved bits should read as ‘0’.

7.5 RCA (relative card address) register

The writable 16-bit relative card address (RCA) register carries the device address assigned by the host during the device identification. This address is used for the addressed host-card communication after the device identification procedure. The default value of the RCA register is ‘0x0001’. The value ‘0x0000’ is reserved to set all cards into the standby state with CMD7. For details refer to section 8.5 of the JEDEC Standard Specification No. JESD84-A43.

7.6 DSR (driver stage register) register

The 16-bit driver stage register (DSR) can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of devices on the bus).

The CSD register contains the information concerning the DSR register usage.

The default value of the DSR register is ‘0x404’. For details refer to section 8.6 of the JEDEC Standard Specification No. JESD84-A43.

7.7 Status register

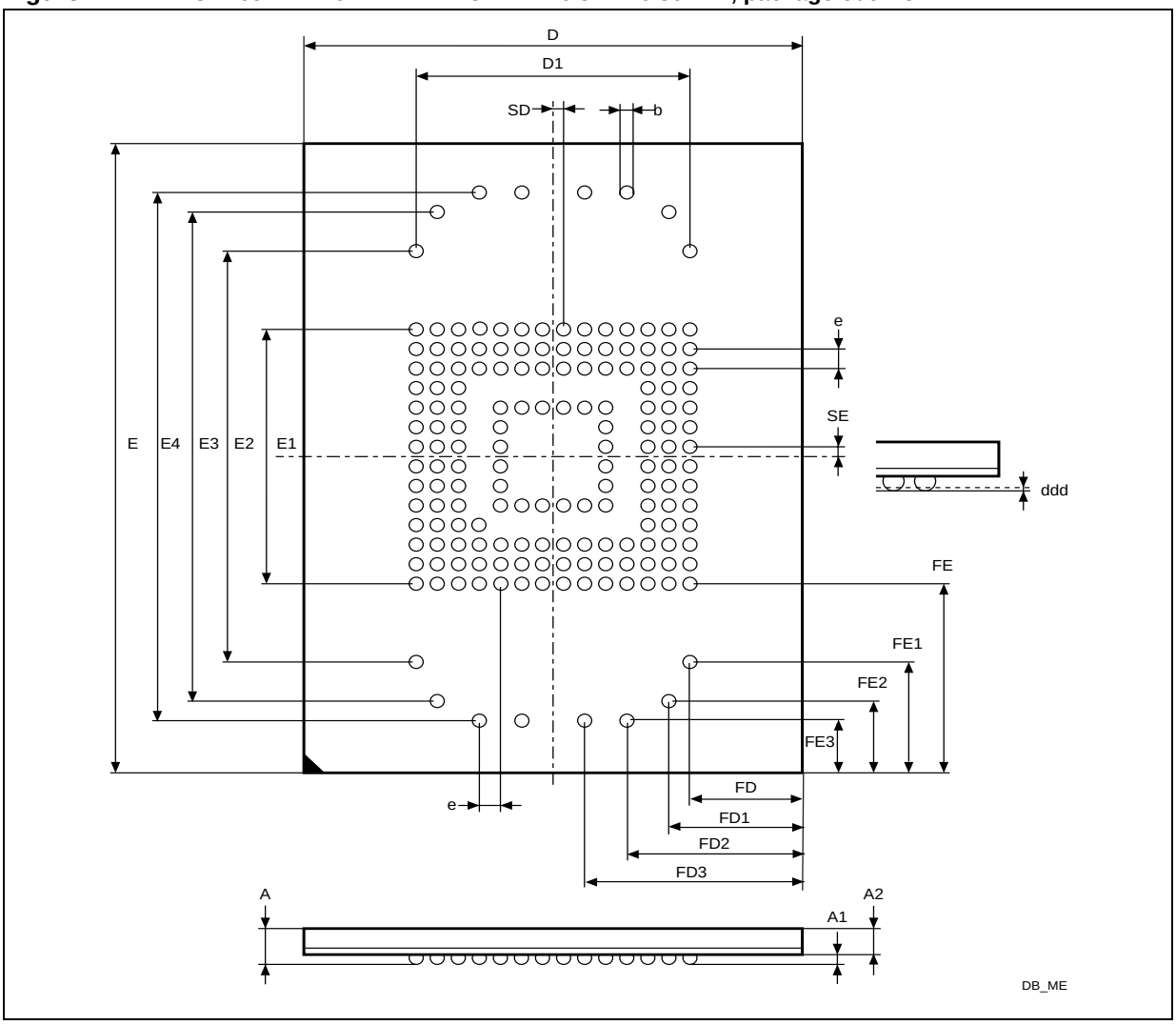
The status register provides information about the device current state and completion codes for the last host command. The device status can be explicitly read (polled) with the SEND_STATUS command. The MultiMediaCard status register structure is defined in section 7.12 of the JEDEC Standard Specification No. JESD84-A43.

8 Package mechanical

To meet environmental requirements, Numonyx offers these devices in RoHS compliant packages, which have a lead-free second-level interconnect. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

RoHS compliant specifications are available at www.numonyx.com.

Figure 7. LFBGA169 12 x 16 x 1.4 mm 132+21+16 3R14 0.50 mm, package outline



1. Drawing is not to scale.

Table 10. LFBGA169 12 x 16 x 1.4 mm 132+21+16 3R14 0.50 mm, mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.40			0.055
A1		0.15			0.006	
A2	1.00			0.039		
b	0.30	0.25	0.35	0.012	0.010	0.014
D	12.00	11.90	12.10	0.472	0.469	0.476
D1	6.50			0.256		
ddd			0.08			0.003
E	16.00	15.90	16.10	0.630	0.626	0.634
E1	6.50			0.256		
E2	10.50			0.413		
E3	12.50			0.492		
E4	13.50			0.531		
e	0.50	–	–	0.020	–	–
FD	2.75			0.108		
FD1	3.25			0.128		
FD2	4.25			0.167		
FD3	5.25			0.207		
FE	4.75			0.187		
FE1	2.75			0.108		
FE2	1.75			0.069		
FE3	1.25			0.049		
SD	0.25	–	–	0.010	–	–
SE	0.25	–	–	0.010	–	–

9 Ordering information

Table 11. Ordering information scheme

Example: NAND64GAH0PZA5E

Device type

NAND flash memory

Density

16G = 2 Gbytes

32G = 4 Gbytes

64G = 8 Gbytes

Operating voltage

A = V_{CC} = 3.3 V, V_{CCQ} = 1.8 V or 3.3 V

Memory type

H = eMMC

Device options

0 = no option

Product version

P = version P

Package

ZA = LFBGA169 12 x 16 x 1.4 mm

Temperature range

5 = –25 to 85 °C

Packing

E = RoHS compliant package, standard packing

F = RoHS compliant package, tape & reel packing

Note: Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available devices and for further information on any aspect of these products, please contact your nearest Numonyx sales office.

10 Revision history

Table 12. Document revision history

Date	Revision	Changes
25-Mar-2009	1	Initial release.
11-Jun-2009	2	Added 4-Gbyte density throughout the document. Modified *Table 3: Current consumption* and *Table 9: Extended CSD*.
09-Sep-2009	3	Modified: *Table 6: OCR register definition*, CID-values in *Table 7: Card identification (CID) register*, CSD-slice values in *Table 8: Card specific data register*, and extended CSD-slice values in *Table 9: Extended CSD*.

Please Read Carefully: