GENERAL INFORMATION

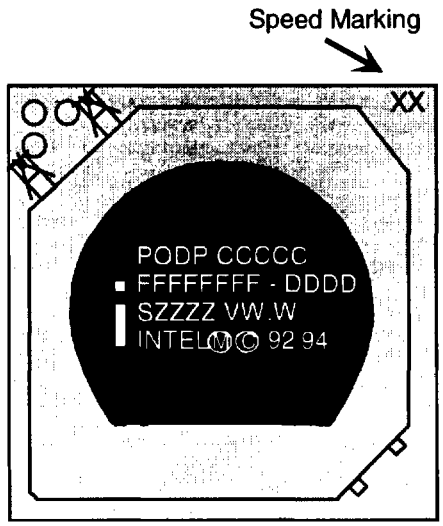
This section covers the various Pentium® OverDrive® processors.

The 63- and 83-MHz Pentium OverDrive processors are Pentium processor technology upgrades for Intel486™ processor-based systems. For more information on the 63- and 83-MHz Pentium OverDrive processors, please refer to the *Intel Pentium OverDrive Processor* datasheet, Order Number 290544.

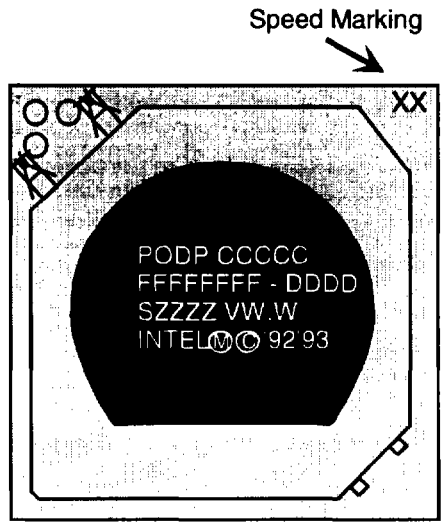
The 120/133-MHz Pentium OverDrive processors are Pentium processor technology upgrades for 60/66-MHz Pentium processor-based systems. The 125, 150, and 166-MHz Pentium OverDrive processors are Pentium processor technology upgrades for 75, 90, and 100-MHz Pentium processor-based systems. For more information on the Pentium OverDrive processors for Pentium processor based systems, please refer to the *Pentium OverDrive Processors for Pentium Processor-Based Systems* datasheet, (Order Number 290579).

Top Markings

The Pentium OverDrive processor can be identified by the number on the base of the heat sink, under the integrated fan. To remove the fan, squeeze the retaining clips in the upper left corner of the chip and lift up. The figure below shows the laser mark found on the heatsink base of the processor. A marking is also used to indicate the speed of the part and is located in the upper right of the package.



63- and 83-MHz Pentium® OverDrive® processors for Intel486™ processor-based systems



120/133-, 125-, 150- and 166-MHz Pentium® OverDrive® processors

NOTES:

- XX or XXX = Core Speed (MHz).
- CCCCC = Product Code
- FFFFFFFF = FPO # (Test Lot Traceability #).
- DDDD = Serialization Code
- SZZZZ = Spec number
- VW.W = Version number
- The FPO - Serial Number is unique for every Pentium® OverDrive® processor.
- The Version Number is used to easily identify major processor steppings: it applies to OverDrive processors only

Basic Pentium® OverDrive® Processor Identification Information

CPUID					Manuf. Stepping[1]	Speed (MHz) Core / Bus	S-Spec	Version	Notes
Product Code	Type	Family	Model	Stepping					
PODP5V63	1	5	3	1	B1	63/25	SZ953	1.0	
PODP5V63	1	5	3	1	B2	63/25	SZ990	1.1	
PODP5V83	1	5	3	2	C0	83/33	SU014	2.1	
PODP5V133	0	5	1	A	tA0	120/60,133/66	SU082	1.0	2
PODP3V125	0	5	2	C	aC0	125/50	SU081	1.0	3
PODP3V150	0	5	2	C	aC0	150/60	SU083	1.0	3
PODP3V166	0	5	2	C	aC0	166/66	SU084	1.0	3

NOTES:

- The Type corresponds to bits [13:12] of the EDX register after RESET, bits [13:12] of the EAX register after the CPUID instruction is executed.
- The Family corresponds to bits [11:8] of the EDX register after RESET, bits [11:8] of the EAX register after the CPUID instruction is executed.
- The Model corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed.
- The Stepping corresponds to bits [3:0] of the EDX register after RESET, bits [3:0] of the EAX register after the CPUID instruction is executed.

1. Manufacturing steppings prefixed with a lower-case "t" refer to the 120/133-MHz Pentium OverDrive processors for 60/66 MHz Pentium processor-based systems. Steppings prefixed with a lower-case "a" refer to the 125/150/166-MHz Pentium OverDrive processors for 75/90/100 MHz Pentium processor-based systems. Steppings without a prefix refer to the 63/83-MHz Pentium OverDrive processors for Intel 486 processor-based systems.
2. The V_{CC} Operating Voltage for these parts is 4.75 - 5.40V.
3. The V_{CC} Operating Voltage for these parts is 3.135 - 3.6V

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the listed Pentium OverDrive processor steppings. Intel intends to correct some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. Any items that are shaded are new for this revision of the document. This table uses the following notations:

CODES USED IN SUMMARY TABLE

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
PP##:	Please refer to Part II: Specification Update for 75-, 90-, 100-, 120-, 133-, 150-, 166- and 200-MHz Pentium® Processors.
Shaded:	**This item is either new or modified from the previous version of the document.**

NO.	B1	B2	C0	tA0	aC0	Refer to:	Plans	SPECIFICATION CHANGES
1	X	X	X				Doc	Clock low time (t_3) change
2		X	X				Doc	Removal of V_{CC} pin A4
3		X	X				Doc	Minimum operating temperature
4	X	X	X			PP12	Doc	STI followed by FP instruction doesn't delay interrupt window
5	X	X	X			PP13	Doc	IDT limit violation causes GP fault, not interrupt 8
6	X	X	X				Doc	Maximum I_{CC} values
7	X	X	X		X	PP19	Doc	Requirements for STPCLK# re-assertion recognition
8				X	X	PP22	Doc	**Leakage current I_{LI}/I_{LO} applies only in the valid logic states**
NO.	**B1**	**B2**	**C0**	**tA0**	**aC0**	**Refer to:**	**Plans**	**ERRATA**
1	X	X	X			PP1	NoFix	Branch trace messages during lock cycles
2	X	X	X			PP2	NoFix	Breakpoint or single-step may be missed for one instruction following STI
3	X	X	X			PP3	NoFix	I/O restart does not function during single-stepping or data breakpoint exceptions

NO.	B1	B2	C0	tA0	aC0	Refer to:	Plans	ERRATA (Cont'd.)
4	X	X	X			PP4	NoFix	NMI or INIT in SMM with I/O restart during single-stepping
5	X	X	X			PP5	NoFix	SMI# and FLUSH# during shutdown
6	X	X					Fixed	BIST disabled
7								Maximum I_{CC} usage (Refer to Spec Change 6)
8	X	X	X			PP6	NoFix	No shutdown after internal error
9	X	X	X			PP7	NoFix	FLUSH# with a breakpoint pending causes false DR6 values
10	X	X	X		X	PP10	NoFix	STPCLK# deassertion not recognized for 5 CLKs after BRDY# returned
11	X	X	X	X	X	PP14	NoFix	NMI or INIT during HALT within an SMM may cause large amount of bus activity
12	X	X	X		X	PP17	NoFix	STPCLK# restrictions during EWBE#
13	X	X					Fixed	CLK required for UP# to be driven
14	X	X				PP18	Fixed	Multiple allocations into branch target buffer
15	X	X	X			PP24	NoFix	FLUSH#, INIT or Machine Check dropped due to floating-point exception
16	X	X	X			PP25	NoFix	Floating-point operations may clear Alignment Check bit
17	X	X	X			PP26	NoFix	CMPXCHG8B across page boundary may cause invalid opcode exception
18	X	X	X			PP27	NoFix	Single-step debug exception breaks out of HALT
19	X	X	X			PP28	NoFix	Branch trace message corruption
20	X	X	X			PP32	NoFix	EIP altered after specific FP operations followed by MOV Sreg, Reg
21	X	X	X	X	X	PP33	NoFix	WRMSR into illegal MSR does not generate GP fault
22	X	X	X			PP34	NoFix	Inconsistent data cache state from concurrent snoop and memory write
23	X	X	X	X	X	PP36	NoFix	Incorrect FIP after RESET
24	X						Fixed	Errors in least significant bit of an FMUL instruction result with specific operands
25	X	X	X	X	X	PP37	NoFix	Second assertion of FLUSH# not ignored
26	X	X	X			PP9	NoFix	SMIACT# premature assertion during replacement writeback cycle
27	X	X	X	X	X	PP38	NoFix	Segment limit violation by FPU operand may corrupt FPU state

NO.	B1	B2	C0	tA0	aC0	Refer to:	Plans	ERRATA (Cont'd.)
28	X	X	X	X	X	PP39	NoFix	FP exception inside SMM with pending NMI hangs system
29	X	X	X			PP40	NoFix	Current in Stop Clock state exceeds specification
30	X	X	X	X	X	PP43	NoFix	Data breakpoint deviations
31	X	X	X	X	X	PP44	NoFix	Event monitor counting discrepancies
32	X	X	X	X	X	PP45	NoFix	VERR type instructions causing page fault task switch with T bit set may corrupt CS:EIP
33	X	X	X		X	PP48	NoFix	Matched but disabled data breakpoint can be lost by STPCLK# assertion
34	X	X	X		X	PP49	NoFix	STPCLK# ignored in SMM when INIT or NMI pending
35	X	X	X	X	X	PP51	NoFix	A fault causing a page fault can cause an instruction to execute twice
36	X	X	X	X	X	PP53	NoFix	FBSTP stores BCD operand incorrectly if address wrap & FPU error both occur
37	X	X	X	X	X	PP54	NoFix	V86 interrupt routine at illegal privilege level can cause spurious pushes to stack
38	X	X	X	X	X	PP55	NoFix	Corrupted HLT flag can cause skipped or incorrect instruction, or CPU hang
39	X	X	X	X	X	PP56	NoFix	Benign exceptions can erroneously cause double fault
40	X	X	X	X	X	PP57	NoFix	Double fault counter may not increment correctly
41	X	X	X	X	X	PP59	NoFix	Short form of mov EAX/ AX/ AL may not pair
42	X	X	X	X	X	PP60	NoFix	Turning off paging may result in prefetch to random location
43	X	X	X		X	PP61	NoFix	STPCLK# or FLUSH# after STI
44	X	X	X		X	PP62	NoFix	REP string instruction not interruptable by STPCLK#
45	X	X	X	X	X	PP63	NoFix	Single step may not be reported on first instruction after FLUSH#
46	X	X	X	X	X	PP66	NoFix	STPCLK# on RSM to HLT causes non-standard behavior
47				X	X	PP15	NoFix	RUNBIST restrictions when run through boundary scan circuitry
48				X	X	PP46	NoFix	BUSCHK# interrupt has wrong priority
49					X	PP50	NoFix	STPCLK# pullup not engaged at RESET
50				X	X	PP52	NoFix	Machine check exception pending, then HLT, can cause skipped or incorrect instruction, or CPU hang

NO.	B1	B2	C0	tA0	aC0	Refer to:	Plans	ERRATA (Cont'd.)
51				X		PP64	NoFix	Double fault may generate illegal bus cycle
52				X	X	PP65	NoFix	TRST# not asynchronous
53				X			NoFix	I/O Buffer Leakage
54				X			NoFix	Break in Boundary Scan Chain
55				X	X		NoFix	Incorrect type field in CPUID
56	X	X	X	X	X	PP67	NoFix	Code cache dump may cause wrong IERR#
57	X	X	X	X	X	PP68	NoFix	Asserting TRST# pin or issuing JTAG instructions does not exit TAP Hi-Z state
58				X			Fix	CLK input capacitance exceeds specification
59	**X**	**X**	**X**	**X**	**X**	**PP69**	**NoFix**	**ADS# may be delayed after HLDA deassertion**
NO.	**B1**	**B2**	**C0**	**tA0**	**aC0**	**Refer to:**	**Plans**	**SPECIFICATION CLARIFICATIONS**
1	X	X	X				Doc	CACHE#, KEN# and BLAST# Behavior
2	X	X	X				Doc	Behavior of writeback support pins in writethrough mode
3	X	X	X				Doc	HITM# deassertion behavior
4	X	X	X	X	X	PP6	Doc	Only one SMI# can be latched during SMM
5	X	X	X	X	X	PP11	Doc	SMIACT# handling during snoop writeback
6	X	X	X	X	X	PP15	Doc	Event monitor counters
7	X	X	X	X	X	PP17	Doc	NMI signal description
8	X	X	X	X	X	PP18	Doc	BTB behavior when entering SMM
9	X	X	X	X	X	PP19	Doc	SMI# activation may cause a nested NMI handling
10	X	X	X	X	X	PP20	Doc	Exiting shutdown with NMI
11	X	X	X	X	X	PP22	Doc	Code breakpoints set on meaningless prefixes not guaranteed to be recognized
12	X	X	X	X	X	PP23	Doc	Resume flag should be set by software
13	X	X	X	X	X	PP24	Doc	Data breakpoints on INS delayed one iteration
14	X	X	X	X	X	PP26	Doc	CPUID Feature flags
15				X	X	PP14	Doc	EADS# recognition
16				X	X	PP16	Doc	KEN# sets cacheability for restarted cycles
17	X	X	X	X	X	PP30	Doc	When L1 cache disabled, inquire cycles are blocked
18	X	X	X	X	X	PP32	Doc	Cache test registers are modified during FLUSH#

NO.	B1	B2	C0	tA0	aC0	Refer to:	Plans	SPECIFICATION CLARIFICATIONS (Cont'd.)
19	X	X	X	X	X	PP33	Doc	For correct translations, the TLB should be flushed after the PSE bit in CR4 is set
20	X	X	X	X	X	PP36	Doc	Extra code break can occur on I/O or HLT instruction if SMI coincides
21	X	X	X	X	X	PP37	Doc	4-MByte page extensions
22				X	X	PP5	Doc	Pullup/pulldown resistor values for some configuration pins
NO.	B1	B2	C0	tA0	aC0	Refer to:	Plans	DOCUMENTATION CHANGES
1	X	X	X	X	X	PP4	Doc	JMP cannot do a nested task switch, Volume 3, page 13-12
2	X	X	X	X	X	PP6	Doc	Interrupt sampling window, Volume 3, page 23-39
3	X	X	X	X	X	PP7	Doc	Errors in the detailed descriptions of FSUB, FSUBR, FDIV, FDIVR and related instructions
4	X	X	X	X	X	PP8	Doc	Figures of TR1 and TR12, Volume 1, page 33-13 and page 33-16
5	X	X	X	X	X	PP10	Doc	PUSHA, PUSHF, POPA & POPF can cause alignment faults
6	X	X	X	X	X	PP11	Doc	Corrections to BT, BTC, BTR and BTS instruction descriptions
7	X	X	X	X	X	PP12	Doc	Corrections for description of a stack overflow on interrupt to inner privilege case
8	X	X	X	X	X	PP13	Doc	FSETPM is like NOP, not like FNOP
9	X	X	X	X	X	PP14	Doc	Corrections in the pseudocode descriptions of the instructions CALL, IRET(D) & RET
10				X	X	PP3	Doc	BF1 pin location, volume 1, page 17-3 and 17-5
11	X	X	X	X	X	PP15	Doc	Errors in 3 tables of special descriptor types
12	X	X	X	X	X	PP16	Doc	Execution tracing - fast messages

SPECIFICATION CHANGES

The Specification Changes listed in this section apply to the Pentium OverDrive Processor datasheets. All Specification Changes will be incorporated into future versions of the appropriate document(s).

1. Clock Low Time (t_3) Change

The AC timings for the Pentium OverDrive processor CLK low time have been changed to better meet the needs of the installed base of Intel486 processor-based systems. The change to the Pentium OverDrive processor CLK low time specification applies to the Pentium OverDrive processor only, and does not affect any other clock specifications, such as CLK High time or rise/fall specifications.

NEW SPECIFICATIONS

Pentium® OverDrive® Processor 25 MHz AC Characteristics
V_{CC} = 5V ±5%; T_A(IN) = 10°C T_O +55°C; C_L = 50PF unless otherwise specified

Symbol	Parameter	Min	Max	Unit
t_3	CLK Low Time	11		nS

Pentium® OverDrive® Processor 33 MHz AC Characteristics
V_{CC} = 5V ±5%; T_A(IN) = 10°C T_O +55°C; C_L = 50PF unless otherwise specified

Symbol	Parameter	Min	Max	Unit
t_3	CLK Low Time	8		nS

2. Removal of V_{CC} Pin A4

To resolve compatibility concerns with a limited number of incorrectly designed motherboards, pin A4 (V_{CC}) will be removed from the Pentium OverDrive processors and will no longer be present on the package. The removal of this V_{CC} pin will not adversely affect the operation of the processor due to the large number of V_{SS} and V_{CC} pins remaining in the outer row.

3. Minimum Operating Temperature

The specification for the minimum operating temperature of the Pentium OverDrive processors has been changed. All other temperature specifications, such as the absolute maximum ratings, remained unchanged. The new temperature specification is detailed in the table below:

$T_{A(IN)}$ Old Specification (°C)	$T_{A(IN)}$ New Specification (°C)
0 to +55	10 to +55

4-5. Refer to Summary Table of Changes

6. Maximum I_{CC} Values

The maximum current requirements originally estimated for the Pentium Over Drive processors were found to be slightly lower than the actual values. The new values are listed in the table below.

Old max	New max	Notes
1.9 A	2.2 A	@ 63/25 MHz
2.6 A	2.8 A	@ 83/33 MHz

7-8. Refer to Summary Table of Changes

ERRATA

1 - 5. Refer to Summary Table of Changes

6. BIST Disabled

PROBLEM: The current production stepping of the Pentium OverDrive processor has disabled the Built-In Self Test (BIST) functionality.

IMPLICATION: If BIST is performed (AHOLD high at the falling edge of RESET), the processor will not actually perform the BIST, but will return a value of 'zero' in the EAX register to indicate that all tests have passed.

WORKAROUND: None required.

STATUS: This erratum has been fixed in the C-0 stepping.

7. Maximum I_{CC} Usage (Refer to Spec. Change 6.)

8 - 12. Refer to Summary Table of Changes

13. CLK Required for UP# to be Driven

PROBLEM: The Upgrade Present (UP#) output pin is intended to be driven low after power-up to indicate that an upgrade processor is present in the system. The UP# pin on the Pentium OverDrive processor requires that the CLK input toggle while the system is starting to insure that RESET reaches the UP# circuitry. If CLK does not toggle, UP# may or may not be driven low, depending on the initial state of the UP# circuitry.

IMPLICATION: If an Intel486 processor system is dependent on having UP# driven low before driving the CLK input on the Pentium OverDrive processor, it may never boot since CLK may never be driven to the processor if UP# remains high. This is generally only a potential issue in systems with two processor sites, such as those with a surface-mount Intel486 processor and a PGA upgrade processor site.

WORKAROUND: Most two site systems have the ability to disable the processor in the surface-mount location so that a different Intel486 (non-upgrade) processor may be used in the PGA socket location. If the system has a jumper or switch that is documented to specifically disable the surface mount processor (or the original processor in a two socket system), use it to disable the second processor and thereby route the CLK signal to the upgrade PGA socket location.

STATUS: This erratum has been fixed in the C-0 stepping.

14. Multiple Allocations Into Branch Target Buffer

PROBLEM: Please refer to Part II of this document. This errata entry for the Pentium OverDrive processor has been added for clarification of the issue as it applies to this processor specifically.

IMPLICATION: Please refer to Part II of this document.

WORKAROUND: Please refer to Part II of this document.

STATUS: This erratum has been fixed in the C-0 stepping. Although this erratum has been recreated in proprietary Intel test systems, it has not been observed on a Pentium OverDrive processor in an actual personal computer system.

15 - 23. Refer to Summary Table of Changes

24. Errors in Least Significant Bit of an FMUL Instruction Result With Specific Operands

PROBLEM: The result of multiplying two operands, one of which is typically close to infinity or close to the smallest representable normal number, may be incorrect in the Least Significant Bit (LSB) and may result in flags that are incorrectly set. This problem is limited to a small percentage of the first production units of the 63MHz Pentium OverDrive processor (specification number SZ953, Ver#: 1.0).

All precisions: single, double and extended are affected. All rounding modes: nearest, up, down and chop are affected. Only specific operand pairs result in errors.

IMPLICATION: Only a fraction of the Pentium OverDrive processors may produce errors in the least significant bit of the result when using the FMUL instruction with one of these specific input operands. Any of the exception flag bits in the FPU status word may also be incorrect.

WORKAROUND: None identified. Intel includes software with the Pentium OverDrive processor that can detect this erratum. Please see the following Status paragraph.

STATUS: The Pentium OverDrive processors currently in production are free from this defect. Only a fraction of the first production units at 63-MHz marked SZ953 may exhibit the defect. Owners of Pentium OverDrive processors should run the diagnostics on the disk supplied with the Pentium OverDrive processor. The diagnostic program tests the processor and will notify the user of pass/fail information. Should the processor fail, the diagnostic program will report that "The Floating Point Conformance Test has Failed" and will wait for a keystroke before continuing. Owners of the Pentium OverDrive processor should contact the Intel support line if there are any questions.

25. Second Assertion of FLUSH# Not Ignored

PROBLEM: Please refer to Part II of this document. This errata entry for the Pentium OverDrive processors has been added for clarification of the issue as it applies to these OverDrive processors specifically.

IMPLICATION: This erratum applies to the Pentium OverDrive processor in Enhanced (WB) bus mode only . Standard bus mode (WT) is not affected. Please refer to Part II of this document for more information.

WORKAROUND: Please refer to Part II of this document

STATUS: For the steppings affected, please see the Summary of Changes table at the beginning of this section.

26 - 28. Refer to Summary Table of Changes

29. Current in Stop Clock State Exceeds Specification

PROBLEM: Please refer to Part II of this document. This errata entry for the Pentium OverDrive processors has been added for clarification of the issue as it applies to these OverDrive processors specifically.

IMPLICATION: Please refer to Part II of this document for more information.

WORKAROUND: None Identified. The workaround as stated in Part II of this document is not valid for the Pentium OverDrive processor since the boundary scan pins are not available on production units.

STATUS: For the steppings affected, please see the Summary of Changes table at the beginning of this section.

30-38. Refer to Summary Table of Changes

39. Benign Exceptions Can Erroneously Cause Double Fault

PROBLEM: Please refer to Part II of this document. This errata entry for the Pentium OverDrive processors has been added for clarification of the issue as it applies to these OverDrive processors specifically.

IMPLICATION: This erratum applies to the Pentium OverDrive processor in Case 1 only. Case 2 "A machine check exception (INT 18) is generated" does not apply. Please refer to Part II of this document for more information.

WORKAROUND: Please refer to Part II of this document

STATUS: For the steppings affected, please see the Summary of Changes table at the beginning of this section.

40-42. Refer to Summary Table of Changes

43. STPCLK# or FLUSH# After STI

PROBLEM: Please refer to Part II of this document. This errata entry for the 63 and 83-MHz Pentium OverDrive processors has been added for clarification of the issue as it applies to these OverDrive processors specifically.

IMPLICATION: In the case of "FLUSH# After STI", this erratum applies to the Pentium OverDrive processor in Enhanced (WB) bus mode only . Standard bus mode (WT) is not affected. Please refer to Part II of this document for more information.

WORKAROUND: Please refer to Part II of this document.

STATUS: For the steppings affected, please see the Summary of Changes table at the beginning of this section.

44. Refer to Summary Table of Changes

45. Single Step May Not be Reported on First Instruction After FLUSH#

PROBLEM: Please refer to Part II of this document. This errata entry for the 63 and 83-MHz Pentium OverDrive processors has been added for clarification of the issue as it applies to these OverDrive processors specifically.

IMPLICATION: This erratum applies to the Pentium OverDrive processor in Enhanced (WB) bus mode only . Standard bus mode (WT) is not affected. Please refer to Part II of this document for more information.

WORKAROUND: Please refer to Part II of this document.

STATUS: For the steppings affected, please see the Summary of Changes table at the beginning of this section.

46-52. Refer to Summary Table of Changes

53. I/O Buffer Leakage

PROBLEM: When an I/O pin is driven high by the Pentium OverDrive processor and then tri-stated, the output is still weakly driven high until the line is driven low by either the processor or another source.

IMPLICATION: If a weak pull-down (greater than 1kΩ) is used on a signal line and the value of the line is expected at a given time after being tri-stated by the processor, the incorrect value can be read.

WORKAROUND: None identified at this time.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

54. Break in Boundary Scan Chain

PROBLEM: The boundary scan problem can most easily be described as a broken link in the boundary scan chain. The effects of this broken link on the output testing are minimal, since the majority of the chain is before the break. This part of the chain can still be filled, and the data sent to the output pins. However, any pins after the break will not be able to send out the correct output data. The effects of this broken link on input testing are more drastic. Only the last four cells worth of data can be collected at the boundary scan output. With respect to operating with other devices, the boundary scan chain will not not be able to shift data through the processor to other devices.

IMPLICATION: This problem only affects operation of the component while in boundary scan mode.

WORKAROUND: The bypass mode for the processor does still work, so other devices in the boundary scan chain can be accessed using this method.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

55. Incorrect Type Field in CPUID

PROBLEM: Execution of the CPUID with a '1' in the EAX register does not return a value of '01' (OverDrive Processor installed) in the type field (Bits 13.12). Instead it returns a '00' (Primary Processor) in the type field.

IMPLICATION: BIOS or application software that relies on the type field to be '01' when an OverDrive processor is installed, may function improperly.

WORKAROUND: BIOS or application software should be written to function properly when '00' is returned in the type field and an OverDrive processor is present in the system.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section

56. Refer to Summary Table of Changes

57. Asserting TRST# Pin or Issuing JTAG Instructions Does not Exit TAP Hi-Z State

PROBLEM: Please refer to Part II of this document. This errata entry for the Pentium OverDrive processor has been added for clarification of the issue as it applies to the 63- and 83-MHz Pentium OverDrive processors for Intel486™ processor-based systems specifically.

IMPLICATION: This erratum applies to the 63- and 83-MHz Pentium OverDrive processors only when issuing JTAG instructions. The 63- and 83-MHz Pentium OverDrive processors do not have a TRST# pin. Please refer to Part II of this document for more information.

WORKAROUND: Please refer to Part II of this document.

STATUS: For the steppings affected, please see the Summary of Changes table at the beginning of this section.

58. CLK Input Capacitance Exceeds Specification

PROBLEM: The input capacitance on the CLK pin is higher than the specification due to the ceramic package design. The specification for the 120/133-MHz Pentium OverDrive processor's input capacitance is 8pF whereas the measured value on the clock pin is 13pF. This added capacitance may cause excessive ringback on the CLK signal.

IMPLICATION: If the CLK signal going to the processor is also used as an input to another device, the ringback can cause the other device to detect an incorrect rising edge on CLK. This can cause the system to not boot or to hang. Only a small percentage of systems appear to be affected by the higher capacitance.

The only confirmed issue is related to some boards with an Intel 82430LX chipset. The 82434LX PCMC's HCLKA output is used to drive the clock to the processor. This clock signal may also be used as a feedback to the chipset to minimize the clock skew between the CPU and PCMC. The capacitance difference will create a reflection on the clock signal that, if sufficient in amplitude, will cause the PCMC to detect a false clock edge and the bus state machines to get out of synchronization causing the system to lock up. This condition is dependent upon not only the capacitance difference but also the physical board design and voltage threshold of the chipset.

WORKAROUND: If an end user experiences any problems, they should remove the Pentium OverDrive processor and install the original 60/66-MHz Pentium processor. The end user should then contact the Intel Customer Support Hotline listed on the OverDrive processor retail box for assistance.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section

59. Refer to Summary Table of Changes

SPECIFICATION CLARIFICATIONS

1. CACHE#, KEN# and BLAST# Behavior

If CACHE# is driven LOW during a read cycle, this implies that the processor intends to perform a linefill; however, this does not imply that BLAST# will be driven HIGH. As with the IntelDX2™ processor, KEN# controls the cacheability of data and can be used to refuse the linefill. If the processor requires only one transfer to get the required data, BLAST# will be driven LOW if KEN# is sampled HIGH.

2. Behavior of Writeback Support Pins in Writethrough Mode

Three new output pins are used to support the internal writeback cache of the Pentium OverDrive processor. These pins are HIT#, HITM# and CACHE#. The writeback mode of the processor can be enabled by driving the WB/WT# pin to the appropriate state during the falling edge of RESET. The clarification is as follows:

The three internal writeback support pins will be driven at all times regardless of the processor cache mode (enhanced (writeback) or standard (writethrough)). This implies that the HIT# and HITM# pins will always be driven HIGH in writethrough mode since there can be no writeback cycles. It also implies that in writethrough mode, the CACHE# pin will be toggled normally for reads and will be driven HIGH for all write cycles.

3. HITM# Deassertion Behavior

The HITM# pin is driven LOW in response to an external snoop that hits a modified line in the cache. It remains low until an appropriate action occurs (usually a writeback cycle) to maintain consistency with main memory. The clarification deals with the deassertion of HITM#.

Previously available documentation stated that HITM# will be driven inactive "after the last RDY#/BRDY# of the writeback cycle" and is "guaranteed to be deasserted before the next ADS#." This means that HITM# can be deasserted anytime between these two points, and hardware should not assume that HITM# is deasserted on any specific CLK. It also implies that the system design should not depend on the Pentium OverDrive processor to deassert HITM# in the same clock the writeback Enhanced IntelDX2 processor.

4. Refer to Summary Table of Changes

5. SMIACT# Handling During Snoop Writeback

Please refer to Part II of this document. This errata entry for the 63 and 83-MHz Pentium OverDrive processors has been added for clarification of the issue as it applies to these OverDrive processors specifically. This erratum applies to the Pentium OverDrive processor in Enhanced (WB) bus mode only . Standard bus mode (WT) is not affected.

6-17. Refer to Summary Table of Changes

18. Cache Test Regs Are Modified During FLUSH#

Please refer to Part II of this document. This errata entry for the Pentium OverDrive processor has been added for clarification of the issue as it applies to these OverDrive processors specifically. This erratum applies to the the 63- and 83-MHz Pentium OverDrive processors in Enhanced (WB) bus mode only. Standard bus mode (WT) is not affected.

19-21. Refer to Summary Table of Changes

22. Pullup/Pulldown Resistor Values for Some Configuration Changes

Please refer to Part II of this document for more details. This specification clarification entry has been added for clarification as it applies to these OverDrive processors specifically. This specification clarification applies to the 120/133-MHz Pentium OverDrive processor only for the BUSCHK# signal. This specification clarification applies to the 125, 150, and 166-MHz Pentium OverDrive processors only for the BUSCHK# and BRDYC# signals.

DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the Pentium OverDrive processor datasheets. All Documentation Changes will be incorporated into the appropriate documentation.

1-12. Refer to Summary Table of Changes