mosaic

Mosaic Semiconductor Inc.

128K x 8 SRAM

MSM8128X-45/55/70

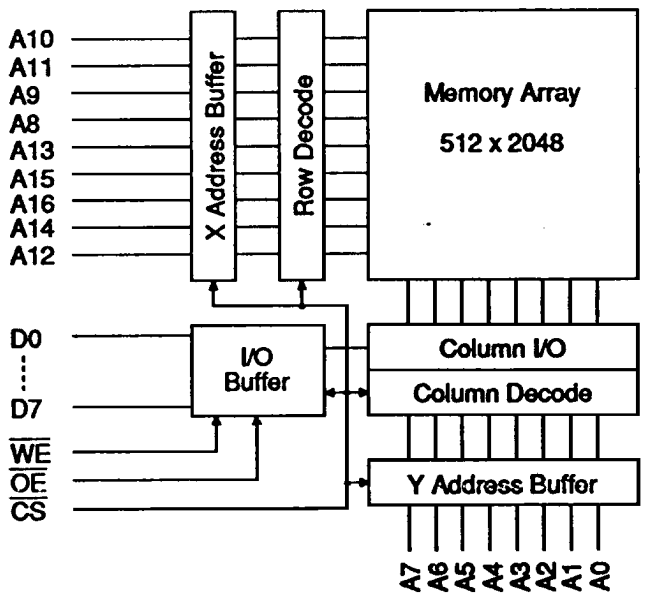
Issue 3.1: April 1992

131,072 x 8 CMOS High Speed Static RAM

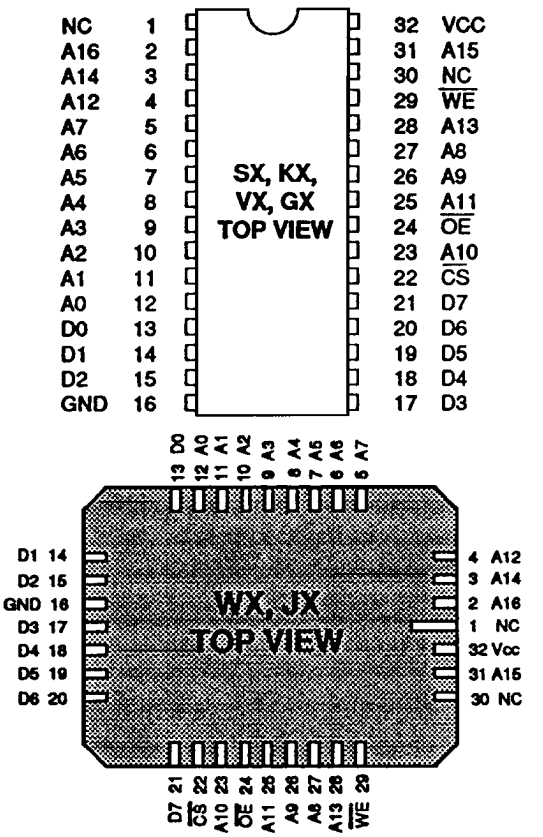
Features

Very Fast Access Times of 45/55/70 ns
JEDEC Compatible to the 1 Megabit Module
VIL™ High Density Package Available
Low Power Standby 50 µW (typ.)
Low Power Operation 150 mW(typ.)
Completely Static Operation
Equal Access and Cycle Times
Directly TTL compatible
Common data inputs & outputs
May be processed in accordance with MIL-STD-883D

Block Diagram



Pin Definition



Pin Functions

A0-A16	Address Inputs
D0-7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
NC	No Connect
V_{cc}	Power (+5V)
GND	Ground

Package Details

Pin Count	Description	Package Type	Material	Pin Out
32	0.6" Dual-in-Line (DIP)	SX	Ceramic	JEDEC ASIC
32	0.4" Dual-in-Line (DIP)	KX	Ceramic	JEDEC ASIC
32	0.1" Vertical-in-Line (VIL™)	VX	Ceramic	JEDEC ASIC
32	Bottom Brazed FlatPack	GX	Ceramic	JEDEC ASIC
32	Extended Leadless Chip Carrier (LCC)	WX	Ceramic	JEDEC ASIC
32	J-Leaded Chip Carrier (JLCC)	JX	Ceramic	JEDEC ASIC

Package dimensions and outlines are displayed on pages 6&7.

VIL is a trademark of Mosaic Semiconductor, Patent number D316251

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}	V_T	-0.5V to +7	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-55 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
(2) V_T can be -3.0V pulse of less than 30ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	5.8	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (8128I)
	T_{AM}	-55	-	125	°C (8128M, MB)

Note : (1) V_{IL} can be -3.0V pulse of less than 30ns.

DC Electrical Characteristics (V_{CC} = 5.0V±10%, T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI}	V_{IN}=0V to V_{CC}	-	-	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH}, $V_{I/O}$=0V to V_{CC}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}	-	-	2	µA
Operating Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA, I/P's Static	-	30	80	mA
Average Supply Current	I_{CC1}	$I_{I/O}$=0mA, Min. Cycle, Duty=100%, WE=V_{IH}	-	60	120	mA
StandbySupplyCurrent	I_{SB}	$\overline{CS}$=V_{IH}, V_{IN}=V_{IH} or V_{IL}	-	-	15	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, .2V≥V_{IN}≥V_{CC}-.2V	-	0.01	2	mA
Output Voltage	V_{OL}	I_{OL}=6.0mA for -45 and -55 speed device I_{OL}=2.1 mA for -70 speed device	-	-	0.4	V
	V_{OH}	I_{OH}=-4.0mA for -45 and -55 speed device I_{OH}=-1 mA for -70 speed device	2.4	-	-	V

Note: (1) Typical values are at V_{CC}=5.0V, T_A=25°C and specified loading.

Capacitance (V_{CC}=5V±10%, T_A=25°C)

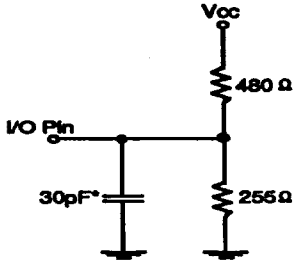
Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
I/P Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	7	pF

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: See Load Diagram
* V_{CC}=5V±10%

Output Load



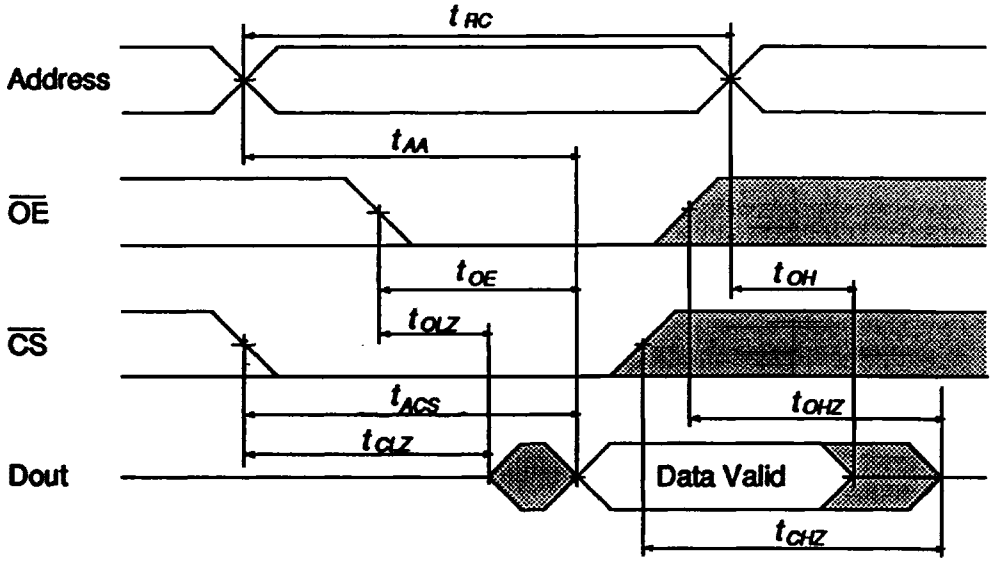
*Including scope and jig

Electrical Characteristics & Recommended AC Operating Conditions

Read Cycle

Parameter	Symbol	-45 min	-45 max	-55 min	-55 max	-70 min	-70 max	Units
Read Cycle Time	t_{RC}	45	-	55	-	70	-	ns
Address Access Time	t_{AA}	-	45	-	55	-	70	ns
Chip Select Access Time	t_{ACS}	-	45	-	55	-	70	ns
Output Enable to Output Valid	t_{OE}	-	25	-	30	-	35	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	ns
Chip Selection to Output in Low Z(3)	t_{CLZ}	5	-	5	-	5	-	ns
Output Enable to Output in Low Z(3)	t_{OLZ}	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z(3)	t_{CHZ}	0	20	-	25	-	30	ns
Output Disable to Output in High Z(3)	t_{OHZ}	0	20	-	25	-	30	ns

Read Cycle Timing Waveform (1,2)

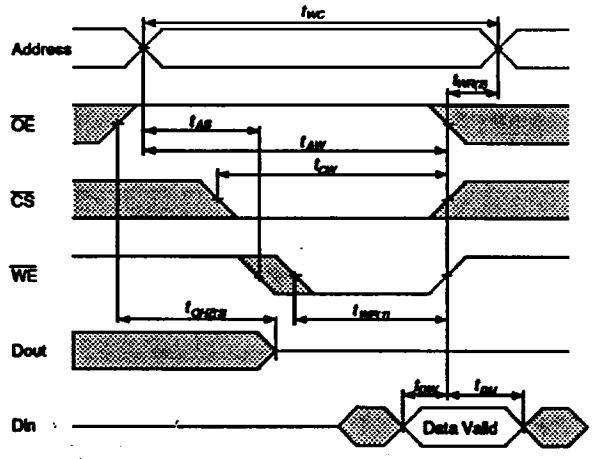


Notes:
(1) $\overline{WE}$ is High for Read Cycle.
(2) Address valid prior to or coincident with $\overline{CS}$ transition Low.
(3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

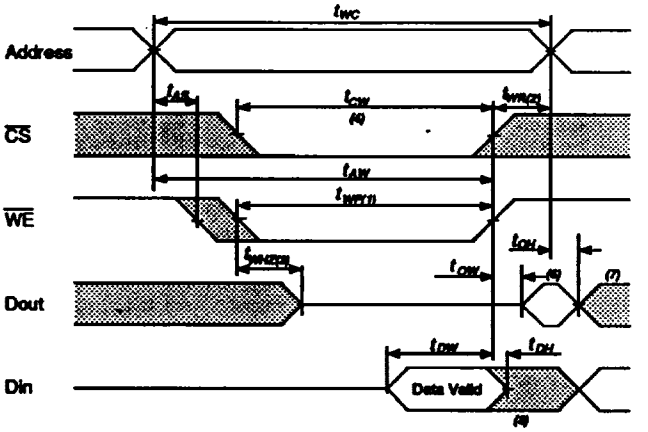
Write Cycle

Parameter	Symbol	-45 min	-45 max	-55 min	-55 max	-70 min	-70 max	Unit
Write Cycle Time	t_{WC}	45	-	55	-	70	-	ns
Chip Selection to End of Write	t_{CW}	40	-	45	-	50	-	ns
Address Valid to End of Write	t_{AW}	40	-	45	-	50	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	35	-	40	-	45	-	ns
Write Recovery Time	t_{WR}	5	-	5	-	5	-	ns
Write to Output in High Z(9)	t_{WHZ}	0	15	0	15	0	15	ns
Data to Write Time Overlap	t_{DW}	20	-	25	-	30	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}	5	-	5	-	5	-	ns

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform (5)



AC Characteristics Notes

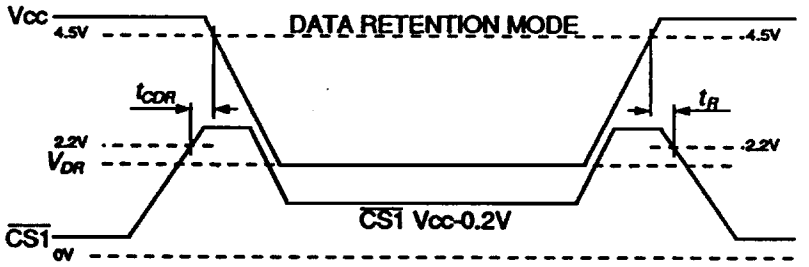
(1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
(2) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
(3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
(4) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
(5) $\overline{OE}$ is continuously low. ($\overline{OE}$=V_s)
(6) Dout is in the same phase as written data of this write cycle.
(7) Dout is the read data of next address.
(8) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.
(9) t_{WHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Low V_{cc} Data Retention Characteristics - L Version Only (T_A=-55°C to +125°C)

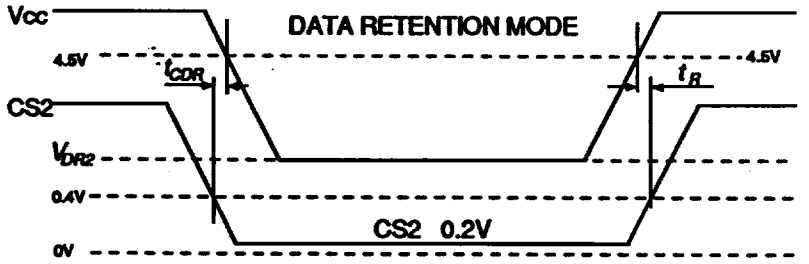
Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{CC}$-0.2V, CS2 ≥ V_{CC}-0.2V or 0V ≤ CS2 ≤ 0.2V. $V_{IN} \geq$ 0V	2.0	-	-	V
Data Retention Current	I_{CCDR}	V_{CC}=3.0V, $V_{IN} \geq$ 0V, $\overline{CS1} \geq V_{CC}$-0.2V, CS2 ≥ V_{CC}-0.2V or 0V ≤ CS2 ≤ 0.2V.	-	-	700	µA
Chip Deselect to Data Retention	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

Notes (1) CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer and $\overline{OE}$ buffer. If CS2 controls data retention mode, Vin levels ($\overline{WE}$,$\overline{OE}$,$\overline{CS1}$,I/O) can be in the high impedance state. If $\overline{CS1}$ controls Data Retention mode, CS2 must be ≥ V_{CC} - 0.2V or 0V ≤ CS2 ≤ 0.2V. The other input levels (address, $\overline{WE}$,$\overline{OE}$,I/O) can be in the high impedance state.

Low V_{CC} Data Retention Timing Waveform 1 ($\overline{CS1}$ controlled)

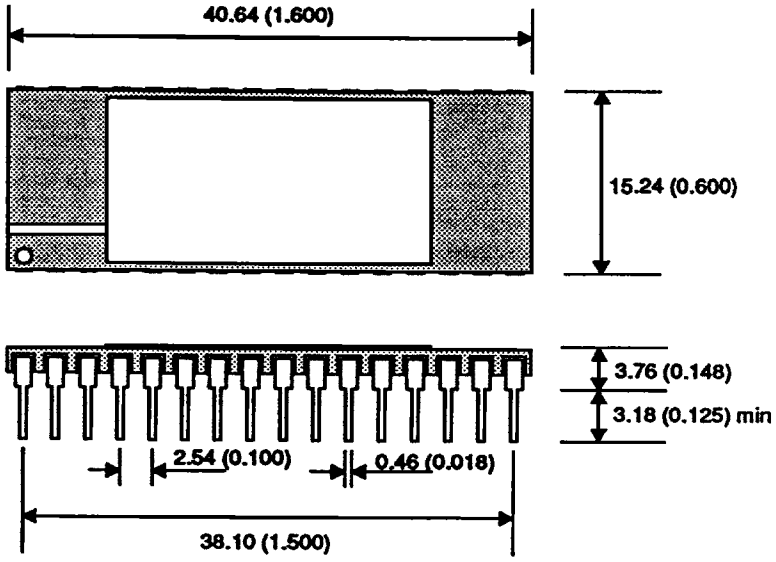


Low V_{CC} Data Retention Timing Waveform 2 (CS2 controlled)

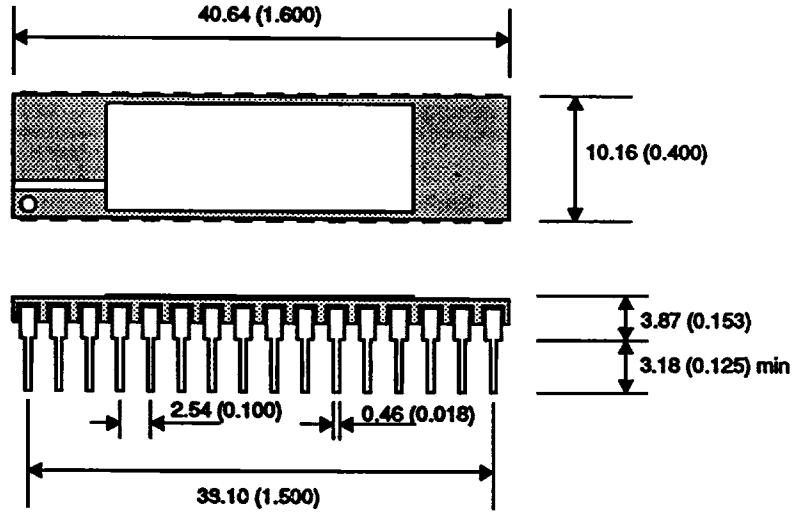


Package Details

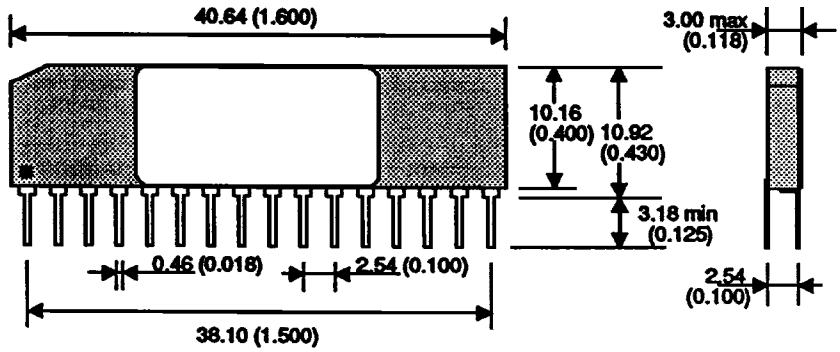
32 pin 0.6" Dual-In-Line (DIP) - 'SX' Package



32 pin 0.4" Dual-In-Line (DIP) - 'KX' Package

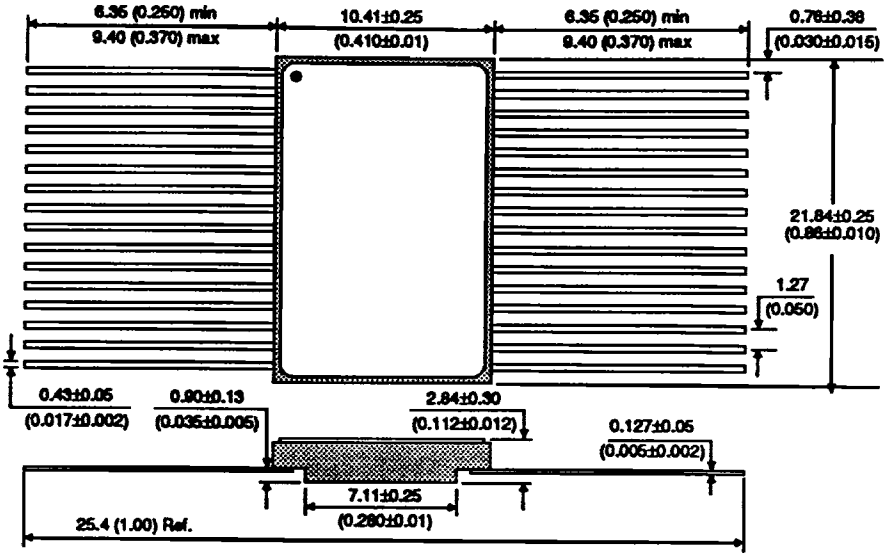


32 pin 0.1" Vertical-In-Line (VIL™) - 'VX' Package

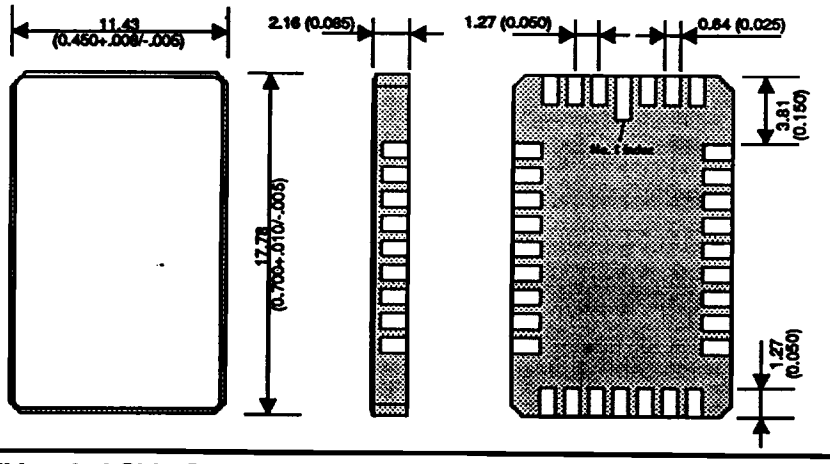


All dimensions in mm (inches). Tolerance on all dimensions +/-0.254 (0.010).

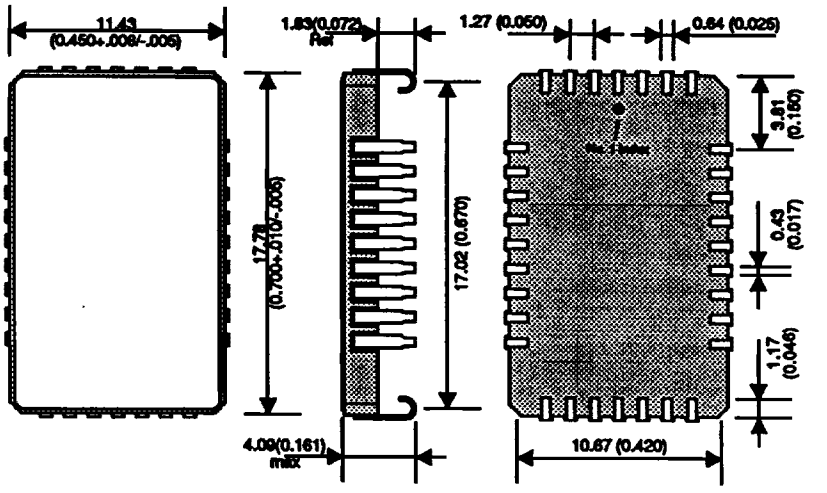
32 pin Ceramic Flatpack - 'GX' Package



32 pin Extended Leadless Chip Carrier (LCC) - 'WX' Package



32 pin Extended 'J' Leaded Chip Carrier (JLCC) - 'JX' Package



All dimensions in mm (inches). Tolerance on all dimensions +/-0.254 (0.010).

Military Screening Procedure

Screening Flow for high reliability non compliant product in accordance with MIL-STD-883D Method 5004 is detailed below.

MB COMPONENT SCREENING FLOW		
SCREEN	**TEST METHOD**	**LEVEL**
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Constant acceleration	2001 Condition E (Y, only) (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25°C	100%
Burn-in	Method 1015,Condition D,T_A=+125°C,160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at T_A=+25°C	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

MSM8128SXLMB-45

Speed	45	= 45 ns
	55	= 55 ns
	70	= 70 ns
Temp. range/screening	Blank	= Commercial
	I	= Industrial
	M	= Military
	MB	= Processed to MIL-STD-883D Method 5004, non-compliant.
	MC	= MIL-STD-883D Compliant
Power Consumption	Blank	= Standard
	L	= Low Power
Package	SX	= 32 pin 0.6" DIP
	KX	= 32 pin 0.4" DIP
	VX	= 32 pin 0.1" VIL
	GX	= 32 lead FlatPack
	WX	= 32 pad LCC
	JX	= 32 pad JLCC

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

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