PEEL™ 22CV8 -5/-7/-10/-25
CMOS Programmable Electrically Erasable Logic Device

Features

- **High Speed, Low Power**
  - Speeds ranging from 5ns to 25ns
  - Less power than quarter-power PALs and GALs
- **CMOS Electrically Erasable Technology**
  - Superior factory testing
  - Reprogrammable in plastic package
  - Reduces retrofit and development costs
- **Development/Programmer Support**
  - Third party software and programmers
  - ICT PLACE Development Software and
  - PDS-3 programmer
- **Architectural Flexibility**
  - 24-pin version of popular PEEL18CV8
  - 74 product term x 44 input array
  - Up to 22 inputs and 8 I/O pins
  - Up to 12 configurations per macrocell
  - Synchronous preset, asynchronous clear
  - Individual product-term driven OE controls
- **Application Versatility**
  - Replaces random logic
  - Super-sets standard PLDs (PAL, GAL, EPLD)
  - Enhanced architecture fits more logic than ordinary PLDs
  - 24-Pin DIP/SOIC/TSSOP, 28-pin PLCC

General Description

The PEEL22CV8 is a Programmable Electrically Erasable Logic (PEEL) device providing an architecture-enhanced low power alternative to ordinary PLDs such as the GAL20V8. The PEEL22CV8 is available in 24-pin DIP/ SOIC/TSSOP and 28-pin PLCC packages (see Figure 1) with speeds ranging from 5ns to 25ns (the 5ns speed grade is available only in the PLCC package). The low power consumption of this device (10mA typical for the 25ns speed grade) makes it ideal for power-sensitive applications such as portable communication equipment, computers and peripherals. EE-reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-reprogrammability also improves factory testability, thus ensuring the highest quality possible. The PEEL22CV8 architecture allows it to replace over 20 standard 24-pin PLDs (PAL, GAL, EPLD, etc.), often at less than half of the power of a quarter power GAL. The device also provides additional architectural features so more logic can be put into every design. Development and programming support for the PEEL22CV8 is provided by popular third-party programmers and development soft-ware. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

Figure 1. Pin Configurations

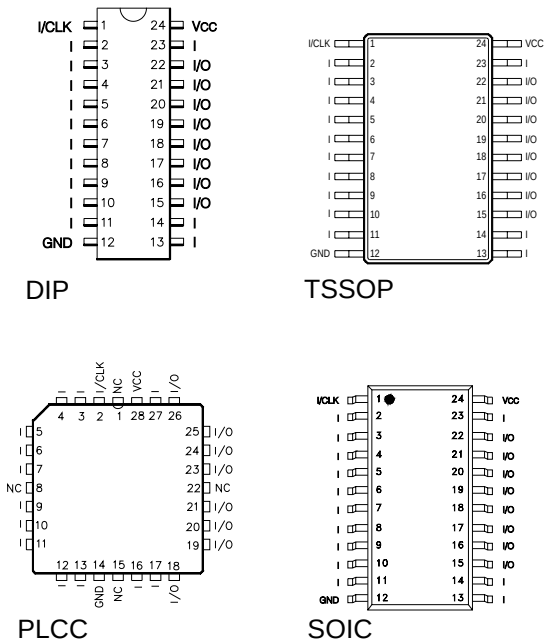
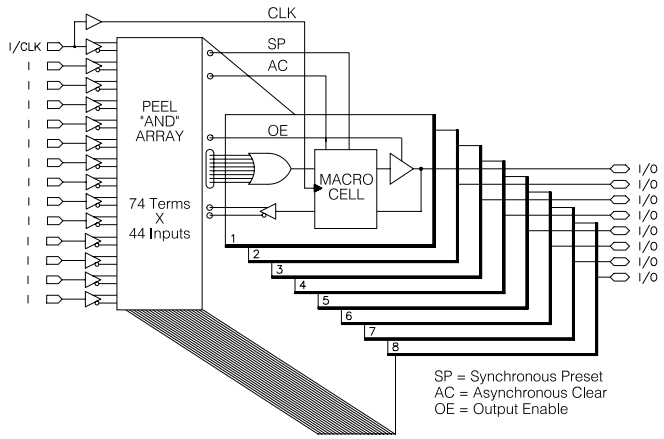


Figure 2. Block Diagram



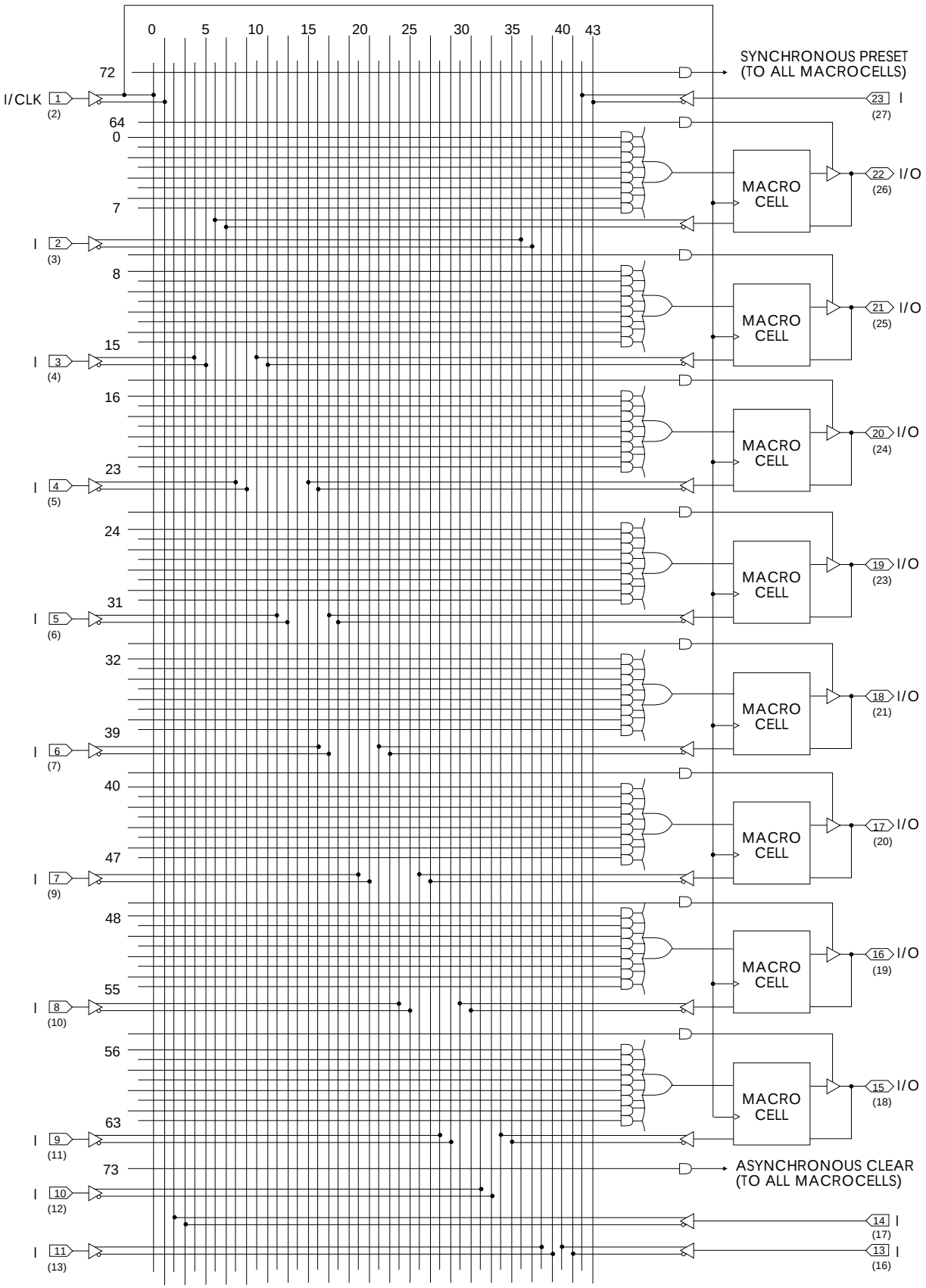


Figure 3. Peel 22CV8 Logic Array Diagram
(Pin numbers are for DIP and SOIC packages, PLCC pin numbers are shown in parentheses.)

Function Description

The PEEL22CV8 implements logic functions as sum-of products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of in-put signals into the array. User-configurable output structures in the form of I/O macrocells further in-crease logic flexibility.

Architecture Overview

The PEEL22CV8 architecture is illustrated in the block diagram of Figure 2. Fourteen dedicated inputs and eight I/Os provide up to 22 inputs and 8 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL22CV8 can implement up to 8 sum-of-products logic expressions.

Associated with each of the 8 OR functions is an I/O macrocell which can be independently programmed to one of 12 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL22CV8 (shown in Figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

- **44 Input Lines:**

  28 input lines carry the true and complement of the signals applied to the 14 input pins
  16 additional lines carry the true and complement values of feedback or input signals from the 8 I/Os

- **74 product terms:**

  64 product terms (arranged in groups of 8) used to form sum-of-products functions
  8 output enable terms (one for each I/O)
  1 global synchronous preset term
  1 global asynchronous clear term

At each input-line/product-term intersection, there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and complement of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections on a product term are opened, a don't care state exists and that term will always be TRUE.

When programming the PEEL22CV8, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program at least one pair of complementary inputs on unused product terms so that they will have no effect on the output function.)

Programmable I/O Macrocell

The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL22CV8 to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in Figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the four EEPROM bits controlling these multiplexers. These bits determine: output polarity, output type (registered or non-registered) and input/feedback path (bi-directional I/O, combinatorial feedback or register feedback). Refer to Table 1 for details.

Equivalent circuits for the twelve macrocell configurations are illustrated in Figure 5. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9 and 10) the macrocell provides eight additional configurations. When creating a PEEL device design, the desired macrocell configuration generally is specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or clocked into the D-type flip-flop (registered function). The D-type flip-flop loads data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if at least one complementary pair of connections is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select

The PEEL22CV8 macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell may be obtained from three different locations: from the I/O pin (bi-directional I/O), directly from the Q output of the flip-flop (registered feedback) or directly from the OR gate (combinatorial feedback).

Bi-directional I/O

The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

Combinatorial Feedback

The signal-select multiplexer gives the macrocell the ability to feedback the output of the OR gate, bypassing the output buffer, regardless of whether the output function is registered or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7 and 8 in Figure 5.)

Registered Feedback

Feedback also can be taken from the register, regardless of whether the output function is to be combinatorial or registered. When implementing combinatorial output functions, registered feedback allows internal registering of states without giving up the use of the external output.

Programmable Input and I/O Pin Pull-ups

The input and I/O pins on this device feature programmable pull-up circuitry which can be globally enabled or disabled during design entry. (In the ICT PLACE software, for example, the pull-ups can be activated by selecting the Design...Auxiliary menu, the default is no pull-ups.) Enabling the pull-ups causes input and I/O pins to be pulled high through nominally 100k ohms.

Design Security

The PEEL22CV8 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

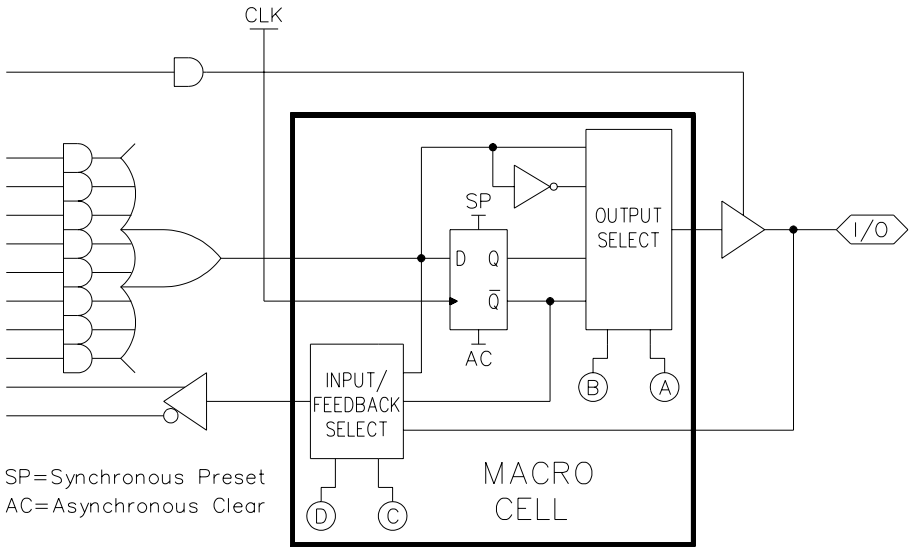


Figure 4. Block Diagram of the PEEL22CV8 I/O Macrocell

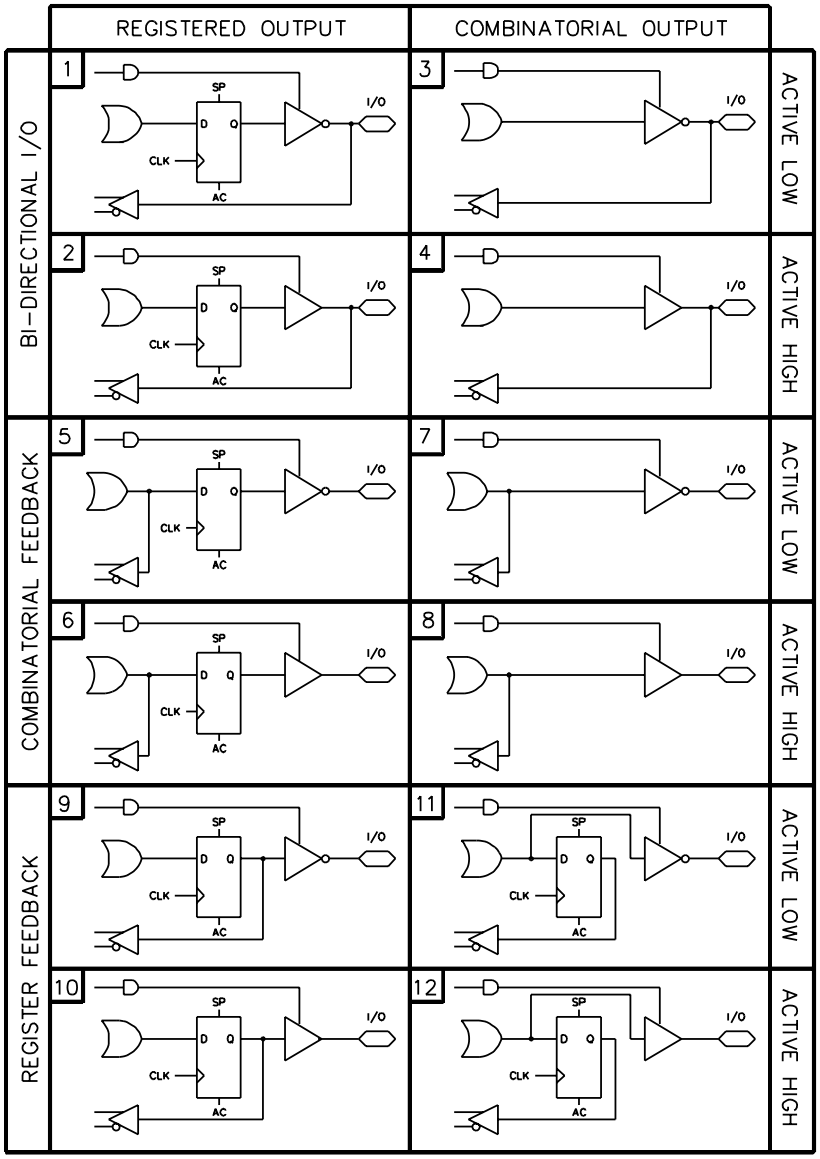


Figure 5. Equivalent Circuits for the Twelve Configurations of the PEEL22CV8 I/O Macrocell

Table 1. PEEL 22CV8 Macrocell Configuration Bits

Configuration					Input/Feedback Select	Output Select	
#	A	B	C	D			
1	1	1	1	1	Bi-Directional I/O	Register	Active Low
2	0	1	1	1			Active High
3	1	0	1	1		Combinatorial	Active Low
4	0	0	1	1			Active High
5	1	1	1	0	Combinatorial Feedback	Register	Active Low
6	0	1	1	0			Active High
7	1	0	1	0		Combinatorial	Active Low
8	0	0	1	0			Active High
9	1	1	0	0	Register Feedback	Register	Active Low
10	0	1	0	0			Active High
11	1	0	0	0		Combinatorial	Active Low
12	0	0	0	0			Active High

This device has been designed and tested for the recommended operating conditions. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin[2]	Relative to Ground[1]	-0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	±25	mA
T_{ST}	Storage Temperature		-65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Table 2. Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Ambient Temperature	Commercial	0	+70	°C
T_R	Clock Rise Time	See Note 3		20	ns
T_F	Clock Fall Time	See Note 3		20	ns
T_{RVCC}	V_{CC} Rise Time	See Note 3		250	ms

Table 3. D.C. Electrical Characteristics over the recommended operating conditions

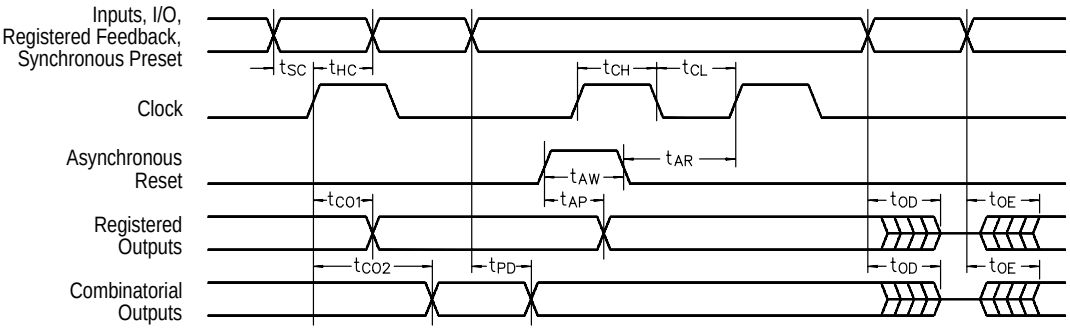
Symbol	Parameter	Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -4.0mA		2.4		V
V_{OHC}	Output HIGH Voltage - CMOS[13]	V_{CC} = Min, I_{OH} = -10µA		V_{CC} - 0.3		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA			0.5	V
V_{OLC}	Output LOW Voltage - CMOS[13]	V_{CC} = Min, I_{OH} = -10µA			0.15	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			-0.3	0.8	V
I_{IL}	Input I/O Leakage Current LOW	V_{CC} = Max, V_{IN} = GND, I/O = High Z			-10	µA
I_{ILP}	Input, I/O Leakage Current LOW-Input and I/O pull-ups enabled	V_{CC} = Max, V_{IN} = GND, I/O = High Z			-100	µA
I_{IH}	Input I/O Leakage Current LOW	V_{CC} = Max, V_{IN} = V_{CC}			10	µA
I_{SC}	Output Short Circuit Current	V_{CC} = 5V, VO = 0.5V[9], T_A= 25°C		-30	-150	mA
I_{CC}[10]	V_{CC} Current (See CR-1 for typical I_{CC})	V_{IN} = 0V or 3V f = 25MHz All outputs disabled[4]	-5	75 (Typ)	110	mA
			-7	60 (Typ)	110	
			-10	60 (Typ)	110	
			-25	10 (Typ)	15	
C_{IN}[7]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1 MHz			6	pF
C_{OUT}[7]	Output Capacitance				12	pF

Table 4. A.C. Electrical Characteristics

Over the Operating Limit[8,11]

Symbol	Parameter	-5		-7		-10		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
tPD	Input[5] to non-registered output		5		7.5		10		25	ns
tOE	Input[5] to output enable[6]		5		7.5		10		20	ns
tOD	Input[5] to output disable[6]		5		7.5		10		20	ns
tCO1	Clock to Output		4		7		7		12	ns
tCO2	Clock to comb. output delay via internal registered feedback		7.5		10		12		30	ns
tCF	Clock to Feedback		2.5		3.5		4		10	ns
tSC	Input[5] or Feedback Setup to Clock	3.5		5		5		15		ns
tHC	Input[5] Hold After Clock	0		0		0		0		ns
tCL, tCH	Clock Low Time, Clock High Time[8]	3		3.5		5		12		ns
tCP	Min Clock Period Ext (tSC + tCO1)	7.5		12		12		27		ns
fMAX1	Internal Feedback (1tSC + tCF)[12]	166.7		117.6		111		40		MHz
fMAX2	External Feedback (1/tCP)[12]	133		83.3		83.3		37		MHz
fMAX3	No Feedback (1/tCL + tCH)[12]	166.7		142.8		100		41.6		MHz
tAW	Asynchronous Reset Pulse Width	5		7.5		10		25		ns
tAP	Input[5] to Asynchronous Reset		5		7.5		10		25	ns
tAR	Asynch. Reset recovery time		5		7.5		10		25	ns
tRESET	Power-on Reset Time for registers in Clear State		5		5		10		5	µs

Switching Waveforms



Notes:

1. Minimum DC input is -0.5V; however, inputs may undershoot to -2.0V for periods less than 20ns.
2. VI and VO are not specified for program/verify operation.
3. Test points for Clock and VCC in tR, tF are referenced at 10% and 90% levels.
4. I/O pins are 0V or 3V.
5. “Input” refers to an input pin signal.
6. .tOE is measured from input transition to VREF ±0.1V, tOD is measured from input transition to VOH - 0.1V or VOL + 0.1V; VREF = VL. See test loads in Section 5 of ICT Data Book.
7. Capacitances are tested on a sample basis.
8. Test conditions assume: signal transition times of 3ns or less form the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
9. Test one output at a time for a duration of less than 1 sec.
10. ICC for a typical application: This parameter is tested with the device programmed as an 10-bit Counter.
11. PEEL Device test loads are specified in Section 6 of the data book.
12. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.
13. Available only for 22CV8-25.

Table 5. Ordering Information

Part Number	Speed	Temperature	Package
PEEL22CV8J-5*	5ns	C	J28
PEEL22CV8P-7*	7.5ns	C	P24
PEEL22CV8J-7*			J28
PEEL22CV8S-7*			S24
PEEL22CV8P-10*	10ns	C	P24
PEEL22CV8J-10*			J28
PEEL22CV8S-10*			S24
PEEL22CV8P-15	15ns	C	P24
PEEL22CV8J-15			J28
PEEL22CV8S-15			S24
PEEL22CV8P-25	25ns	C	P24
PEEL22CV8J-25			J28
PEEL22CV8S-25			S24

*Contact ICT for availability of this device in -5, -7, -10 speed grades, as well as all speed grades in TSSOP packages.

Part Number