MV1820

VIDEO PROGRAMME DELIVERY CONTROL INTERFACE CIRCUIT

(Supersedes version in October 1995 Media IC Handbook, HB3120 - 3.0)

The MV1820 is a high speed CMOS receiver for Programme Delivery Control (PDC) messages broadcast in World System Teletext (WST) Format Two Broadcast Service Data Packets (BSDP). The PDC message can be read on an I²C bus with data format similar to standard Video Programming Service (VPS) decoders. Additional data is appended to include new PDC features.

It is intended for use in Video Cassette Recorders to provide automatic recording of suitably labelled Television programmes requested by the user.

FEATURES

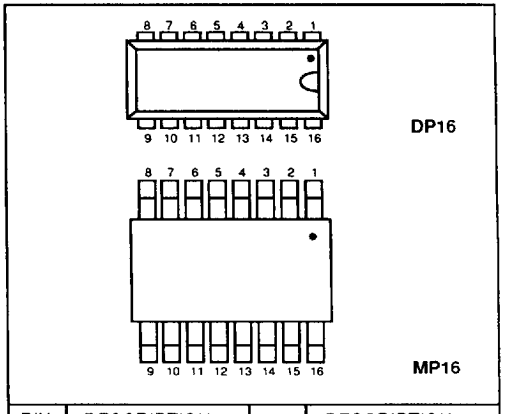
- On chip data slicing
- Low external component count
- I²C bus for low cost interfacing
- Advanced CMOS technology gives low power dissipation and high reliability

ABSOLUTE MAXIMUM RATINGS

Supply voltage	0.3V to 7V
All inputs	-0.3 to V_{DD} +0.3V
Operating temperature	0 to +70°C
Storage temperature	-55 to 125°C

ORDERING INFORMATION

MV1820F/CG/DPAS
MV1820F/CG/MPES



PIN	DESCRIPTION	PIN	DESCRIPTION
1	$\overline{\text{RESET}}$	16	$\overline{\text{XTI}}$
2	$\overline{\text{EXT/INT}}$	15	$\overline{\text{XTO}}$
3	BLC	14	$\overline{\text{DAV}}$
4	WLC	13	SDA
5	VIDEO	12	VDD
6	GND	11	SCL
7	TCR	10	SYNC I/O
8	AS	9	DATA I/O

Fig.1 Pin connections - top view

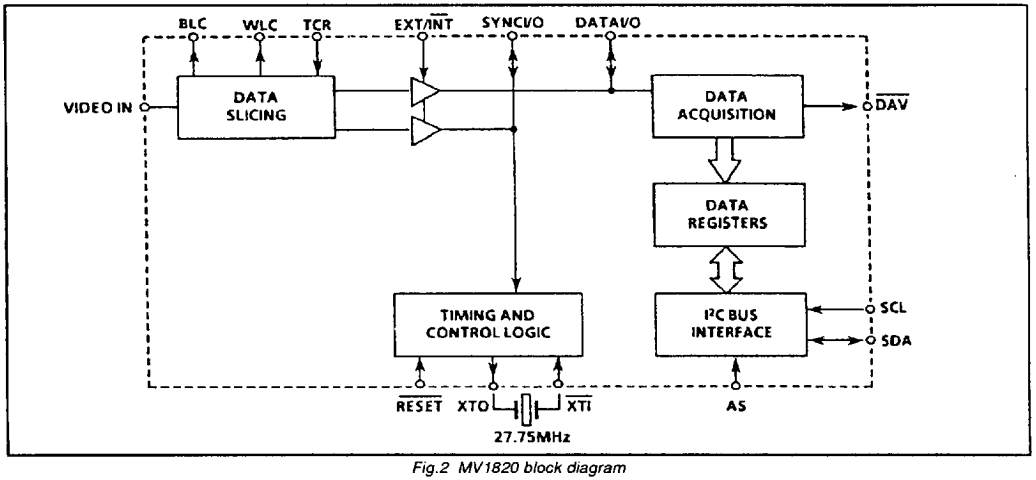


Fig.2 MV1820 block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)
T_{amb} = 0 to 70°C, V_{DD} = 5V ± 10%

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply voltage	12	4.5	5.0	5.5	V	
Supply current	12		20	25	mA	
Video input	5					
Video amplitude		0.8	1.8	3.0	Vpp	Bottom of sync to white (pk to pk)
Source impedance				250	Ω	
TCR input	7					
External resistance		4.7	4.7	200	kΩ	Connected to V_{DD}
BLC and WLC	3 & 4					
Capacitor value			10		nF	Connected to GND
Capacitor tolerance		-10%		+10%		
Effective series resistance				5	Ω	1MHz
DATA I/O and SYNC I/O	9 & 10					
Output voltage High		V_{DD}-1.0	4.5		V	I_{OH} = -1.2mA
Output voltage Low			0.2	0.4	V	I_{OL} = 2.4mA
Input voltage Low		0		0.8	V	
Input voltage High		V_{DD}-1.0		V_{DD}	V	
Input current		-30		+30	µA	V_{IN} = V_{SS} or V_{DD}
EXT/INT	2					100k (nom) pull-down resistor
Input voltage Low		0		0.8	V	
Input voltage High		V_{DD}-1.0		V_{DD}	V	
Input current Low		-10		+10	µA	V_{IN} = V_{SS}
Input current High		22	50	220	µA	V_{IN} = V_{DD}
AS	8					100k (nom) pull-down resistor
Input voltage Low		0		1.0	V	
Input voltage High		V_{DD}-1.0		V_{DD}	V	
Input current Low		-10		+10	µA	V_{IN} = V_{SS}
Input current High		22	50	220	µA	V_{IN} = V_{DD}
$\overline{XTI}$ Input	16					
Input current Low		-0.5	-5.0	-20	µA	-0.3<V_{IN}<V_{IL} max
Input current High		0.5	5.0	20	µA	V_{IH}min<V_{IN}<(V_{DD} + 0.3)
XTO Output	15					
Output voltage High		V_{DD}-1.0	4.5		V	I_{OH} = -1.0mA
Output voltage Low			0.2	0.4	V	I_{OL} = 2.0mA
Frequency			27.750		MHz	±100ppm

ELECTRICAL CHARACTERISTICS (continued)

These characteristics are guaranteed over the following conditions (unless otherwise stated)
T_{amb} = 0 to 70°C, V_{DD} = 5V ± 10%

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
I2C bus						
SCL, SDA Schmitt inputs	11, 13					Not clamped when V_{DD} = 0V
Input voltage Low		0		1.5	V	
Input voltage High		3.5		V_{DD}	V	
Output voltage Low			0.1	0.4	V	I_{OL} = 3.0mA
SCL clock frequency	11		100	1000	kHz	
$\overline{DAV}$ data available						100k (nom) pull-up resistor
Output voltage low			0.2	0.4	V	I_{OH} = 2.4mA
$\overline{RESET}$ Schmitt input	1					100k (nom) pull-up resistor
Input voltage Low		0		0.8	V	
Input voltage High		V_{DD}-1.0		V_{DD}	V	
Input current Low		-22	-50	-220	µA	V_{IN} = Vss
Input current High		-10		+10	µA	V_{IN} = V_{DD}

NOTE
Input voltage low and input voltage high for $\overline{EXT/INT}$, AS and $\overline{XTI}$ are as specified for DATA I/O.

PIN DESCRIPTION Symbol	Pin	Pin Name and Description
$\overline{RESET}$	1	**Active Low Reset.** Includes a 100kΩ pull - up resistor
$\overline{EXT/INT}$	2	**Control Pin for SYNC I/O and DATA I/O.** Includes a 100kΩ pull - down resistor. When low or not connected, internal SYNC and DATA are used, pins 9 and 10 are outputs. When high, supply SYNC and DATA from an external source, pins 9 and 10 are inputs.
BLC	3	**Black level capacitor.**
WLC	4	**White level capacitor.**
VIDEO	5	**Input for composite video signal with negative going syncs**
GND	6	**Ground 0 volts.**
TCR	7	**Time constant resistor.** Controlling discharge rate of black and white level capacitor voltages.
AS	8	**Address select for I²C bus.** [0010 0001] with AS set high, or [0010 0011] with AS set low. Includes 100kΩ pull - down resistor.
DATA I/O	9	**Data input/output.**
SYNC I/O	10	**Sync input/output.**
SCL	11	**I²C bus serial clock.**
VDD	12	**Positive supply voltage +5V ± 10%**
SDA	13	**I²C bus bi-directional data port.**
$\overline{DAV}$	14	**Active low open drain output data available signal to microprocessor.** Includes 100kΩ pull - up resistor
XTO	15	**Crystal out,** 27.75MHz fundamental crystal with on-chip 1MΩ resistor to $\overline{XTI}$.
$\overline{XTI}$	16	**Crystal input.**

CRYSTAL SPECIFICATION

Parallel resonant fundamental frequency 27.750000MHz. AT cut.
Tolerance at -10°C to 60°C ± 50ppm.
Tolerance overall ± 100ppm.
Nominal load capacitance 20pF.
Equivalent series resistance <20Ω.

FUNCTIONAL DESCRIPTION

The video signal is sliced to produce data and synchronising signals. Timing circuits monitor the sync signal to enable the MV1820 to lock onto the broadcast signal. A timing window, for the Vertical Blanking Interval (VBI) lines 6 - 22 and 318 - 335, is established to enable the acquisition circuit to monitor the sliced data signal for valid teletext data.

The framing code is checked for valid World System Teletext (WST) data. Magazine, packet and designation code bytes are checked and valid Broadcast Service Data Packets (BSDP) format two type only are accepted. These are known as packet 8/30. Format two is signalled by byte six, data bit two being set high and bits 3 and 4 set low. Bytes 13 to 25 inclusive are Hamming decoded (8,4) and stored in seven registers each of eight bits. If the complete message is correctly received with no uncorrectable Hamming errors, an interrupt to the microprocessor is signalled by the DAV (bar) pin going low. At the same time the data is transferred to a second bank of registers, reorganised with original numbered bytes 14, 15, 24, 25 and 13 placed after byte 23, to be read out on the I²C bus when so requested. Subsequent valid messages will continue to be transferred to the output registers overwriting any existing data. In this way the output registers always contain the latest PDC message.

The MV1820 is configured as an I²C bus slave transmitter with a selectable address. The I²C bus address is 0010 0001 (20 + 1 hex) with the address select (AS) pin set high, or 0010 0011 (22 + 1 hex) with the AS pin set low. The read bit (LSB) must always be set, it is not possible to write to the MV1820.

On recognising its address, the MV1820 will send an acknowledge and then transmit on the SDA line the first byte from the output registers (decoded byte 16 and 17) most significant bit (MSB) first. It will then monitor the SDA line for an acknowledge from the microprocessor. If the microprocessor does NOT send an acknowledge, the MV1820 will release the data line to allow the microprocessor to send a stop condition. If the microprocessor does send an acknowledge, the following bytes of the message will be output provided each byte is acknowledged. The final data will be byte 13 followed by the four '1's.

When readout is complete, the DAV (bar) pin is reset high and the output registers are all set high. If the microprocessor continues to send clocks on the SCL line, the MV1820 will output FF bytes on the SDA line. Also, if the MV1820 is re-addressed before another PDC message is received, the MV1820 will output FF bytes on the SDA line. The microprocessor can prematurely stop the message by NOT sending an Acknowledge followed by a STOP condition after any byte has been sent by the MV1820. The registers will then be reset to FF bytes and the $\overline{DAV}$ pin will be reset high.

To prevent any corruption of the data in the output registers during I²C bus activity, valid PDC messages are held in the incoming registers until I²C bus activity ceases. Here they may be overwritten by new PDC messages until the I²C bus activity ceases and they can then be transferred to the output registers.

System clock is provided by an on - chip 27.75MHz oscillator together with an external parallel resonant fundamental frequency AT cut crystal.

Following a reset, $\overline{RESET}$ pulled low, the output I²C bus registers will contain FF bytes and the $\overline{DAV}$ pin will be set high. When the power supply is removed, the I²C bus will not be clamped to ground, leaving it free for other I²C bus traffic.

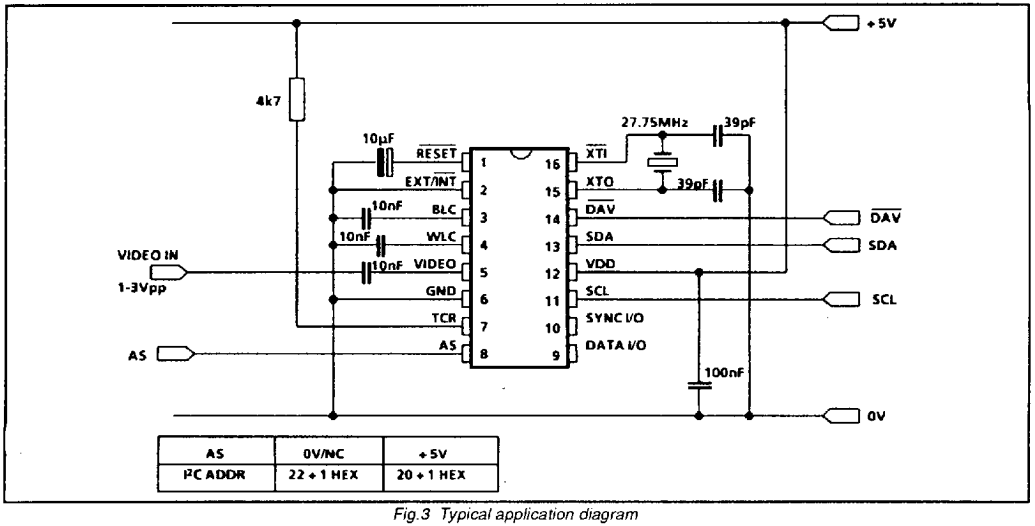


Fig.3 Typical application diagram

ORDER OF DATA OUTPUT ON THE I²C BUS

Bit Order		EBU Numbering		Bit Value	VPS Equivalence
byte 1	bit 7	byte 16	bit 0 - CNI b9	reserved	[byte 11
	bit 6		bit 1 - CNI b10	64 network (or programme provider)	
	bit 5		bit 2 - PIL b1	16	
	bit 4		bit 3 - PIL b2	8	
	bit 3	byte 17	bit 0 - PIL b3	4 day	
	bit 2		bit 1 - PIL b4	2	
	bit 1		bit 2 - PIL b5	1	
	bit 0		bit 3 - PIL b6	8	[
byte 2	bit 7	byte 18	bit 0 - PIL b7	4	[byte 12
	bit 6		bit 1 - PIL b8	2 month	
	bit 5		bit 2 - PIL b9	1	
	bit 4		bit 3 - PIL b10	16	
	bit 3	byte 19	bit 0 - PIL b11	8	
	bit 2		bit 1 - PIL b12	4 hour	
	bit 1		bit 2 - PIL b13	2	
	bit 0		bit 3 - PIL b14	1	[
byte 3	bit 7	byte 20	bit 0 - PIL b15	32	[byte 13
	bit 6		bit 1 - PIL b16	16	
	bit 5		bit 2 - PIL b17	8	
	bit 4		bit 3 - PIL b18	4 minute	
	bit 3	byte 21	bit 0 - PIL b19	2	
	bit 2		bit 1 - PIL b20	1	
	bit 1		bit 2 - CNI b5	8	
	bit 0		bit 3 - CNI b6	4	[
byte 4	bit 7	byte 22	bit 0 - CNI b7	2 country	[byte 14
	bit 6		bit 1 - CNI b8	1	
	bit 5		bit 2 - CNI b11	32	
	bit 4		bit 3 - CNI b12	16	
	bit 3	byte 23	bit 0 - CNI b13	8 network (or programme provider)	
	bit 2		bit 1 - CNI b14	4	
	bit 1		bit 2 - CNI b15	2	
	bit 0		bit 3 - CNI b16	1	[
byte 5	bit 7	byte 14	bit 0 - PCS b1	2 status (define the analog sound	[byte 5
	bit 6		bit 1 - PCS b2	1 transmission system)	
	bit 5		bit 2 - unallocated		
	bit 4		bit 3 - unallocated		
	bit 3	byte 15	bit 0 - CNI b1	128	
	bit 2		bit 1 - CNI b2	64	
	bit 1		bit 2 - CNI b3	32 country	
	bit 0		bit 3 - CNI b4	16	[
byte 6	bit 7	byte 24	bit 0 - PTY b1	128	[byte 15
	bit 6		bit 1 - PTY b2	64	
	bit 5		bit 2 - PTY b3	32	
	bit 4		bit 3 - PTY b4	16 programme type	
	bit 3	byte 25	bit 0 - PTY b5	8	
	bit 2		bit 1 - PTY b6	4	
	bit 1		bit 2 - PTY b7	2	
	bit 0		bit 3 - PTY b8	1	[
byte 7	bit 7	byte 13	bit 0 - LCI b1	2 Label Channel Identifier	
	bit 6		bit 1 - LCI b2	1 Interleave up to four PIL messages	
	bit 5		bit 2 - LUF	1 Label Update Flag (LUF)	
	bit 4		bit 3 - unallocated		
	bit 3		-set to 1		
	bit 2		-set to 1	NOTE: Data is output on the	
	bit 1		-set to 1	I²C bus MSB first	
	bit 0		-set to 1		