

# 1.5V Drive Pch + Pch MOSFET

## TT8J13

### ● Structure

Silicon P-channel MOSFET

### ● Features

- 1) Low On-resistance.
- 2) Small high power package.
- 3) Low voltage drive(1.5V drive).

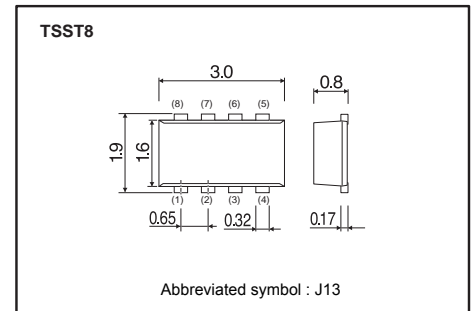
### ● Application

Switching

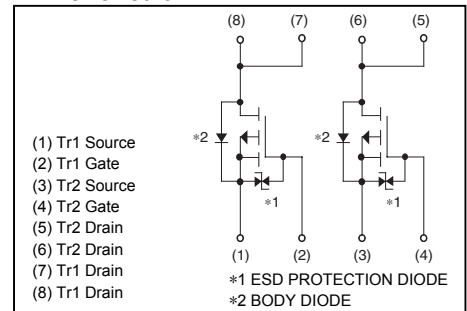
### ● Packaging specifications

Type	Package	Taping
	Code	TCR
	Basic ordering unit (pieces)	3000
TT8J13		○

### ● Dimensions (Unit : mm)



### ● Inner circuit



### ● Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Drain-source voltage	$V_{DSS}$	-12	V
Gate-source voltage	$V_{GSS}$	0 to -8	V
Drain current	Continuous	$I_D$	$\pm 2.5$ A
	Pulsed	$I_{DP}$ *1	$\pm 5$ A
Source current (Body Diode)	Continuous	$I_s$	-0.8 A
	Pulsed	$I_{sp}$ *1	-5 A
Power dissipation	$P_D$ *2	1.25	W / TOTAL
		1	W / ELEMENT
Channel temperature	Tch	150	°C
Range of storage temperature	Tstg	-55 to +150	°C

\*1  $P_w \leq 10 \mu s$ , Duty cycle  $\leq 1\%$

\*2 Mounted on a ceramic board.

### ● Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to Ambient	$R_{th}(ch-a)^*$	100	°C / W / TOTAL
		125	°C / W / ELEMENT

\* Mounted on a ceramic board.

● **Electrical characteristics** (Ta = 25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	$I_{GSS}$	-	-	-10	$\mu\text{A}$	$V_{GS}=-8\text{V}, V_{DS}=0\text{V}$
Drain-source breakdown voltage	$V_{(BR)DSS}$	-12	-	-	V	$I_D=-1\text{mA}, V_{GS}=0\text{V}$
Zero gate voltage drain current	$I_{DSS}$	-	-	-10	$\mu\text{A}$	$V_{DS}=-12\text{V}, V_{GS}=0\text{V}$
Gate threshold voltage	$V_{GS(th)}$	-0.3	-	-1.0	V	$V_{DS}=-6\text{V}, I_D=-1\text{mA}$
Static drain-source on-state resistance	$R_{DS(on)}$	-	44	62	m $\Omega$	$I_D=-2.5\text{A}, V_{GS}=-4.5\text{V}$
		-	55	77		$I_D=-1.2\text{A}, V_{GS}=-2.5\text{V}$
		-	75	110		$I_D=-1.2\text{A}, V_{GS}=-1.8\text{V}$
		-	90	180		$I_D=-0.5\text{A}, V_{GS}=-1.5\text{V}$
Forward transfer admittance	$ Y_{fs} ^*$	3.5	-	-	S	$I_D=-2.5\text{A}, V_{DS}=-6\text{V}$
Input capacitance	$C_{iss}$	-	2000	-	pF	$V_{DS}=-6\text{V}$
Output capacitance	$C_{oss}$	-	130	-	pF	$V_{GS}=0\text{V}$
Reverse transfer capacitance	$C_{rss}$	-	120	-	pF	$f=1\text{MHz}$
Turn-on delay time	$t_{d(on)}^*$	-	11	-	ns	$I_D=-1.2\text{A}, V_{DD}=-6\text{V}$
Rise time	$t_r^*$	-	40	-	ns	$V_{GS}=-4.5\text{V}$
Turn-off delay time	$t_{d(off)}^*$	-	160	-	ns	$R_L=5\Omega$
Fall time	$t_f^*$	-	60	-	ns	$R_G=10\Omega$
Total gate charge	$Q_g^*$	-	16	-	nC	$I_D=-2.5\text{A}$
Gate-source charge	$Q_{gs}^*$	-	2.4	-	nC	$V_{DD}=-6\text{V}$
Gate-drain charge	$Q_{gd}^*$	-	2.2	-	nC	$V_{GS}=-4.5\text{V}$

\*Pulsed

● **Body diode characteristics** (Source-Drain) (Ta = 25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	$V_{SD}^*$	-	-	-1.2	V	$I_s=-2.5\text{A}, V_{GS}=0\text{V}$

\*Pulsed

●Electrical characteristic curves (Ta=25°C)

Fig.1 Typical output characteristics( I )

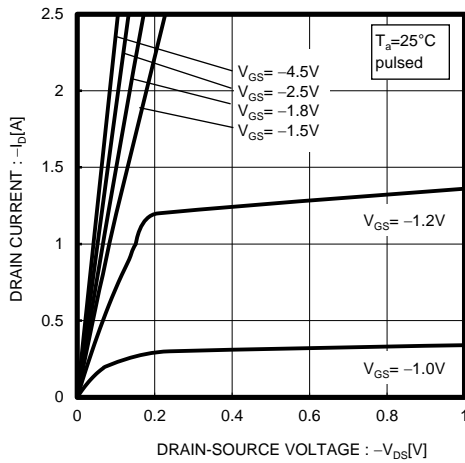


Fig.2 Typical output characteristics( II )

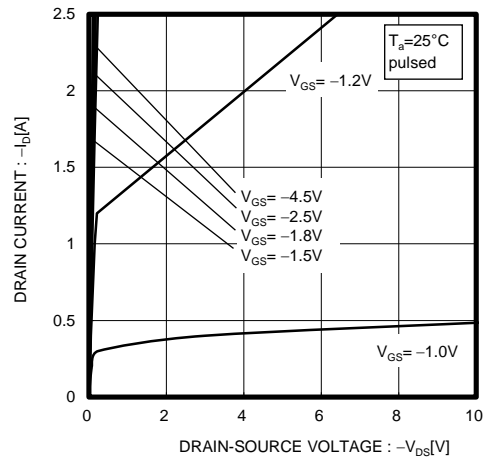


Fig.3 Typical Transfer Characteristics

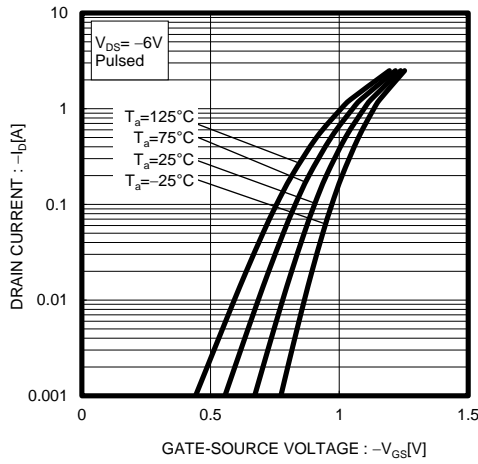


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current ( I )

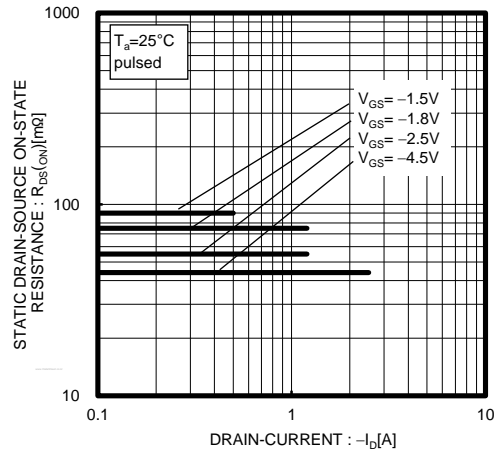


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current( II )

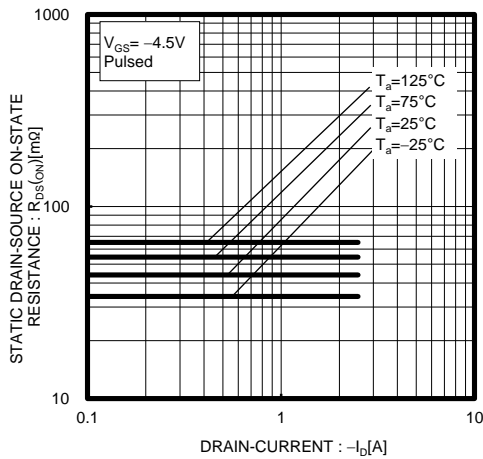


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current( III )

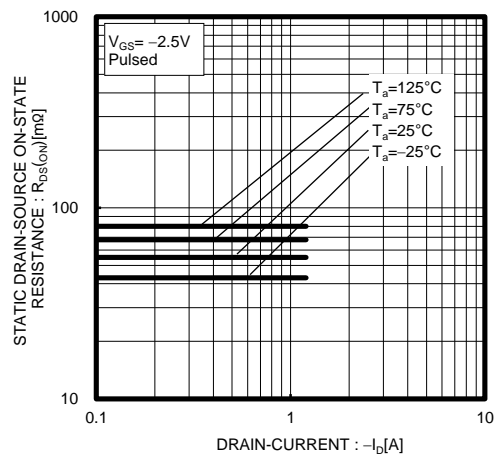


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(I<sub>D</sub>)

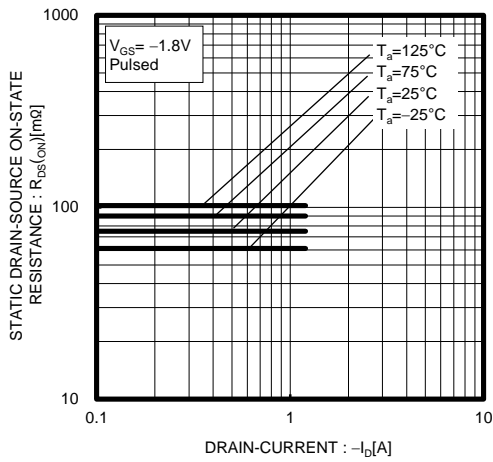


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(I<sub>D</sub>)

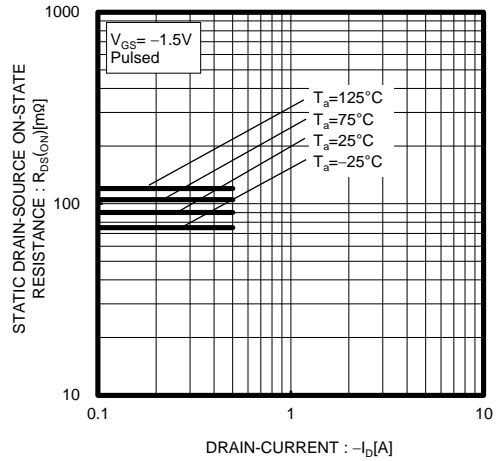


Fig.9 Forward Transfer Admittance vs. Drain Current

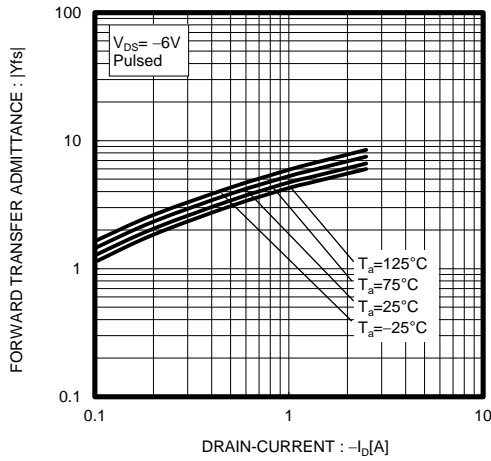


Fig.10 Reverse Drain Current vs. Source-Drain Voltage

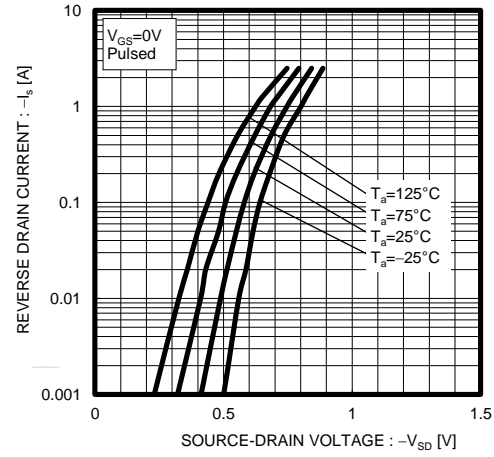


Fig.11 Static Drain-Source On-State Resistance vs. Gate Source Voltage

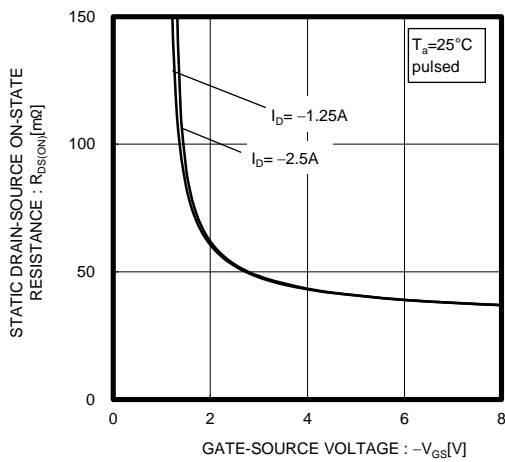


Fig.12 Switching Characteristics

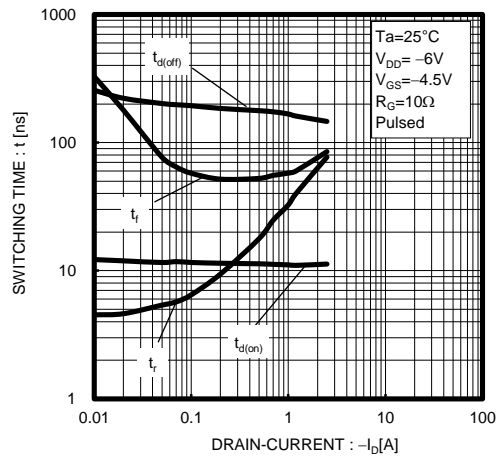


Fig.13 Dynamic Input Characteristics

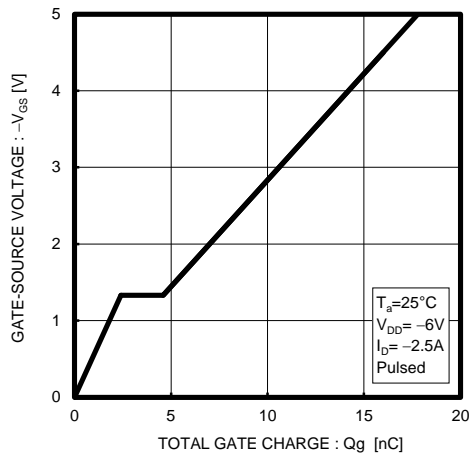
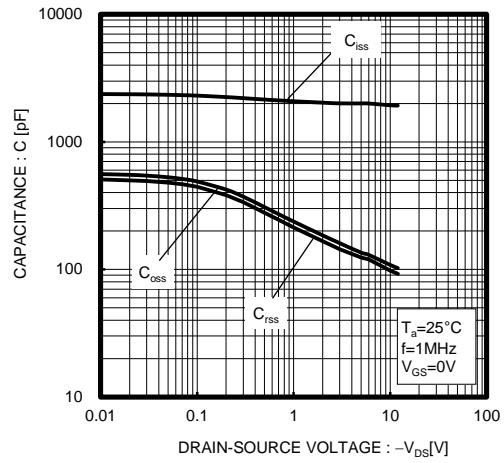


Fig.14 Typical Capacitance vs. Drain-Source Voltage



● Measurement circuits

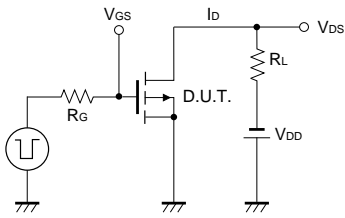


Fig.1-1 Switching Time Measurement Circuit

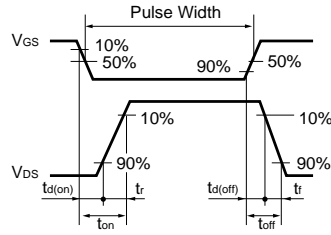


Fig.1-2 Switching Waveforms

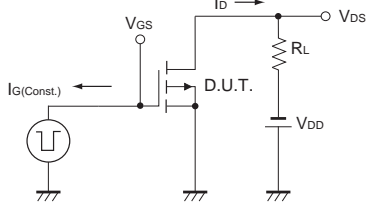


Fig.2-1 Gate Charge Measurement Circuit

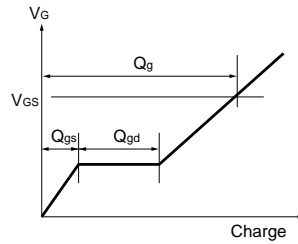


Fig.2-2 Gate Charge Waveform

● Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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