HB56HW164DB-7A/8A

Preliminary

1,048,576-Word x 64-Bit High Density Dynamic RAM Module

HITACHI

Rev. 0. 1
Nov. 13, 1995

The HB56HW164DB is a 1M x 64 dynamic RAM Small Outline Dual In-line Memory Module(S.O.DIMM), mounted 4 pieces of 16-Mbit DRAM (HM51W16165ATT) sealed in TSOP package and 1 pieces of serial EEPROM (24C02) for Presence Detect(PD).
The HB56HW164DB offers Extended Data Out (EDO) Page Mode as a high speed access mode.
An outline of the HB56HW164DB is 144-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, the HB56HW164DB makes high density mounting possible without surface mount technology.
The HB56HW164DB provides common data inputs and outputs.
Decoupling capacitors are mounted beside each TSOP on the module board.

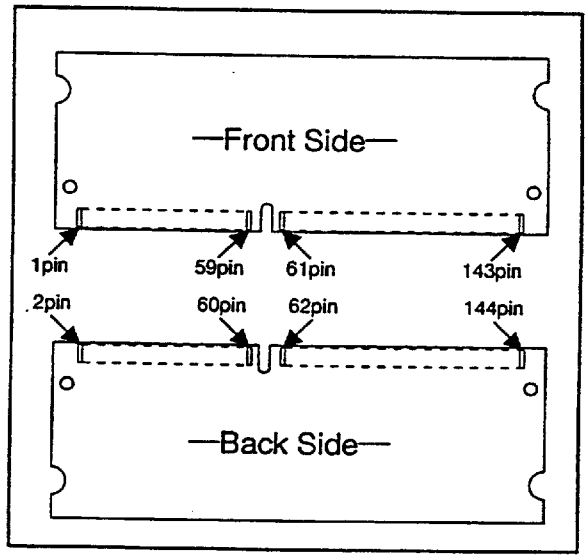
Ordering Information

Type No.	Access time	Package	Contact pad
HB56HW164DB-7A	70ns	Small Outline DIMM(144-pin)	Gold
HB56HW164DB-8A	80ns		

Features

- 144-pin Zig Zag Dual tabs socket type
  - Lead pitch : 0.80 mm
- Single 3.3 V (±0.3 V) supply
- High speed
  - Access time : tRAC =70 / 80 ns (max.)
  - Access time : tCAC =18 / 20 ns (max.)
- Low power dissipation
  - Active mode: 1.3 / 1.2 W (max.)
  - Standby mode(TTL) : 28.8 mW (max.)
  - Standby mode(CMOS): 14.4 mW (max.)
- EDO page mode capability
- 4,096 refresh cycle/64 ms
- 3 variations of refresh
  - /RAS - only refresh
  - /CAS - before - /RAS refresh
  - Hidden refresh
- TTL compatible

Pin Arrangement



Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

ADE-203-482(A)(Z)

Pin Arrangement

Front Side				Back Side			
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	Vss	73	/OE	2	Vss	74	NC
3	DQ0	75	Vss	4	DQ32	76	Vss
5	DQ1	77	NC	6	DQ33	78	NC
7	DQ2	79	NC	8	DQ34	80	NC
9	DQ3	81	Vcc	10	DQ35	82	Vcc
11	Vcc	83	DQ16	12	Vcc	84	DQ48
13	DQ4	85	DQ17	14	DQ36	86	DQ49
15	DQ5	87	DQ18	16	DQ37	88	DQ50
17	DQ6	89	DQ19	18	DQ38	90	DQ51
19	DQ7	91	Vss	20	DQ39	92	Vss
21	Vss	93	DQ20	22	Vss	94	DQ52
23	/CE0	95	DQ21	24	/CE4	96	DQ53
25	/CE1	97	DQ22	26	/CE5	98	DQ54
27	Vcc	99	DQ23	28	Vcc	100	DQ55
29	A0	101	Vcc	30	A3	102	Vcc
31	A1	103	A6	32	A4	104	A7
33	A2	105	A8	34	A5	106	A11
35	Vss	107	Vss	36	Vss	108	Vss
37	DQ8	109	A9	38	DQ40	110	NC
39	DQ9	111	A10	40	DQ41	112	NC
41	DQ10	113	Vcc	42	DQ42	114	Vcc
43	DQ11	115	/CE2	44	DQ43	116	/CE6
45	Vcc	117	/CE3	46	Vcc	118	/CE7
47	DQ12	119	Vss	48	DQ44	120	Vss
49	DQ13	121	DQ24	50	DQ45	122	DQ56
51	DQ14	123	DQ25	52	DQ46	124	DQ57
53	DQ15	125	DQ26	54	DQ47	126	DQ58
55	Vss	127	DQ27	56	Vss	128	DQ59
57	NC	129	Vcc	58	NC	130	Vcc
59	NC	131	DQ28	60	NC	132	DQ60
61	NC	133	DQ29	62	NC	134	DQ61
63	Vcc	135	DQ30	64	Vcc	136	DQ62
65	NC	137	DQ31	66	NC	138	DQ63
67	/WE	139	Vss	68	NC	140	Vss
69	/RE0	141	SDA	70	NC	142	SCL
71	NC	143	Vcc	72	NC	144	Vcc

Pin Description

Pin Name	Function
A0 to A11	Address Input : A0 to A11 -Row Address : A0 to A11 -Column Address : A0 to A7 -Refresh Address : A0 to A11
DQ0 to DQ63	Data - in / Data - out
/RE0	Row Address Strobe (/RAS)
/CE0 to /CE7	Column Address Strobe (/CAS)
/WE	Read / Write Enable
/OE	Output Enable
Vcc	Power Supply
Vss	Ground
SDA	Serial Data Out (Bit0 to 7)
SCL	Clock for Presence Detect
NC	Non Connection

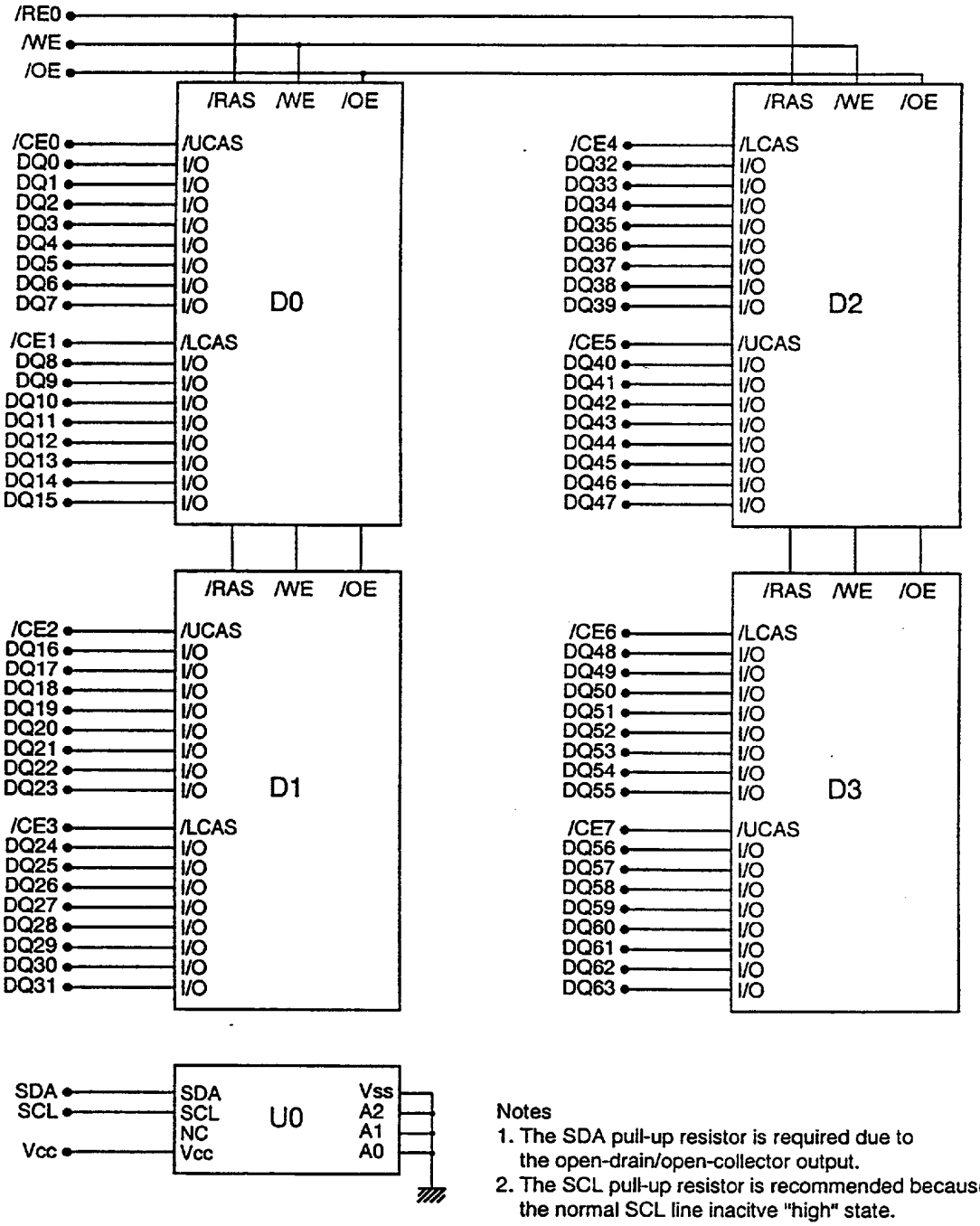
Serial-PD Matrix

Byte Number	Function Described		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
0	Number Serial PD Bytes		0	0	0	0	1	1	0	1	13
1	Serial Memory		0	0	0	0	1	0	0	0	256 Byte
2	Fundamental Memory Type		0	0	0	0	0	0	1	0	EDO
3	Number of Rows		0	0	0	0	1	1	0	0	12
4	Number of Columns		0	0	0	0	1	0	0	0	8
5	Numder of Banks		0	0	0	0	0	0	0	1	1
6	Data Width		0	1	0	0	0	0	0	0	64
7	Data Width (continued)		0	0	0	0	0	0	0	0	0(+)
8	Supply Votage and Interface Levels		0	0	0	1	0	0	0	1	LVTTL(3.3V)
9	/RAS Access Time	70 ns	0	1	0	0	0	1	1	0	
		80 ns	0	1	0	1	0	0	0	0	
10	/CAS Access Time	18 ns	0	0	0	1	0	0	1	0	
		20 ns	0	0	0	1	0	1	0	0	
11	Error Detection / Correction		0	0	0	0	0	0	0	0	None
12	Refresh Period		0	0	0	0	0	0	0	0	Normal (15.625 μs)

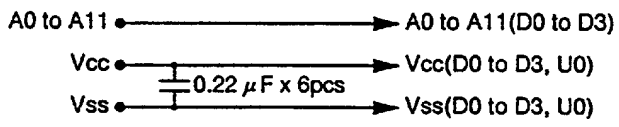
Note : Serial-PD Datas are not protected.

0 : Serial Data, "driven to Low"
1 : Serial Data, "driven to High"

Block Diagram



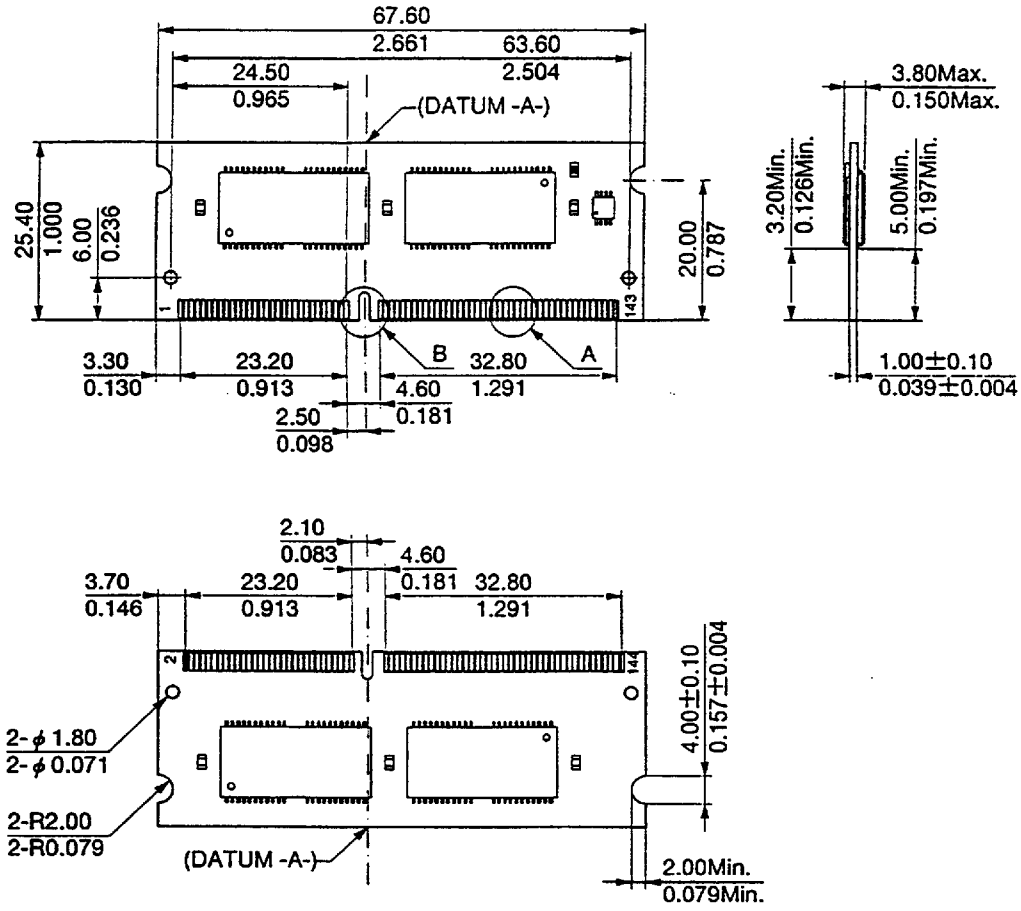
Notes
1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.



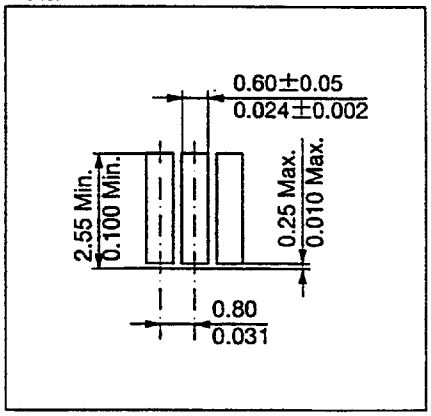
* D0 to D3 : HM51W16165
  U0 : 24C02

Physical Outline

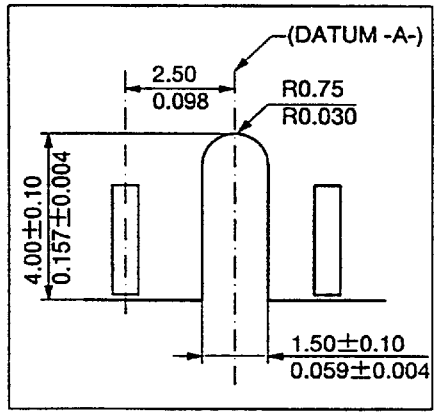
Unit : mm / inch



Detail A



Detail B



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	VT	-0.5 to +4.6	V
Supply voltage relative to Vss	Vcc	-0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	Pt	4	W
Operating temperature	Topr	0 to +70	℃
Storage temperature	Tstg	-55 to +125	℃

Recommended DC Operating Conditions (Ta = 0 to 70 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	Vss	0	0	0	V	
	Vcc	3.0	3.3	3.6	V	1
Input high voltage	ViH	2.0	-	Vcc+0.3	V	1
Input low voltage	ViL	-0.3	-	0.8	V	1

Note : 1. All voltage referenced to Vss.

DC Characteristics (Ta=0 to 70°C , Vcc=3.3V±0.3V , Vss=0 V)

Parameter	Symbol	70ns		80ns		Unit	Test Condition	Note
		Min.	Max.	Min.	Max.			
Operating current	Icc1	-	360	-	320	mA	tRC=min.	1,2
Standby current	Icc2	-	8	-	8	mA	TTL interface /RAS,/CAS=ViH Dout=High-Z	
		-	4	-	4	mA	CMOS interface /RAS,/CAS≧Vcc-0.2V Dout=High-Z	
/RAS-only refresh current	Icc3	-	360	-	320	mA	tRC=min.	2
Standby current	Icc5	-	20	-	20	mA	/RAS=ViH /CAS=ViL Dout=enable	1
/CAS-before-/RAS refresh current	Icc6	-	360	-	320	mA	tRC=min.	
EDO page mode current	Icc7	-	460	-	400	mA	tHPC=min.	1,3
Input leakage current	ILI	-10	10	-10	10	μA	0V≦Vin≦4.6V	
output leakage current	ILO	-10	10	-10	10	μA	0V≦Vout≦4.6V Dout=disable	
output high voltage	VoH	2.4	Vcc	2.4	Vcc	V	High Iout=-2mA	
output low voltage	VoL	0	0.4	0	0.4	V	Low Iout=2mA	

Notes : 1. Icc depends on output load condition when the device is selected , Icc max. is specified at the output open condition.
2. Address can be changed once or less while /RAS=ViL.
3. Address can be changed once or less while /CAS=ViH.

Capacitance (Ta=25°C , Vcc=3.3V±0.3V)

Parameter		Symbol	Typ.	Max.	Unit	Notes
Input capacitance	(Address)	CI1	-	40	pF	1
Input capacitance	(/RAS, /WE, /OE)	CI2	-	48	pF	1
Input capacitance	(/CAS)	CI3	-	22	pF	1
I/O capacitance	(DQ)	CI/O	-	17	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. /CAS=ViH to disable Dout.

AC Characteristics (Ta=0 to 70°C, Vcc=3.3V±0.3V, Vss=0V) *1, *2, *18, *19

Test Conditions

Input rise and fall times : 2 ns
Input level : ViL=0V, ViH=3.0V
Input timing reference levels : 0.8 V, 2.4 V
Output timing reference levels : 0.8 V, 2.0 V
Output load : 1 TTL gate + CL (100 pF) (Including scope and jig)

• **Read , Write , Read-Modify-Write and Refresh Cycles (Common parameters)**

Parameter	Symbol	70ns		80ns		Unit	Notes
		Min.	Max.	Min.	Max.		
Random read or write cycle time	tRC	124	-	144	-	ns	
/RAS precharge time	tRP	50	-	60	-	ns	
/CAS precharge time	tCP	13	-	15	-	ns	
/RAS pulse width	tRAS	70	10000	80	10000	ns	
/CAS pulse width	tCAS	13	10000	15	10000	ns	
Row address setup time	tASR	0	-	0	-	ns	
Row address hold time	tRAH	10	-	10	-	ns	
Column address setup time	tASC	0	-	0	-	ns	
Column address hold time	tCAH	13	-	15	-	ns	
/RAS to /CAS delay time	tRCD	20	45	20	53	ns	3
/RAS to column address delay time	tRAD	15	35	15	40	ns	4
/RAS hold time	tRSH	18	-	20	-	ns	
/CAS hold time	tCSH	58	-	68	-	ns	
/CAS to /RAS precharge time	tCRP	5	-	5	-	ns	
/OE to Din delay time	tOED	18	-	20	-	ns	5
/OE delay time from Din	tDZO	0	-	0	-	ns	6
/CAS delay time from Din	tDZC	0	-	0	-	ns	6
Transition time (rise and fall)	tT	2	50	2	50	ns	7
Refresh period (4,096 cycles)	tREF	-	64	-	64	ms	

• **Read Cycle**

Parameter	Symbol	70ns		80ns		Unit	Notes
		Min.	Max.	Min.	Max.		
Access time from /RAS	tRAC	-	70	-	80	ns	8, 9
Access time from /CAS	tCAC	-	18	-	20	ns	9,10,17
Access time from address	tAA	-	35	-	40	ns	9,11,17
Access time from /OE	tOEA	-	18	-	20	ns	9,21
Read command setup time	tRCS	0	-	0	-	ns	
Read command hold time to /CAS	tRCH	5	-	5	-	ns	12
Read command hold time from /RAS	tRCHR	70	-	80	-	ns	
Read command hold time to /RAS	tRRH	0	-	0	-	ns	12
Column address to /RAS lead time	tRAL	35	-	40	-	ns	
Column address to /CAS lead time	tCAL	23	-	28	-	ns	
/CAS to output in low-Z	tCLZ	0	-	0	-	ns	
Output data hold time	tOH	3	-	3	-	ns	
Output data hold time from /OE	tOHO	3	-	3	-	ns	
Output buffer turn-off time	tOFF	-	15	-	15	ns	13
Output buffer turn-off to /OE	tOEZ	-	15	-	15	ns	13
/CAS to Din delay time	tCDD	18	-	20	-	ns	5
Output data hold time from /RAS	tOHR	3	-	3	-	ns	
Output buffer turn-off time to /RAS	tOFR	-	15	-	15	ns	
Output buffer turn-off to /WE	tWEZ	-	15	-	15	ns	
/WE to Din delay time	tWED	18	-	20	-	ns	
/RAS to Din delay time	tRDD	18	-	20	-	ns	

• **Write Cycle**

Parameter	Symbol	70ns		80ns		Unit	Notes
		Min.	Max.	Min.	Max.		
Write command setup time	tWCS	0	-	0	-	ns	14
Write command hold time	tWCH	13	-	15	-	ns	
Write command pulse width	tWP	10	-	10	-	ns	
Write command to /RAS lead time	tRWL	13	-	15	-	ns	
Write command to /CAS lead time	tCWL	13	-	15	-	ns	
Data-in setup time	tDS	0	-	0	-	ns	15
Data-in hold time	tDH	13	-	15	-	ns	15

• **Read-Modify-Write Cycle**

Parameter	Symbol	70ns		80ns		Unit	Notes
		Min.	Max.	Min.	Max.		
Read-modify-write cycle time	tRWC	175	-	199	-	ns	
/RAS to /WE delay time	tRWD	95	-	107	-	ns	14
/CAS to /WE delay time	tCWD	43	-	47	-	ns	14
Column address to /WE delay time	tAWD	60	-	67	-	ns	14
/OE hold time from /WE	tOEH	18	-	20	-	ns	

• **Refresh Cycle**

Parameter	Symbol	70ns		80ns		Unit	Notes
		Min.	Max.	Min.	Max.		
/CAS setup time (CBR refresh cycle)	tCSR	5	-	5	-	ns	
/CAS hold time (CBR refresh cycle)	tCHR	10	-	10	-	ns	
/RAS precharge to /CAS hold time	tRPC	0	-	0	-	ns	

• **EDO Page Mode Cycle**

Parameter	Symbol	70ns		80ns		Unit	Notes
		Min.	Max.	Min.	Max.		
EDO page mode cycle time	tHPC	30	-	35	-	ns	20
EDO page mode /RAS pulse width	tRASP	-	100000	-	100000	ns	16
Access time from /CAS precharge	tCPA	-	40	-	45	ns	9, 17
/RAS hold time from /CAS precharge	tCPRH	40	-	45	-	ns	
Output data hold time from /CAS low	tDOH	5	-	5	-	ns	9, 17
/CAS hold time refferd /OE	tCOL	13	-	15	-	ns	
/CAS to /OE setup time	tCOP	5	-	5	-	ns	
Read command hold time from /CAS precharge	tRCHC	40	-	45	-	ns	

• **EDO Page Mode Read-Modify-Write Cycle**

Parameter	Symbol	70ns		80ns		Unit	Notes
		Min.	Max.	Min.	Max.		
EDO page mode read-modify-write cycle time	tHPRWC	90	-	99	-	ns	
/WE delay time from /CAS precharge	tCPW	62	-	69	-	ns	14

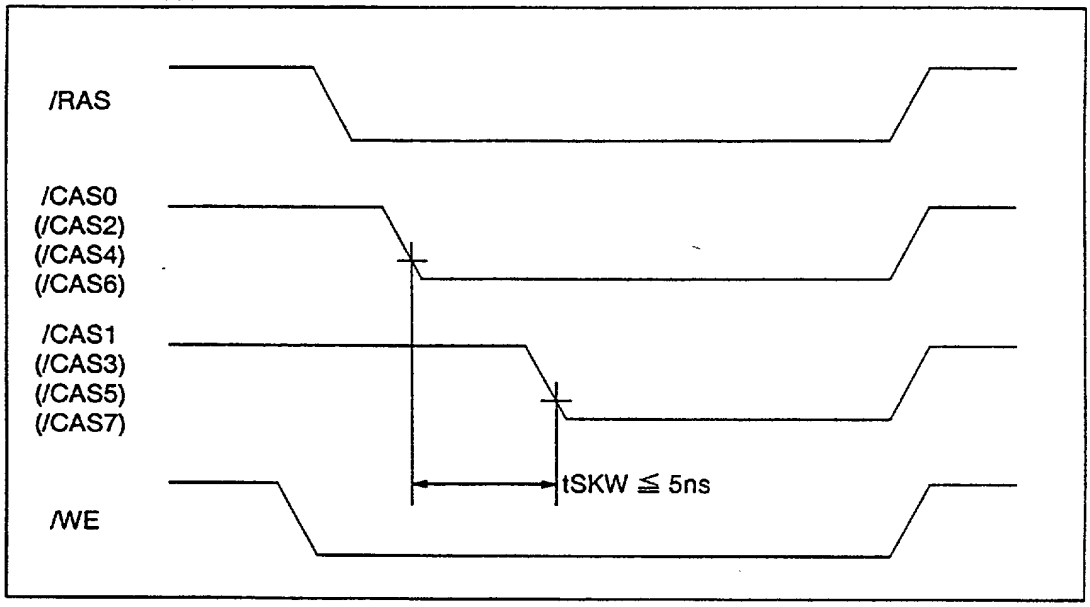
Notes:

1. AC measurements assume tT=2ns.
2. An initial pause of 200us is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing /RAS-only refresh cycle or /CAS-before-/RAS refresh).
3. Operation with the tRCD(max.) limit insures that tRAC(max.) can be met, tRCD(max.) is specified as a reference point only; if tRCD≧tRAD(max.)+tAA(max.)-tCAC(max.), then access time is controlled exclusively by tCAC.
4. Operation with the tRAD(max.) limit insures that tRAC(max.) can be met, tRAD(max.) is specified as a reference point only; if tRAD is greater than the specified tRAD(max.) limit, then access time is controlled exclusively by tAA.
5. Either tOED or tCDD must be satisfied.
6. Either tDZO or tDZC must be satisfied.
7. ViH(min.) and ViL(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between ViH(min.) and ViL(max.).
8. Assumes that tRCD≦tRCD(max.) and tRAD≦tRAD(max.). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC exceeds the value shown.
9. Measured with a load circuit equivalent to 1TTL loads and 100pF.
10. Assumes that tRCD≧tRCD(max.)+tAA(max.)-tCAC(max.) and tRAD≦tRAD(max.).
11. Assumes that tRCD≦tRCD(max.) and tRAD≧tRAD(max.).
12. Either tRCH or tRRH must be satisfied for a read cycles.
13. tOFF(max.) and tOEZ(max.) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. tWCS, tRWD, tCWD, tAWD and tCPW are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if tWCS≧tWCS(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if tRWD≧tRWD(min.), tCWD≧tCWD(min.), and tAWD≧tAWD(min.) or tCWD≧ tCWD(min.), tAWD≧tAWD(min.) and tCPW≧ tCPW(min.), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to /CAS leading edge in early write cycles and to /WE leading edge in delayed write or read-modify-write cycles.
16. tRASP defines /RAS pulse width in EDO page mode cycles.
17. Access time is determined by the longest among tAA or tCAC or tCPA.
18. In delayed write or read-modify-write cycles, /OE must disable output buffer prior to applying data to the device. After /RAS is reset, if tOEH≧tCWL, the DQ pin will remain open circuit (high impedance); tOEH≦tCWL, invalid data will be out at each DQ.
19. All the Vcc and Vss pins shall be supplied with the same voltages.
20. tHPC(min.) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode /RAS cycle (EDO page mode mix cycle (1), (2)), minimum value of /CAS cycle (tCAS+tCP+2tT) becomes greater than the specified tHPC(min.) value. The value of /CAS cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large Vcc/Vss line noise, which causes to degrade ViH min./ViL max. level.

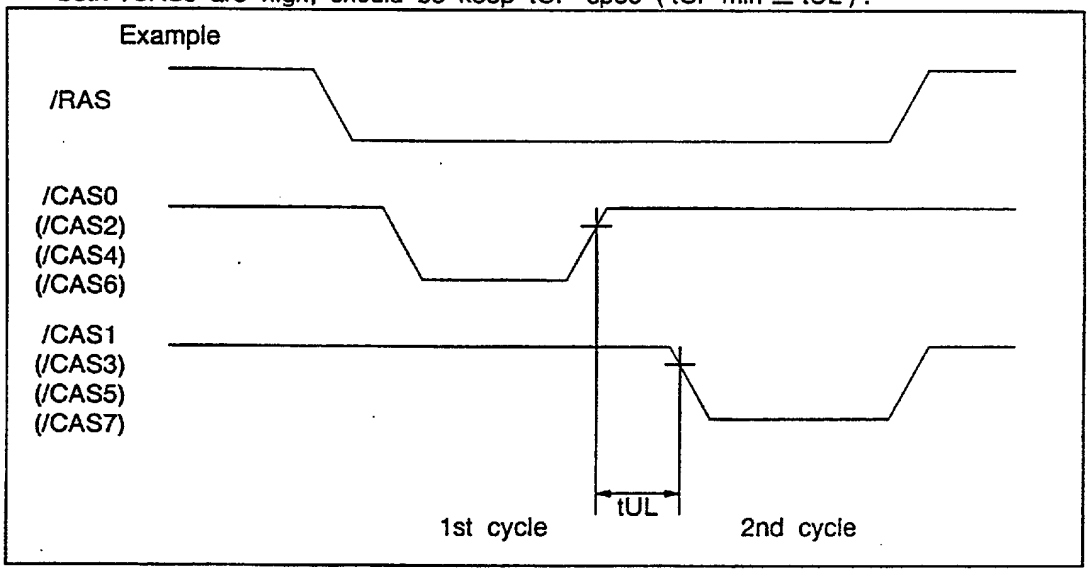
Notes concerning 2/CAS control

(1) In one memory cycle, activate both of 2/CASs (/CAS0 and /CAS1 (or /CAS2, 4, 6 and /CAS3, 5, 7)) or only one of them or neither of them.

(2) To activate both of 2/CASs in an early write cycle or a page mode early write cycle, please keep tSKW (skew between /CAS0 and /CAS1 (or /CAS2, 4 , 6 and /CAS3, 5, 7)) 5ns or less.

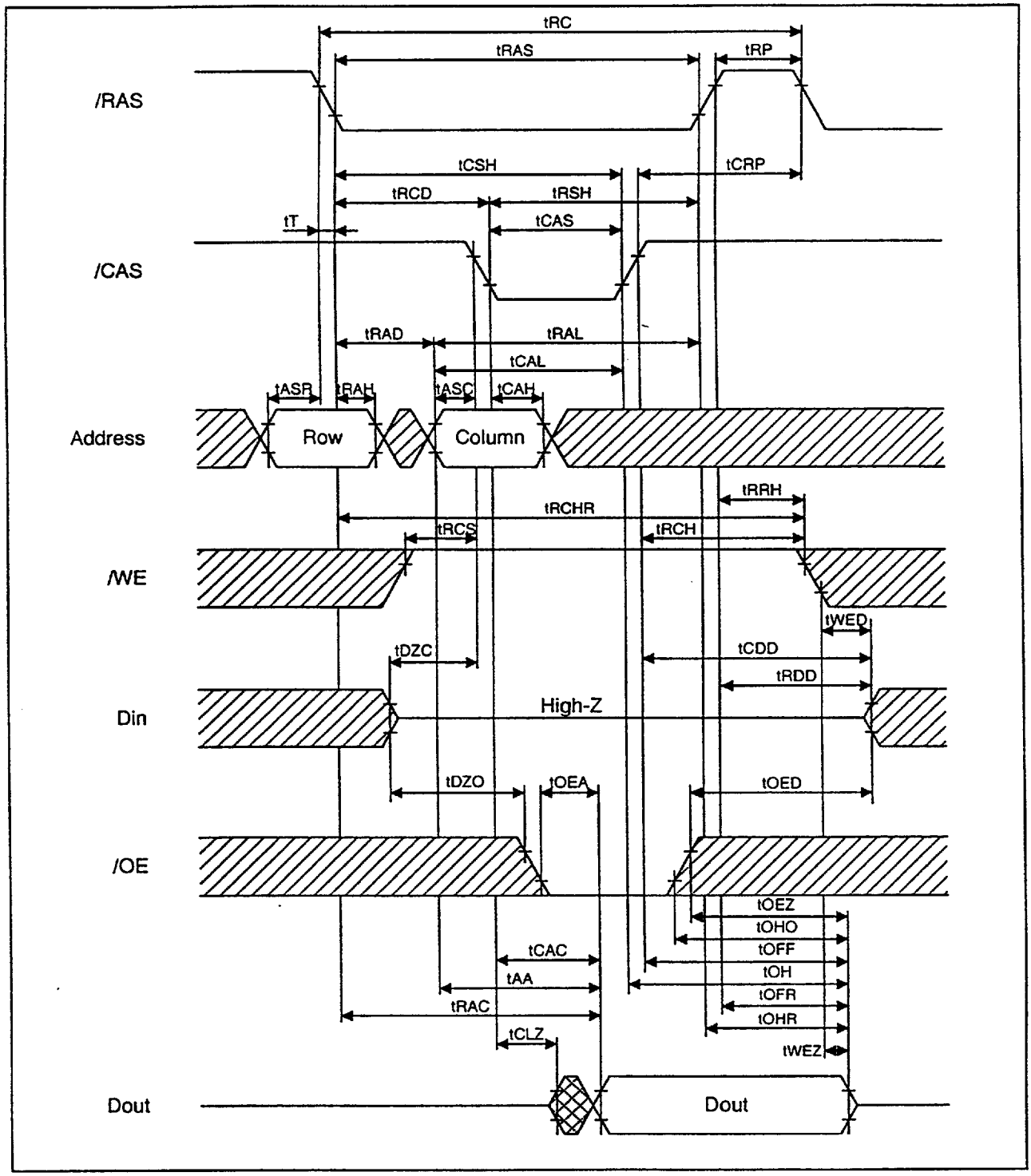


(3) If the differnt /CASs are activated in the consecutive page cycles, tUL the period that both /CASs are high, should be keep tCP spec (tCP min ≦ tUL) .



Timing Waveform

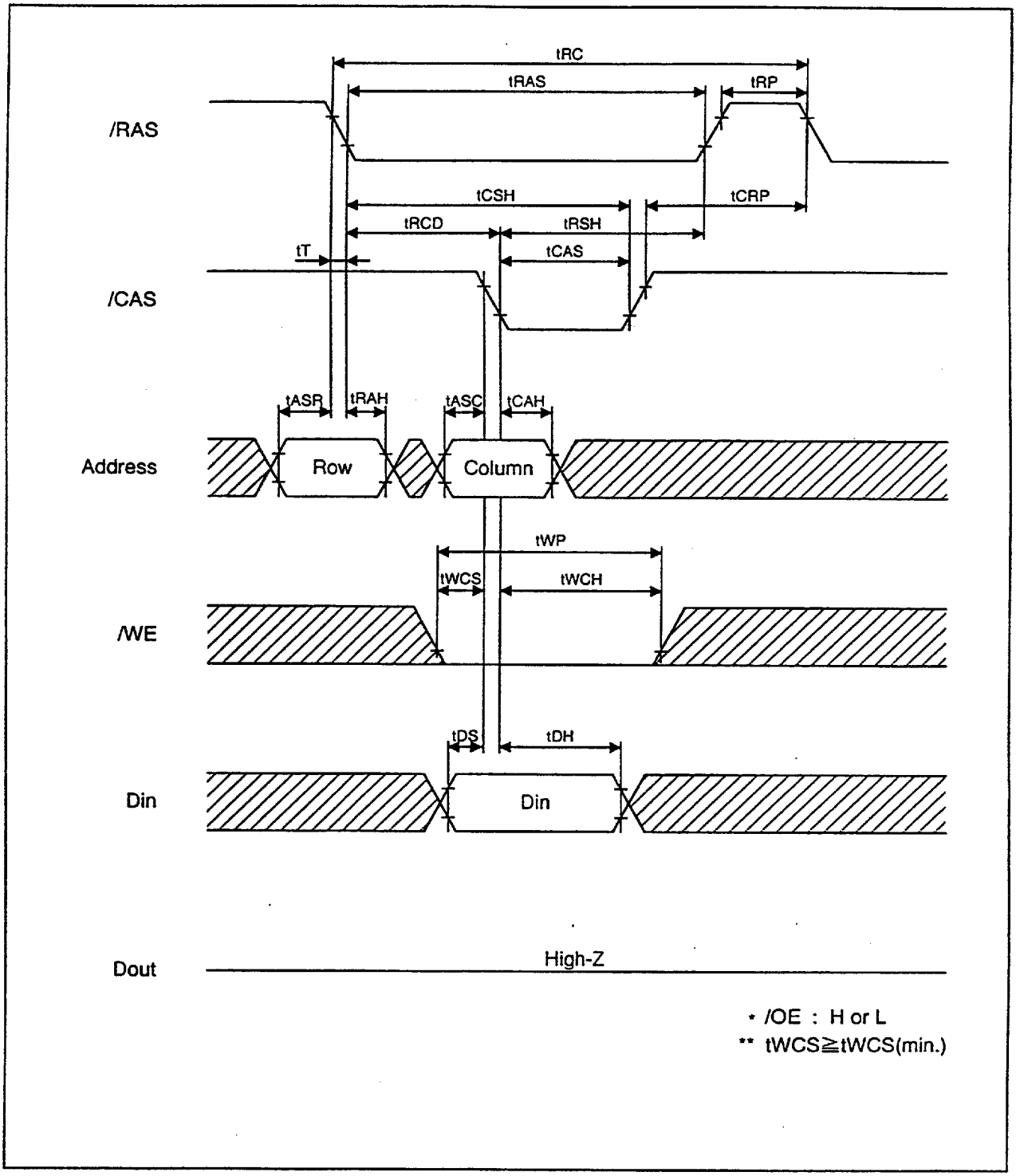
Read Cycle



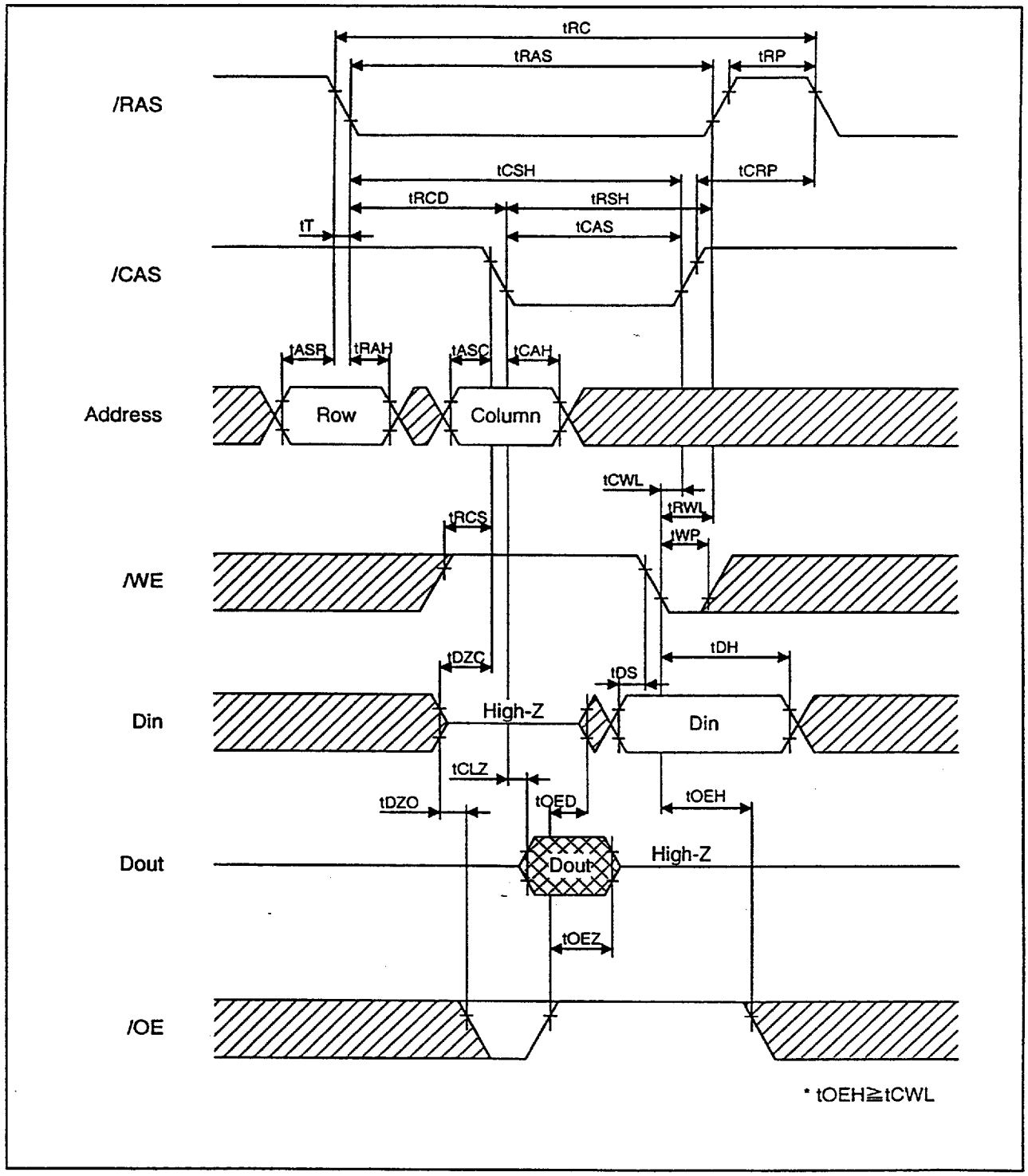
Note : ▨ : H or L (H : ViH(min.)≦Vin≦ViH(max.), L : ViL(min.)≦Vin≦ViL(max.))

▩ : Invalid Dout

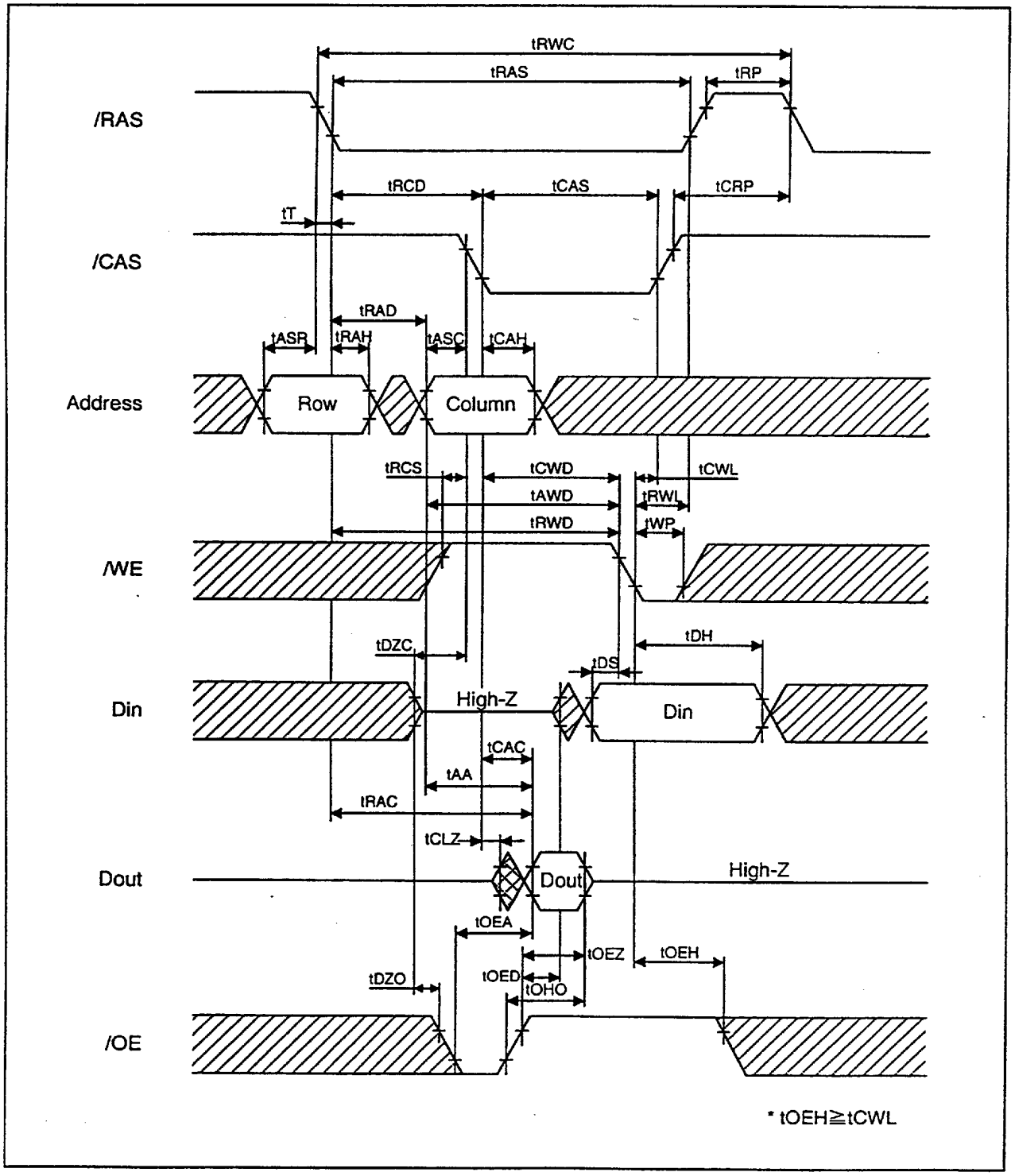
Early Write Cycle



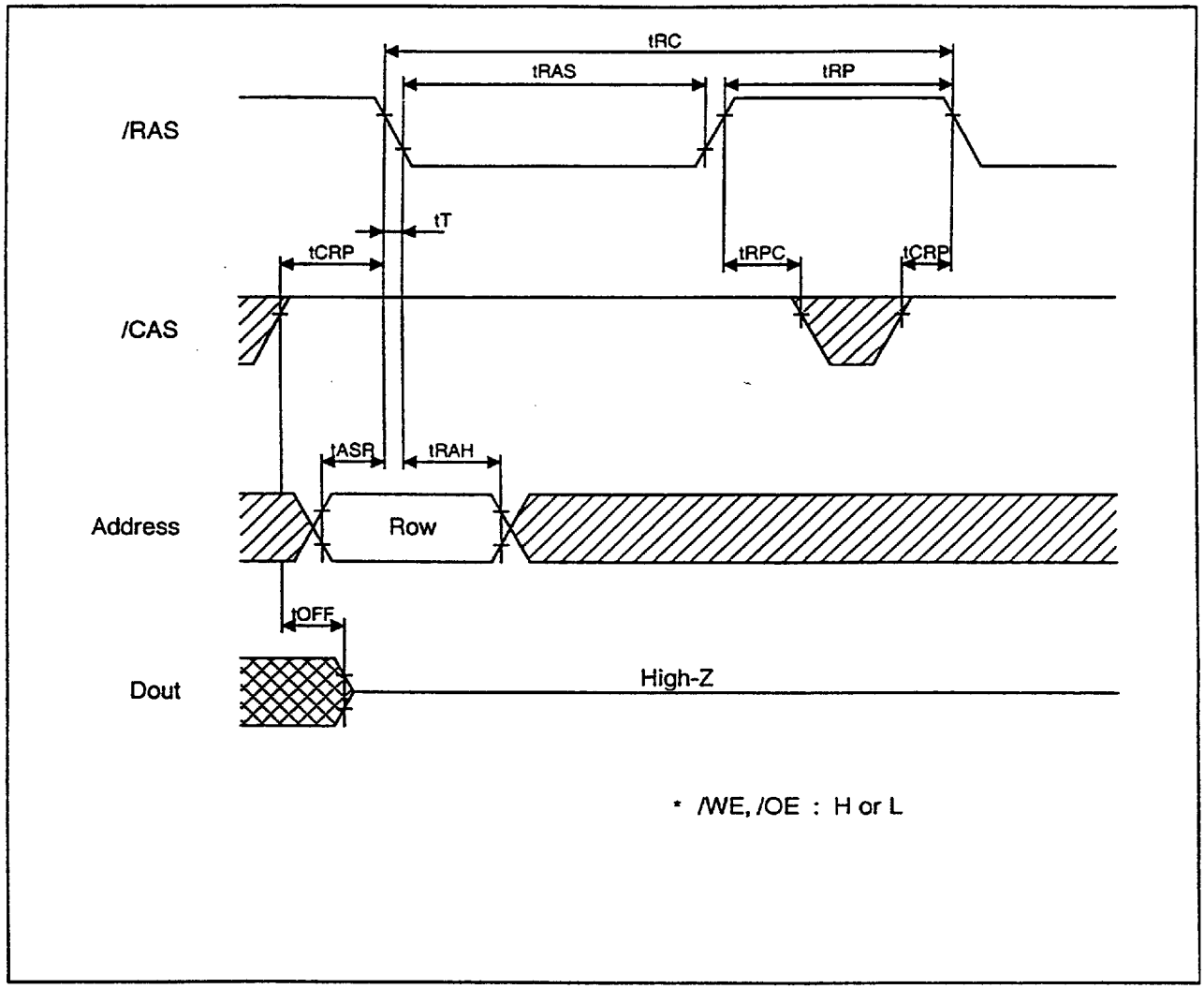
Delayd Write Cycle



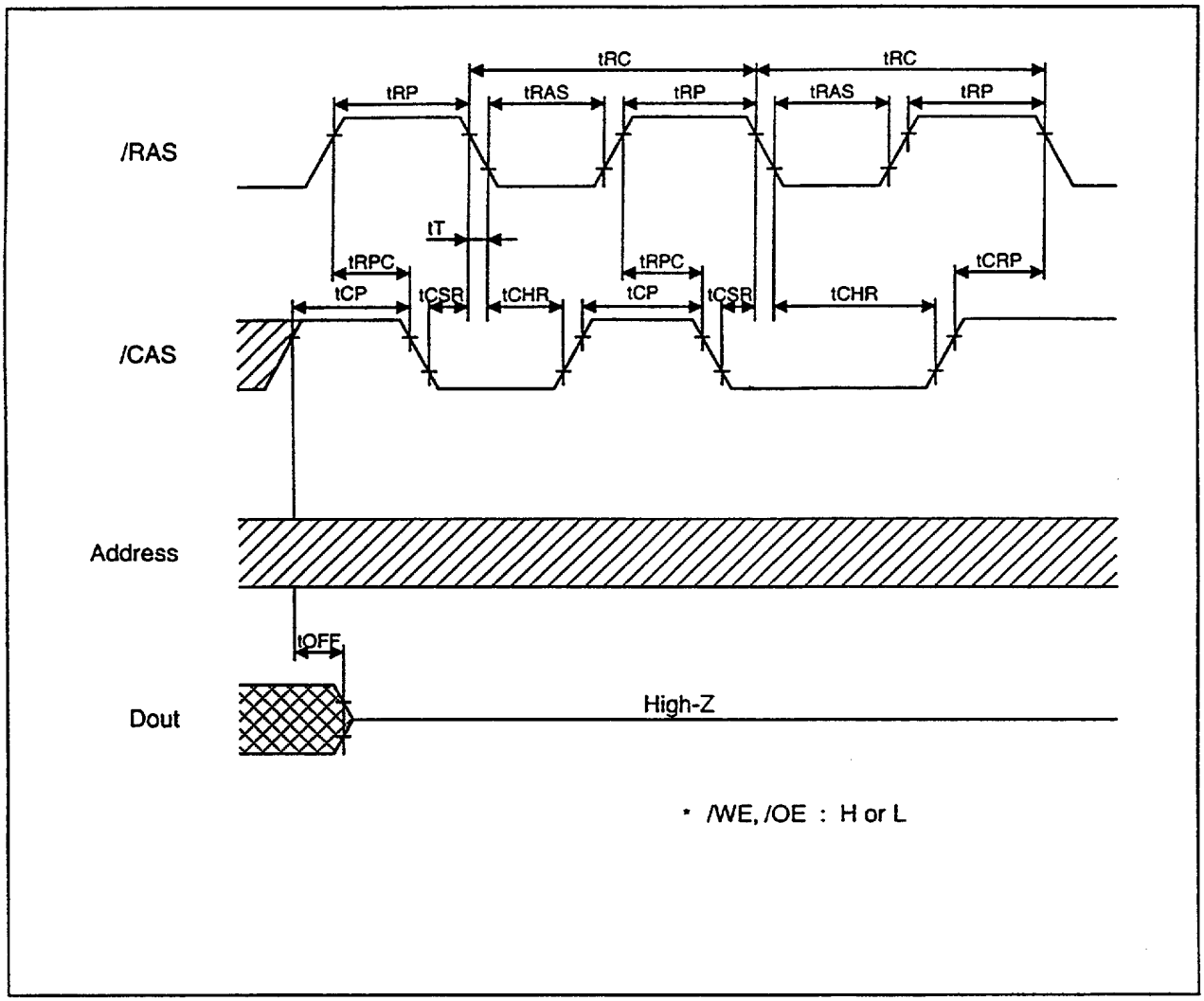
Read - Modify - Write Cycle



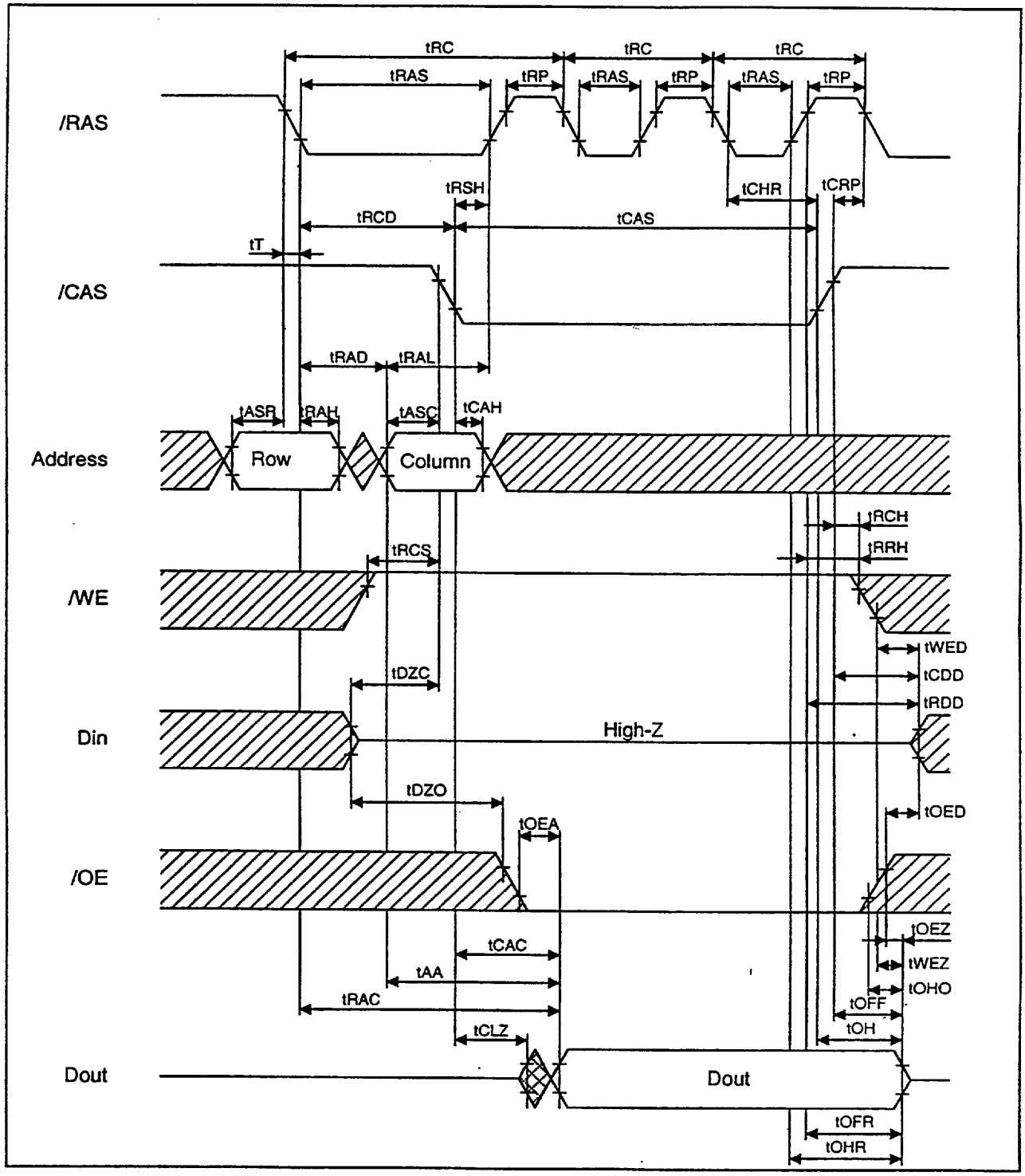
/RAS - Only Refresh Cycle



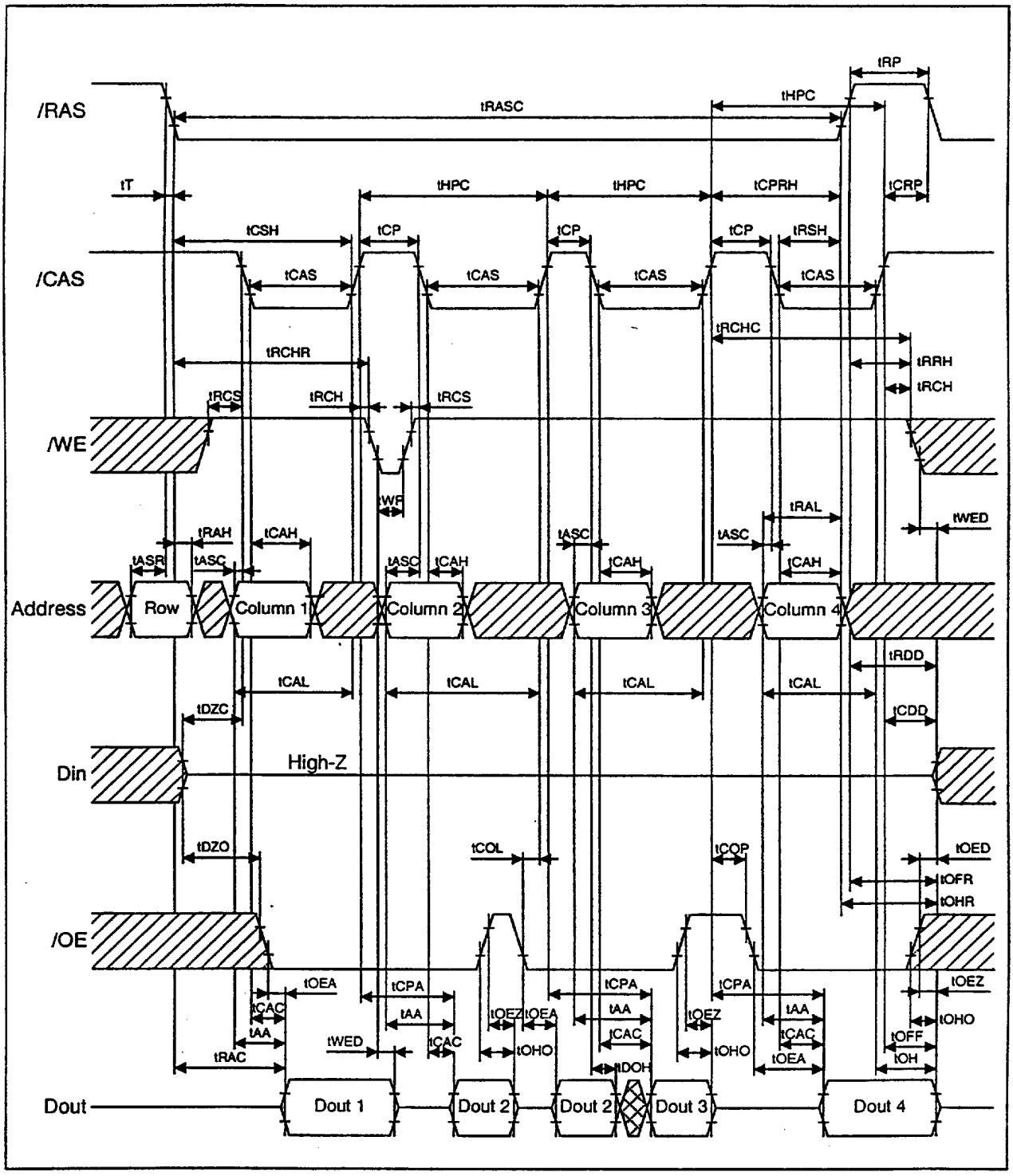
/CAS - Before - /RAS Refresh Cycle



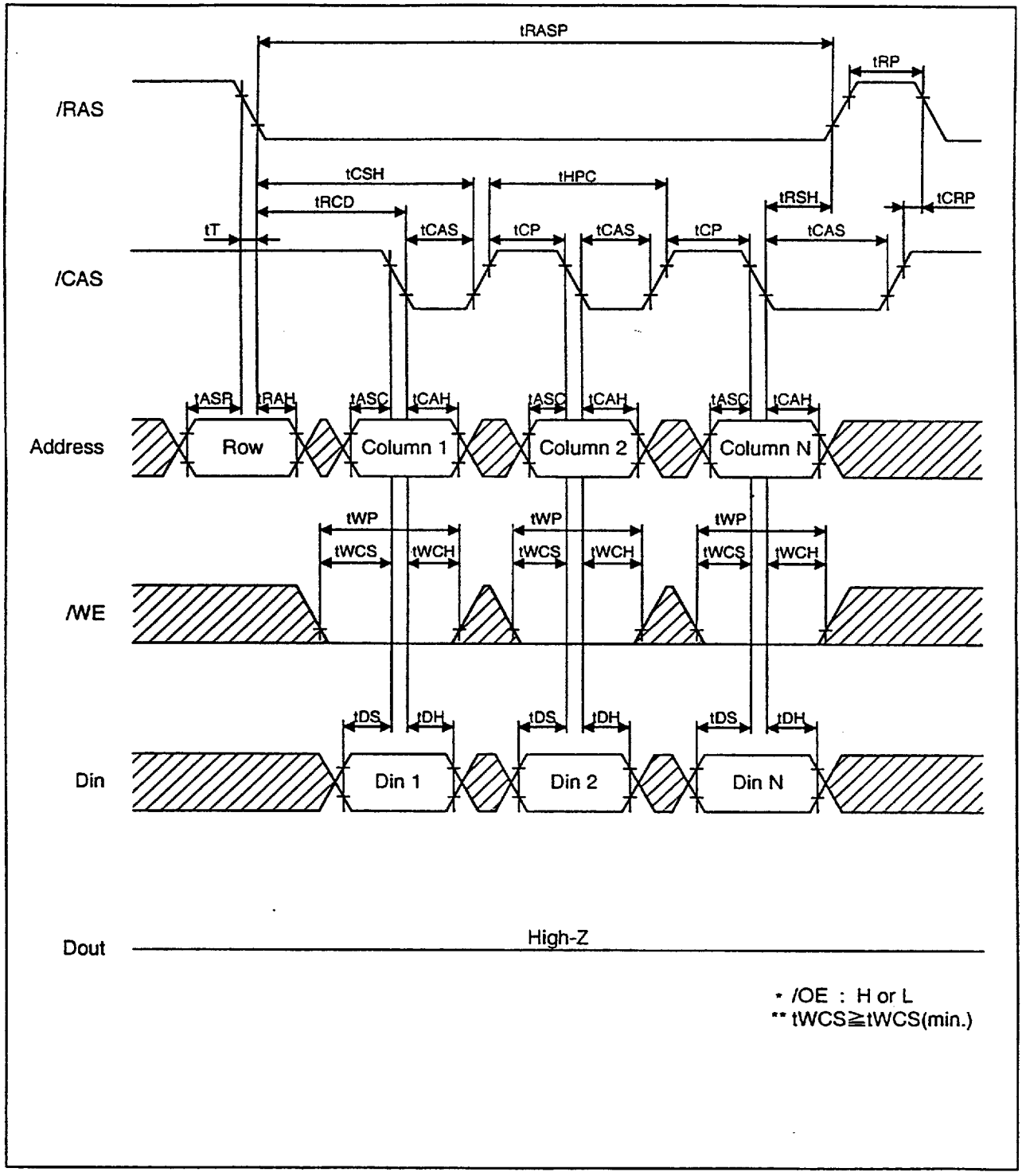
Hidden Refresh Cycle



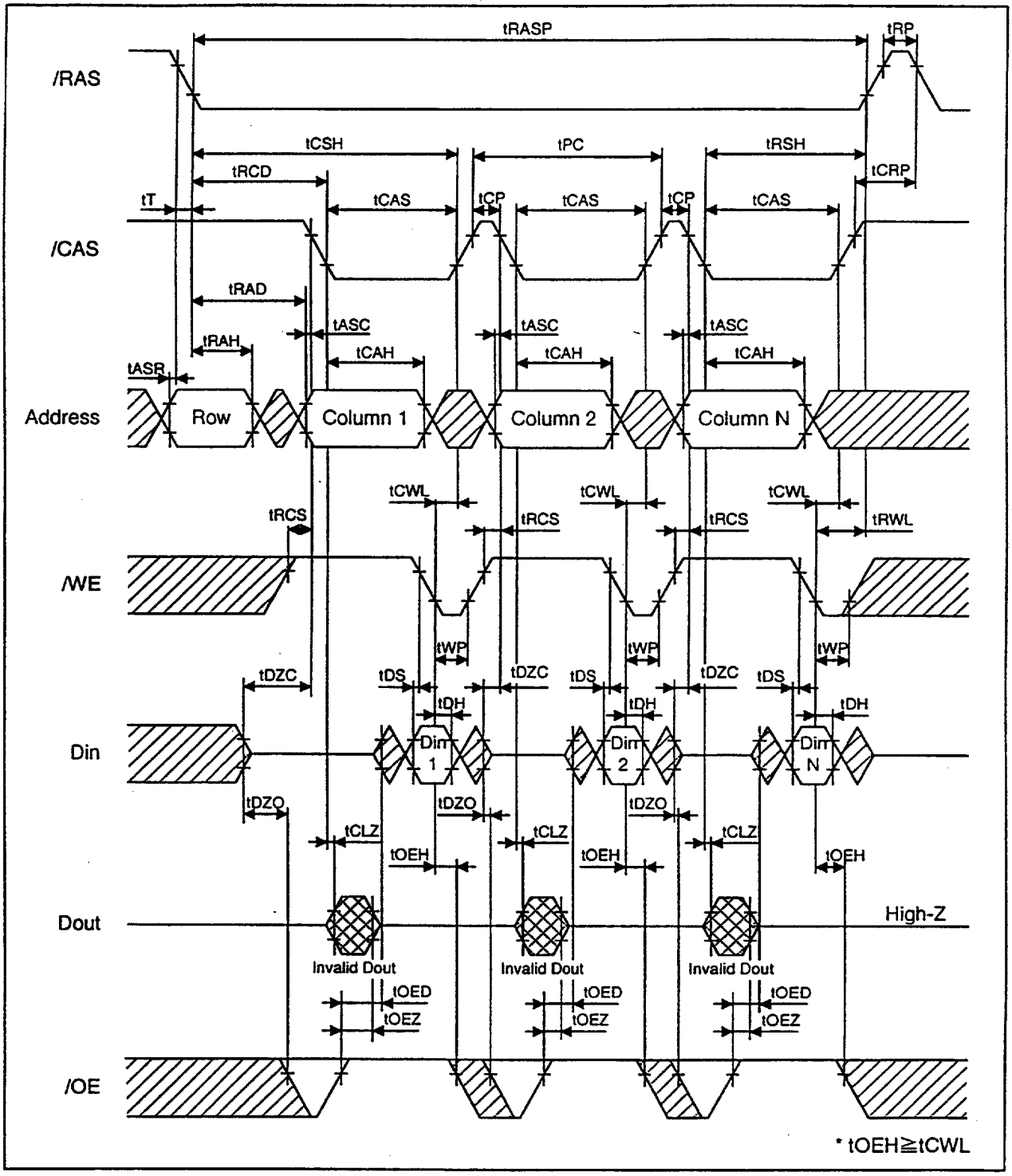
EDO Page Mode Read Cycle



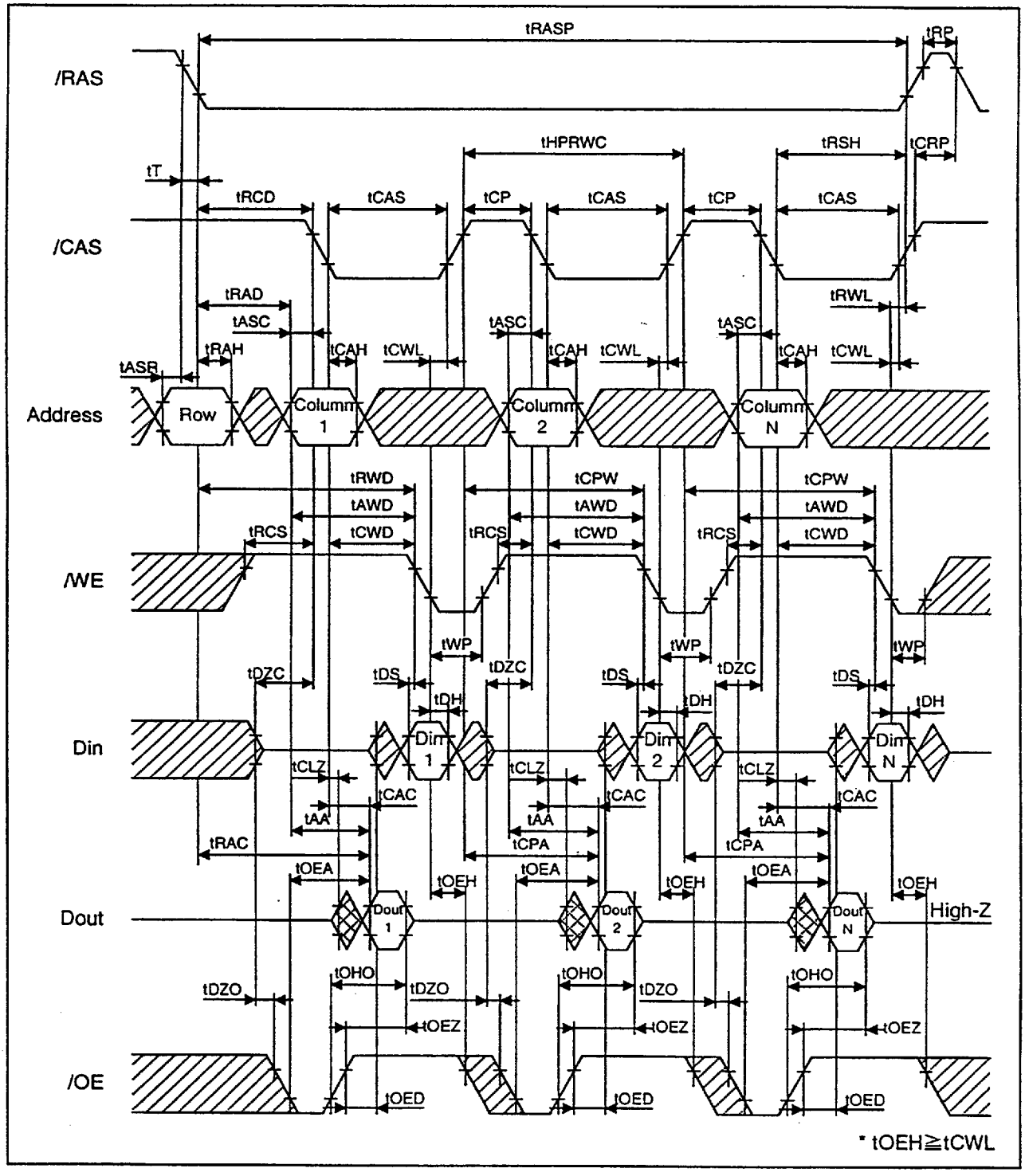
EDO Page Mode Eary Write Cycle



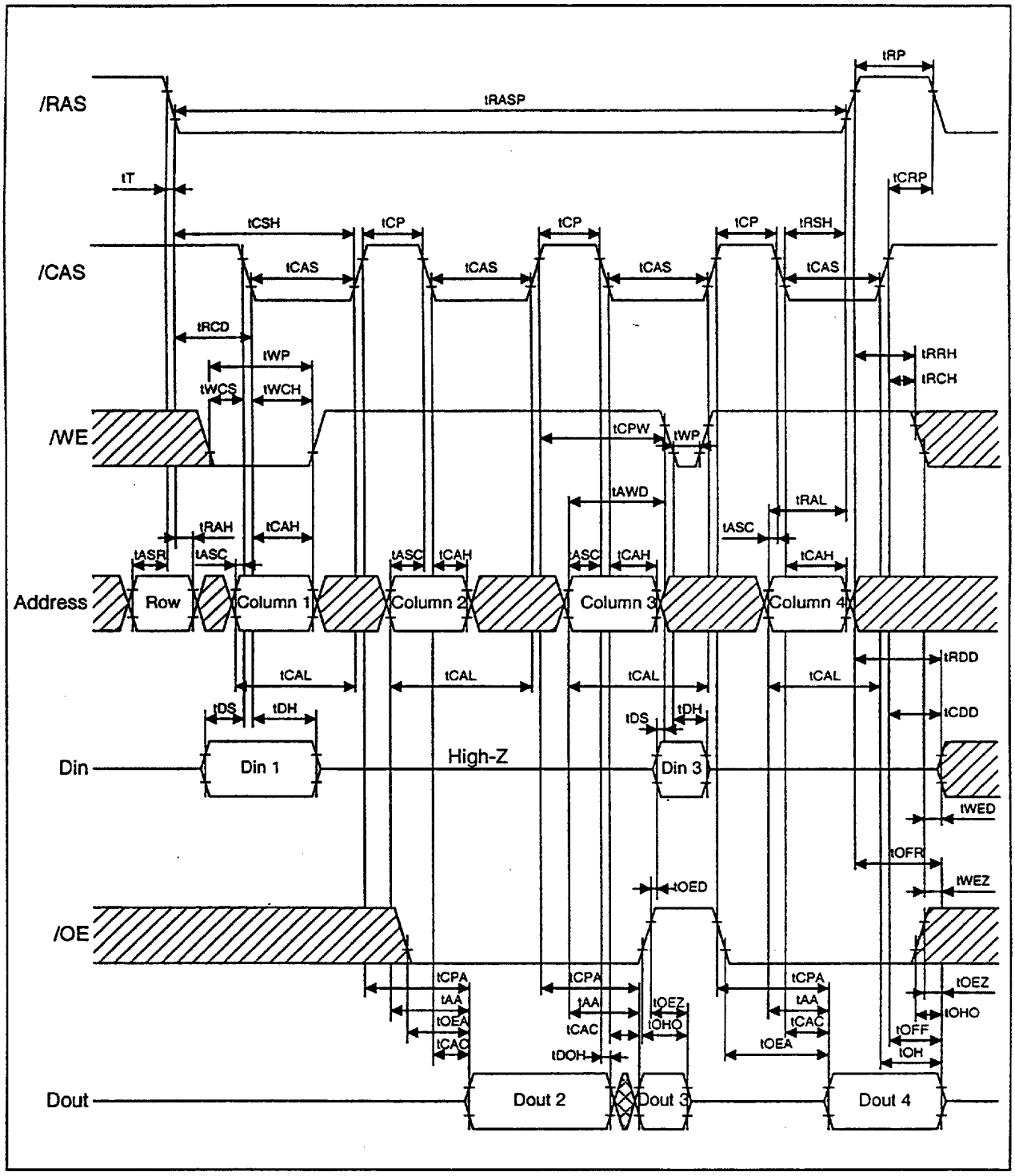
EDO Page Mode Delayed Write Cycle



EDO Page Mode Read - Modify - Write Cycle



EDO Page Mode Mix Cycle (1)



EDO Page Mode Mix Cycle (2)