



SANYO Semiconductors

# DATA SHEET

## LA6541NH — Monolithic Linear IC For CD Players and Recorders Four-Channel Driver IC

### Overview

The LA6541NH is a four-channel driver IC for CD players and recorders (four BTL amplifier channels).

### Functions

- Four BTL connection power amplifier channels
- $I_O$  max 0.7A
- Built-in level shifters
- Muting circuit (on/off control of all outputs)  
(This circuit applies to the BTL amplifier circuits. It does not control operation of the regulator.)
- Built-in regulator (provides a 5V output using an external pnp transistor)
- Thermal protection circuit (thermal shutdown circuit)

### Specifications

Maximum Ratings at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}$ max		14	V
Maximum input voltage	$V_{IN}$		13	V
Maximum output current	$I_O$ max	For each of the channel 1 to 4 outputs	0.7	A
Muting pin application voltage	VMUTE		13	V
Allowable power dissipation	Pd max	Independent IC	0.8	W
		Specified circuit board	1.8	W
Operating temperature	Topr		-30 to +85	$^\circ\text{C}$
Storage temperature	Tstg		-55 to +150	$^\circ\text{C}$

\* Specified substrate : 76.1mm×114.3mm×1.6mm, glass epoxy board.

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**SANYO Semiconductor Co., Ltd.**

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# LA6541NH

## Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	$V_{CC1}$		5.6 to 13	V
Supply voltage 2	$V_{CC2}$	Only used by the BTL amplifiers (Not used by the 5V regulator circuit)	3.9 to 13	V

## Electrical Characteristics at $T_a = 25^\circ\text{C}$ , $V_{CC1} = V_{CC2} = 8\text{V}$ , $V_{REF} = 2.5\text{V}$ , unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
<b>Overall Characteristics</b>						
No-load current drain, on state	$I_{CCON}$	All outputs on, MUTE : high		20	40	mA
No-load current drain, off state	$I_{CCOFF}$	All outputs off, MUTE : low		15	35	mA
Thermal shutdown circuit operating temperature	TSD	(Design guarantee value *1)	150	175	200	$^\circ\text{C}$
<b>Output Amplifier Block</b>						
Output offset voltage	$V_{OFF}$	The voltage difference between each of the + or - outputs.	-50		50	mV
VREF input voltage range	$V_{IN}V_{REF}$		1.5		$V_{CC}-1.5$	V
Output voltage	$V_O$	The voltage across the outputs when $R_L = 8\Omega$	4	4.7		V
Voltage gain, input to output	VG	The voltage gain from an input to the corresponding +/- outputs.*2		9		dB
Slew rate	SR	(Design guarantee value *1)		0.15		$\text{V}/\mu\text{s}$
Muting on voltage	$V_{MUTE}$	The voltage at which the output on/off state changes		1.2		V
<b>Power Supply Block (Using a 2SB632K)</b>						
5V power supply voltage		$I_O = 200\text{mA}$	4.75	5.00	5.25	V
Line regulation	$\Delta V_{OLIN}$	$5.6\text{V} \leq V_{CC} \leq 12\text{V}$		20	100	mV
Load regulation	$\Delta V_{OLOAD}$	$5\text{mA} \leq I_O \leq 200\text{mA}$		50	150	mV
<b>Reset Block</b>						
RESET pin high-level voltage	$V_{ORH}$		4.73	4.98	5.23	V
RESET pin low-level voltage	$V_{ORL}$	$I_{SRL} = 2\text{mA}$ , Cd-GND		100	200	mV
RESET pin threshold voltage	$V_{RT}$	*4		4.2		V
RESET pin hysteresis	$V_{HYS}$	*5	40	100	200	mV
RESET pin output delay time	td	Cd = $0.1\mu\text{F}$		10		ms

\*1 : These parameters are not tested.

\*2 : The gain from input to output when only the  $V_{IN}^*$  pins are used.

\*3 : The MUTE pin voltage when the output changes between the on and off states. When the MUTE pin is high, all the BTL amplifiers will be on, and the when MUTE is low, all the BTL amplifiers will be off.

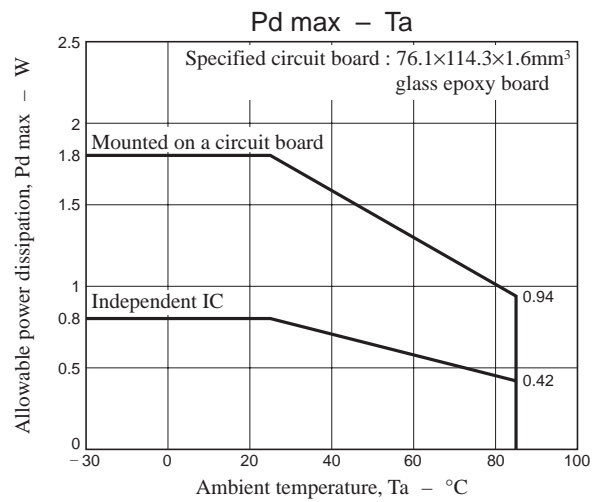
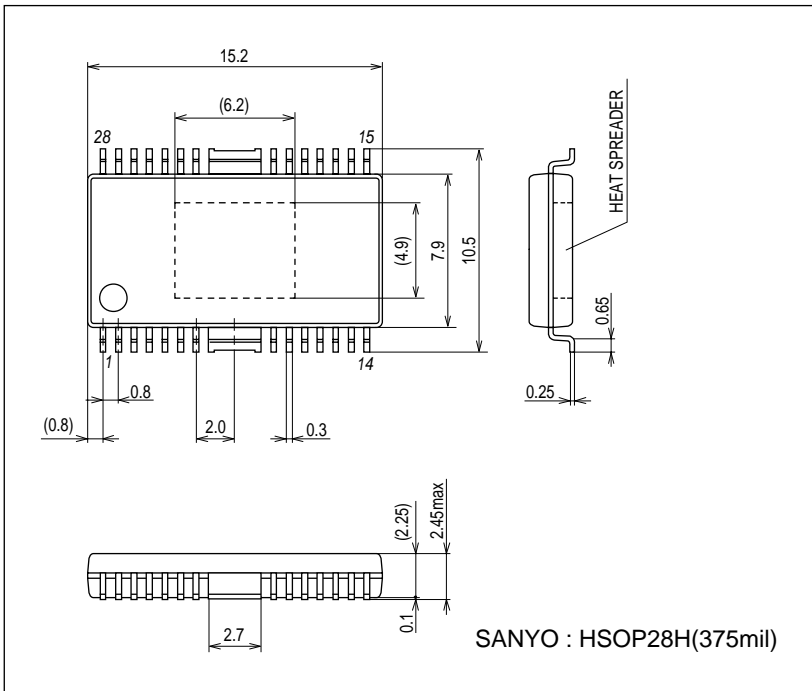
\*4 : The 5V regulator voltage when the RESET pin goes from high to low.

\*5 : The 5V regulator voltage difference between the RESET pin going from high to low the RESET pin going from low to high. That is, the hysteresis.

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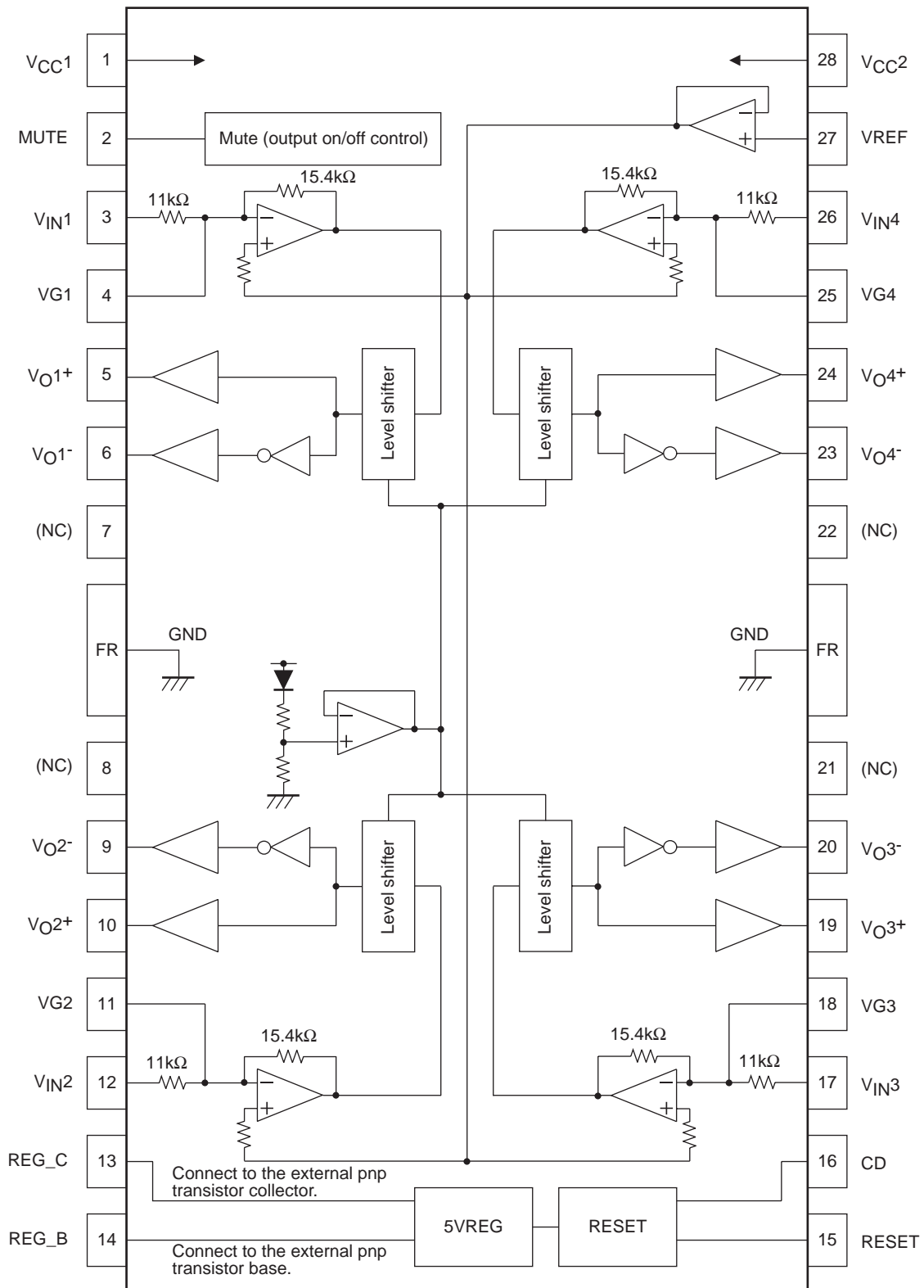
## Package Dimensions

unit : mm (typ)  
3233B



# LA6541NH

## Block Diagram



# LA6541NH

## Pin Functions

Pin No.	Pin	Description
1	V <sub>CC</sub> 1	Power supply (This pin is shorted to V <sub>CC</sub> 2 (pin 28))
2	MUTE	Output on/off control
3	V <sub>IN</sub> 1	Channel 1 input
4	VG1	Channel 1 input (Gain setting)
5	V <sub>O</sub> 1 <sup>+</sup>	Channel 1 output (+)
6	V <sub>O</sub> 1 <sup>-</sup>	Channel 1 output (-)
7	(NC)	(This pin must not be used.)
8	(NC)	(This pin must not be used.)
9	V <sub>O</sub> 2 <sup>-</sup>	Channel 2 output (-)
10	V <sub>O</sub> 2 <sup>+</sup>	Channel 2 output (+)
11	VG2	Channel 2 input (Gain setting)
12	V <sub>IN</sub> 2	Channel 2 input
13	REG_C	Connect this pin to the external pnp transistor collector. (This is the 5 V regulator output)
14	REG_B	Connect this pin to the external pnp transistor base.
15	RESET	Reset output
16	CD	Connection for the reset delay time setting capacitor
17	V <sub>IN</sub> 3	Channel 3 input (Gain setting)
18	VG3	Channel 3 input (Gain setting)
19	V <sub>O</sub> 3 <sup>+</sup>	Channel 3 output (+)
20	V <sub>O</sub> 3 <sup>-</sup>	Channel 3 output (-)
21	(NC)	(This pin must not be used.)
22	(NC)	(This pin must not be used.)
23	V <sub>O</sub> 4 <sup>-</sup>	Channel 4 output (-)
24	V <sub>O</sub> 4 <sup>+</sup>	Channel 4 output (+)
25	VG4	Channel 4 input (Gain setting)
26	V <sub>IN</sub> 4	Channel 4 input (Gain setting)
27	VREF	Reference voltage input
28	V <sub>CC</sub> 2	Power supply (This pin is shorted to V <sub>CC</sub> 1 (pin 1))

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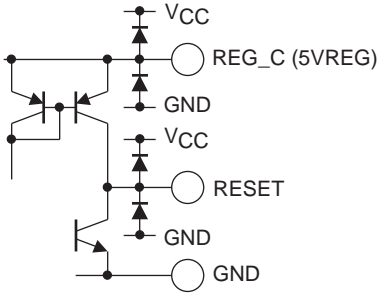
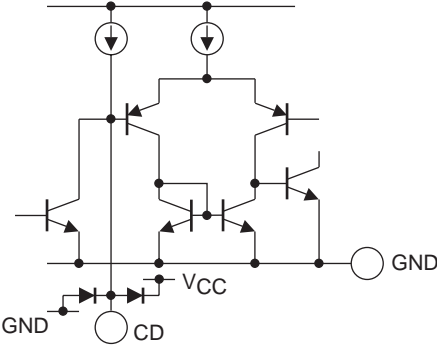
## Equivalent Circuits

Pin No.	Pin	Description	Equivalent circuit
3 4 12 11 17 18 26 25	$V_{IN1}$ $VG1$ $V_{IN2}$ $VG2$ $V_{IN3}$ $VG3$ $V_{IN4}$ $VG4$	Input pins.	<p>The diagram shows a differential pair of transistors. Each input pin is connected to the base of a transistor. The bases are also protected by diodes connected to GND and VCC. A 11kΩ resistor is connected between the two bases and VCC.</p>
5 6 10 9 19 20 24 23	$V_{O1+}$ $V_{O1-}$ $V_{O2+}$ $V_{O2-}$ $V_{O3+}$ $V_{O3-}$ $V_{O4+}$ $V_{O4-}$	Output pins.	<p>The diagram shows a differential pair of transistors. The output pins are connected to the collectors. A 33kΩ resistor is connected between the two collectors and VCC.</p>
2	MUTE	Muting control input. The outputs will be on when the MUTE pin is at the high level. The outputs will be off when the MUTE pin is at the low level ; in particular, the outputs go to the high-impedance state at this time.	<p>The diagram shows a transistor whose base is connected to the MUTE pin through a 40kΩ resistor. The base is also connected to GND through a 30kΩ resistor. The emitter is connected to GND, and the collector is connected to the output stage.</p>
27	VREF	Reference voltage input.	<p>The diagram shows a differential pair of transistors. The VREF pin is connected to the base of one transistor. The bases are also protected by diodes connected to GND and VCC. A resistor is connected between the two bases and VCC.</p>

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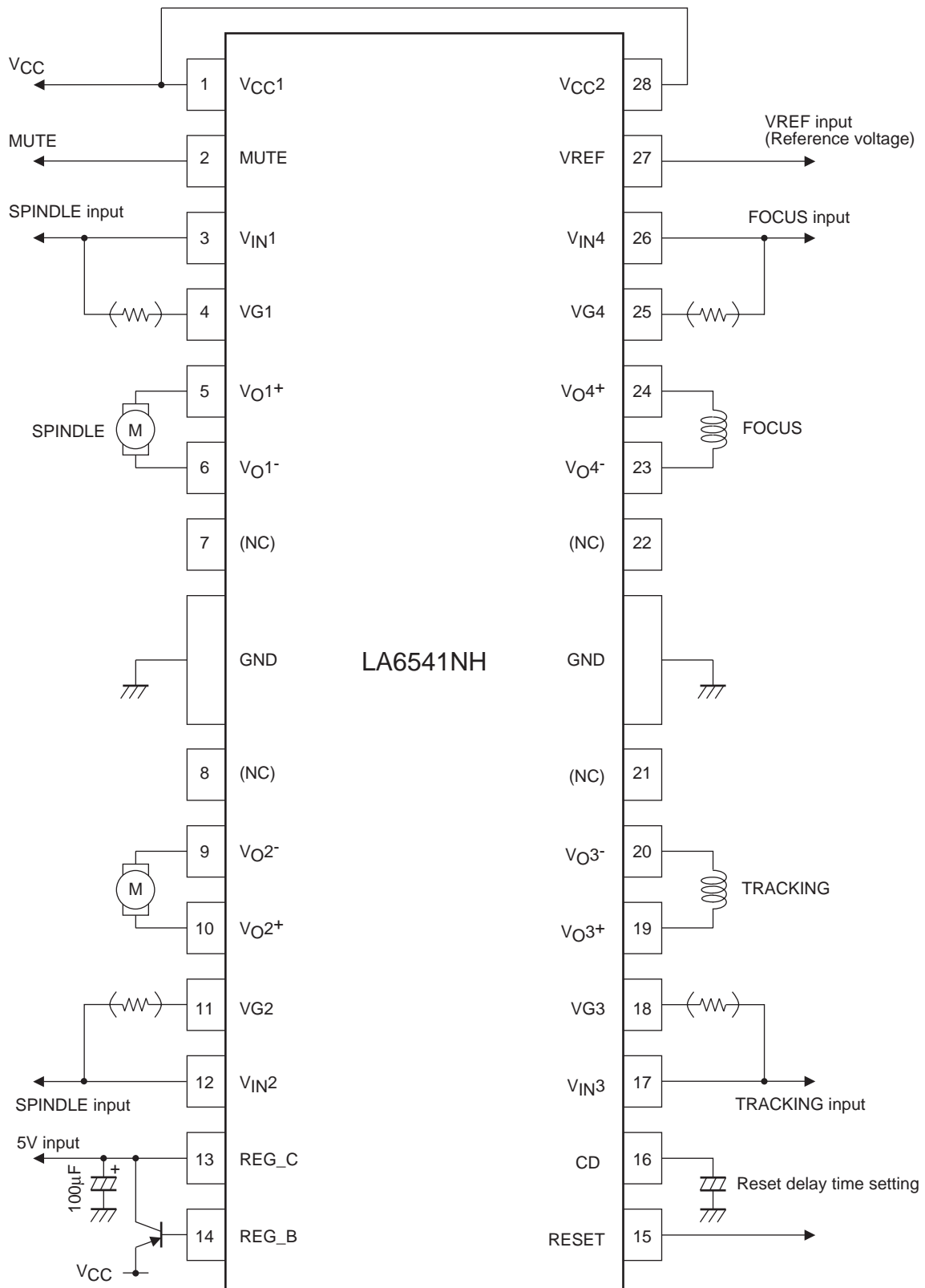
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Pin No.	Pin	Description	Equivalent circuit
15	RESET	<p>Reset output.</p> <p>When REG C (5VREG) is high, RESET will be high.</p> <p>When REG C (5VREG) is low, RESET will be low.</p> <p>See section 11, Reset Operation, for details on the reset operation.</p>	
16	CD	<p>Reset output delay time setting.</p> <p>The delay time until the point the reset output switches from low to high is set by the capacitor connected between this pin and ground.</p> <p>See section 11, Reset Operation, for details on the reset operation.</p>	

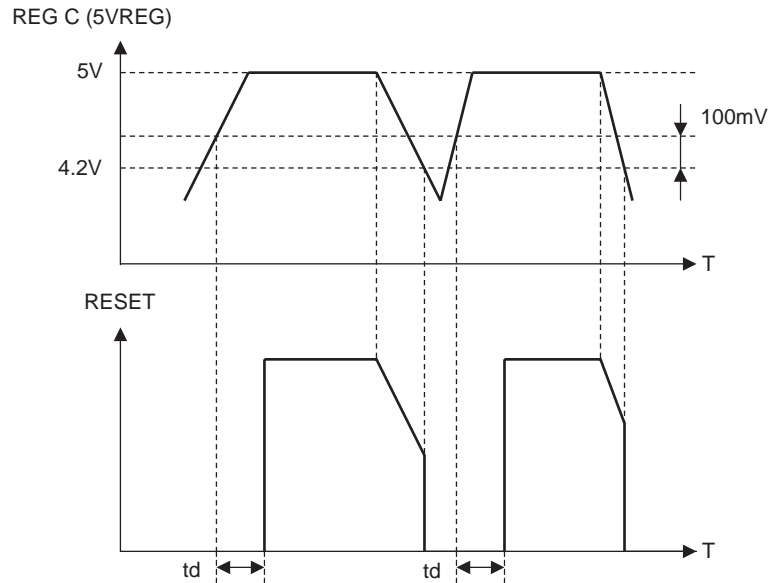
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## Application Circuit Example





## Reset Operation



\*1 :  $t_d$  is the delay time. It is set by an external capacitor connected between the CD pin and ground).

\*2 : The voltage at which RESET changes state is a typical value (voltage).

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