REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30			

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Thomas M. Hess	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thomas M. Hess APPROVED BY Monica L. Poelking DRAWING APPROVAL DATE 95-03-31 REVISION LEVEL	MICROCIRCUIT, DIGITAL, CMOS, 32-BIT EMBEDDED MICROPROCESSOR, MONOLITHIC SILICON SIZE A | CAGE CODE 67268 | 5962-95570 SHEET 1 OF 30

DESC FORM 193
JUL 94

5962-E149-95

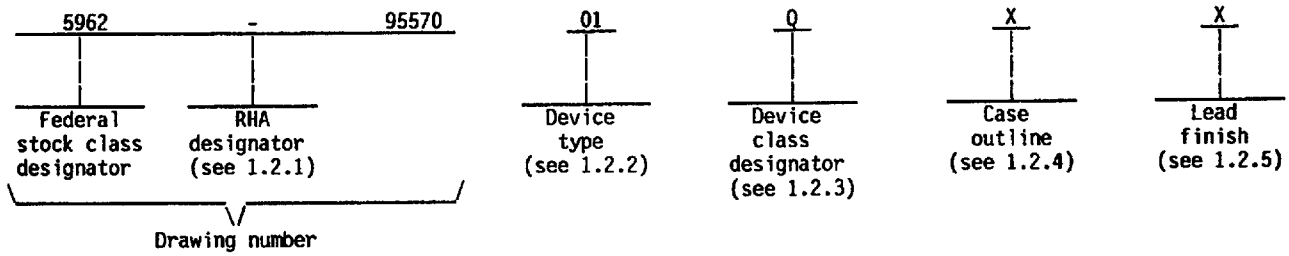
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0012130 902

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Three product assurance classes consisting of space application (device class V), military high reliability (device classes M and Q), and non-traditional military (device class N) with a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". For device class N, the user is cautioned to assure that the device is appropriate for the application environment. When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes N, Q, and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	80386EX	32-bit embedded microprocessor 1/2/
02	80386EX	32-bit embedded microprocessor 1/2/

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
N	Certification and qualification to MIL-I-38535 with a non-traditional performance environment 3/
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	168	Ceramic pin grid array.

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes N, Q, and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ The case operating temperature, T_C, for device 01 is -55°C to +125°C, device 02 is -40°C to +125°C.
2/ The JTAG feature for this device is available however, at this time the limits have not been characterized. JTAG limits will be added when available.
3/ Any device outside the traditional performance environment; i.e., an operating temperature range of -55°C to +125°C and which requires hermetic packaging.

1.3 Absolute maximum ratings. 4/

Storage temperature range	-65°C to +150°C
Supply voltage with respect to ground	-0.5 V dc to +6.5 V dc
Voltage on any pin with respect to ground	-0.5 V dc to V_{CC} + 0.5 V dc
Lead temperature (soldering 10 seconds)	+300°C
Junction temperature (T_J)	+150°C
Thermal resistance, junction-to-case (θ_{JC}): Case X	3.0°C/W
Thermal resistance, junction-to-ambient (θ_{JA}): Case X	22.0°C/W

1.4 Recommended operating conditions.

Case operating temperature range	
Device 01	-55°C to +125°C
Device 02	-40°C to +125°C
Supply voltage, V_{CC}	4.75 V dc ≤ V_{CC} ≤ 5.25 V dc

1.5 Digital logic testing for device classes N, Q, and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	93 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

4/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2.2 Non Government publications. The following document(s) for a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issueof the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies shouldbe addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational sevices.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes N, Q, and V and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Boundary Scan Instruction Codes. For device 01 and 02 the boundary scan instruction codes shall be as specified on figure 5.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes N, Q, and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes N, Q, and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes N, Q, and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

3.11 IEEE 1149.1 compliance. Device type 01 and 02 shall be compliant with IEEE 1149.1.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}		1,2,3	All	-0.5	0.3 V_{CC}	V
Input high voltage	V_{IH}		1,2,3	All	0.7 V_{CC}	V_{CC}+0.5	V
Output low voltage all pins except PORT3 PORT3	V_{OL}	 I_{OL} = 8.0 mA I_{OL} = 16.0 mA	1,2,3	All		 0.40 0.40	V
Output high voltage all pins except PORT3 PORT3	V_{OH}	 I_{OH} = -8.0 mA I_{OH} = -16.0 mA	1,2,3	All	 V_{CC}-0.8 V_{CC}-0.8		V
Input leakage current	I_{LI}	$0 \le V_{IN} \le V_{CC}$	1,2,3	All		+/-15	µA
Output leakage current	I_{LO}	$0.45 < V_{OUT} < V_{CC}$	1,2,3	All		+/-15	µA
Powerdown current	I_{PD}		1,2,3	All		100	µA
Idle mode current	I_{IDLE}	25 MHz, V_{CC} = 5.25 V	4,5,6	All		85	mA
Supply current	I_{CC}	25 MHz, V_{CC} = 5.25 V	4,5,6	All		250	mA
Pin capacitance	C_S	See 4.4.1.c	4	All		10	pF
Functional tests		See 4.4.1.b	7,8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Operating frequency		One-half CLK2 frequency	9,10,11	All	0	25	MHz
Clock period	t1	See figure 4	9,10,11	All	20		ns
Clock high time	t2a	At $V_{CC}/2$ 3/ See figure 4	9,10,11	All	7		ns
Clock high time	t2b	At V_{CC} - 0.8 V 3/ See figure 4	9,10,11	All	4		ns
Clock low time	t3a	At $V_{CC}/2$ 3/ See figure 4	9,10,11	All	7		ns
Clock low time	t3b	At 0.8 V 3/ See figure 4	9,10,11	All	5		ns
Clock fall time	t4	V_{CC} - 0.8 V to 0.8 V 3/ See figure 4	9,10,11	All		7	ns
Clock rise time	t5	0.8 V to V_{CC} - 0.8 V 3/ See figure 4	9,10,11	All		7	ns
A25:1 valid delay	t6	C_L = 50 pF 4/ See figure 4	9,10,11	All	4	29	ns
A25:1 float delay	t7	5/ See figure 4	9,10,11	All	4	36	ns
$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ valid delay	t8	C_L = 50 pF 4/ See figure 4	9,10,11	All	4	29	ns
$\overline{SMIACT}$ valid delay	t8a	C_L = 50 pF 4/ See figure 4	9,10,11	All	4	29	ns
$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ float delay	t9	5/ See figure 4	9,10,11	All	4	30	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 4.75 V ≤ V_{CC} ≤ 5.25 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$, $\overline{REFRESH}$ valid delay	t10	C_L = 50 pF 4/ See figure 4	9,10,11	All	4	29	ns
$\overline{RD}$, $\overline{WR}$ valid delay	t10a		9,10,11	All	4	31	ns
W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{RD}$, $\overline{WR}$, $\overline{ADS}$ float delay	t11	5/ See figure 4	9,10,11	All	4	39	ns
D15:0 write data valid delay	t12	C_L = 50 pF 4/ See figure 4	9,10,11	All	4	31	ns
D15:0 write data float delay	t13	5/ See figure 4	9,10,11	All	4	24	ns
HLDA valid delay	t14	C_L = 50 pF 4/ See figure 4	9,10,11	All	4	27	ns
$\overline{NA}$ set-up time	t15	See figure 4	9,10,11	All	5		ns
$\overline{NA}$ hold time	t16	See figure 4	9,10,11	All	10		ns
$\overline{READY}$ setup time	t19	See figure 4	9,10,11	All	9		ns
$\overline{BS8}$ setup time	t19a	See figure 4	9,10,11	All	11		ns
$\overline{READY}$, $\overline{BS8}$ hold time	t20	See figure 4	9,10,11	All	4		ns
D15:0 read set-up time	t21	See figure 4	9,10,11	All	7		ns
D15:0 read hold time	t22	See figure 4	9,10,11	All	7		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Hold set-up time	t23	See figure 4	9,10,11	All	9		ns
Hold hold time	t24	See figure 4	9,10,11	All	3		ns
RESET set-up time	t25	See figure 4	9,10,11	All	8		ns
RESET hold time	t26	See figure 4	9,10,11	All	4		ns
NMI, set-up time	t27	See figure 4 6/	9,10,11	All	12		ns
$\overline{SMI}$ set-up time	t27a		9,10,11	All	12		ns
NMI, hold time	t28	See figure 4 6/	9,10,11	All	6		ns
$\overline{SMI}$ hold time	t28a		9,10,11	All	6		ns
PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$ set-up time	t29	See figure 4 6/	9,10,11	All	6		ns
PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$ hold time	t30		9,10,11	All	5		ns
$\overline{Ready}$ valid delay	t31	See figure 4	9,10,11	All	4	36	ns
$\overline{Ready}$ float delay	t32	See figure 4	9,10,11	All	4	34	ns
$\overline{LBA}$ valid delay	t33	See figure 4	9,10,11	All	4	32	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{CS6:0}$, $\overline{UCS}$ valid delay	t34	See figure 4	9,10,11	All	4	39	ns
A25:1, $\overline{BHE}$, $\overline{BLE}$ valid to $\overline{WR}$ low	t41	See figure 4	9,10,11	All	0		ns
$\overline{CS6:0}$, $\overline{UCS}$ valid to $\overline{WR}$ low	t41a	See figure 4	9,10,11	All	0		ns
A25:1, $\overline{BHE}$, $\overline{BLE}$ hold after $\overline{WR}$ high	t42	See figure 4	9,10,11	All	5		ns
$\overline{UCS}$, $\overline{CS6:0}$ hold after $\overline{WR}$ high	t42a	See figure 4	9,10,11	All	5		ns
D15:0 output valid to $\overline{WR}$ high	t43	See figure 4 7/	9,10,11	All	3CLK2 -27		ns
D15:0 output hold after $\overline{WR}$ high	t44	See figure 4	9,10,11	All	CLK2 -10		ns
$\overline{WR}$ high to D15:0 float	t45	See figure 4 5/	9,10,11	All		CLK2 +10	ns
$\overline{WR}$ pulse width	t46	See figure 4	9,10,11	All	3CLK2 -15		ns
A25:1, $\overline{BHE}$, $\overline{BLE}$ valid to D15:0 valid	t47	See figure 4 7/	9,10,11	All		4CLK2 -36	ns
$\overline{UCS}$, $\overline{CS6:0}$ valid to D15:0 valid	t47a		9,10,11	All		4CLK2 -46	ns
$\overline{RD}$ low to D15:0 input valid	t48		9,10,11	All		3CLK2 -36	ns
D15:0 hold after $\overline{RD}$ high	t49	See figure 4	9,10,11	All	2		ns

See footnotes at the end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{RD}$ high to D15:0 float	t50	See figure 4 5/	9,10,11	All		10	ns
A25:1, $\overline{BHE}$, $\overline{BLE}$ hold after $\overline{RD}$ high	t51	See figure 4	9,10,11	All	0		ns
$\overline{UCS}$, $\overline{CS6:0}$ hold after $\overline{RD}$ high	t51a	See figure 4	9,10,11	All	0		ns
$\overline{RD}$ pulse width	t52	See figure 4	9,10,11	All	3CLK2 -15		ns
SYNCHRONOUS SERIAL I/O (SSIO) UNIT							
STXCLK, SRXCLK FREQ (master mode)	t100	See figure 4	9,10,11	All		CLK2/8	MHz
STXCLK, SRXCLK FREQ (slave mode)	t101	See figure 4 CLK2/4 or 6.25 MHz, whichever is less.	9,10,11	All		CLK2/4	MHz
STXCLK, SRXCLK low time	t102	See figure 4	9,10,11	All	3CLK2/2		ns
STXCLK, SRXCLK high time	t103	See figure 4	9,10,11	All	3CLK2/2		ns
STXCLK low to SSIOTX delay	t104	See figure 4	9,10,11	All		10	ns
SSIORX to SRXCLK high set-up time	t105	See figure 4	9,10,11	All	10		ns
SSIORX from SRXCLK hold time	t106	See figure 4	9,10,11	All	10		ns

See footnotes at the end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TIMER CONTROL UNIT (TCU): INPUTS							
TMRCLKn frequency	t107	See figure 4	9,10,11	All		8	ns
TMRCLKn low	t108	See figure 4	9,10,11	All	60		ns
TMRCLKn high	t109	See figure 4	9,10,11	All	60		ns
TMRGATEn high width	t110	See figure 4	9,10,11	All	50		ns
TMRGATEn low width	t111	See figure 4	9,10,11	All	50		ns
TMRGATEn to TMRCLK set-up time (external TMRCLK only)	t112	See figure 4	9,10,11	All	10		ns
TIMER CONTROL UNIT (TCU): OUTPUTS							
TMRGATEn low to TMROUT valid	t113	See figure 4	9,10,11	All		36	ns
TMRCLKn low to TMROUT valid	t114	See figure 4	9,10,11	All		36	ns
INTERRUPT CONTROL UNIT (ICU): INPUTS							
D7:0 set-up time ($\overline{\text{INTA}}$ cycle 2)	t115	See figure 4	9,10,11	All	7		ns
D7:0 hold time ($\overline{\text{INTA}}$ cycle 2)	t116	See figure 4	9,10,11	All	5		ns
INTERRUPT CONTROL UNIT (ICU): OUTPUTS							
CLK2 high to CAS2:0 valid	t117	See figure 4	9,10,11	All		34	ns

See footnotes at the end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DMA UNIT INPUTS							
DREQ set-up time (SYNC mode)	t118	See figure 4	9,10,11	All	17		ns
DREQ hold time (SYNC mode)	t119	See figure 4	9,10,11	All	4		ns
DREQ set-up time (ASYNC mode)	t120	See figure 4	9,10,11	All	10		ns
DREQ hold time (ASYNC mode)	t121	See figure 4	9,10,11	All	10		ns
$\overline{EOP}$ set-up time (SYNC mode)	t122	See figure 4	9,10,11	All	13		ns
$\overline{EOP}$ hold time (SYNC mode)	t123	See figure 4	9,10,11	All	4		ns
$\overline{EOP}$ set-up time (ASYNC mode)	t124	See figure 4	9,10,11	All	10		ns
$\overline{EOP}$ hold time (ASYNC mode)	t125	See figure 4	9,10,11	All	11		ns
DMA UNIT OUTPUTS							
$\overline{DACK}$ output valid delay	t126	See figure 4	9,10,11	All	4	29	ns
$\overline{EOP}$ active delay	t127	See figure 4	9,10,11	All	4	30	ns
$\overline{EOP}$ float delay	t128	See figure 4 5/	9,10,11	All	4	33	ns
JTAG TEST-LOGIC UNIT							
TCK frequency	t129	See figure 4	9,10,11	All		10	MHz

See footnotes at the end of table.

Notes:

1/ The case temperature range (T_C), for device 01 is -55°C to +125°C, for device 02 is -40°C to +125°C. All testing to be performed using worst case test conditions unless otherwise specified.

2/ Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.

3/ These are not tested. They are guaranteed by characterization.

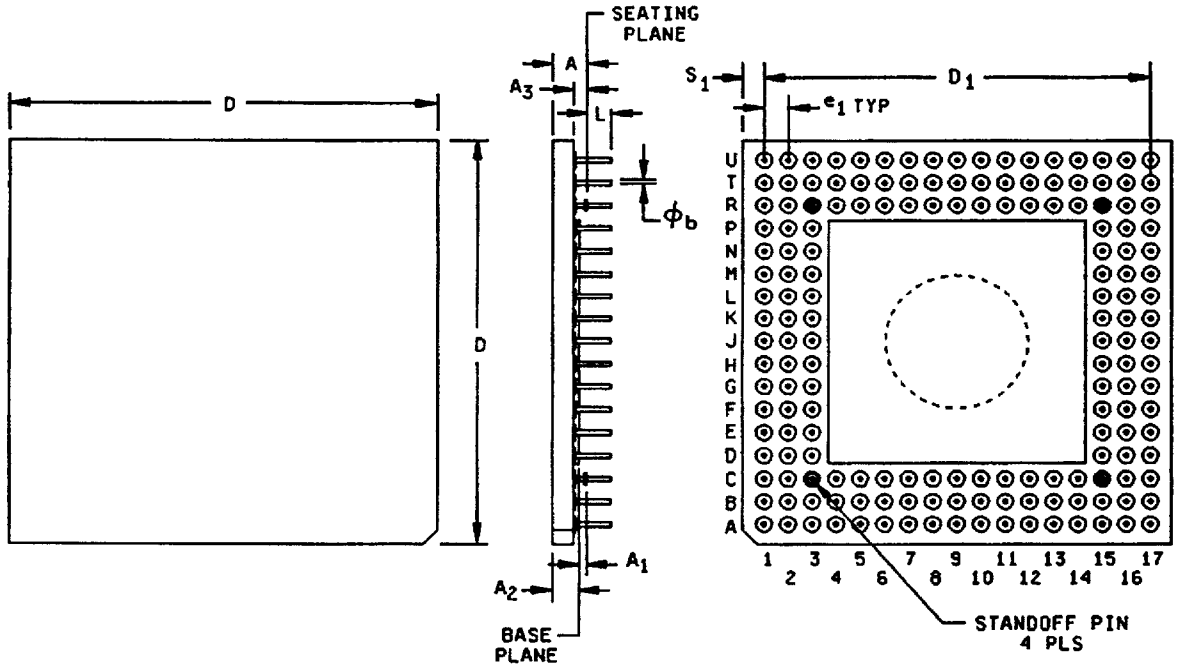
4/ Tested with CL set at 50 pF.

5/ Float condition occurs when maximum output current becomes less than ILO in magnitude. Float delay is not fully tested.

6/ These inputs may be asynchronous to CLK2. The set-up and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.

7/ These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.

Case X



Family: Ceramic pin grid array package					
Symbol	Inches		Millimeters		
	Min	Max	Min	Max	Notes
A	.140	.180	3.56	4.57	
A_1	.025	.045	0.64	1.14	
A_2	.110	.140	0.23	0.30	Solid lid
A_3	.045	.055	1.14	1.40	Solid lid
B	.017	.020	0.43	0.51	
D	1.740	1.780	44.19	45.21	
D_1	1.595	1.605	40.51	40.77	
e_1	.090	.110	2.29	2.79	
L	.100	.130	2.54	3.30	
N	168		168		
S_1	.060	.100	1.52	2.54	
ISSUE	IWS 11/29/88				

FIGURE 1. Case outline - Continued.

Device type 01, 02

Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	A20	C9	A6	J15	NC	Q10	$\overline{\text{SMIACT}}$
A2	NC	C10	A5	J16	V_{SS}	Q11	P2.1/$\overline{\text{CS1}}$
A3	A19	C11	A2	J17	V_{CC}	Q12	P2.2/$\overline{\text{CS2}}$
A4	A16/CAS0	C12	A1	K1	P3.2/INT0	Q13	DACK0/$\overline{\text{CS5}}$
A5	A14	C13	$\overline{\text{BLE}}$	K2	P3.3/INT1	Q14	V_{SS}
A6	V_{CC}	C14	V_{SS}	K3	NC	Q15	NC
A7	A10	C15	NC	K15	D9	Q16	V_{CC}
A8	A7	C16	V_{CC}	K16	V_{CC}	Q17	D1
A9	V_{CC}	C17	NC	K17	V_{SS}	R1	INT6/TMRCLK1
A10	V_{SS}	D1	A24	L1	P3.4/INT2	R2	DSR1/STXCLK
A11	A4	D2	NC	L2	P3.5/INT3	R3	V_{CC}
A12	V_{CC}	D3	V_{SS}	L3	P3.6/PWRDOWN	R4	P1.1/$\overline{\text{RTS0}}$
A13	$\overline{\text{NA}}$	D15	V_{SS}	L15	D6	R5	P1.4/$\overline{\text{RI0}}$
A14	$\overline{\text{BHE}}$	D16	$\overline{\text{D/C}}$	L16	D7	R6	V_{SS}
A15	$\overline{\text{WR}}$	D17	TMS	L17	D8	R7	P1.7/HLDA
A16	$\overline{\text{RD}}$	E1	P3.0/TIMEROUT0	M1	V_{CC}	R8	WDTOUT
A17	$\overline{\text{BS8}}$	E2	A25	M2	V_{SS}	R9	V_{SS}
B1	NC	E3	A23	M3	P3.7/COMCLK	R10	$\overline{\text{TRST}}$
B2	A21	E15	W/$\overline{\text{R}}$	M15	D2	R11	P2.0/$\overline{\text{CS0}}$
B3	V_{CC}	E16	TDO	M16	V_{SS}	R12	V_{SS}
B4	A18/CAS2	E17	TDI	M17	V_{CC}	R13	P2.4/$\overline{\text{CS4}}$
B5	A15	F1	V_{CC}	N1	PEREQ/TMRCLK2	R14	P2.6/TXD0
B6	V_{SS}	F2	V_{SS}	N2	NMI	R15	V_{CC}
B7	A11	F3	$\overline{\text{SMI}}$	N3	$\overline{\text{ERROR}}$/TMROUT2	R16	$\overline{\text{UCS}}$
B8	A8	F15	M/$\overline{\text{IO}}$	N15	$\overline{\text{LBA}}$	R17	NC
B9	V_{SS}	F16	V_{SS}	N16	D4	S1	INT7/TMRGATE1
B10	V_{CC}	F17	V_{CC}	N17	D5	S2	$\overline{\text{FLT}}$
B11	A3	G1	$\overline{\text{DTR1}}$/SRXCLK	P1	$\overline{\text{BUSY}}$/TMRGATE2	S3	P1.0/$\overline{\text{DCD0}}$
B12	V_{SS}	G2	TCK	P2	INT4/TMRCLK0	S4	P1.3/$\overline{\text{DSR0}}$
B13	$\overline{\text{ADS}}$	G3	P3.1/TIMEROUT1	P3	V_{SS}	S5	P1.6/HOLD
B14	NC	G15	D15	P15	V_{SS}	S6	V_{CC}
B15	NC	G16	D14	P16	D0	S7	$\overline{\text{DACK1}}$/TXD1
B16	NC	G17	D13	P17	D3	S8	$\overline{\text{EOP}}$/$\overline{\text{CTS1}}$
B17	$\overline{\text{READY}}$	H1	V_{SS}	Q1	INT5/TMRGATE0	S9	V_{CC}
C1	A22	H2	V_{CC}	Q2	V_{CC}	S10	DRQ1/RXD1
C2	V_{CC}	H3	$\overline{\text{RI1}}$/SSIORX	Q3	NC	S11	V_{SS}
C3	NC	H15	D12	Q4	NC	S12	V_{CC}
C4	V_{SS}	H16	D11	Q5	P1.2/$\overline{\text{DTR0}}$	S13	P2.3/$\overline{\text{CS3}}$
C5	A17/CAS1	H17	D10	Q6	P1.5/$\overline{\text{LOCK}}$	S14	P2.5/RXD0
C6	A13	J1	V_{CC}	Q7	RESET	S15	P2.7/$\overline{\text{CTS0}}$
C7	A12	J2	V_{SS}	Q8	$\overline{\text{CLK2}}$	S16	NC
C8	A9	J3	$\overline{\text{RTS1}}$/SSIOTX	Q9	DRQ0/$\overline{\text{DCD1}}$	S17	$\overline{\text{CS6}}$/REFRESH

FIGURE 2. Terminal connections - Continued.

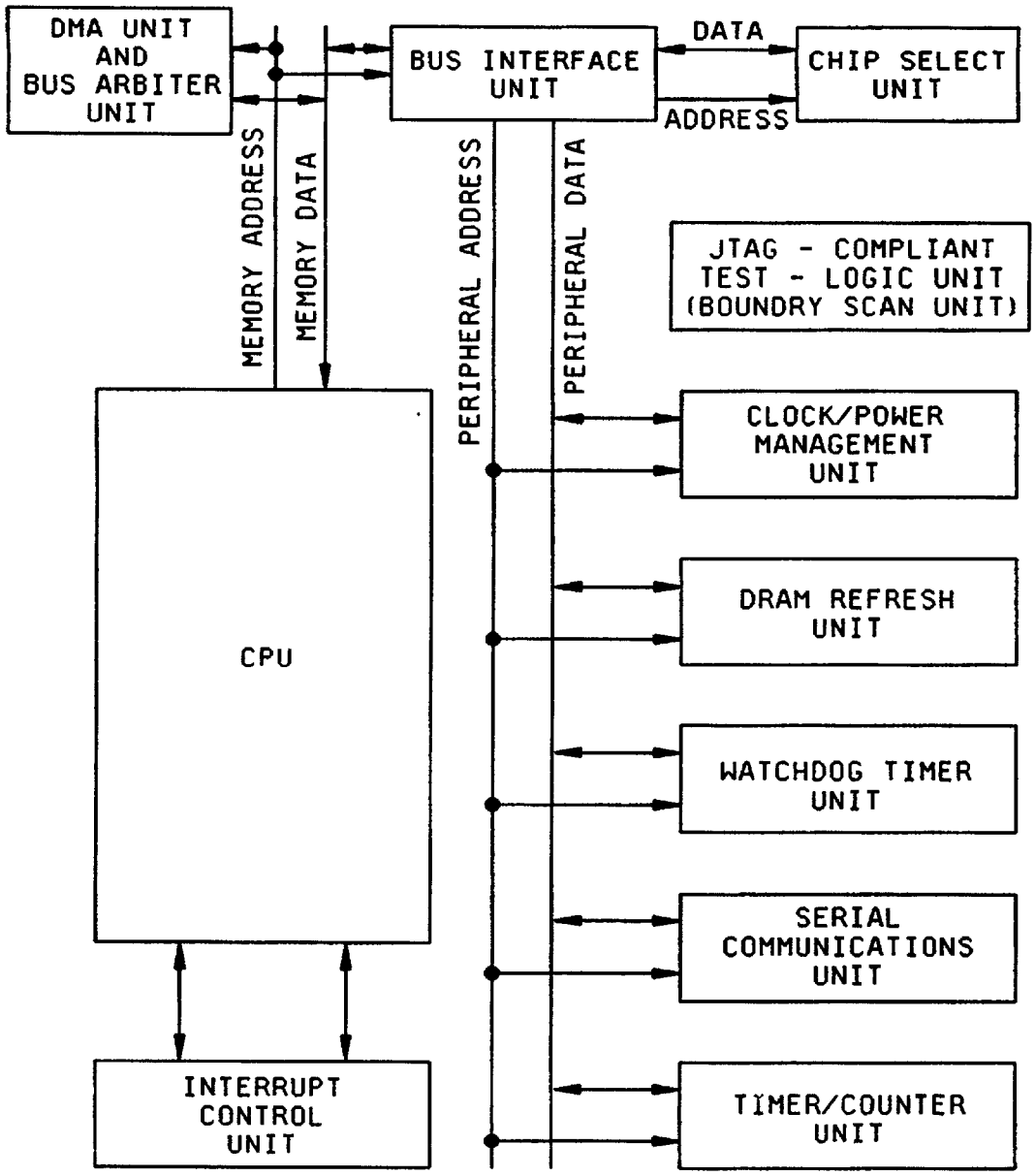
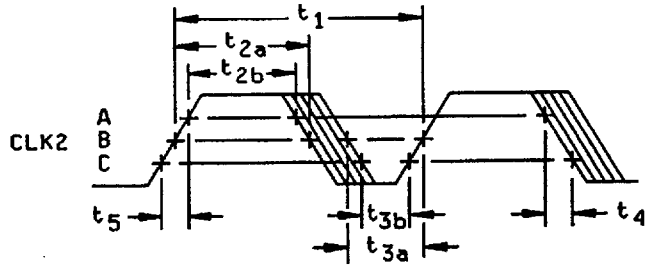
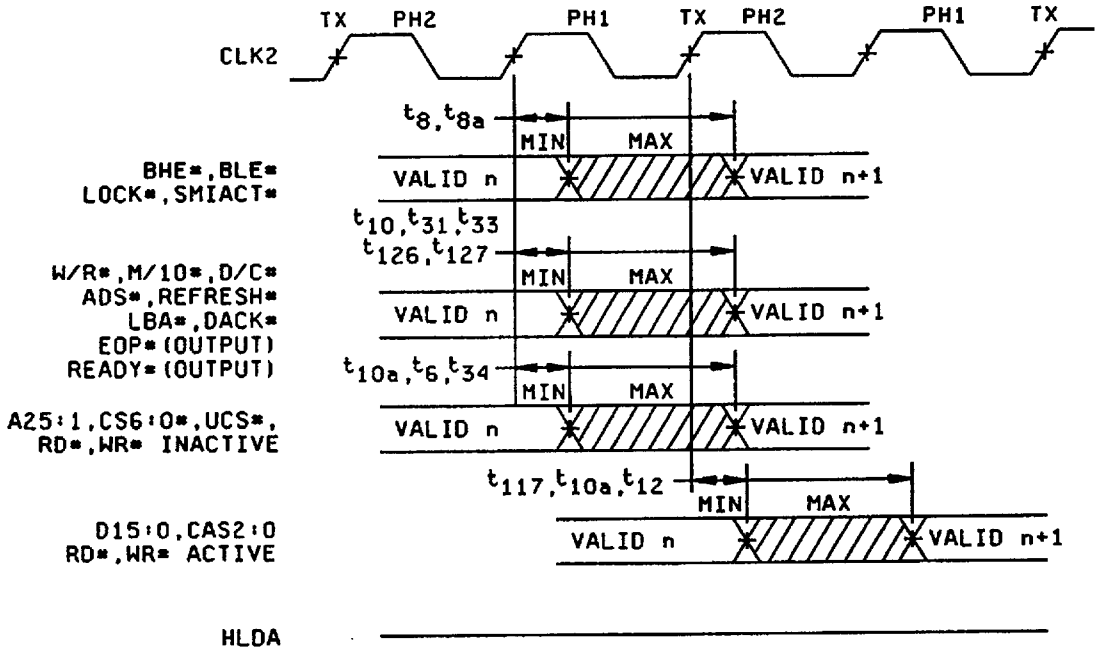


FIGURE 3. Block diagram.



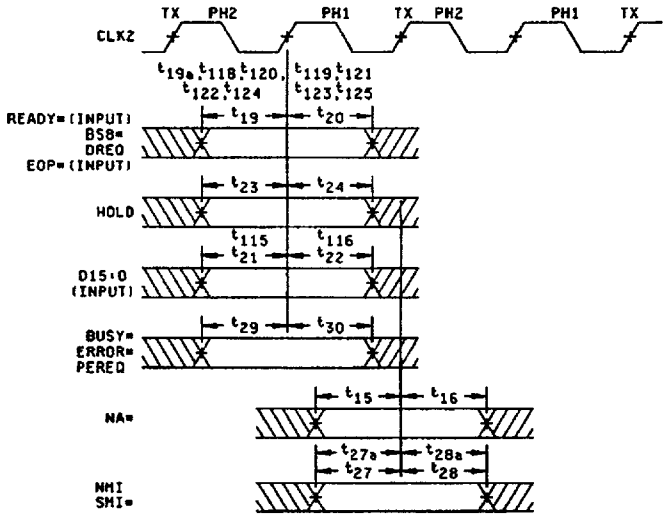
CLK2 WAVEFORM

A = V_{CC}-0.8 FOR V_{CC}= 4.75-5.25
B = $V_{CC}/2$
C = 0.8 V

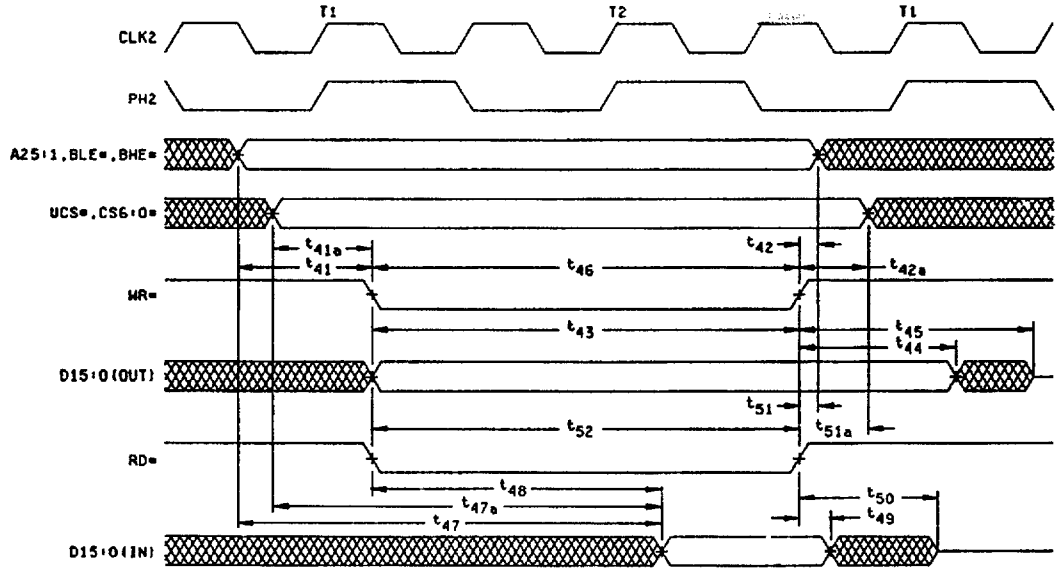


Output valid delay timing

FIGURE 4. Timing waveforms.

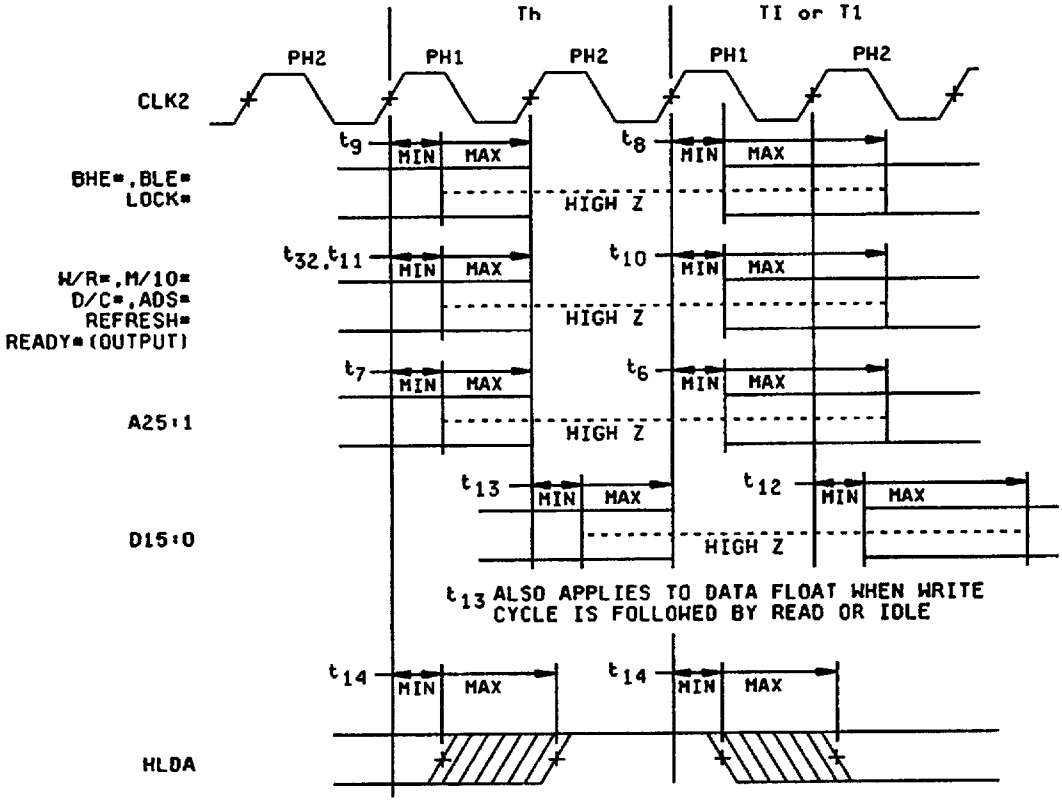


INPUT SETUP AND HOLD TIMING

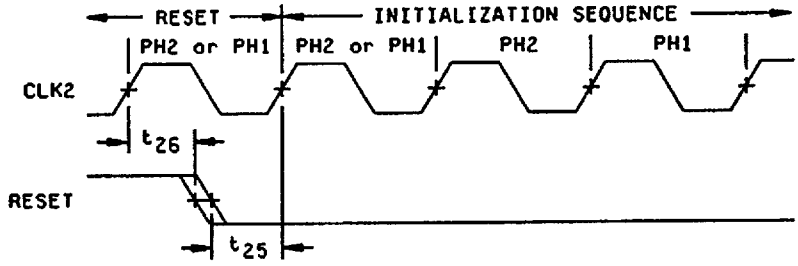


RELATIVE SIGNAL TIMING

FIGURE 4. Timing waveforms - Continued.



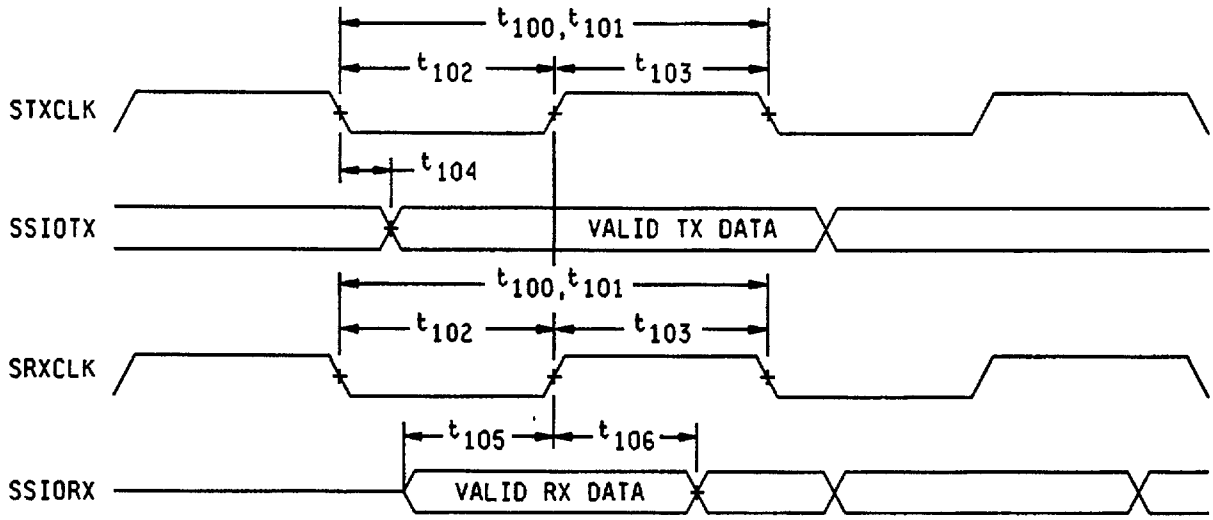
OUTPUT FLOAT DELAY AND HLDA VALID DELAY TIMING



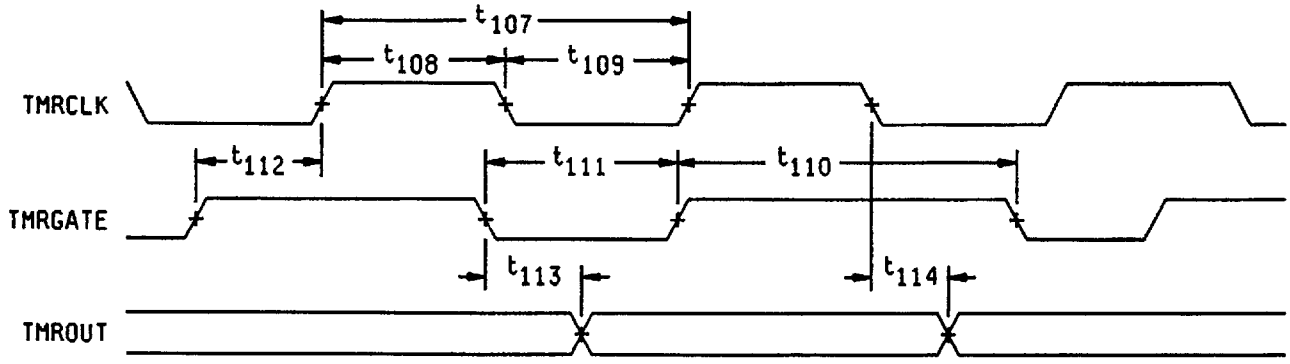
RESET SETUP AND HOLD TIMING AND INTERNAL PHASE

FIGURE 4. Timing waveforms - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-95570
		REVISION LEVEL	SHEET 20

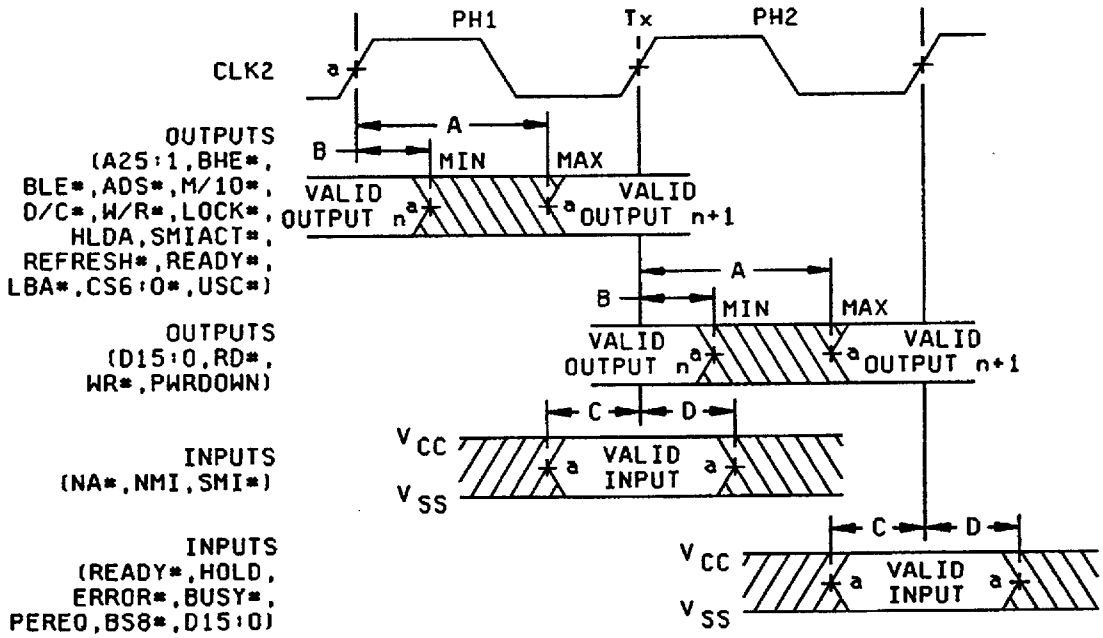


SSIO TIMING



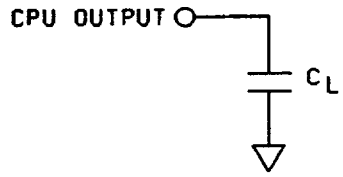
TIMER/COUNTER TIMING

FIGURE 4. Timing waveforms - Continued.



LEGEND
a-$V_{CC}/2$
A-MAXIMUM OUTPUT DELAY SPEC
B-MINIMUM OUTPUT DELAY SPEC
C-MINIMUM INPUT SETUP SPEC
D-MINIMUN INPUT HOLD SPEC

DRIVE LEVELS AND MEASUREMENT POINTS FOR AC SPECIFICATIONS



AC TEST LOADS

C_L = 50 pF

FIGURE 4. Timing waveforms - Continued.

Instruction code	Instruction name
0000	EXTEST
0001	SAMPRE
0010	ICODE
0011	PRIVATE
0100	PRIVATE
0101	PRIVATE
0110	PRIVATE
0111	PRIVATE
1000	HIGHZ
1001	INTEST
1010	PRIVATE
1011	PRIVATE
1100	PRIVATE
1101	PRIVATE
1110	PRIVATE
1111	BYPASS

FIGURE 5. Boundry scan instruction codes.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes N, Q, and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing. For device classes Q and V only, the electrical subgroup requirements specified in Table II herein are the baseline requirements but may be modified in the device manufacturers approved QM plan.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_S measurement) shall be measured only for the initial test and after process or design changes which may affect input or output capacitance. Test all applicable pins on five devices with zero failures.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)		
	Device class M	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9		
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 1/	1, 2, 3, 4, 5, 6, 7, 8, 9 1/ 10, 11	2, 3, 5, 6, 8, 10, 11 1/	2, 3, 5, 6, 8, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5 6, 7, 8, 9, 10 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 8, 10	2, 8a, 10	2, 8a, 10	2, 8, 10
Group D end-point electrical parameters (see 4.4)	2, 8, 10	2, 8a, 10	2, 8a, 10	2, 8, 10
Group E end-point electrical parameters (see 4.4)				

1/ PDA applies to subgroup 1 (I_{CC} only).
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes N, Q, and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes N, Q, and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331 and as follows:

Symbol	TypeName	and function
A25:1	O	Address Bus outputs physical memory or port I/O addresses. These signals are valid when $\overline{ADS}$ is active and remain valid until the next T1, T2P, or Ti. During HOLD cycles they are driven to a high-impedance state. A18:16 are multiplexed with CAS2:0.
$\overline{ADS}$	O	Address Status indicates that the processor is driving a valid bus-cycle definition and address (W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, A25:1, $\overline{BHE}$, $\overline{BLE}$) onto its pins.
$\overline{BHE}$	O	Byte High Enable indicates that the processor is transferring a high data byte.
$\overline{BLE}$	O	Byte Low Enable indicates that the processor is transferring a low data byte.
$\overline{BS8}$	I	Bus Size indicates that an 8-bit device is currently being addressed.
$\overline{BUSY}$	I	Busy indicates that the math coprocessor is busy. If $\overline{BUSY}$ is sampled low at the falling edge of RESET, the processor performs an internal self test. $\overline{BUSY}$ is multiplexed with TMRGATE2.

Symbol	Type	Name and function
CAS2:0	O	Cascade Address carries the slave address information from the 8259A master interrupt module during interrupt acknowledge bus cycles. CAS2:0 are multiplexed with A18:16.
CLK2	ST	Clock Input is connected to an external clock that provides the fundamental timing for the device.
COMCLK	I	Serial Communications Baud Clock is an alternate clock source for the asynchronous serial port. COMCLK is multiplexed with P3.7.
$\overline{\text{CTS1:0}}$	I	Clear to Send 1 and 0 prevent the transmission of data to the asynchronous serial port's RXD1 and RXD0 pin, respectively. $\overline{\text{CTS1}}$ is multiplexed with $\overline{\text{EOP}}$ and $\overline{\text{CTOS}}$ is multiplexed with P2.7. $\overline{\text{CTS1}}$ requires an external pull-up resistor.
D15:0	I/O	Data Bus inputs data during memory read, I/O read, and interrupt acknowledge cycles and outputs data during memory and I/O write cycles. During writes, this bus is driven during phase 2 of T1 and remains active until phase 2 of the next T1, T1P, or Ti. During reads, data is latched on the falling edge of phase 2.
DACK1:0	O	DMA Acknowledge 1 and 0 signal to an external device that the processor has acknowledged the corresponding DMA request and is relinquishing the bus. DACK1 is multiplexed with TXD1, and DACK0 is multiplexed with $\overline{\text{GCS5}}$
D/$\overline{\text{C}}$	O	Data/Control indicates whether the current bus cycle is a data cycle (memory or I/O read or write) or a control cycle (interrupt acknowledge, halt, or code fetch).
$\overline{\text{DCD1:0}}$	I	Data Carrier Detect SIO1 and SIO0 indicate that the modem or data set has detected the corresponding asynchronous serial channel's data carrier. $\overline{\text{DCD1}}$ is multiplexed with DRQ0 and $\overline{\text{DCD0}}$ is multiplexed with P1.0.
DRQ1:0	I	DMA External Request 1 and 0 indicate that a peripheral requires DMA service. DRQ1 is multiplexed with RXD1 and DRQ0 is multiplexed with $\overline{\text{DCD1}}$.
$\overline{\text{DSR1:0}}$	I	Data Set Ready SIO1 and SIO0 indicate that the modem or data set is ready to establish a communication link with the corresponding asynchronous serial channel. $\overline{\text{DSR1}}$ is not multiplexed; $\overline{\text{DSR0}}$ is multiplexed with P1.3.
$\overline{\text{DTR1:0}}$	O	Data Terminal Ready SIO1 and SIO0 indicate that the corresponding asynchronous serial channel is ready to establish a communication link with the modem data set. $\overline{\text{DTR1}}$ is multiplexed with SRXCLK, and $\overline{\text{DTR0}}$ is multiplexed with P1.2.
$\overline{\text{EOP}}$	I/OD	End of Process indicates that the processor has reached terminal count during a DMA transfer. An external device can also pull this pin low. $\overline{\text{EOP}}$ is multiplexed with $\overline{\text{CTS1}}$.
$\overline{\text{ERROR}}$	I	Error indicates that the math coprocessor has an error condition. $\overline{\text{ERROR}}$ is multiplexed with TMROUT2.
$\overline{\text{FLT}}$	I	Float forces all bidirectional and output signals, including HKDA, to a high-impedance state.
$\overline{\text{CS6:0}}$	O	Chip Selects are activated when the address of a memory or I/O bus cycle is within the address region programmed by the user, $\overline{\text{CS5}}$ is multiplexed with DACK0, and $\overline{\text{CS4:0}}$ are multiplexed with P2.4:0. $\overline{\text{CS6}}$ is multiplexed with refresh
HLDA	O	Bus Hold Acknowledge indicates that the processor has surrendered control of its local bus to another bus master. HLDA remains active until HOLD is deasserted. HLDA is multiplexed with P1.7.
HOLD	I	Bus Hold Request allows another bus master to request control of the local bus. HLDA active indicates that bus control has been granted. HOLD is multiplexed with P1.6.

Symbol	Type	Name and function
INT7:0	I	Interrupt Requests are maskable inputs that cause the CPU to suspend execution of the current program and then execute an interrupt acknowledge cycle. They are multiplexed as follows: INT7 with TMRGATE1, INT6 with TMRCLK1, INT5 with TMRGATE0, INT4 with TMRCLK0, and INT3:0 with P3.5:2.
$\overline{\text{LBA}}$	O	Local Bus Access is asserted whenever the processor provides the $\overline{\text{READY}}$ signal to terminate a bus transaction. This occurs when an internal perpheral address is accessed or when the chip-select unit provides the $\overline{\text{READY}}$ signal.
$\overline{\text{LOCK}}$	O	Bus Lock prevents other bus masters from gaining control of the system bus. $\overline{\text{LOCK}}$ is multiplexed with P1.5
$\overline{\text{M/IO}}$	O	Memory/IO indicates whether the current bus cycle is a memory cycle or an I/O cycle. When $\overline{\text{M/IO}}$ is high, the bus cycle is a memory cycle; when $\overline{\text{M/IO}}$ is low, the bus cycle is an I/O cycle.
$\overline{\text{NA}}$	I	Next Address requests address pipelining.
NMI	ST	Non-Maskable Interrupt Request is a nonmaskable input that causes the CPU to suspend execution of the current program and execute an interrupt acknowledge cycle.
PEREQ	I	Processor Extension Request indicates that the math coprocessor has data to transfer to the processor. PEREQ is multiplexed with TMRCLK2.
P1.7:0	I/O	Port 1, Pins 7:0 are multipurpose bidirectional port pins. They are multiplexed as follows: P1.7 with HLDA, P1.6 with HOLD, P1.5 with $\overline{\text{LOCK}}$, P1.4 with $\overline{\text{RIO}}$, P1.3 with $\overline{\text{DSR0}}$, P1.2 with $\overline{\text{DTR0}}$, P1.1 with $\overline{\text{RTS0}}$, and P1.0 with $\overline{\text{DCD0}}$.
P2.7:0	I/O	Port 2, Pins 7:0 are multipurpose bidirectional port pins. They are multiplexed as follows: P2.7 with $\overline{\text{CTS0}}$, P2.6 with TXD0, P2.5 with RXD0, and P2.4:0 with $\overline{\text{GCS4:0}}$.
P3.7:0	I/O	Port 3, Pins 7:0 are multipurpose bidirectional port pins. They are multiplexed as follows: P3.7 with COMCLK, P3.6 with PWRDOWN, P3.5:2 with INT3:0, and P3.1:0 with TMROUT1:0.
PWRDOWN	O	Powerdown indicates that the processor is in powerdown mode. PWRDOWN is multiplexed with P3.6.
$\overline{\text{READY}}$	I/OD	Ready indicates that the current bus transaction has completed. An external device or an internal signal can drive $\overline{\text{READY}}$. Internally, the chip-select waitstate logic can generate the ready signal and drive the $\overline{\text{READY}}$ pin active.
RESET	ST	Reset suspends any operation in progress and places the processor into a known reset state.
$\overline{\text{RD}}$	O	Read Enable indicates that the current bus cycle is a read cycle.
$\overline{\text{REFRESH}}$	O	Refresh indicates that the current bus cycle is a refresh cycle.
$\overline{\text{RI1:0}}$	I	Ring Indicator SI01 and SI00 indicate that the modem or data set has received a telephone ringing signal. RI1 is multiplexed with SSIORX, and RI0 is multiplexed with P1.4.
$\overline{\text{RTS1:0}}$	O	Request-to-Send SI01 and SI00 indicate that the corresponding asynchronous serial channel is ready to exchange data with the modem or data set. $\overline{\text{RTS1}}$ is multiplexed with SSIOTX, and $\overline{\text{RTSQ}}$ is multiplexed with P1.1.
RXD1:0	I	Receive Data SI01 and SI00 accept serial data from the modem or data set to the corresponding asynchronous serial channel. RXD1 is multiplexed with DRQ1, and RXD0 is multiplexed with P2.5.

Symbol	Type	Name and function
$\overline{SMI}$	ST	System Management Interrupt invokes System Management Mode (SMM). SMI is the highest priority interrupt. It is latched on its falling edge and it forces the CPU into SMM upon completion of the current instruction. $\overline{SMI}$ is recognized on an instruction boundary and at each iteration for repeat string instructions. $\overline{SMI}$ cannot interrupt LOCKed bus cycles or a currently executing SMM. If the processor receives a second $\overline{SMI}$ while it is in SMM, it will latch the second $\overline{SMI}$ on the $\overline{SMI}$ falling edge. However, the processor must exit SMM by executing a Resume instruction (RSM) before it can service the second $\overline{SMI}$.
$\overline{SMIACT}$	O	System Management Interrupt Active indicates that the processor is operating in System Management Mode (SMM). It is asserted when the processor initiates an SMM sequence and remains asserted (low) until the processor executes the Resume instruction(RSM).
SRXCLK	I/O	SSIO Receive Clock synchronizes data being accepted by the synchronous serial port. SSIORX is multiplexed with $\overline{DTR1}$
STXCLK	I/O	SSIO Transmit Clock synchronizes data being sent by the synchronous serial port. STXCLK is multiplexed with $\overline{DTR1}$
SSIORX	I	SSIO Receive Serial Data accepts serial data (most-significant bit first) being sent to the synchronous serial port. SSIORX is multiplexed with $\overline{RI1}$.
SSIOTX	O	SSIO Transmit Serial Data sends serial data (most-significant bit first) from the synchronous serial port. SSIOTX is multiplexed with $\overline{RTS1}$.
TCK	I	JTAG TAP (Test Access Port) Controller Clock provides the clock input for the JTAG logic.
TDI	I	JTAG TAP (Test Access Port) Controller Data Input is the serial input for test instructions and data.
TDO	O	JTAG TAP (Test Access Port) Controller Data Output is the serial output for test instructions and data.
TMRCLK2:0	I	Timer/Counter Clock Inputs provide the output of the corresponding timer/counter. (The timer/counters can also be clocked internally.) TMRCLK2 is multiplexed with PEREQ; TMRCLK1, with INT6; and TMRCLK0, with INT4.
TMRGATE2:0	I	Timer/Counter Gate Inputs can control the corresponding timer/counter's counting (enable, disable, or trigger, depending on the programmed mode). (Alternatively, a V_{CC} pin can serve this function.) TMRGATE2 is multiplexed with $\overline{BUSY}$; TMRGATE1, with INT7; and TMRGATE0, with INT5.
TMROUT2:0	O	Timer/Counter Outputs provide the output of the corresponding timer/counter. The form of the output depends on the programmed mode. TMROUT2 is multiplexed with ERROR; TMROUT1, with P3.1; and TMROUT0, with P3.0.
TMS	I	JTAG TAP (Test Access Port) Controller Mode Select controls the sequence of the TAP controller's states.
$\overline{TRST}$	ST	JTAG TAP (Test Access Port) Controller Rest resets the TAP controller at power-up.
TXD1:0	O	Transmit Data SSIO1/SSIO0 transmits serial data from the individual serial channel. TXD1 is multiplexed with DACK1 and TXD0 is multiplexed with P2.6.
$\overline{UCS}$	O	Upper Chip Select is activated when the address of a memory or I/O bus cycle is within the address region programmed by the user.

Symbol	Type	Name and function
V_{CC}	P	System Power provides the nominal dc supply input. Connected externally to a V_{CC} board plane.
V_{SS}	G	System Ground provides the OV connection from which all inputs and outputs are measured. Connected externally to a ground board plane.
WDTOUT	O	Watchdog Timer Output indicates that the watchdog timer has expired.
$W/\overline{R}$	O	Write/Read indicates whether the current bus cycle is a write cycle or a read cycle. When $W/\overline{R}$ is high, the bus cycle is a write cycle; when $W/\overline{R}$ is low, the bus cycle is a read cycle.
$\overline{WR}$	O	Write Enable indicates that the current bus cycle is a write cycle.

I	Standard CMOS Input signal.
O	Standard CMOS Output signal.
I/O	Input and Output signal.
I/OD	Input and Open-Drain Output signal.
ST	Schmitt-Triggered Input signal.
P	Power pin
G	Ground pin

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(N, Q, or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.