ANALOG DEVICES

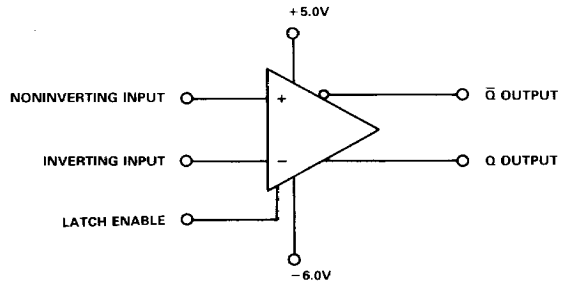
# High-Speed TTL Voltage Comparator

# AD9686

**FEATURES**
**7ns Propagation Delay**
**Complementary TTL Outputs**
**85dB CMRR**
**+5V, −6V Supply Voltages**

**APPLICATIONS**
**High-Speed Triggers**
**High-Speed Line Receivers**
**Peak Detectors**
**Threshold Detectors**

**AD9686 FUNCTIONAL BLOCK DIAGRAM**

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## GENERAL DESCRIPTION

The AD9686 is a high-speed voltage comparator with complementary TTL outputs. The AD9686 is manufactured in a high-performance bipolar process which provides an excellent match between high-speed ac switching and dc accuracy. The AD9686 operates with a propagation delay of only 7ns.

The AD9686 incorporates a Latch Enable control line providing operation in either a sample-hold mode or a track-hold mode. The Latch Enable setup times are less than 2ns which allows very high-speed voltage sampling.

The precision differential input stage has less than 2mV of offset voltage and requires an input bias current of only 4μA. This combined with the 85dB common-mode rejection ratio, makes the AD9686 especially well suited for high-speed analog signal processing.

The AD9686 is offered as both an industrial temperature range device, −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. Both versions are available packaged in a TO-100 metal can and in a ceramic DIP. The extended temperature range device is also available in a ceramic LCC package.

## ORDERING INFORMATION

| Device | Temperature Range | Description | Package Options* |
|---|---|---|---|
| AD9686BH | −25°C to +85°C | 10-Pin Can, Industrial | H-10A |
| AD9686BQ | −25°C to +85°C | 16-Pin DIP, Industrial | Q-16 |
| AD9686TE | −55°C to +125°C | 20-Pin LCC, Extended Temperature | E-20A |
| AD9686TH | −55°C to +125°C | 10-Pin Can, Extended Temperature | H-10A |
| AD9686TQ | −55°C to +125°C | 16-Pin DIP, Extended Temperature | Q-16 |

*See Section 16 for package outline information.

# SPECIFICATIONS

**ABSOLUTE MAXIMUM RATINGS**[1]

Positive Supply Voltage ($+V_S$) . . . . . +7V
Negative Supply Voltage ($-V_S$) . . . . . −7V
Input Voltage Range[2] . . . . . ±5V
Differential Input Voltage . . . . . 6.0V
Latch Enable Voltage . . . . . 0V to $+V_S$
Output Current Sourcing . . . . . 4mA
Sinking . . . . . 14mA
Power Dissipation . . . . . 600mW
Operating Temperature Range[3]
AD9686BH/BQ . . . . . −25°C to +85°C
AD9686TE/TH/TQ . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

## ELECTRICAL CHARACTERISTICS (Supply Voltages = −6.0V and +5.0V, unless otherwise stated)

| Parameter | Mil[4] Sub Group | Temp | Industrial −25°C to +85°C AD9686BH/BQ Min | Typ | Max | Military −55°C to +125°C AD9686TE/TH/TQ Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | | | | | |
| Input Offset Voltage[5] | 1 | +25°C | | 1.0 | 2.0 | | 1.0 | 2.0 | mV |
| | 2, 3 | Full | | | 3.0 | | | 3.0 | mV |
| Input Offset Drift | | Full | | 10 | | | 10 | | µV/°C |
| Input Bias Current | 1 | +25°C | | 4 | 10 | | 4 | 10 | µA |
| | 2, 3 | Full | | | 13 | | | 13 | µA |
| Input Offset Current | 1 | +25°C | | 0.4 | 1.0 | | 0.4 | 1.0 | µA |
| | 2, 3 | Full | | | 1.3 | | | 1.3 | µA |
| Input Resistance | | +25°C | | 100 | | | 100 | | kΩ |
| Input Capacitance | | +25°C | | 3 | | | 3 | | pF |
| Input Voltage Range | 1, 2, 3 | Full | −3.3 | | +4.5 | −3.3 | | +4.5 | V |
| Common-Mode Rejection Ratio | | Full | | 85 | | | 85 | | dB |
| ENABLE INPUT | | | | | | | | | |
| Logic "1" Voltage | 1, 2, 3 | Full | | | 2.0 | | | 2.0 | V |
| Logic "0" Voltage | 1, 2, 3 | Full | 0.8 | | | 0.8 | | | V |
| Logic "1" Current | 1, 2, 3 | Full | | | 100 | | | 100 | µA |
| Logic "0" Current | 1, 2, 3 | Full | | | 100 | | | 100 | µA |
| DIGITAL OUTPUTS | | | | | | | | | |
| Logic "1" Voltage (Source 1mA) | 1, 2, 3 | Full | 2.4 | 3.5 | | 2.4 | 3.5 | | V |
| Logic "0" Voltage (Sink 10mA) | 1, 2, 3 | Full | | 0.3 | 0.4 | | 0.3 | 0.4 | V |
| SWITCHING PERFORMANCE | | | | | | | | | |
| Propagation Delays | | | | | | | | | |
| Input to Output HIGH | | +25°C | | 7 | | | 7 | | ns |
| Input to Output LOW | | +25°C | | 7 | | | 7 | | ns |
| Latch Enable to Output HIGH | | +25°C | | 7 | | | 7 | | ns |
| Latch Enable to Output LOW | | +25°C | | 7 | | | 7 | | ns |
| Delta Delay Between Outputs | | +25°C | | 2 | | | 2 | | ns |
| Latch Enable | | | | | | | | | |
| Minimum Pulse Width | 12 | +25°C | | 2 | 3 | | 2 | 3 | ns |
| Minimum Setup Time | 12 | +25°C | | 1 | 2 | | 1 | 2 | ns |
| Minimum Hold Time | 12 | +25°C | | 1 | 2 | | 1 | 2 | ns |
| POWER SUPPLY[6] | | | | | | | | | |
| Positive Supply Current (+5.0V) | 1, 2, 3 | Full | | 30 | 35 | | 30 | 35 | mA |
| Negative Supply Current (−6.0V) | 1, 2, 3 | Full | | 26 | 32 | | 26 | 32 | mA |
| Power Supply Rejection Ratio[7] | | Full | | 65 | | | 65 | | dB |

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Under no circumstances should the input voltages exceed the supply voltages.

[3]Typical thermal impedance . . .
AD9686 Metal Can $\theta_{JA} = 172°C/W; \theta_{JC} = 52°C/W$
AD9686 Ceramic $\theta_{JA} = 115°C/W; \theta_{JC} = 57°C/W$
AD9686 LCC $\theta_{JA} = 102°C/W; \theta_{JC} = 45°C/W$

[4]Military subgroups apply to military qualified devices only.

[5]$R_S = 100\Omega$.

[6]Supply voltage should remain stable within ±5% for normal operation.

[7]Measured at ±5% of $+V_S$ and $-V_S$.

Specifications subject to change without notice.

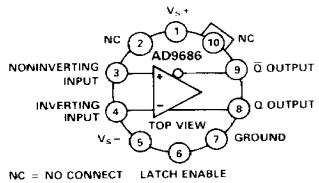
**EXPLANATION OF GROUP A MILITARY SUBGROUPS**

Subgroup 1 – Static tests at +25°C.
Subgroup 2 – Static tests at max rated oper. temp.
Subgroup 3 – Static tests at min rated oper. temp.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at max rated oper. temp.
Subgroup 6 – Dynamic tests at min rated oper. temp.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at max and min rated oper. temp.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at max rated oper. temp.
Subgroup 11 – Switching tests at min rated oper. temp.
Subgroup 12 – Periodically sample tested.

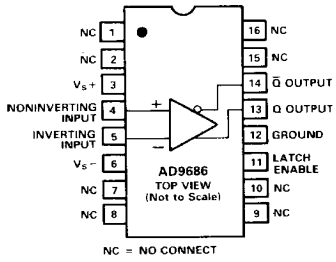
## FUNCTIONAL DESCRIPTION

| PIN NAME | DESCRIPTION |
|---|---|
| $+V_S$ | – Positive supply terminal, nominally +5.0V. |
| NONINVERTING INPUT | – Noninverting analog input of the differential input stage. The NONINVERTING INPUT must be driven in conjunction with the INVERTING INPUT. |
| INVERTING INPUT | – Inverting analog input of the differential input stage. The INVERTING INPUT must be driven in conjunction with the NONINVERTING INPUT. |
| $-V_S$ | – Negative supply terminal, nominally −6.0V. |
| LATCH ENABLE | – In the "compare" mode (logic LOW), the output will track changes at the input of the comparator. In the "latch" mode (logic HIGH), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. |
| GROUND | – Analog and digital ground. |
| Q OUTPUT | – One of two complementary outputs. Q will be at logic HIGH if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE for additional information. |
| $\overline{Q}$ OUTPUT | – One of two complementary outputs. $\overline{Q}$ will be at logic LOW if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE for additional information. |
| NC | – "NO CONNECT" pins are not internally connected. |

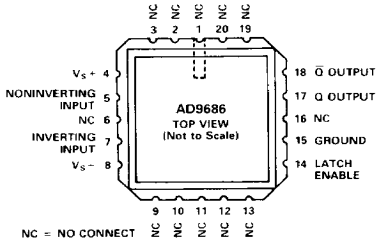
## PINOUT CONFIGURATIONS




TO-100
10-Pin Can

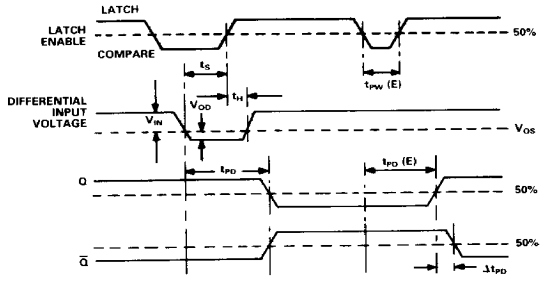



16-Pin DIP



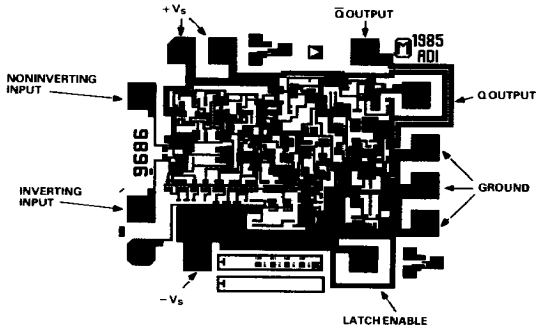

20-Pin LCC

## SYSTEM TIMING DIAGRAM




$t_S$ – Minimum Setup Time
$t_H$ – Minimum Hold Time
$t_{PD}$ – Input to Output Delay
$t_{PD}(E)$ – LATCH ENABLE to Output Delay
$t_{PW}(E)$ – Minimum LATCH ENABLE Pulse Width
$V_{OS}$ – Input Offset Voltage
$V_{OD}$ – Overdrive Voltage
$\Delta t_{PD}$ – Delta Delay Between Complementary Outputs

## DIE LAYOUT AND MECHANICAL INFORMATION




| | |
|---|---|
| Die Dimensions | 59 × 50 × 18 (max) mils |
| Pad Dimensions | 4 × 4 mils |
| Metalization | Aluminum |
| Backing | None |
| Substrate Potential | $-V_S$ |
| Passivation | Oxynitride |
| Die Attach | Gold Eutectic |
| Bond Wire | 1.25 mil, Aluminum; Ultrasonic Bonding or 1 mil, Gold; Gold Ball Bonding |