

Silicon Power Transistors

The MJ21195 and MJ21196 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain -

 $h_{FE} = 25 \text{ Min } @ I_{C} = 8 \text{ Adc}$

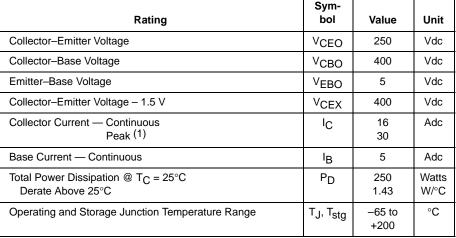
- Excellent Gain Linearity
- High SOA: 3 A, 80 V, 1 Second

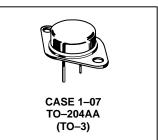
MJ21195* NPN MJ21196*

*ON Semiconductor Preferred Device

16 AMPERE
COMPLEMENTARY
SILICON POWER
TRANSISTORS
250 VOLTS
250 WATTS

MAXIMUM RATINGS Svm-





THERMAL CHARACTERISTICS

Characteristic		Max	Unit
Thermal Resistance, Junction to Case		0.7	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C \pm 5^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit	
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I _C = 100 mAdc, I _B = 0)	VCEO(sus)	250	_	_	Vdc	
Collector Cutoff Current (V _{CE} = 200 Vdc, I _B = 0)	ICEO	_	_	100	μAdc	

(1) Pulse Test: Pulse Width = 5 μ s, Duty Cycle \leq 10%.

(continued)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS				•		•
Emitter Cutoff Current (VCE = 5 Vdc, IC = 0)		I _{EBO}	_	_	100	μAdc
Collector Cutoff Current (V _{CE} = 250 Vdc, V _{BE(off)} = 1.5 Vdc)		ICEX	_	_	100	μAdc
SECOND BREAKDOWN				•		•
Second Breakdown Collector Current with Base Forward Biased (VCE = 50 Vdc, t = 1 s (non-repetitive) (VCE = 80 Vdc, t = 1 s (non-repetitive)		I _{S/b}	5 2.5	=		Adc
ON CHARACTERISTICS						
DC Current Gain (IC = 8 Adc, VCE = 5 Vdc) (IC = 16 Adc, VCE = 5 Vdc)		hFE	25 8	_ _	75	
Base–Emitter On Voltage (IC = 8 Adc, VCE = 5 Vdc)		V _{BE(on)}	_	_	2.2	Vdc
Collector–Emitter Saturation Voltage (I _C = 8 Adc, I _B = 0.8 Adc) (I _C = 16 Adc, I _B = 3.2 Adc)		V _{CE(sat)}		_	1.4 4	Vdc
DYNAMIC CHARACTERISTICS						
Total Harmonic Distortion at the Output V _{RMS} = 28.3 V, f = 1 kHz, P _{LOAD} = 100 W _{RMS}	hFE unmatch	THD		0.8		%
ed (Matched pair hFE = 50 @ 5 A/5 V)	h _{FE} matched		_	0.08	_	
Current Gain Bandwidth Product (I _C = 1 Adc, V _{CE} = 10 Vdc, f _{test} = 1 MHz)		fΤ	4	_	_	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1 MHz)		C _{ob}	_	_	500	pF

⁽¹⁾ Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%

6.5 f_{T} , CURRENT BANDWIDTH PRODUCT (MHz) 6.0 V_{CE} = 10 V 5.5 5.0 5 V 4.5 4.0 3.5 3.0 2.5 2.0 1.5 T_J = 25°C 1.0 f_{test} = 1 MHz 0.5 0 0.1 1.0 10 IC, COLLECTOR CURRENT (AMPS)

PNP MJ21195

Figure 1. Typical Current Gain Bandwidth Product

NPN MJ21196

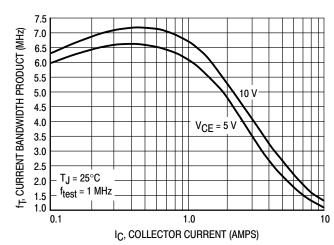


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

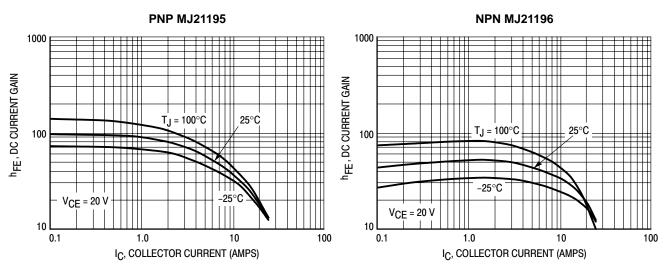


Figure 3. DC Current Gain, V_{CE} = 20 V

Figure 4. DC Current Gain, VCE = 20 V

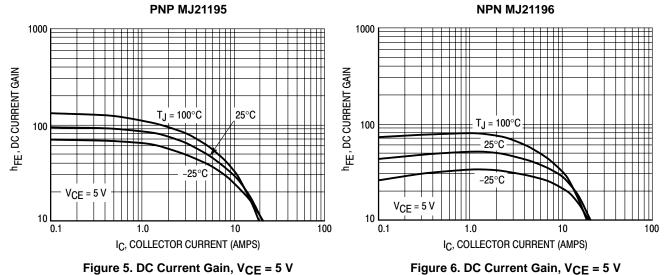


Figure 5. DC Current Gain, VCE = 5 V

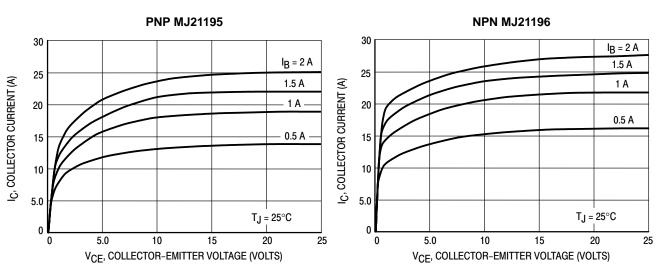


Figure 7. Typical Output Characteristics

Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

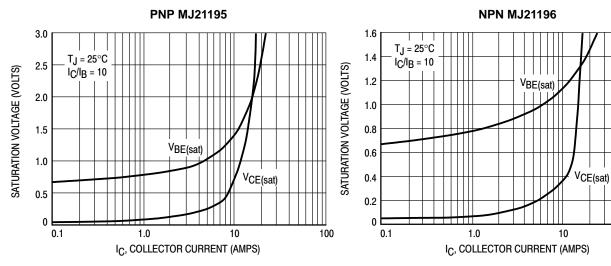


Figure 9. Typical Saturation Voltages

Figure 10. Typical Saturation Voltages

100

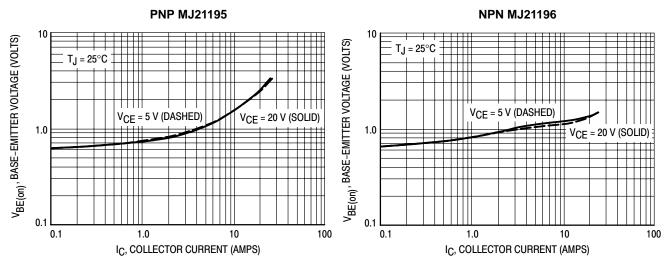


Figure 11. Typical Base-Emitter Voltage

Figure 12. Typical Base-Emitter Voltage

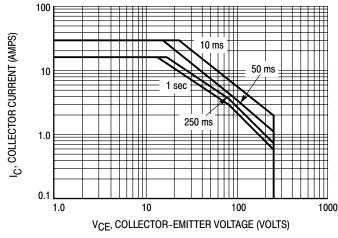


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)} = 200^{\circ}C$; T_{C} is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

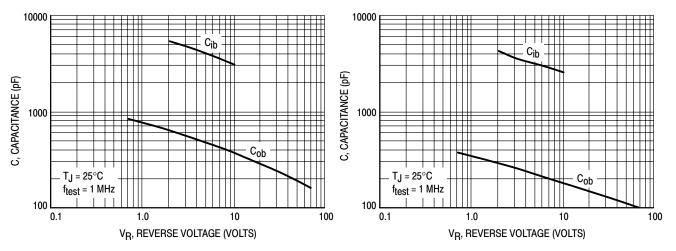


Figure 14. MJ21195 Typical Capacitance

Figure 15. MJ21196 Typical Capacitance

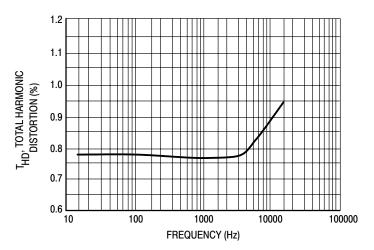


Figure 16. Typical Total Harmonic Distortion

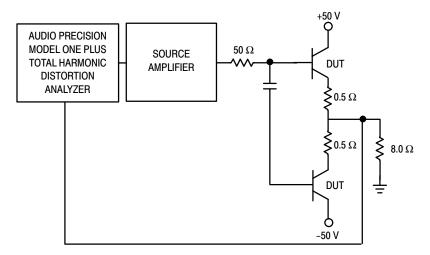
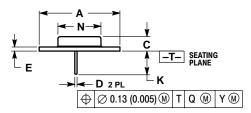
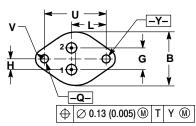


Figure 17. Total Harmonic Distortion Test Circuit

PACKAGE DIMENSIONS

TO-204 (TO-3) CASE 1-07 **ISSUE Z**





- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: INCH.

 3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

	INC	HES	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	1.550	REF	39.37 REF		
В		1.050		26.67	
С	0.250	0.335	6.35	8.51	
D	0.038	0.043	0.97	1.09	
E	0.055	0.070	1.40	1.77	
G	0.430 BSC		10.92 BSC		
Н	0.215 BSC		5.46 BSC		
K	0.440	0.480	11.18	12.19	
L	0.665 BSC		16.89 BSC		
N		0.830		21.08	
Q	0.151	0.165	3.84	4.19	
U	1.187 BSC		30.15 BSC		
٧	0.131	0.188	3.33	4.77	



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